TLP535(Short)

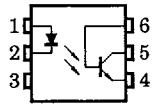
(TLP535(Short))

PROGRAMMABLE CONTROLLERS.
AC/DC-INPUT MODULE.
SOLID STATE RELAY.

The TOSHIBA TLP535 (Short) consists of a photo-transistor optically coupled to a gallium arsenide infrared emitting diode in a six lead plastic DIP package.

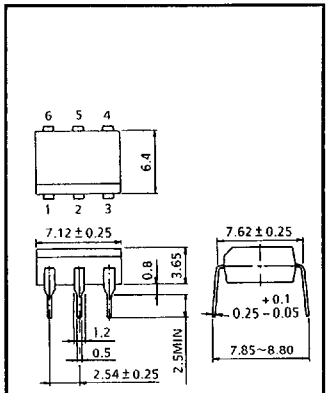
- Collector-Emitter Voltage : 55V Min.
- Current Transfer Ratio : 50% Min.
  Rank GB : 100% Min.
- Isolation Voltage : 2500V_{rms} Min.
- UL Recognized : UL1577 File No. E67349

PIN CONFIGURATIONS (TOP VIEW)



1 : ANODE
2 : CATHODE
3 : NC
4 : EMITTER
5 : COLLECTOR
6 : BASE

Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	11-7A1

Weight : 0.4g

TLP552

GaAℓAs IRED & PHOTO-IC

(TLP552)

ISOLATED LINE RECEIVER

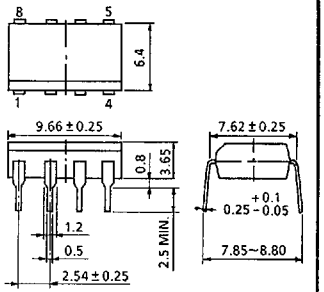
SIMPLEX / MULTIPLEX DATA TRANSMISSION

COMPUTER-PERIPHERAL INTERFACE

MICROPROCESSOR SYSTEM INTERFACE

DIGITAL ISOLATION FOR A / D, D / A CONVERSION

Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	11-10C1

Weight : 0.54g

The TOSHIBA TLP552 is a photocoupler which combines a GaAℓAs IRED as the emitter and an integrated high gain, high speed photodetector. This unit is 8-lead DIP package.
The output of the detector circuit is an open collector, Schottky clamped transistor.

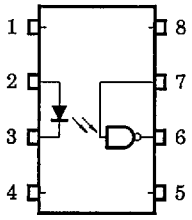
- TTL / LSTTL Compatible : V_{CC}=5V
- Isolation Voltage : 2500V_{rms} (Min.)
- Switching Speed : t_{pHL}, t_{pLH}=60ns (Typ.) (@R_L=350Ω)
- Guaranteed Performance Over Temp. : 0°C~70°C
- UL Recognized : UL1577, File No. E67349

TRUTH TABLE (Positive Logic)

INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

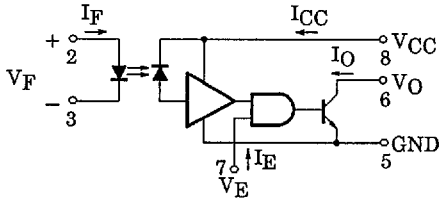
A 0.1μF bypass capacitor must be connected between pins 8 and 5 (See Note 3).

PIN CONFIGURATION (TOP VIEW)



1.: NC
2.: ANODE
3.: CATHODE
4.: NC
5.: GND
6.: OUTPUT (OPEN COLLECTOR)
7.: ENABLE
8.: V_{CC}

SCHEMATIC



(TLP552)

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Current, Low Level	I_{FL}	0	—	250	μA
Input Current, High Level	I_{FH}	7	—	20	mA
Supply Voltage, Output	V_{CC}	4.5	—	5.5	V
High Level Enable Voltage	V_{EH}	2.0	—	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	—	0.8	V
Fan Out (TTL Load)	N	—	—	8	—
Operating Temperature	T_{opr}	0	—	70	°C

MAXIMUM RATINGS (Ta = 25°C)

	CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current		I_F	20	mA
	Pulse Forward Current	(Note 1)	I_{FP}	40	mA
	Peak Transient Forward Current	(Note 2)	I_{FPT}	0.5	A
	Reverse Voltage		V_R	5	V
	Diode Power Dissipation		P_D	40	mW
DETECTOR	Output Current		I_O	50	mA
	Output Voltage		V_O	7	V
	Supply Voltage (1 Minute Maximum)		V_{CC}	7	V
	Enable Input Voltage (Not to exceed V_{CC} by more than 500mV)		V_E	5.5	V
	Output Collector Power Dissipation		P_O	85	mW
Operating Temperature Range			T_{opr}	0~70	°C
Storage Temperature Range			T_{stg}	−55~125	°C
Lead Solder Temperature (10sec.)**			T_{sold}	260	°C
Isolation Voltage (R.H.≦60%, AC/1min., Note 4)			BV_S	2500	V_{rms}

** Soldering portion of lead : up to 2mm from the body of the device.

Note 1 : 50% duty cycle, 1ms pulse width.

Note 2 : Pulse width≦1μs, 300pps.

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ELECTRICAL CHARACTERISTICS (For 0°C≦Ta≦70°C, unless otherwise specified.)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Forward Voltage	V_F	I_F=10mA, Ta=25°C	—	1.65	1.8	V
Input Diode Temperature Coefficient	$\Delta V_F / \Delta Ta$	I_F=10mA	—	−2.0	—	mV/°C
Input Reverse Current	I_R	V_R=5V, Ta=25°C	—	—	10	μA
Input Capacitance	C_T	V_F=0, f=1MHz	—	45	—	pF
High Level Output Current	I_{OH}	V_{CC}=5.5V, V_O=5.5V I_F=250μA, V_E=2.0V	—	10	250	μA
Low Level Output Voltage	V_{OL}	V_{CC}=5.5V, I_F=5mA V_{EH}=2.0V IOL=(Sinking)=13mA	—	0.4	0.6	V
Input Current Logic Low Output Level	I_{FH}	I_{OL}=13mA (Sinking), V_O=0.6V V_{CC}=5.5V, V_{EH}=2.0V	—	—	5	mA
High Level Enable Current	I_{EH}	V_{CC}=5.5V, V_E=2.0V	—	−0.1	—	mA
Low Level Enable Current	I_{EL}	V_{CC}=5.5V, V_E=0.5V	—	−1.6	−2.0	mA
High Level Supply Current	I_{CCH}	V_{CC}=5.5V, I_F=0 V_E=0.5V	—	7	15	mA
Low Level Supply Current	I_{CCL}	V_{CC}=5.5V, I_F=10mA V_E=0.5V	—	12	18	mA
Current Transfer Ratio	CTR	I_F=5.0mA, R_L=100Ω V_{CC}=5V, Ta=25°C	—	1000	—	%
Resistance (Input-Output)	R_S	V_S=500V, R.H.≦60% Ta=25°C (Note 4)	—	10^{12}	—	Ω
Capacitance (Input-Output)	C_S	f=1MHz, V_S=0, Ta=25°C (Note 4)	—	0.6	—	pF

* All typical values are at V_{CC}=5V, Ta=25°C.

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SWITCHING CHARACTERISTICS (Ta = 25°C, V_{CC} = 5V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to High Output Level (L→H)	t_{pLH}	1	R_L=350Ω, C_L=15pF I_F=7.5mA	—	60	120	ns
Propagation Delay Time to Low Output Level (H→L)	t_{pHL}		R_L=350Ω, C_L=15pF I_F=7.5mA	—	60	120	ns
Output Rise Fall Time (10~90%)	t_r, t_f		R_L=350Ω, C_L=15pF I_F=7.5mA	—	30	—	ns
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	2	R_L=350Ω, C_L=15pF I_F=7.5mA, V_{EH}=3.0V	—	25	—	ns
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		R_L=350Ω, C_L=15pF I_F=7.5mA, V_{EH}=3.0V	—	25	—	ns
Common Mode Transient Immunity at Logic High Output Level	CM_H	3	V_{CM}=200V, R_L=350Ω V_O (min.)=2V, I_F=0mA (Note 6)	—	200	—	V/μs
Common Mode Transient Immunity at Logic Low Output Level	CM_L		V_{CM}=200V, R_L=350Ω V_O (max.)=0.8V, I_F=5mA (Note 6)	—	−500	—	V/μs

Note 3 : A ceramic capacitor (0.1μF) should be connected from pin 8 and pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 1cm.

Note 4 : Device considered a two-terminal device : Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

Note 5 : Enable Input : No pull up resistor required as the device has an internal pull up resistor.

Note 6 : CM_L : The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V_{OUT}<0.8V).
CM_H : The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., V_{OUT}>2.0V).
Measured in volts per microsecond (V/μs).

Note 7 : Maximum electrostatic discharge voltage for any pins : 180V (C=200pF, R=0)

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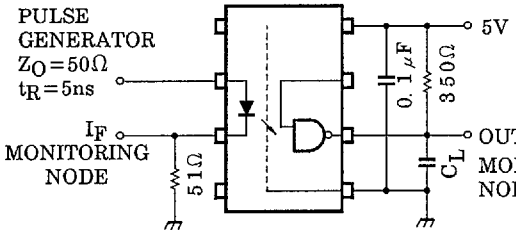
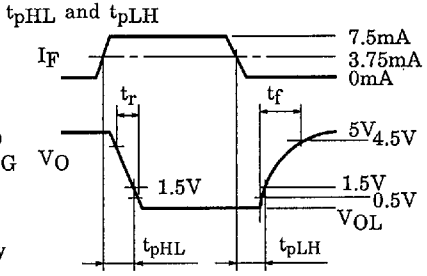
TEST CIRCUIT 1

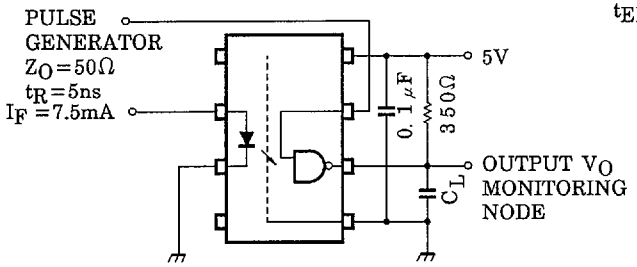


C_L is approximately 15pF which includes probe and stray wiring capacitance.

t_{pHL} and t_{pLH}

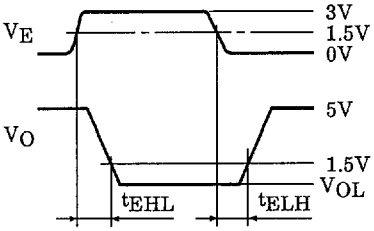


TEST CIRCUIT 2

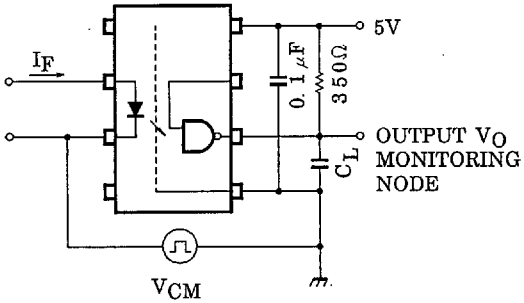


C_L is approximately 15pF which includes probe and stray wiring capacitance.

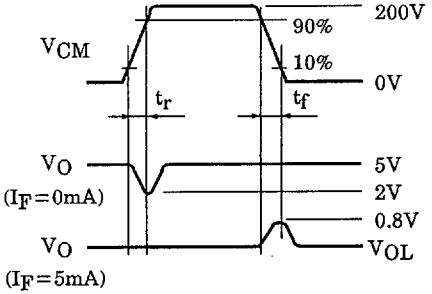
t_{ELH} and t_{EHL}



TEST CIRCUIT 3



Transient Immunity and Typical Waveform



$$CM_H = \frac{160\,(V)}{t_r\,(\mu s)},\ CM_L = \frac{160\,(V)}{t_f\,(\mu s)}$$

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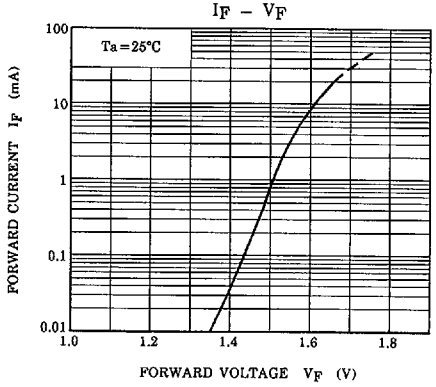
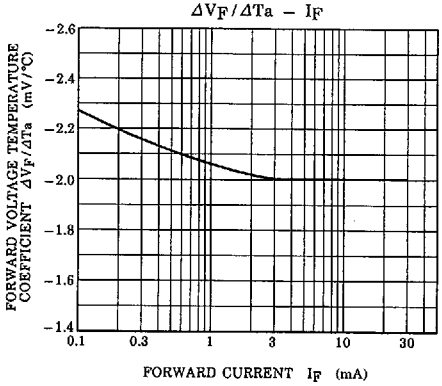
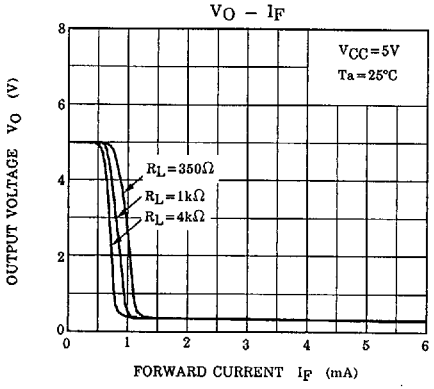
$I_F - V_F$



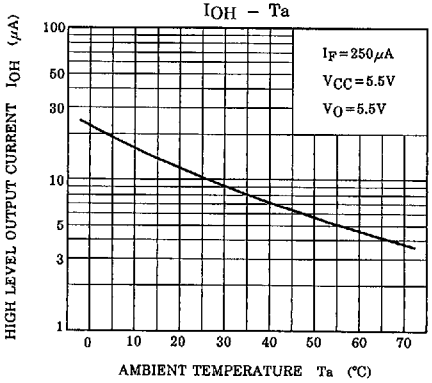
$\Delta V_F / \Delta Ta - I_F$



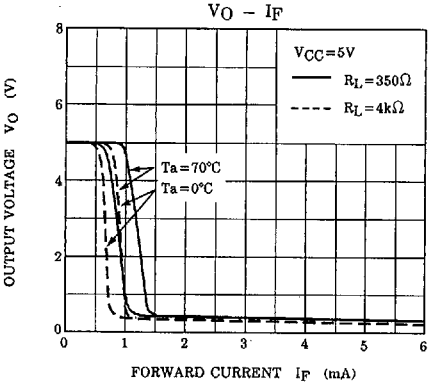
$V_O - I_F$



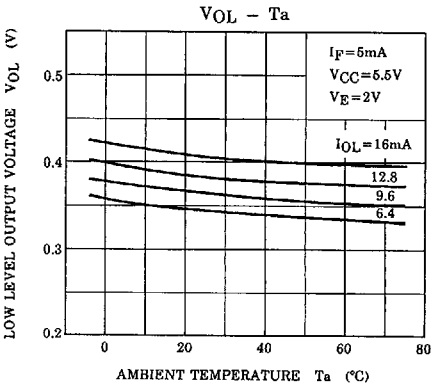
$I_{OH} - Ta$



$V_O - I_F$



$V_{OL} - Ta$



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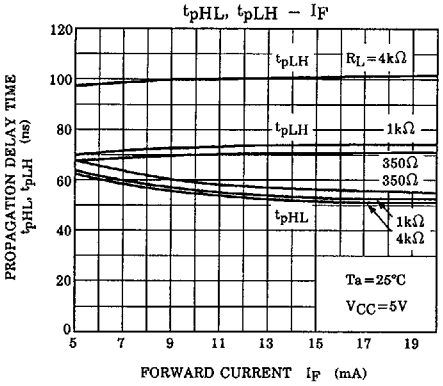
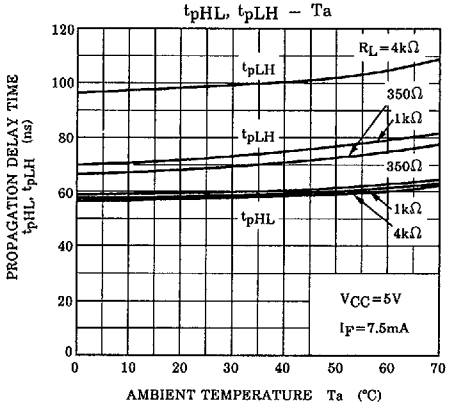
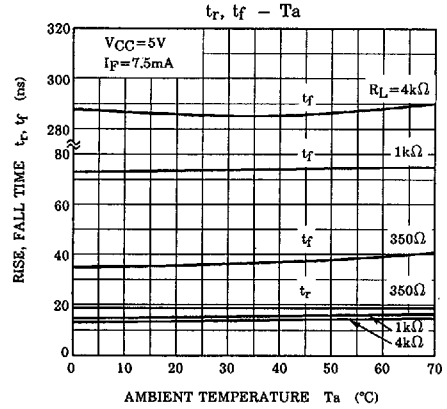
t_{pHL}, t_{pLH} – I_F



t_{pHL}, t_{pLH} – Ta



t_r, t_f – Ta



t_{EHL}, t_{ELH} – Ta