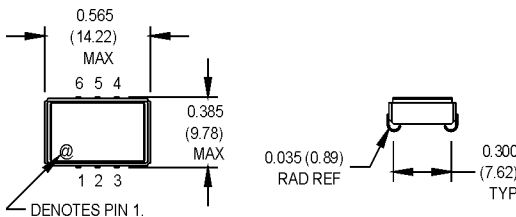


MPV3J Series

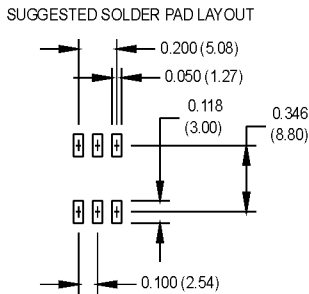
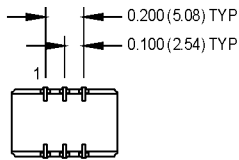
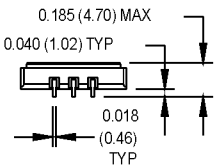
9x14 mm, 3.3 Volt, PECL/LVDS, VCXO



- Ultra low jitter VCXO approaching SAW jitter performance but with the temperature stability advantage of a crystal based resonator



All dimensions in inches (mm).



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Output Enable or N/C
3	Ground/Case
4	Output Q
5	Output Q or N/C
6	+Vcc

Ordering Information

MPV3J 1 0 B 1 P J -R MHz 00.0000

Product Series _____

Temperature Range _____

1: 0°C to +70°C 2: -40°C to +85°C

6: -20°C to +70°C 8: 0°C to +50°C

Stability _____

0: Nominal per APR selection

Output Type _____

B: Complementary, Enable (Enable High)

S: Complementary, Enable (Enable Low)

U: Complementary Output

Absolute Pull Range _____

1: ±50 ppm (±35 ppm typ. Stability)

8: ±25 ppm (±50 ppm typ. Stability)

***Symmetry/Output Logic Type** _____

P: 45/55% PECL Q: 40/60% PECL

Package/Lead Configurations _____

J: J-lead

RoHS Compliance _____

Blank: non-RoHS compliant part

-R: RoHS compliant part

Frequency (customer specified) _____

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	30		800	MHz	See Note 1	
Operating Temperature	T _A	(See Ordering Information)					
Storage Temperature	T _S	-55		+125	°C		
Frequency Stability	ΔF/F	(See Ordering Information)					
Aging						See Note 2	
1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz	
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz	
Pullability/APR		(See Ordering Information)					
Control Voltage	V _c	0	1.65	3.3	V	Pin 1 Voltage	
Linearity			5	10	%	Positive Monotonic Slope	
Modulation Bandwidth	f _m	10			kHz	-3 dB bandwidth	
Input Impedance	Z _{in}	50k			Ohms		
Input Voltage	V _{cc}	3.135	3.3	3.465	V		
Input Current	I _{cc}		60	70	mA		
Output Type						PECL/LVDS	
Load						See Note 4	
Symmetry (Duty Cycle)						V _{cc} - 1.3 VDC	
Output Skew				200	ps		
Differential Voltage	V _o	250	350	450	mV	LVDS	
Logic "1" Level	V _{oh}	V _{cc} - 1.02			V	PECL	
Logic "0" Level	V _{ol}			V _{cc} - 1.63	V	PECL	
Rise/Fall Time	T _r /T _f		0.35	0.55	ns	@ 20/80% LVPECL	
			0.50	1.0	Ns	@ 20/80% LVDS	
Enable/Disable Logic		80% V _{cc} min or N/C: output active					Output Option B
		20% V _{cc} max: output disables to high-Z					
		PECL low, GND, or N/C - output active					Output Option S
		PECL high - output disables to high-Z					
Start up Time			5		ms		
Phase Jitter	φ _J						
@ 155.52 MHz			0.3	0.55	ps RMS	Integrated 12 kHz - 20 MHz	
@ 622.08 MHz			0.25	0.5	ps RMS	Integrated 12 kHz - 20 MHz	
Phase Noise (Typical)							
@ 155.52 MHz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier	
	-50	-80	-115	-135	-140	dBc/Hz	

Note 1: Consult factory for exact frequency availability

Note 2: Stability given for deviation over temperature

Note 3: APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging

Note 4: PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.

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