BSR58LT1

JFET Chopper Transistor

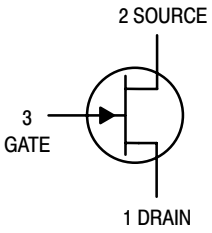
N–Channel – Depletion

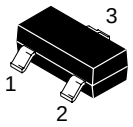
ON Semiconductor®

http://onsemi.com

MAXIMUM RATINGS

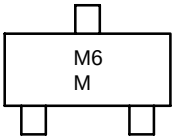
Rating	Symbol	Value	Unit
Drain–Gate Voltage	V_{DG}	–40	Vdc
Gate–Source Voltage	V_{GS}	–35	Vdc
Gate Current	I_G	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	 350 2.8	 mW mW/°C
Lead Temperature	T_L	300	°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C





SOT–23
CASE 318
STYLE 10

MARKING DIAGRAM



M6 = Specific Device Code
M = Date Code

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage (I_G = –1.0 μAdc)	$V_{(BR)GSS}$	40	–	Vdc
Gate Reverse Current (V_{GS} = –15 Vdc)	I_{GSS}	–	–1.0	nAdc
Gate Source Cutoff Voltage (V_{DS} = 5.0 Vdc, I_D = 1.0 μAdc)	$V_{GS(off)}$	–0.8	–4.0	Vdc
Drain–Cutoff Current (V_{DS} = 5.0 Vdc, V_{GS} = –10 Vdc)	$I_{D(off)}$	–	1.0	nAdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current (Note 1) (V_{DS} = 15 Vdc)	I_{DSS}	8.0	80	mAdc
Static Drain–Source On Resistance (V_{DS} = 0.1 Vdc)	$r_{DS(on)}$	–	60	Ω
Drain Gate and Source Gate On–Capacitance (V_{DS} = V_{GS} = 0, f = 1.0 MHz)	$C_{dg(on)}$ + $C_{sg(on)}$	–	28	pF
Drain Gate Off–Capacitance (V_{GS} = –10 Vdc, f = 1.0 MHz)	$C_{dg(off)}$	–	5.0	pF
Source Gate Off–Capacitance (V_{GS} = –10 Vdc, f = 1.0 MHz)	$C_{sg(off)}$	–	5.0	pF

1. Pulse Width = 300 μs, Duty Cycle = 3.0%.

ORDERING INFORMATION

Device	Package	Shipping
BSR58LT1	SOT–23	3000/Tape & Reel

TYPICAL SWITCHING CHARACTERISTICS

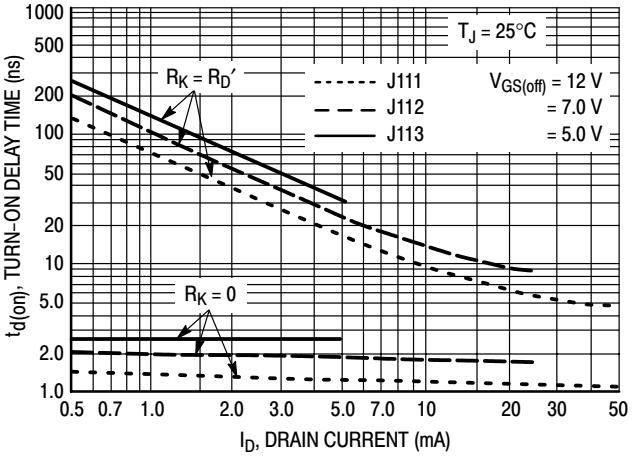


Figure 1. Turn–On Delay Time

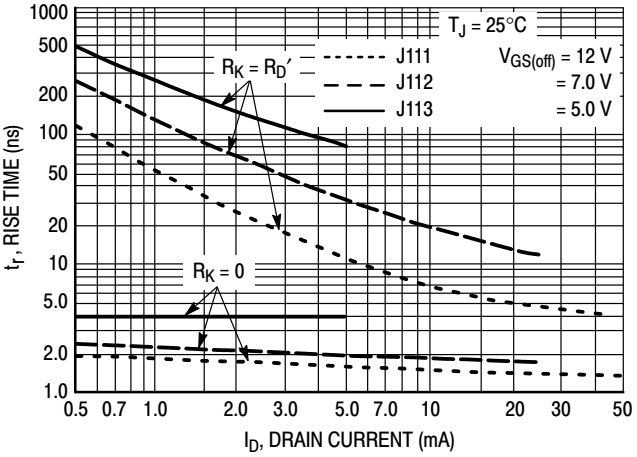


Figure 2. Rise Time

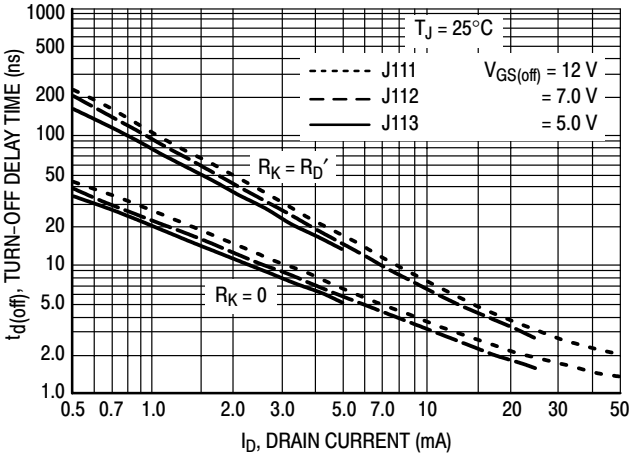


Figure 3. Turn–Off Delay Time

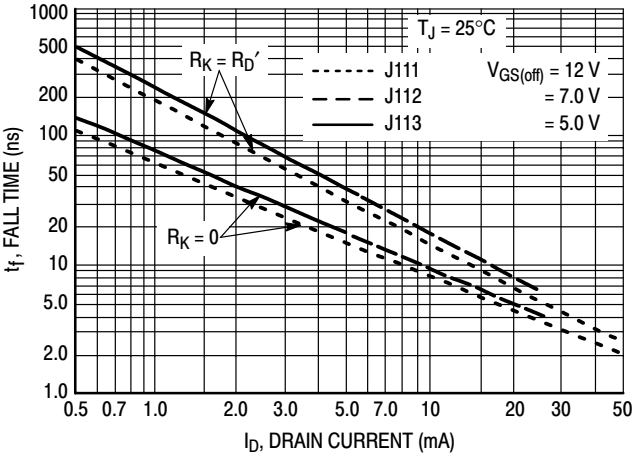


Figure 4. Fall Time

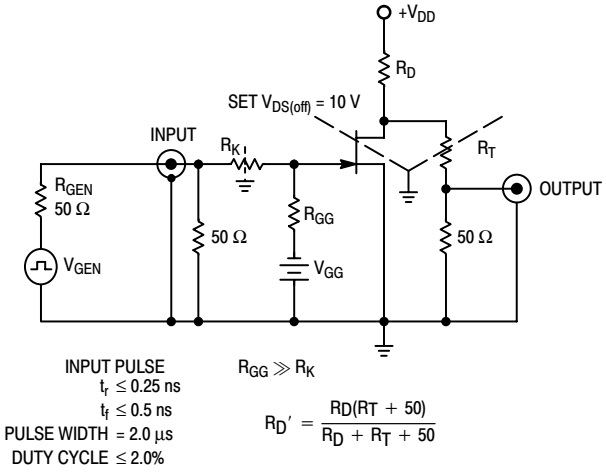


Figure 5. Switching Time Test Circuit

NOTE 1

The switching characteristics shown above were measured using a test circuit similar to Figure 5. At the beginning of the switching interval, the gate voltage is at Gate Supply Voltage ($-V_{GG}$). The Drain–Source Voltage (V_{DS}) is slightly lower than Drain Supply Voltage (V_{DD}) due to the voltage divider. Thus Reverse Transfer Capacitance (C_{rss}) or Gate–Drain Capacitance (C_{gd}) is charged to $V_{GG} + V_{DS}$.

During the turn–on interval, Gate–Source Capacitance (C_{gs}) discharges through the series combination of R_{Gen} and R_K. C_{gd} must discharge to $V_{DS(on)}$ through R_G and R_K in series with the parallel combination of effective load impedance (R'_D) and Drain–Source Resistance (r_{ds}). During the turn–off, this charge flow is reversed.

Predicting turn–on time is somewhat difficult as the channel resistance r_{ds} is a function of the gate–source voltage. While C_{gs} discharges, V_{GS} approaches zero and r_{ds} decreases. Since C_{gd} discharges through r_{ds}, turn–on time is non–linear. During turn–off, the situation is reversed with r_{ds} increasing as C_{gd} charges.

The above switching curves show two impedance conditions; 1) R_K is equal to R_D, which simulates the switching behavior of cascaded stages where the driving source impedance is normally the load impedance of the previous stage, and 2) $R_K = 0$ (low impedance) the driving source impedance is that of the generator.

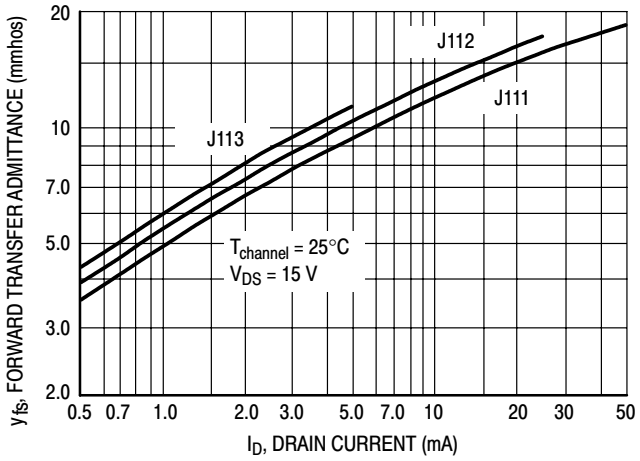


Figure 6. Typical Forward Transfer Admittance

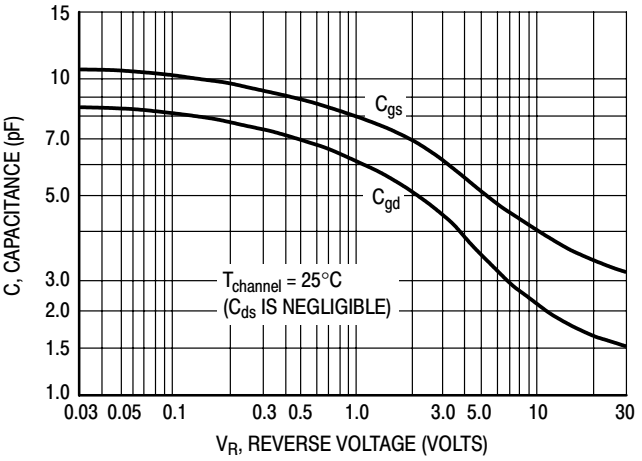


Figure 7. Typical Capacitance

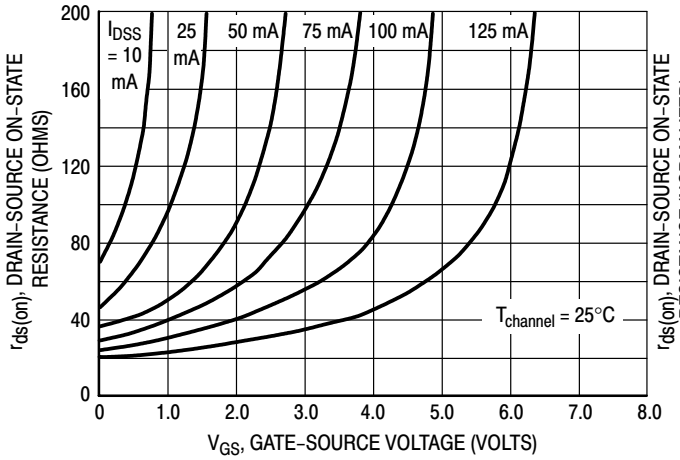


Figure 8. Effect of Gate–Source Voltage On Drain–Source Resistance

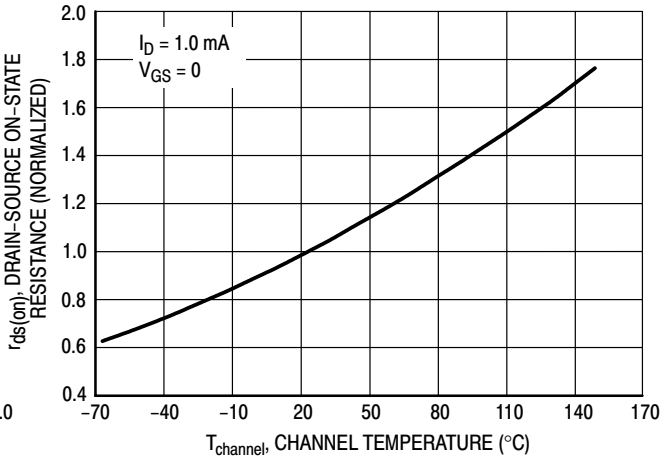


Figure 9. Effect of Temperature On Drain–Source On–State Resistance

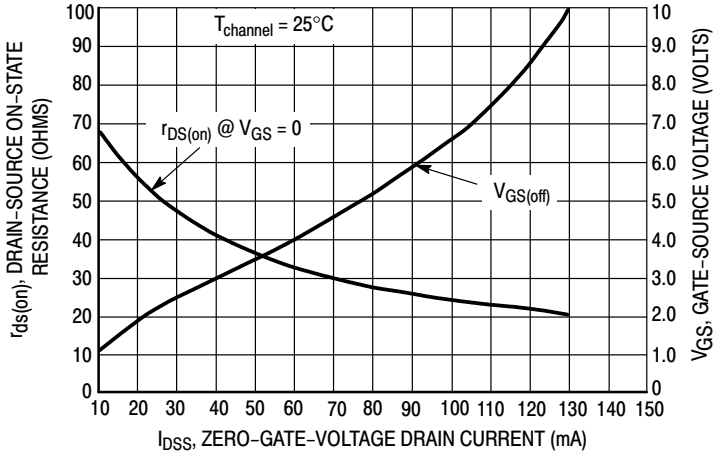


Figure 10. Effect of I_{DSS} On Drain–Source Resistance and Gate–Source Voltage

NOTE 2

The Zero–Gate–Voltage Drain Current (I_{DSS}), is the principle determinant of other J-FET characteristics. Figure 10 shows the relationship of Gate–Source Off Voltage ($V_{GS(off)}$ and Drain–Source On Resistance ($r_{ds(on)}$) to I_{DSS}. Most of the devices will be within ±10% of the values shown in Figure 10. This data will be useful in predicting the characteristic variations for a given part number.

For example:

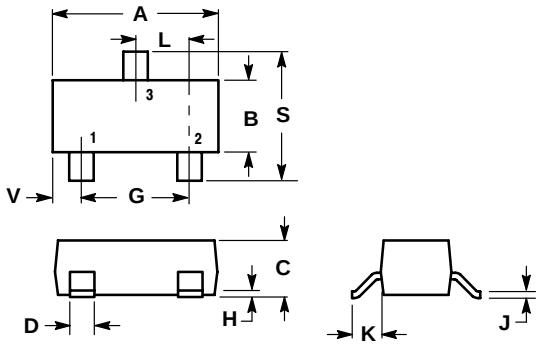
Unknown

$r_{ds(on)}$ and V_{GS} range for an J112

The electrical characteristics table indicates that an J112 has an I_{DSS} range of 25 to 75 mA. Figure 10, shows $r_{ds(on)}$ = 52 Ohms for I_{DSS} = 25 mA and 30 Ohms for I_{DSS} = 75 mA. The corresponding V_{GS} values are 2.2 volts and 4.8 volts.

PACKAGE DIMENSIONS

SOT–23 (TO–236)
CASE 318–08
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318–03 AND –07 OBSOLETE, NEW STANDARD 318–08.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
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