Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (2K X 8 BIT)

IDT6116SA
IDT6116LA

NOTICE
SEE ORDER OF DATA FOR ERRATA INFORMATION

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed
  - — Military: 20/25/35/45/55/70/90/120/150ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low-power operation
  - — IDT6116SA
    Active: 180mW (typ.)
    Standby: 100µW (typ.)
  - — IDT6116LA
    Active: 160mW (typ.)
    Standby: 20µW (typ.)
- Battery backup operation - 2V data retention voltage (LA version only)
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (± 10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin THINDIP and plastic DIP, 24-, 28- and 32-pin LCC, 24-pin SOIC and 24-lead CERPACK
- Military product compliant to MIL-STD-833, Class B
- Standard Military Drawing# 84036 is listed on this function. Refer to Section 2/page 2-4

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology - CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

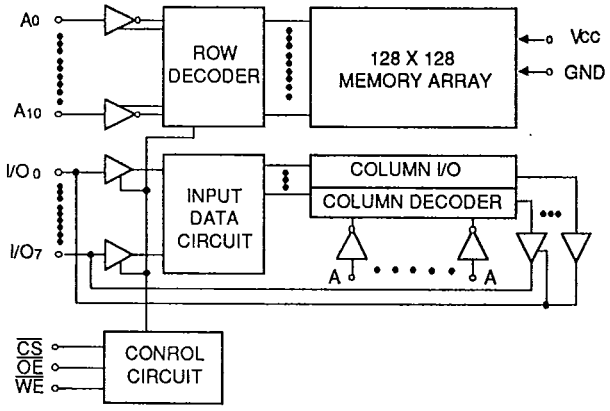
Access times as fast as 15ns are available with maxim power consumption of only 666mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains high. In the standby mode, the low-power device consumes less than 20µW typically. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-, 28- and 32-pin leadless chip carriers, 24-lead CERPACK, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

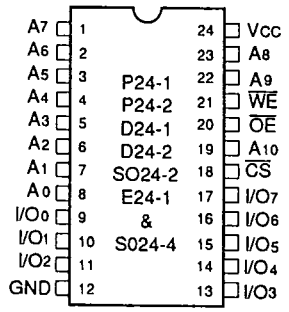


2954 drw 02

CEMOS is a trademark of Integrated Device Technology, Inc.

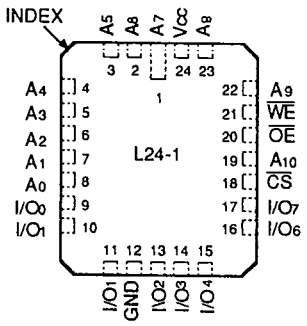
1-46-23-12

PIN CONFIGURATIONS



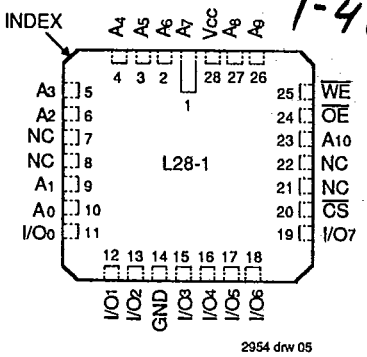
2954 drw 01

DIP/SOIC/CERPACK/SOJ
TOP VIEW



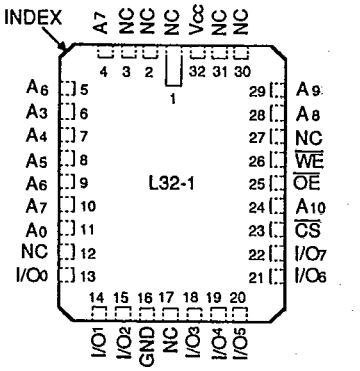
2954 drw 03

24-PIN LCC
TOP VIEW



2954 drw 05

28-PIN LCC
TOP VIEW



2954 drw 04

32-PIN LCC
TOP VIEW

PIN NAMES

A_0- A_{10}	Address	$\overline{WE}$	Write Enable
I/O_0 - I/O_7	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
Vcc	Power		

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to + 7.0	V
T_A	Operating Temperature	0 to + 70	-55 to + 125	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	-65 to + 135	°C
T_{STG}	Storage Temperature	-55 to + 125	-65 to + 150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	3.5	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V
CL	Output Load	—	—	30	pF

NOTE:
1. VIL = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions		IDT6116SA Min.	IDT6116SA Typ.(1)	IDT6116SA Max.	IDT6116LA Min.	IDT6116LA Typ.(1)	IDT6116LA Max.	Unit
|ILI|	Input Leakage Current	Vcc = Max., VIN = GND to Vcc	MIL.	—	—	10	—	—	10	µA
			COM'L.	—	—	5	—	—	2	
|ILO|	Output Leakage Current	Vcc = Max. $\overline{CS}$ = VIH, VOUT = GND to Vcc	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
VOL	Output Low Voltage	IOL = 8mA, Vcc = Min.		—	—	0.4	—	—	0.4	V
VOH	Output High Voltage	IOH = -4mA, Vcc = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at Vcc = 5.0V, + 25°C ambient.

5

AC ELECTRICAL CHARACTERISTICS (1)

Vcc = 5.0V ± 10%, VLC = 0.2V, VHC = Vcc - 0.2V

Symbol	Parameter	Power	6116SA15(2) 6116LA15(2) Com'l.	6116SA15(2) 6116LA15(2) Mil.	6116SA20 6116LA20 Com'l.	6116SA20 6116LA20 Mil.	6116SA25 6116LA25 Com'l.	6116SA25 6116LA25 Mil.	6116SA35 6116LA35 Com'l.	6116SA35 6116LA35 Mil.	Unit
ICC1	Operating Power Supply Current, $\overline{CS}$ = VIL, Outputs Open, Vcc = Max., f = 0	SA	125	—	110	130	100	110	80	90	mA
		LA	115	—	100	120	90	105	75	85	
ICC2	Dynamic Operating Current, $\overline{CS}$ = VIL, Vcc = Max., Outputs Open, f = fMAX(4)	SA	150	—	130	150	120	135	100	115	mA
		LA	140	—	120	140	110	125	95	105	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ VIH, Vcc = Max., Outputs Open, f = fMAX(4)	SA	40	—	40	50	40	45	25	35	mA
		LA	35	—	35	45	35	40	25	30	
ISB1	Full Standby Power Supply Current (CMOS Level), $\overline{CS}$ ≥ VHC, Vcc = Max., VIN ≥ VHC or VIN ≤ VLC, f = 0	SA	2	—	2	10	2	10	2	10	mA
		LA	0.1	—	0.1	0.9	0.1	0.9	0.1	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. -55°C to + 125°C temperature range only.
4. fMAX = 1/tRC

T-46-23-12

AC ELECTRICAL CHARACTERISTICS [1] (Continued)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA45 6116LA45 Com'l.	6116SA45 6116LA45 Mil.	6116SA55[3] 6116LA55[3] Com'l.	6116SA55[3] 6116LA55[3] Mil.	6116SA70[3] 6116LA70[3] Com'l.	6116SA70[3] 6116LA70[3] Mil.	6116SA90[3] 6116LA90[3] Com'l.	6116SA90[3] 6116LA90[3] Mil.	6116SA120[3] 6116LA120[3] Com'l.	6116SA120[3] 6116LA120[3] Mil.	6116SA150[3] 6116LA150[3] Com'l.	6116SA150[3] 6116LA150[3] Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	SA	80	90	—	90	—	90	—	90	—	90	—	90	mA
		LA	75	85	—	85	—	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Outputs Open, f = f_{MAX}[4]	SA	100	100	—	100	—	100	—	100	—	1005	—	90	mA
		LA	90	95	—	90	—	90	—	85	—	85	—	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[4]	SA	25	25	—	25	—	25	—	25	—	25	—	25	mA
		LA	20	20	—	20	—	20	—	25	—	15	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0	SA	2	10	—	10	—	10	—	10	—	10	—	10	mA
		LA	0.1	0.9	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. -55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

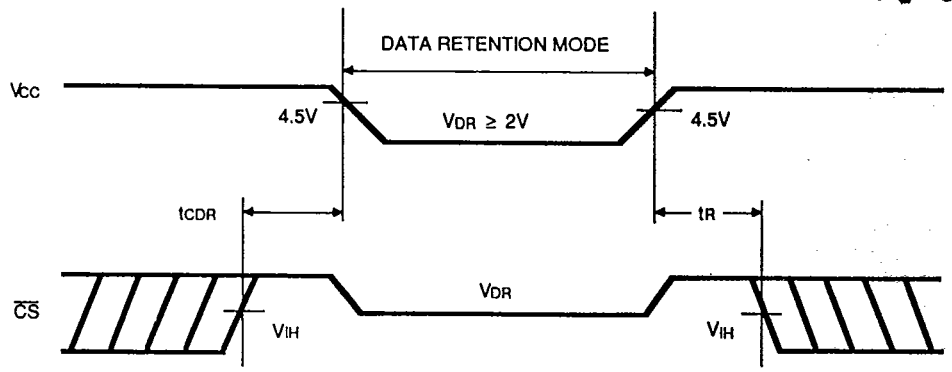
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.[1] Vcc @ 2.0V	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC}	MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CCR}[3]	Data Deselect to Data Retention Time	V_{IN} ≥ V_{HC} or ≤ V_{LC}		—	0	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = + 25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed, but not tested.

T-46-23-12

LOW Vcc DATA RETENTION WAVEFORM



2954 drw 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

5

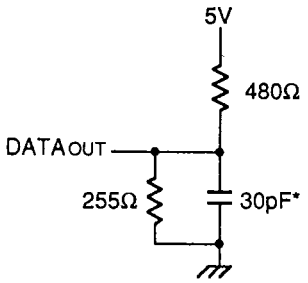


Figure 1. Output Load

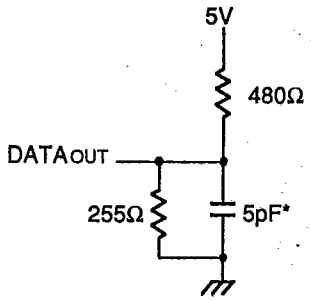


Figure 2. Output Load
(for tOLZ, tCLZ, tOHZ, tWHZ, tCHZ, tOW)

2954 drw 08

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

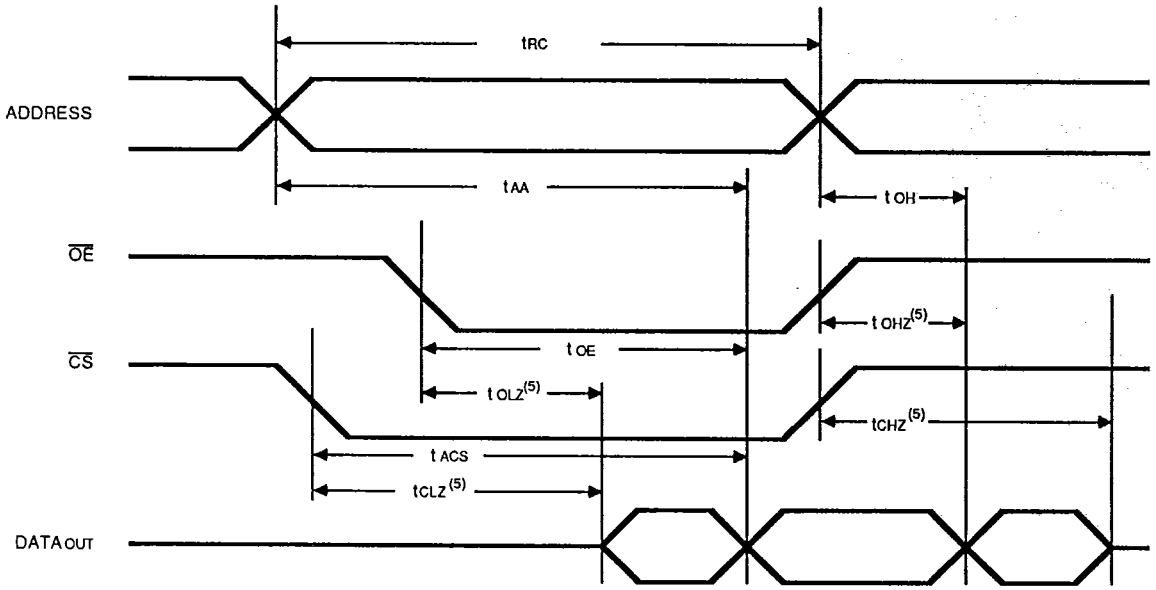
Symbol	Parameter	6116SA15[1] 6116LA15[1] Min.	6116SA15[1] 6116LA15[1] Max.	6116SA20 6116LA20 Min.	6116SA20 6116LA20 Max.	6116SA25 6116LA25 Min.	6116SA25 6116LA25 Max.	6116SA35 6116LA35 Min.	6116SA35 6116LA35 Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
tCLZ	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	10	—	13	—	20	ns
tOLZ	Output Enable to Output in Low Z[3]	0	—	0	—	5	—	5	—	ns
tCHZ	Chip Deselect to Output in High Z[3]	—	10	—	11	—	12	—	15	ns
tOHZ	Output Disable to Output in High Z[3]	—	8	—	8	—	10	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	5	—	5	—	ns

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges) (Continued)

Symbol	Parameter	6116SA45 6116LA45 Min.	6116SA45 6116LA45 Max.	6116SA55[2] 6116LA55[2] Min.	6116SA55[2] 6116LA55[2] Max.	6116SA70[2] 6116LA70[2] Min.	6116SA70[2] 6116LA70[2] Max.	6116SA90[2] 6116LA90[2] Min.	6116SA90[2] 6116LA90[2] Max.	6116SA120[2] 6116LA120[2] Min.	6116SA120[2] 6116LA120[2] Max.	6116SA150[2] 6116LA150[2] Min.	6116SA150[2] 6116LA150[2] Max.	Unit
READ CYCLE														
tRC	Read Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tAA	Address Access Time	—	45	—	55	—	70	—	90	—	120	—	150	ns
tACS	Chip Select Access Time	—	45	—	50	—	65	—	90	—	120	—	150	ns
tCLZ	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	25	—	40	—	50	—	60	—	80	—	100	ns
tOLZ	Output Enable to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Deselect to Output in High Z[3]	—	20	—	30	—	35	—	40	—	40	—	40	ns
tOHZ	Output Disable to Output in High Z[3]	—	15	—	30	—	35	—	40	—	40	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns

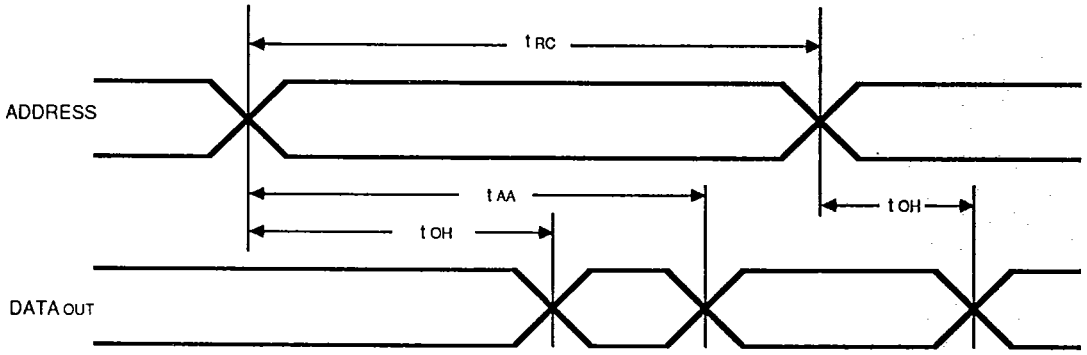
NOTES:
1. 0°C to + 70°C temperature range only.
2. -55°C to + 125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



2954 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2, 4]

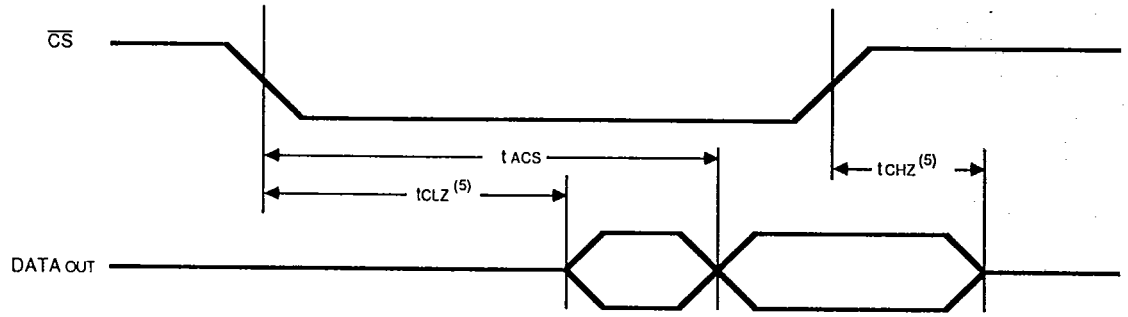


2954 drw 10

NOTE:
1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig.)

T-46-23-12

TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



2954 drw 11

NOTE:
1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig.)

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15(1) 6116LA15(1)		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	15	—	20	—	25	—	35	—	ns
tCW	Chip Select to End of Write	13	—	15	—	17	—	25	—	ns
tAW	Address Valid to End of Write	14	—	15	—	17	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tOHZ	Output Disable to Output in High Z(3)	—	8	—	8	—	10	—	13	ns
tWHZ	Write to Output in High Z(3)	—	7	—	8	—	16	—	20	ns
tDW	Data to Write Time Overlap	12	—	12	—	13	—	15	—	ns
tDH	Data Hold from Write Time(4)	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write(3,4)	0	—	0	—	0	—	0	—	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.

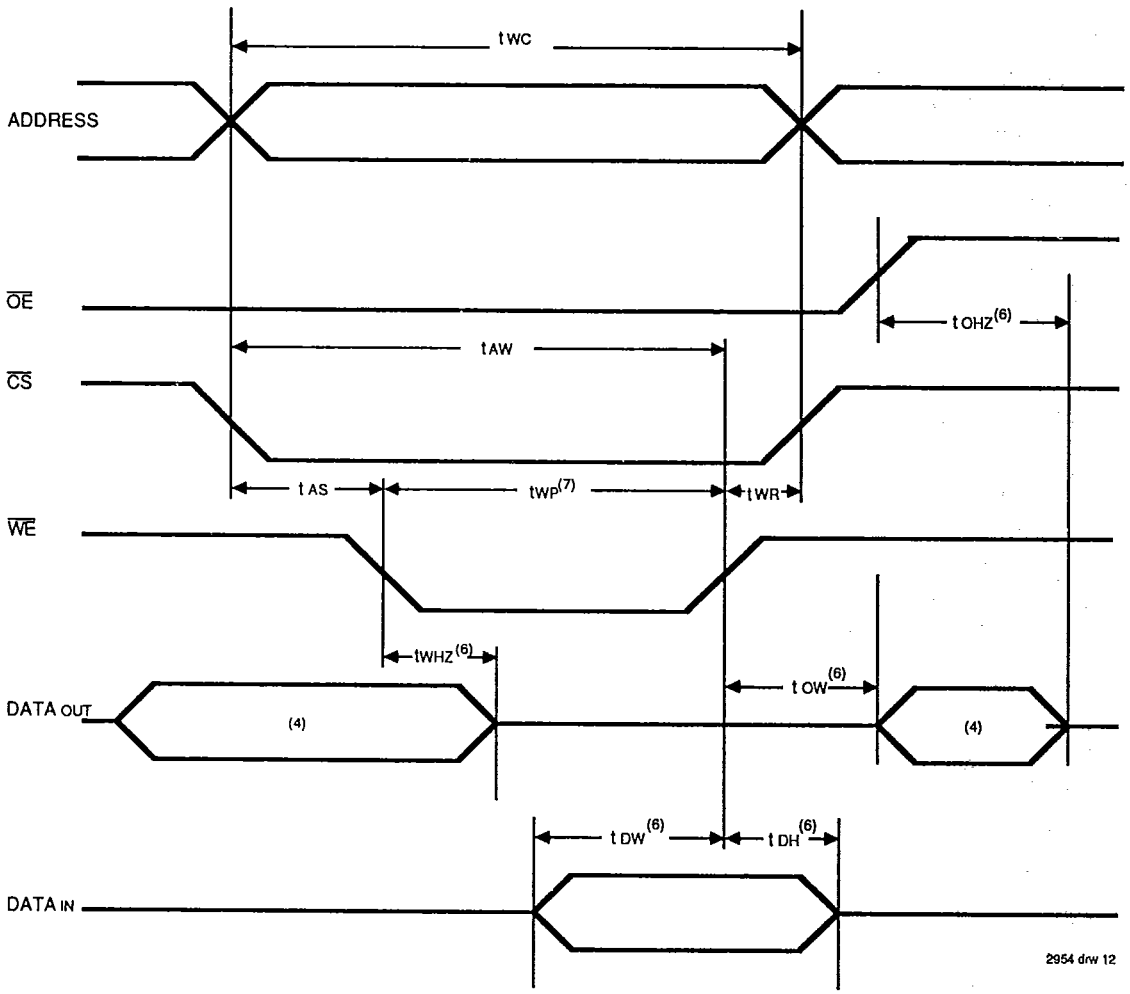
AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges) (Continued)

Symbol	Parameter	6116SA45 6116LA45		6116SA55[2] 6116LA55[2]		6116SA70[2] 6116LA70[2]		6116SA90[2] 6116LA90[2]		6116SA120[2] 6116LA120[2]		6116SA150[2] 6116LA150[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE														
tWC	Write Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tCW	Chip Select to End of Write	30	—	40	—	40	—	55	—	70	—	90	—	ns
tAW	Address Valid to End of Write	30	—	45	—	65	—	80	—	105	—	120	—	ns
tAS	Address Set-up Time	0	—	5	—	15	—	15	—	20	—	20	—	ns
tWP	Write Pulse Width	25	—	40	—	40	—	55	—	70	—	90	—	ns
tWR	Write Recovery Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOHZ	Output Disable to Output in High Z[3]	—	25	—	30	—	35	—	40	—	40	—	40	ns
tWHZ	Write to Output in High Z[3]	—	25	—	30	—	35	—	40	—	40	—	40	ns
tDW	Data to Write Time Overlap	20	—	25	—	30	—	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time[4]	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOW	Output Active from End of Write[3,4]	0	—	0	—	0	—	0	—	0	—	0	—	ns

5

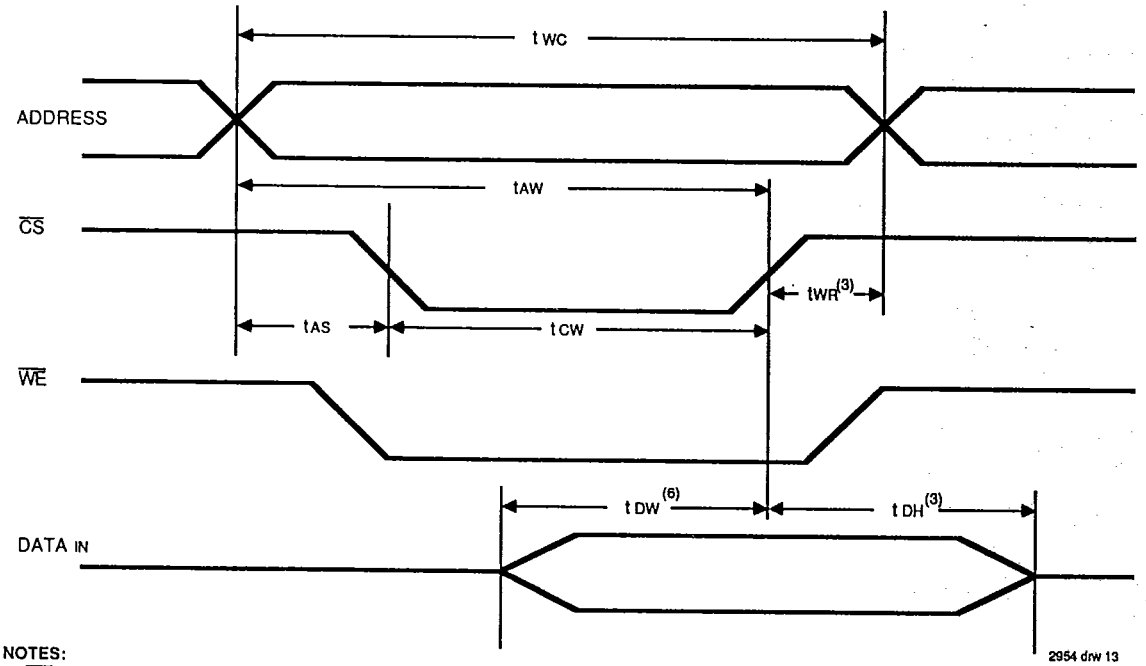
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tow values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tow.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state wih a 5pF load (includng scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be a short as the specified tWP.

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state wih a 5pF load (includng scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be a short as the specified tWP.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High Z
Read	L	L	H	DATAOUT
Read	L	H	H	High Z
Write	L	X	L	DATAIN

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

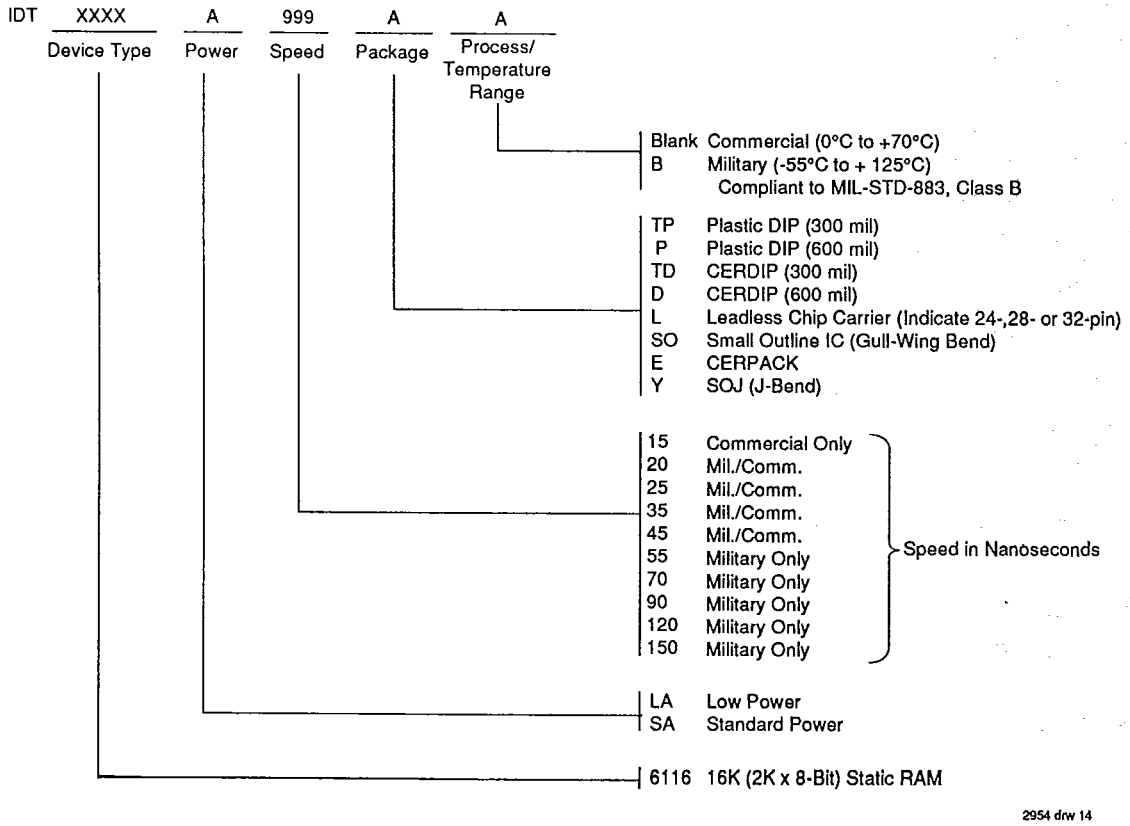
Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

THERMAL RESISTANCE (Typical)

Package	Pin Count	ΦJA	ΦJC	Unit
300 Mil Plastic DIP	24	54-58	28-32	°C/ WATT
600 Mil Plastic DIP	24	53-56	25-30	
300 Mil CERDIP	24	48-52	24-28	
600 Mil CERDIP	24	50-55	17-25	
Flatpack	24	85-90	24-28	
LCC	24	85-110	30-45	
LCC	28	85-90	28-35	
LCC	32	80-90	25-35	
SOIC, SOJ	24	45-70	25-30	

ORDERING INFORMATION



2954 drw 14