

KH207

Low Distortion Wideband Op Amp

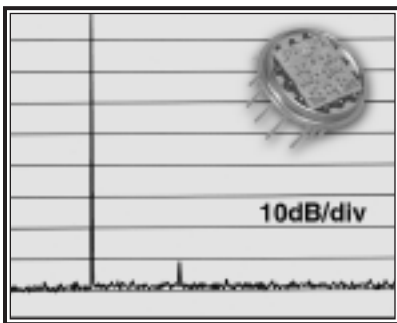
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Features

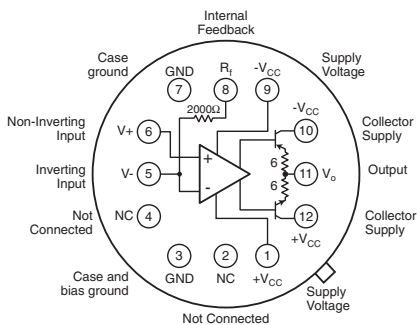
- -80/-85dBc 2nd/3rd HD at 20MHz
- -3dB bandwidth of 170MHz
- 0.1% settling in 22ns
- Complete overdrive protection
- 2400V/ μ s slew rate
- 3M Ω input resistance
- Output may be current limited
- Direct replacement for CLC207

Applications

- Fast, precision A/D conversion
- Automatic test equipment
- Input/output amplifiers
- Photodiode, CCD preamps
- High-speed modems, radios
- Line drivers



Bottom View



Pin 8 provides access to a 2000 Ω feedback resistor which can be connected to the output or left open if an external feedback resistor is desired.

General Description

The KH207 is a wideband, low distortion operational amplifier designed specifically for applications requiring both high speed and wide dynamic range. Utilizing a proprietary current feedback architecture, the KH207 offers performance far superior to that of conventional voltage feedback op amps.

The most attractive feature of the KH207 is its extremely low distortion: -80/-85dBc 2nd/3rd harmonics at 20MHz ($2V_{pp}$, $R_L = 200\Omega$). The KH207 also provides -3dB bandwidth of 170MHz at a gain of +20, settles to 0.1% in 22ns and slews at a rate of 2400V/ μ s. The combination of these features positions the KH207 as the right choice for high speed applications requiring exceptional signal purity.

High speed, high resolution A/D and D/A converter systems requiring low distortion operation will find the KH207 an excellent choice. Wide dynamic range systems such as radar and communication receivers will find that the KH207's low harmonic distortion and low noise make it an attractive high speed solution.

The addition of the KH207 to the KH205/206 Series of high speed operational amplifiers broadens the selection of features available from which to choose. The KH205 offers low power operation, the KH206 offers higher drive operation, and the KH207 offers operation with extremely low distortion, all of which are pin compatible and overdrive protected.

The KH207 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

KH207AI	-25°C to +85°C	12-pin TO-8 can
KH207AK	-55°C to +125°C	12-pin TO-8 can, features burn-in & hermetic testing
KH207AM	-55°C to +125°C	12-pin TO-8 can, environmentally screened and electrically tested to MIL-STD-883
KH207HXC	-55°C to +125°C	SMD#: 5962-9097701HXC
KH207HXA	-55°C to +125°C	SMD#: 5962-9097701HXA

Typical Performance

Parameter	Gain Setting						Units
	+7	+20	+50	-1	-20	-50	
-3dB bandwidth	220	170	80	220	130	80	MHz
rise time	1.7	2.2	4.7	1.7	2.9	4.7	ns
slew rate	2.4	2.4	2.4	2.4	2.4	2.4	V/ns
settling time (to 0.1%)	22	20	21	20	19	20	ns

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KH207 Electrical Characteristics ($A_v = +20V$, $V_{CC} = \pm 15V$, $R_L = 200\Omega$, $R_f = 2k\Omega$; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN & MAX RATINGS			UNITS	SYM
Ambient Temperature	KH207AI	+25°C	-25°C	+25°C	+85°C		
Ambient Temperature	KH207AK/AM/HXC/HXA	+25°C	-55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
+ -3dB bandwidth	$V_o < 2V_{pp}$	170	>140	>140	>125	MHz	SSBW
large-signal bandwidth	$V_o < 10V_{pp}$	100	>72	>80	>80	MHz	FPBW
gain flatness	$V_o < 2V_{pp}$						
+ peaking	0.1 to 35MHz	0	<0.3	<0.3	<0.5	dB	GFPL
+ peaking	>35MHz	0	<0.8	<0.5	<0.8	dB	GFPH
+ rolloff	at 70MHz	-	<0.8	<0.8	<0.8	dB	GFR
group delay	to 70MHz	$3.0 \pm .2$	-	-	-	ns	GD
linear phase deviation	to 50MHz	0.8	<3.0	<2.0	<3.0	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	2V step	2.2	<2.6	<2.6	<3.0	ns	TRS
	10V step	4.8	<5.5	<5.5	<5.5	ns	TRL
settling time to 0.1%	10V step, note 2	22	<27	<27	<27	ns	TS
to 0.05%	10V step, note 2	24	<30	<30	<30	ns	TSP
overshoot	5V step	7	<14	<14	<14	%	OS
slew rate	20V _{pp} at 50MHz	2.4	>1.8	>2.0	>2.0	V/ns	SR
NOISE AND DISTORTION RESPONSE							
+ 2nd harmonic distortion	+ 2V _{pp} , 20MHz, $R_L = 200\Omega$	-80	<-68	<-76	<-76	dBc	HD2
	2V _{pp} , 20MHz, $R_L = 100\Omega$	-69	<-64	<-64	<-64	dBc	HD2
+ 3rd harmonic distortion	+ 2V _{pp} , 20MHz, $R_L = 200\Omega$	-85	<-76	<-76	<-76	dBc	HD3
	2V _{pp} , 20MHz, $R_L = 100\Omega$	-69	<-64	<-64	<-64	dBc	HD3
equivalent input noise							
voltage	>100kHz	1.6	<1.8	<1.8	<1.8	nV/√Hz	VN
inverting current	>100kHz	20	<23	<23	<23	pA/√Hz	ICN
non-inverting current	>100kHz	2.2	<2.5	<2.5	<2.5	pA/√Hz	NCN
noise floor	>100kHz	-158	<-157	<-157	<-157	dBm(1Hz)	SNF
integrated noise	1kHz to 150MHz	33	<38	<38	<38	μV	INV
integrated noise	5MHz to 150MHz	33	<38	<38	<38	μV	INV
STATIC, DC PERFORMANCE							
* input offset voltage		3.5	<8.0	<8.0	<11.0	mV	VIO
average temperature coefficient		11	<25	<25	<25	μV/°C	DVIO
* input bias current	non-inverting	3.0	<25	<15	<15	μA	IBN
average temperature coefficient		15	<100	<100	<100	nA/°C	DIBN
* input bias current	inverting	2.0	<22	<10	<25	μA	IBI
average temperature coefficient		20	<150	<150	<150	nA/°C	DIBI
* power supply rejection ratio		69	>55	>55	>55	dB	PSRR
common mode rejection ratio		60	>50	>50	>50	dB	CMRR
* supply current	no load	25	<27	<27	<29	mA	ICC
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance	DC	3.0	>1.0	>1.0	>1.0	MΩ	RIN
non-inverting input capacitance	70MHz	5.0	<7.0	<7.0	<7.0	pF	CIN
output impedance	DC	-	<0.1	<0.1	<0.1	Ω	RO
output voltage range	no load	±12	>±11	>±11	>±11	V	VO
internal feedback resistor		2.0	-	-	-	kΩ	RF
absolute tolerance		-	-	<0.2	-	%	RFA
temperature coefficient		-	-	-100 ±40	-	ppm/°C	RFTC
inverting input current self limit		2.2	<3.0	<3.0	<3.2	mA	ICL

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

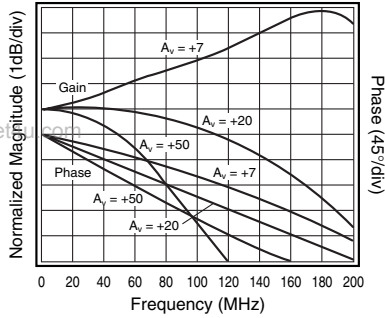
V_{CC}	±20V
I_o	±150mA
common mode input voltage, V_o	$ V_{CC} > 15V \pm(29 - V_{CC})V$ $ V_{CC} \leq 15V \pm(V_{CC} - 1)V$
differential input voltage	±3V
thermal resistance	(see thermal model)
junction temperature	+175°C
operating temperature	AI: -25°C to +85°C AK/AM/HXC/HXA: -55°C to +125°C
storage temperature	-65°C to +150°C
lead temperature (soldering 10s)	+300°C

Recommended Operating Conditions

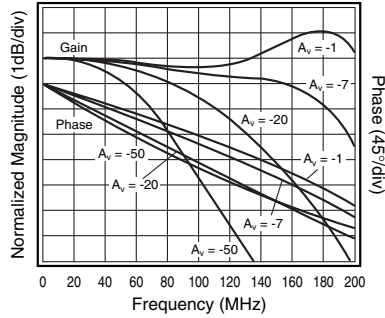
V_{CC}	±5V to ±15V
I_o	±100mA
common mode input voltage	±(V_{CC} - 5)V
gain range	+7 to +50, -1 to -50
note 1:	* AI/AK/AM/HXC/HXA 100% tested at +25°C † AK/AM/HXC/HXA 100% tested at +25°C and sample tested at -55°C and +125°C
	† AI sample tested at +25°C
note 2:	Settling time specifications require the use of an external feedback resistor (2kΩ).

KH207 Typical Performance Characteristics ($T_A = +25^\circ\text{C}$, $A_V = +20$, $V_{CC} = \pm 15\text{V}$, $R_f = 20\Omega$, $R_L = 200\Omega$; unless specified)

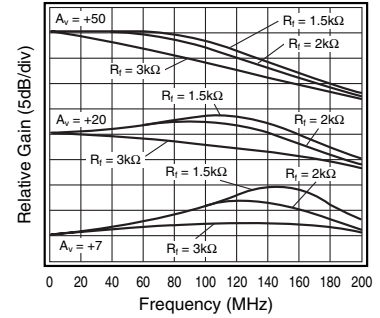
Non-Inverting Frequency Response



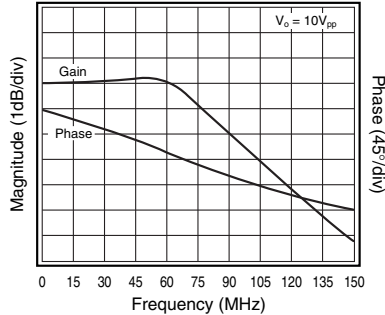
Inverting Frequency Response



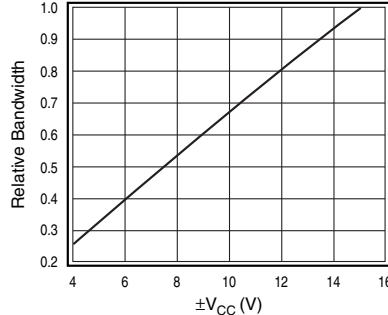
Frequency Response vs. External R_f



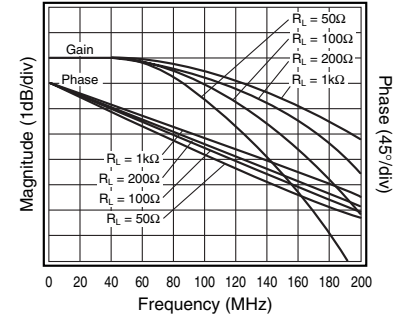
Large Signal Gain and Phase



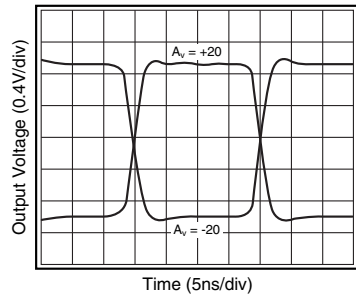
Relative Bandwidth vs. V_{CC}



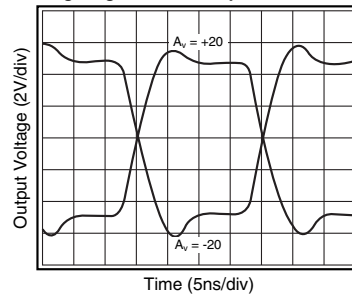
Gain and Phase for Various Loads



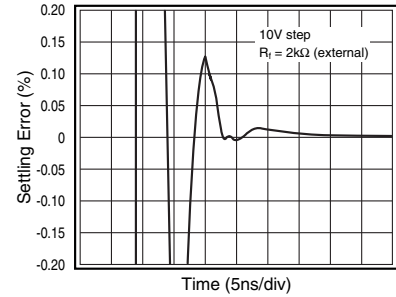
Small Signal Pulse Response



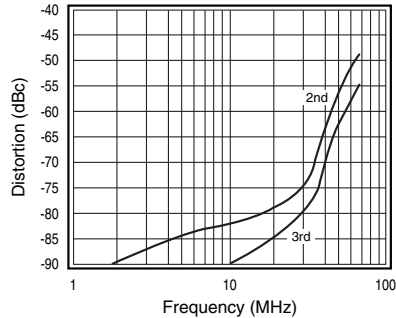
Large Signal Pulse Response



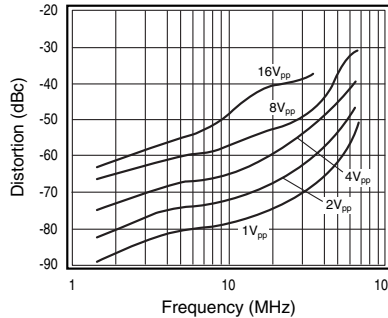
Settling Time



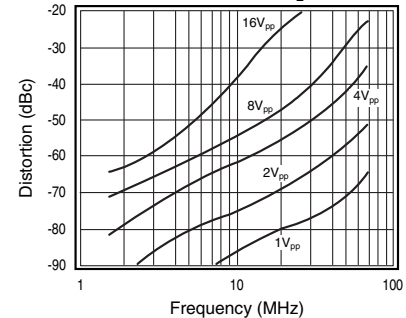
2nd and 3rd Harmonic Distortion



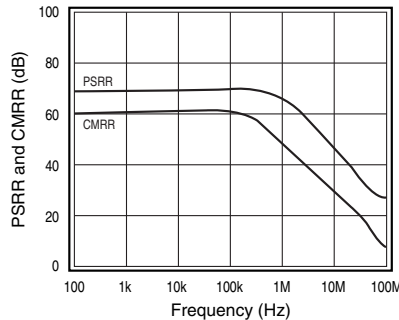
2nd Harmonic Distortion, $R_L = 100\Omega$



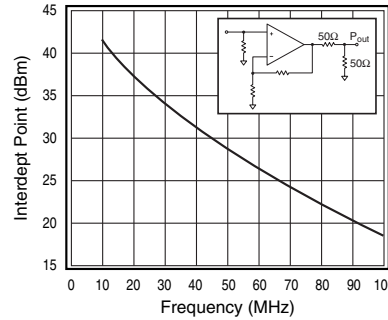
3rd Harmonic Distortion, $R_L = 100\Omega$



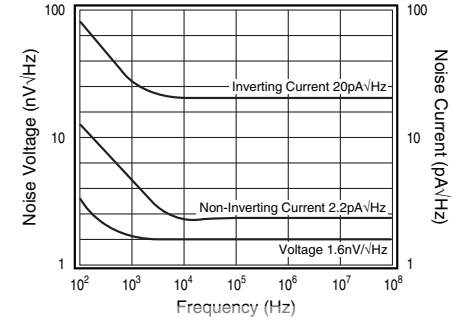
CMRR and PSRR



2-Tone, 3rd Order Intermod. Intercept



Equivalent Input Noise



Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

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Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximated by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \frac{R_f}{Z(j\omega)}} \quad \text{Equation 1}$$

where:

- A_v is the closed loop DC voltage gain
- R_f is the feedback resistor
- $Z(j\omega)$ is the CLC205's open loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the -3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

Overdrive Protection

Unlike most other high-speed op amps, the KH207 is not damaged by saturation caused by overdriving input signals (where $V_{in} \times \text{gain} > \text{max. } V_o$). The KH207 self limits the current at the inverting input when the output is saturated (see the inverting input current self limit specification); this ensures that the amplifier will not be damaged due to excessive internal currents during overdrive. For protection against input signals which would exceed either the maximum differential or common mode input voltage, the diode clamp circuits below may be used.

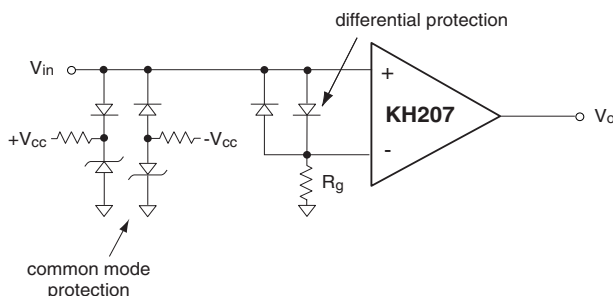


Figure 1: Diode Clamp Circuits for Common Mode and Differential Mode Protection

Short Circuit Protection

Damage caused by short circuits at the output may be prevented by limiting the output current to safe levels. The most simple current limit circuit calls for placing resistors between the output stage collector supplies and the output stage collectors (pins 12 and 10). The value of this resistor is determined by:

$$R_C = \frac{V_C}{I_l} - R_l$$

where I_l is the desired limit current and R_l is the minimum expected load resistance (0Ω for a short to ground). Bypass capacitors of $0.01\mu F$ on should be used on the collectors as in Figures 2 and 3.

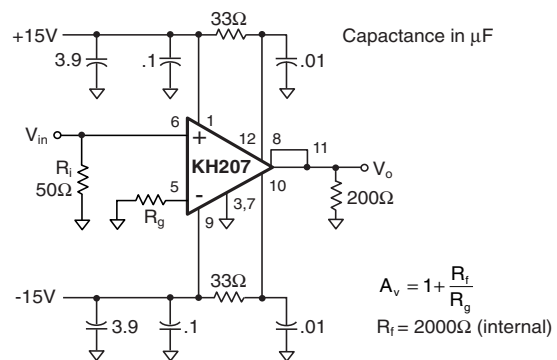


Figure 2: Recommended Non-Inverting Gain Circuit

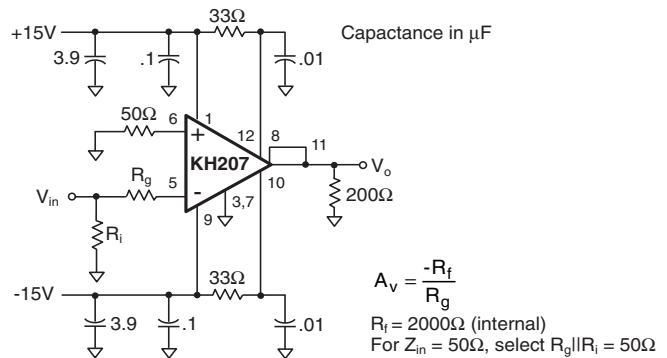


Figure 3: Recommended Inverting Gain Circuit

A more sophisticated current limit circuit which provides a limit current independent of R_l is shown in Figure 4 on page 5.

With the component values indicated, current limiting occurs at 50mA. For other values of current limit (I_l), select R_C to equal V_{be}/I_l . Where V_{be} is the base to emitter voltage drop of Q3 (or Q4) at a current of $[2V_{CC} - 1.4] / R_x$, where $R_x \leq [(2V_{CC} - 1.4) / I_l] B_{min}$.

Also, B_{min} is the minimum beta of Q1 (or Q2) at a current of I_l . Since the limit current depends on V_{be} , which is temperature dependent, the limit current is likewise temperature dependent.

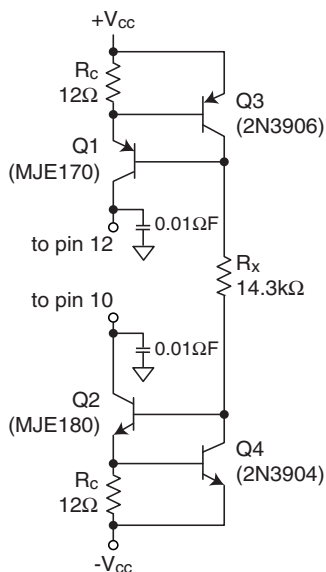


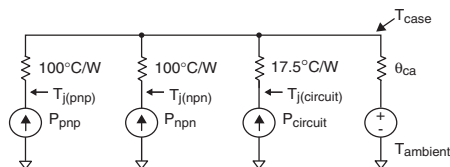
Figure 4: Active Current Limit Circuit (50mA)

Controlling Bandwidth and Passband Response

In most applications, a feedback resistor value of 2kΩ will provide optimum performance; nonetheless, some applications may require a resistor of some other value. The response versus R_f plot on the previous page shows how decreasing R_f will increase bandwidth (and frequency response peaking, which may lead to instability). Conversely, large values of feedback resistance tend to roll off the response.

The best settling time performance requires the use of an external feedback resistor (use of the internal resistor results in a 0.1% to 0.2% settling tail). The settling performance may be improved slightly by adding a capacitance of 0.4pF in parallel with the feedback resistor (settling time specifications reflect performance with an external feedback resistor but with no external capacitance).

Thermal Model



Noise Analysis

Approximate noise figure can be determined for the KH207 using the **Equivalent Input Noise** plot on page 3 and the equations shown below.

$kT = 4.00 \times 10^{-21}$ Joules at 290°K

V_n is spot noise voltage (V/√Hz)

i_n is non-inverting spot noise current (A/√Hz)

i_i is inverting spot noise current (A/√Hz)

$$F = 10 \log \left[1 + \frac{R_s}{R_n} + \frac{R_s}{4kT} \cdot \left(i_n^2 + \frac{V_n^2}{R_p^2} + \frac{R_f^2 i_i^2}{R_p^2 A_v^2} \right) \right]$$

where $R_p = \frac{R_s R_n}{R_s + R_n}$; $A_v = \frac{R_f}{R_g} + 1$

Figure 5: Noise Figure Diagram and Equations (Noise Figure is for the Network Inside this Box.)

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the KH207 will improve stability and settling performance.

Transmission Line Matching

One method for matching the characteristic impedance (Z_0) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier. Figure 6 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

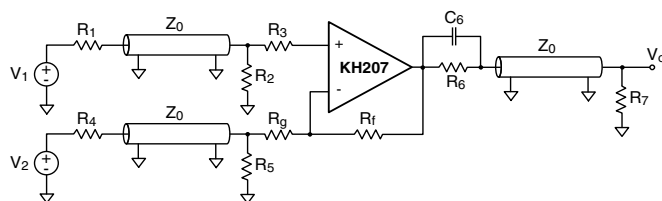


Figure 6: Transmission Line Matching

Non-inverting gain applications:

- Connect R_g directly to ground.
- Make R_1 , R_2 , R_6 , and R_7 equal to Z_0 .
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

$P_{circuit} = [(+V_{CC}) - (-V_{CC})]^2 / 1.77k\Omega$

$P_{xxx} = [(\pm V_{CC}) - V_{out} - (I_{col}) (R_{col} + 6)] (I_{col})$
(% duty cycle)

(For positive V_o and V_{CC} , this is the power in the npn output stage.)
(For negative V_o and V_{CC} , this is the power in the pnp output stage.)

$\theta_{ca} = 65^\circ\text{C/W}$ in still air without a heatsink.
 35°C/W in still air without a Thermalloy 2268.
 15°C/W in 300ft/min air with a Thermalloy 2268
(Thermalloy 2240 works equally well.)

$I_{col} = V_{out}/R_{load}$ or 3mA, whichever is greater.
(Include feedback R in R_{load} .)

R_{col} is a resistor (33Ω recommended) between the xxx collector and $\pm V_{CC}$.

$T_j(pnp) = P_{pnp} (100 + \theta_{ca}) + (P_{cir} + P_{nnp})\theta_{ca} + T_a$, similar for $T_j(npn)$.

$T_j(cir) = P_{cir} (17.5 + \theta_{ca}) + (P_{pnp} + P_{nnp})\theta_{ca} + T_a$.

Inverting gain applications:

- Connect R_3 directly to ground.
- Make the resistors R_4 , R_6 , and R_7 equal to Z_o .
- Make $R_5 \parallel R_g = Z_o$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

Dynamic Range (Intermods)

For RF applications, the KH207 specifies a third order intercept of 26dBm at 60MHz and $P_o = 10$ dBm. A **2-Tone, 3rd Order IMD Intercept** plot is found in the **Typical Performance Characteristics** section. The output power level is taken at the load. Third-order harmonic distortion is calculated with the formula:

$$HD\ 3^{rd} = 2 \cdot (IP3_o - P_o)$$

where:

- $IP3_o$ = third-order output intercept, dBm at the load.
- P_o = output power level, dBm at the load.
- $HD\ 3^{rd}$ = third-order distortion from the fundamental, -dBc.
- dBm is the power in mW, at the load, expressed in dB.

Realized third-order output distortion is highly dependent upon the external circuit. Some of the common external circuit choices that improve 3rd order distortion are:

- short and equal return paths from the load to the supplies.
- de-coupling capacitors of the correct value.
- higher load resistance.
- a lower ratio of the output swing to the power supply voltage.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance the performance of the KH207. Good ground plane construction and power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal stray capacitance to the ground plane or other nodes. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

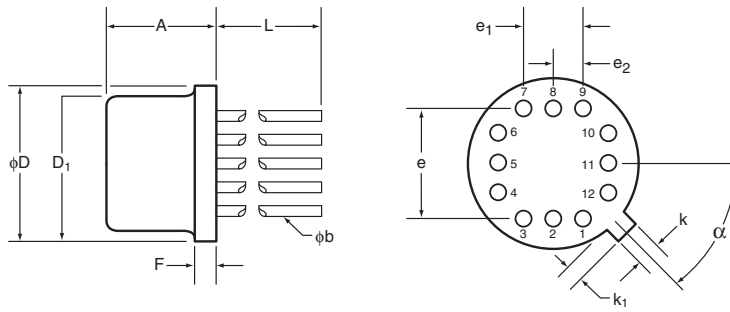
General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8 μ F tantalum and 0.1 μ F ceramic capacitors on both supplies.
- Place the 6.8 μ F capacitors within 0.75 inches of the power pins.
- Place the 0.1 μ F capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

An evaluation PC board (part number 730009) for the KH207 is available to aid in device testing.

KH207 Package Dimensions

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TO-8				
SYMBOL	INCHES		MILIMETERS	
	Minimum	Maximum	Minimum	Maximum
A	0.142	0.181	3.61	4.60
ϕb	0.016	0.019	0.41	0.48
ϕD	0.595	0.605	15.11	15.37
ϕD_1	0.543	0.555	13.79	14.10
e	0.400 BSC		10.16 BSC	
e ₁	0.200 BSC		5.08 BSC	
e ₂	0.100 BSC		2.54 BSC	
F	0.016	0.030	0.41	0.76
k	0.026	0.036	0.66	0.91
k ₁	0.026	0.036	0.66	0.91
L	0.310	0.340	7.87	8.64
α	45° BSC		45° BSC	

NOTES:
 Seal: cap weld
 Lead finish: gold per MIL-M-38510
 Package composition:
 Package: metal
 Lid: Type A per MIL-M-38510

Life Support Policy

Cadeca's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Cadeca Microcircuits, Inc. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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