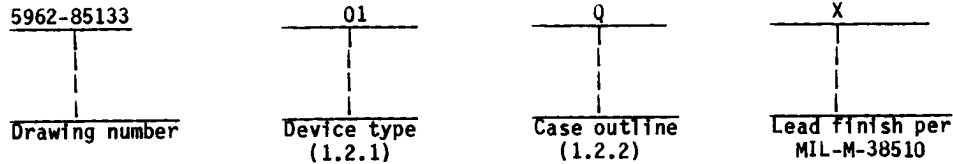




1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	80287-10	80-bit HMOS numeric processor extension	10 MHz
02	80287-8	80-bit HMOS numeric processor extension	8 MHz
03	80287-6	80-bit HMOS numeric processor extension	6 MHz

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 9/16" x 2 1/16"), dual-in-line package

1.3 Absolute maximum ratings.

Storage temperature range - - - - -	-65°C to +150°C
Voltage on any pin with respect to ground - - - - -	-1.0 V dc to +7 V dc
Maximum power dissipation (P <sub>D</sub> ) - - - - -	3.15 W
Lead temperature (soldering, 10 seconds) - - - - -	300°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) - - - - -	See MIL-M-38510, appendix C
Junction temperature (T <sub>J</sub> ) - - - - -	150°C

1.4 Recommended operating conditions.

Case operating temperature range - - - - -	-55°C to +125°C
Supply voltage (V <sub>CC</sub> ) - - - - -	4.75 V dc to 5.25 V dc

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $T_C = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 5\%$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	$V_{IL}$		1, 2, 3	A11	-.5	.8	V
Input high voltage	$V_{IH}$		1, 2, 3	A11	2.0	$V_{CC} \pm .5$	V
Clock input low voltage: CKM = 1 CKM = 0	$V_{ILC}$		1, 2, 3	A11	2.0	$V_{CC} + 1$ $3.8 V_{CC} + 1$	V
Output low voltage	$V_{OL}$	$I_{OL} = 0.3\text{ mA}$	1, 2, 3	A11		.45	V
Output high voltage	$V_{OH}$	$I_{OH} = -400\text{ }\mu\text{A}$	1, 2, 3	A11	2.4		V
Input leakage current	$I_{LI}$	$0\text{ V} \leq V_{IN} \leq V_{CC}$	1, 2, 3	A11		$\pm 10$	$\mu\text{A}$
Output leakage current	$I_{LO}$	$.45\text{ V} \leq V_{OUT} \leq V_{CC}$	1, 2, 3	A11		$\pm 10$	$\mu\text{A}$
Power supply current	$I_{CC}$	$T_C = -55^\circ\text{C}$	3	A11		600	mA
Input capacitance	$C_{IN}$	FC = 1 MHz See 4.3.1c	4	A11		10	pF
Input/output capacitance (D0-D15)	$C_0$	FC = 1 MHz See 4.3.1c	4	A11		20	pF
CLK capacitance	$C_{CLK}$	FC = 1 MHz See 4.3.1c	4	A11		12	pF
CLK period CKM = 1  CKM = 0	$t_{CLCL}$	<u>1/</u>	9, 10, 11	01 02 03 01 02 03	100 125 166 40 50 62.5	500 500 500 166 166 166	ns
CLK low time CKM = 1  CKM = 0	$t_{CLCH}$	at 0.8 V <u>1/</u>  at 0.6 V	9, 10, 11	01 02 03 01 02, 03	53 68 100 11 15	343 343 343 146 146	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $T_C = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 5\%$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLK high time CKM = 1	$t_{CHCL}$	at 2.0 V	9, 10, 11	01	28	230	ns
CKM = 0		at 3.6 V		02	43	230	
				03	50	230	
				01	18	151	
				02, 03	20	151	
CLK rise time	$t_{CH1CH2}$ $t_{2/}$	1.0 V to 3.6 V if CKM = 1 $\frac{1}{}$	9, 10, 11	A11		10	ns
CLK fall time	$t_{CL2CL1}$ $t_{2/}$	3.6 V to 1.0 V if CKM = 1 $\frac{1}{}$	9, 10, 11	A11		10	ns
Data setup to $\overline{\text{NPWR}}$ inactive	$t_{DVWH}$	$\frac{1}{}$	9, 10, 11	A11	75		ns
Data hold from $\overline{\text{NPWR}}$ inactive	$t_{WHDX}$	$\frac{1}{}$	9, 10, 11	01, 02 03	18 30		ns
$\overline{\text{NPWR}}$ , $\overline{\text{NPRD}}$ active time	$t_{WLWH}$ $t_{RLRH}$	at 0.8 V $\frac{1}{}$	9, 10, 11	01, 02 03	90 95		ns
Command valid to $\overline{\text{NPWR}}$ or $\overline{\text{NPRD}}$ active	$t_{AVRL}$ $t_{AVWL}$	$\frac{1}{}$	9, 10, 11	A11	0		ns
Minimum delay from $\overline{\text{PEREQ}}$ active to $\overline{\text{NPRD}}$ active	$t_{MHRL}$	$\frac{1}{}$	9, 10, 11	01 02, 03	100 130		ns
$\overline{\text{PEACK}}$ active time	$t_{KLKH}$	at 0.8 V $\frac{1}{}$	9, 10, 11	01 02, 03	60 85		ns
$\overline{\text{PEACK}}$ inactive time	$t_{KHKL}$	at 2.0 V $\frac{1}{}$	9, 10, 11	01 02, 03	200 250		ns
$\overline{\text{PEACK}}$ inactive to $\overline{\text{NPWR}}$ , $\overline{\text{NPRD}}$ inactive	$t_{KHCH}$	$\frac{1}{}$	9, 10, 11	01, 02 03	40 50		ns
$\overline{\text{NPWR}}$ , $\overline{\text{NPRD}}$ inactive to $\overline{\text{PEACK}}$ active	$t_{CHKL}$	$\frac{1}{}$	9, 10, 11	A11	-30		ns
Command hold from $\overline{\text{NPWR}}$ , $\overline{\text{NPRD}}$ inactive	$t_{WHAX}$ $t_{RHAX}$	$\frac{1}{}$	9, 10, 11	01 02, 03	22 30		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $T_C = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 5\%$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
PEACK active setup to NPWR, NPRD active	t <sub>KLCL</sub>	<u>1/</u>	9, 10, 11	01, 02 03	40 50		ns
NPWR, NPRD to CLK setup time	t <sub>IVCL</sub>	<u>1/ 3/</u>	9, 10, 11	01 02, 03	53 70		ns
NPWR, NPRD from CLK hold time	t <sub>CLIH</sub>	<u>1/ 3/</u>	9, 10, 11	01 02, 03	37 45		ns
RESET to CLK setup time	t <sub>RSCL</sub>	<u>1/ 3/</u>	9, 10, 11	A11	20		ns
RESET from CLK hold time	t <sub>CLRS</sub>	<u>1/ 3/</u>	9, 10, 11	A11	20		ns
NPRD inactive to data float	t <sub>RHQZ</sub>	<u>1/ 4/</u>	9, 10, 11	01 02 03		25 35 37.5	ns
NPRD active to data valid	t <sub>RLQV</sub> 5/	DO-D15 loading: $C_L = 100\text{ pF}$ <u>1/</u>	9, 10, 11	A11		60	ns
ERROR active to BUSY inactive	t <sub>ILBH</sub>	BUSY loading = $C_L = 100\text{ pF}$ <u>1/</u>	9, 10, 11	A11	10J		ns
NPWR active to BUSY active	t <sub>WLBV</sub> 5/	BUSY loading = $C_L = 100\text{ pF}$ <u>1/</u>	9, 10, 11	A11		100	ns
PEACK active to PEREQ inactive	t <sub>KLML</sub>	On last data transfer of numeric instruction <u>1/</u>	9, 10, 11	A11		127	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $T_C = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 5\%$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Command inactive time	$t_{CMDI}$	at 2.0 V	<u>1/</u>	9, 10, 11			ns
Write-to-write					01 02, 03	75 95	
Read-to-read					01 02, 03	75 95	
Write-to-read					01 02, 03	75 95	
Read-to-write					01 02, 03	75 95	
Data hold from NPRD inactive	$t_{RHQH}$	D0-D15 loading = $C_L = 100\text{ pF}$	<u>1/</u>	9, 10, 11	A11	3	ns

- 1/ See figures 3 and 4.
- 2/ Guaranteed if not tested.
- 3/ This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific CLK edge.
- 4/ Float condition occurs when output current is less than  $I_{LO}$  on D0-D15.
- 5/ Due to test equipment limitations, actual tested values may differ from those specified, but specified values are guaranteed.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(Hot), 10
Additional electrical subgroups for group C periodic inspections	---

\*PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$ ,  $C_O$ , and  $C_{CLK}$  measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
  - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

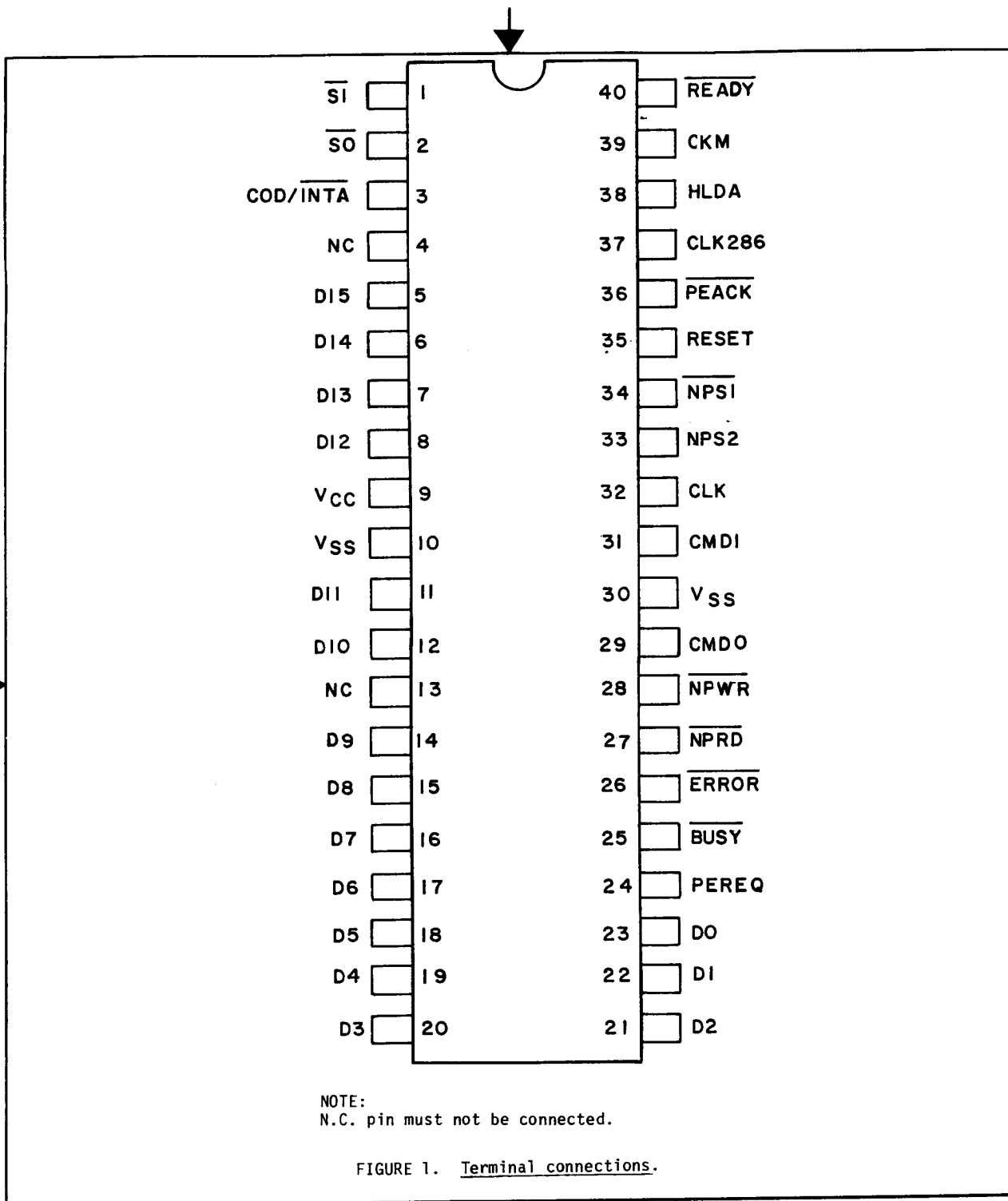
5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

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NOTE:  
N.C. pin must not be connected.

FIGURE 1. Terminal connections.

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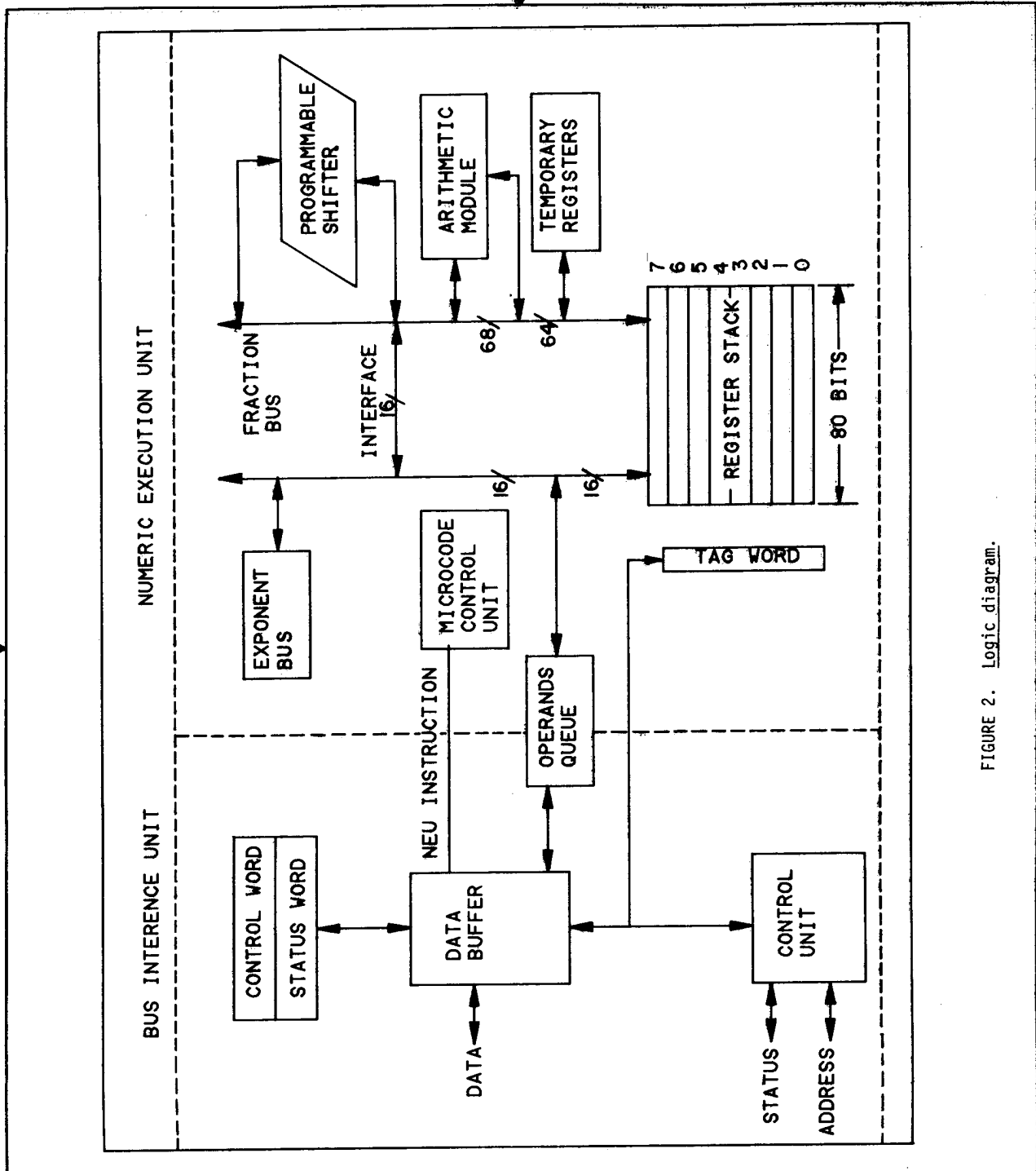
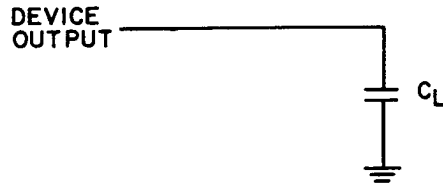


FIGURE 2. Logic diagram.

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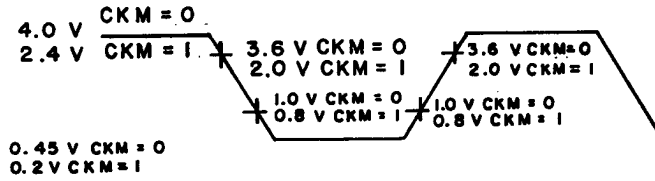
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AC test loading on output

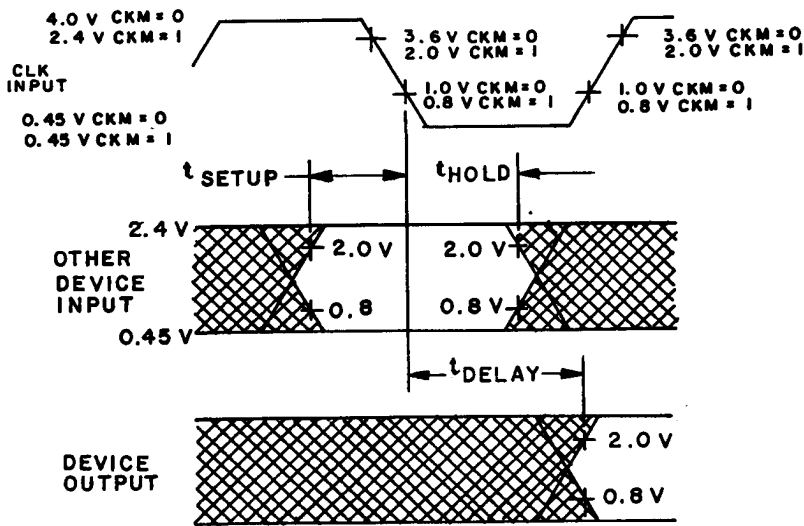


AC test loading on outputs

FIGURE 3. Output load.



AC drive and measurement points -CLK input



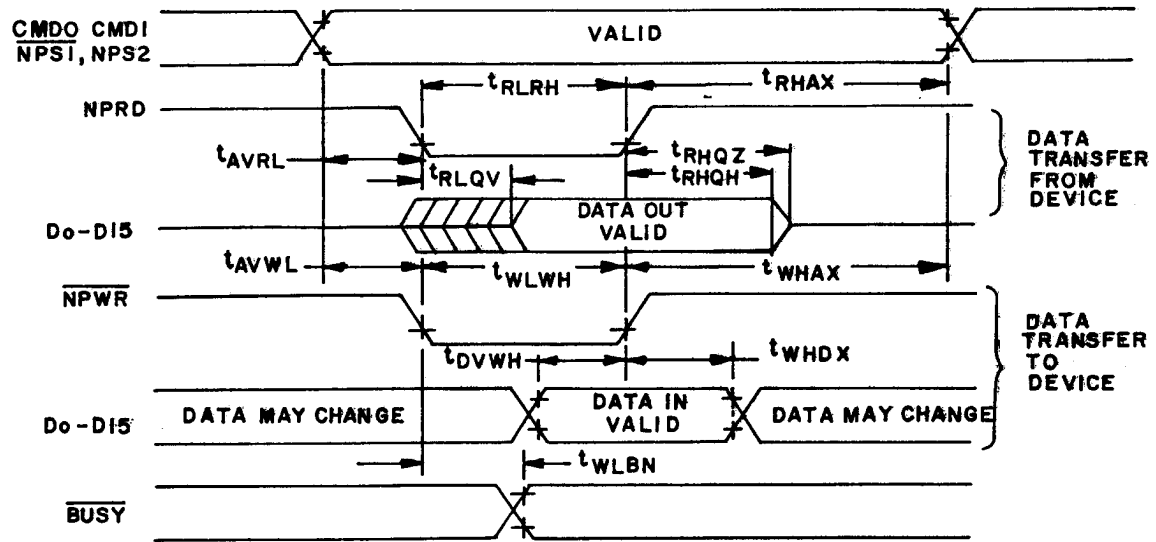
AC setup, hold and delay time measurement - general

FIGURE 4. Waveforms.

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DATA TRANSFER TIMING (INITIATED BY MICROPROCESSOR)



DATA CHANNEL TIMING (INITIATED BY PROCESSOR EXTENSION)

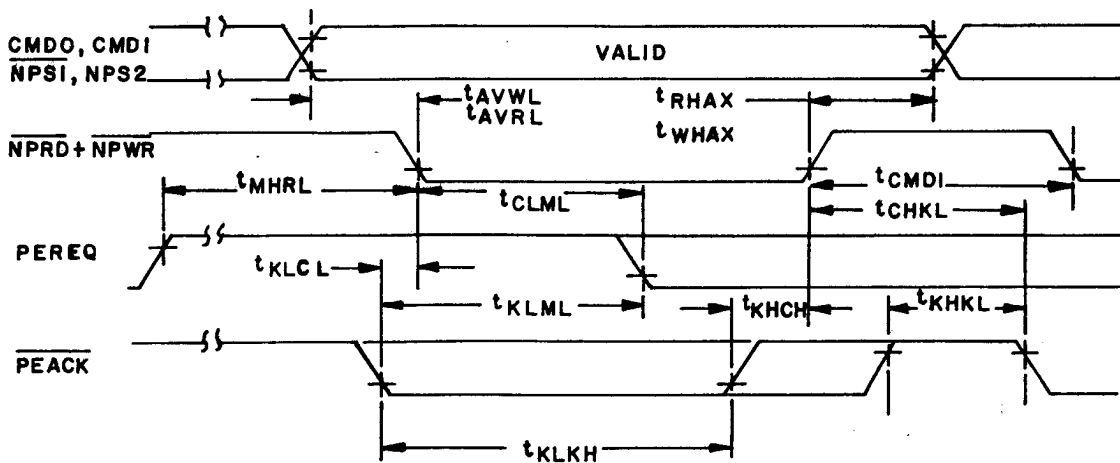
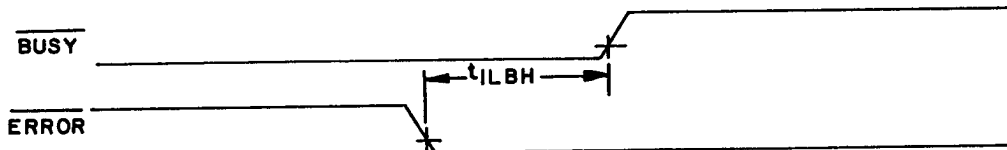


FIGURE 4. Waveforms - Continued

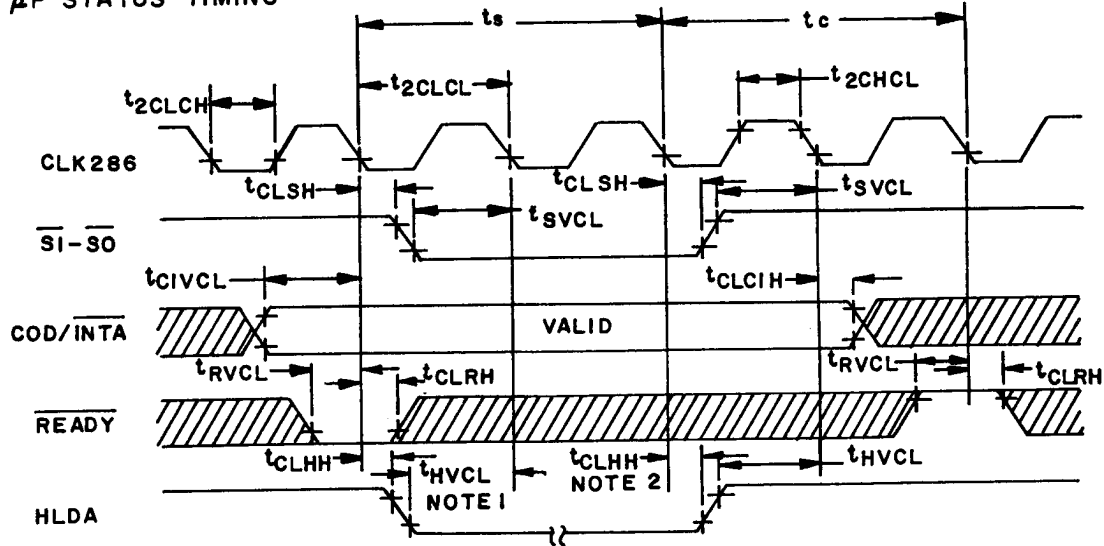
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**ERROR OUTPUT TIMING**



**μP STATUS TIMING**



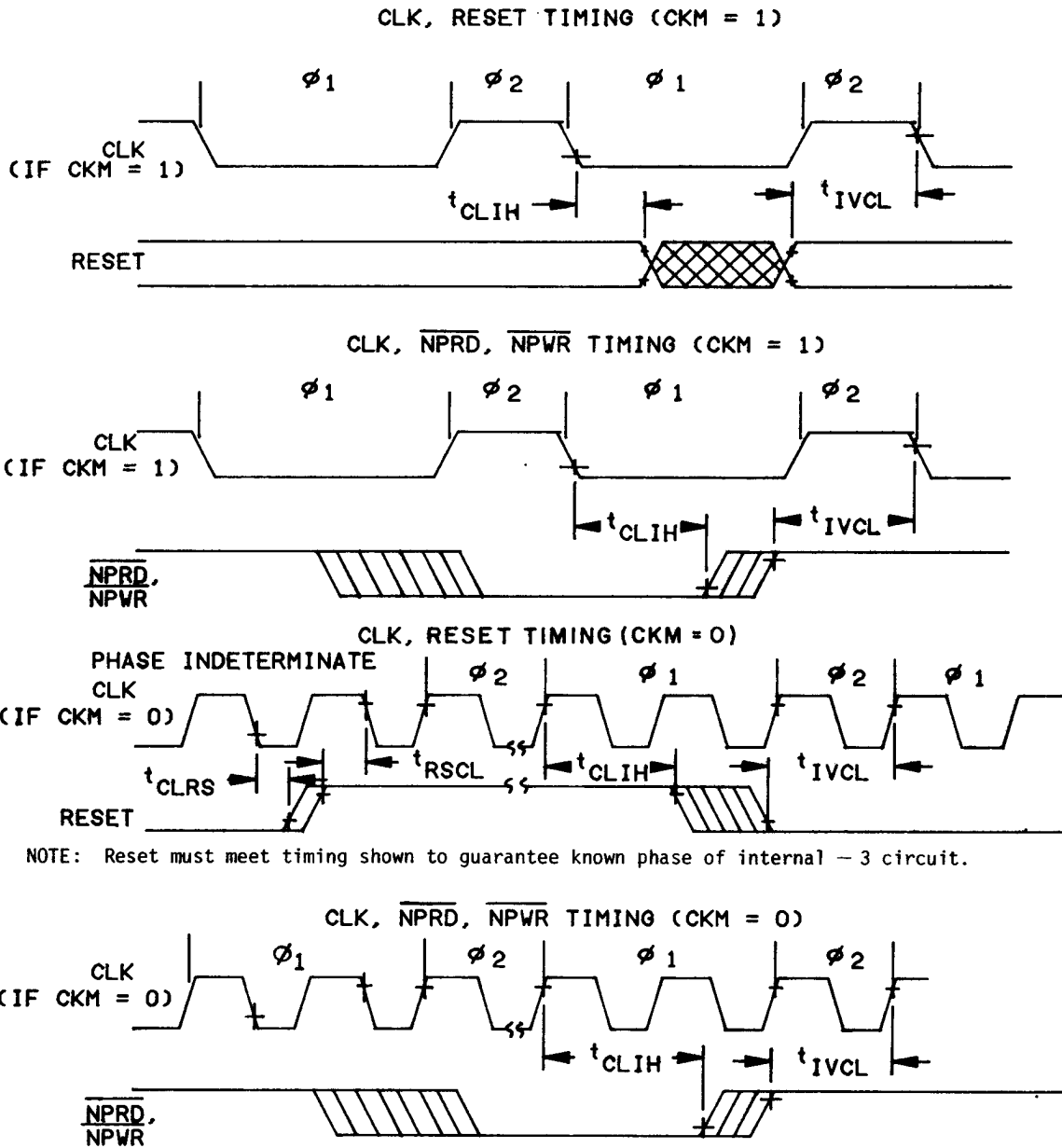
- NOTES:  
 1. This input transition occurs before  $t_s$ .  
 2. This input transition occurs after  $t_c$ .

FIGURE 4. Waveforms - Continued.

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(Reset, NPWR, NPRD are inputs asynchronous to CLK. Timing requirements on this page are given for testing purposes only to assure recognition at a specific CLK edge).



NOTE: Reset must meet timing shown to guarantee known phase of internal - 3 circuit.

FIGURE 4. Waveforms - Continued.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin descriptions. Pin descriptions and functions are as follows:

Symbols	Type	Name and function
CLK	I	Clock input: This clock provides the basic timing for internal device operations. Special MOS level inputs are required.
CKM	I	Clock mode signal: Indicates whether CLK is to be divided by 3 or used directly. A high input will cause CLK to be used directly. This input may be connected to V <sub>CC</sub> or V <sub>SS</sub> as appropriate. This input must be either high or low 20 CLK cycles before RESET goes low.
RESET	I	System reset: Causes the device to immediately terminate its present activity and enter a dormant state. RESET is required to be high for more than 4 device CLK cycles. For proper initialization the high-low transition must occur no sooner than 50 μs after V <sub>CC</sub> and CLK meet their dc and ac specifications.
D15-D0	I/O	Data: 16-bit bidirectional data bus. Inputs to these pins may be applied asynchronous to the device clock.
BUSY	0	Busy status: Asserted by the device to indicate that it is currently executing a command.
ERROR	0	Error status: Reflects the ES bit of the status word. This signal indicates that an unmasked error condition exists.
PEREQ	0	Processor extension data channel operand transfer request: A high on this output indicates that the device is ready to transfer data. PEREQ will be disabled upon assertion of PEACK or upon actual data transfer, whichever occurs first, if no more transfers are required.
PEACK	I	Processor extension data channel operand transfer acknowledge: Acknowledges that the request signal (PEREQ) has been recognized. Will cause the request (PEREQ) to be withdrawn in case there are no more transfers required. PEACK may be asynchronous to the device clock.

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Symbols	Type	Name and function
NPRD	I	Numeric processor read: Enables transfer of data from the device. This input may be asynchronous to the device clock.
NPWR	I	Numeric processor write: Enables transfer of data to the device. This input may be asynchronous to the device clock.
NPS1, NPS2	I	Numeric processor selects: Indicates the CPU is performing an ESCAPE instruction. Concurrent assertion of these signals (i.e., NPS1 is low and NPS2 is high) enables the device to perform floating point instructions. No data transfers involving the device will occur unless the device is selected via these lines. These inputs may be asynchronous to the device clock.
CMD1, CMD0	I	Command lines: These along with select inputs, allow the CPU to direct the operation of the device. These inputs may be asynchronous to the device clock.
CLK286	I	CPU clock: This input provides a sampling edge for the device inputs $\overline{SI}$ , $\overline{SO}$ , $COD/INTA$ , $READY$ , and $HLDA$ . It must be connected to the central processor CLK input.
$\overline{SI}$ , $\overline{SO}$ $COD/INTA$	I	Status: These inputs must be connected to the corresponding device pins.
HLDA	I	Hold acknowledge: This input informs the device when the central processor controls the local bus. It must be connected to the central processor $HLDA$ output.
READY	I	Ready: The end of a bus cycle is signaled by this input. It must be connected to the central processor $READY$ input.
VSS	I	System ground, both pins must be connected to ground.
VCC	I	+5 V supply.

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6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>	Replacement military specification part number
5962-8513301QX	34649	MD80287-10/B	
5962-8513302QX	34649	MD80287-8/B	
5962-8513303QX	34649	MD80287-6/B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

34649

Vendor name and address

Intel Corporation  
5000 W. Williams Field Road  
Chandler, AZ 85224

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