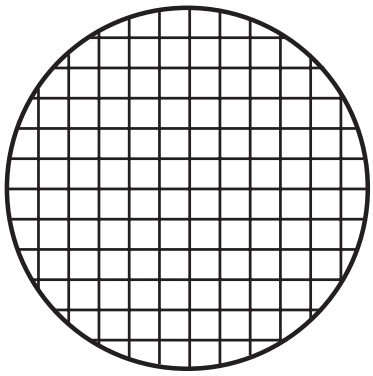
M69KM096AA

64 Mbit (4 Mb x16), 83MHz clock rate, 1.8V Supply, Multiplexed I/O, Bare Die, Burst PSRAM

Preliminary Data

Feature summary

- Supply Voltage
  - V_{CC} = 1.7 to 1.95V core supply voltage
  - V_{CCQ} = 1.7 to V_{CC} for I/O buffers
- Multiplexed Address/Data bus
- Asynchronous Operating Modes
  - Random Read: 70ns access time
  - Asynchronous Write
- Synchronous modes
  - Synchronous Read:
    Fixed length (4-, 8-, 16-, and 32-Word) or continuous burst
    Clock Frequency: 83MHz (max)
  - Synchronous Write: continuous burst
- Low Power Consumption
  - Active Current: < 25mA
  - Standby Current: 140µA
  - Deep Power-Down Current: < 10µA
- Low Power Features
  - Partial Array Self-Refresh (PASR)
  - Deep Power-Down (DPD) Mode
  - Automatic Temperature-compensated Self-Refresh
- Operating Temperature
  - –30°C to +85°C



Wafer

The M69KM096AA is only available as part of a multi-chip package Product.

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1 Summary description

The M69KM096AA is a 64 Mbit (67,108,864 bit) PSRAM, organized as 4,194,304 Words by 16 bits. It uses a high-speed CMOS DRAM technology implemented using a one transistor-per-cell topology that achieves bigger array sizes. It provides a high-density solution for low-power handheld applications.

The device operates from a 1.7 to 1.95V supply voltage. It has a 16-bit data bus. To reduce the number of pins. the first sixteen address lines are multiplexed with the Data Input/Output signals on the multiplexed address/data bus ADQ0-ADQ15. The remaining address lines A16-A21 are the MSB addresses.

The PSRAM interface supports various operating modes:

- Asynchronous Random Read and Write - when operating in one of these modes, the M69KM096AA is compatible with low power SRAMs.
- Synchronous modes that increase read and write speeds. Two types of Synchronous modes are available:
  - Flash-NOR: the device operates in Synchronous mode for read operations and Asynchronous mode for write operations.
  - Full Synchronous: the device supports Synchronous transfers for both read and write operations.

The M69KM096AA features three registers:

- The Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR): user-programmable configuration registers, which are used to define the device operation.
- A read-only Device ID Register (DIDR) containing device identification information.

The Bus Configuration Register (BCR) indicates how the device interacts with the system memory bus. The Refresh Configuration Register (RCR) is used to control how the memory array refresh is performed. At Power-Up, these registers are automatically loaded with default settings and can be updated any time during normal operation.

PSRAMs are based on the DRAM technology, but have a transparent internal self-refresh mechanism that requires no additional support from the system memory microcontroller. To minimize the value of the Standby current during self-refresh operations, the M69KM096AA includes three system-accessible mechanisms configured via the Refresh Configuration Register (RCR):

- Partial Array Self Refresh (PASR) performs a limited refresh of the part of the PSRAM array that contains essential data.
- Deep Power-Down (DPD) mode completely halts the refresh operation. It is used when no essential data is being held in the device.
- Automatic Temperature Compensated Self Refresh (TCSR) adjusts the refresh rate according to the operating temperature.

Figure 1. Logic Diagram

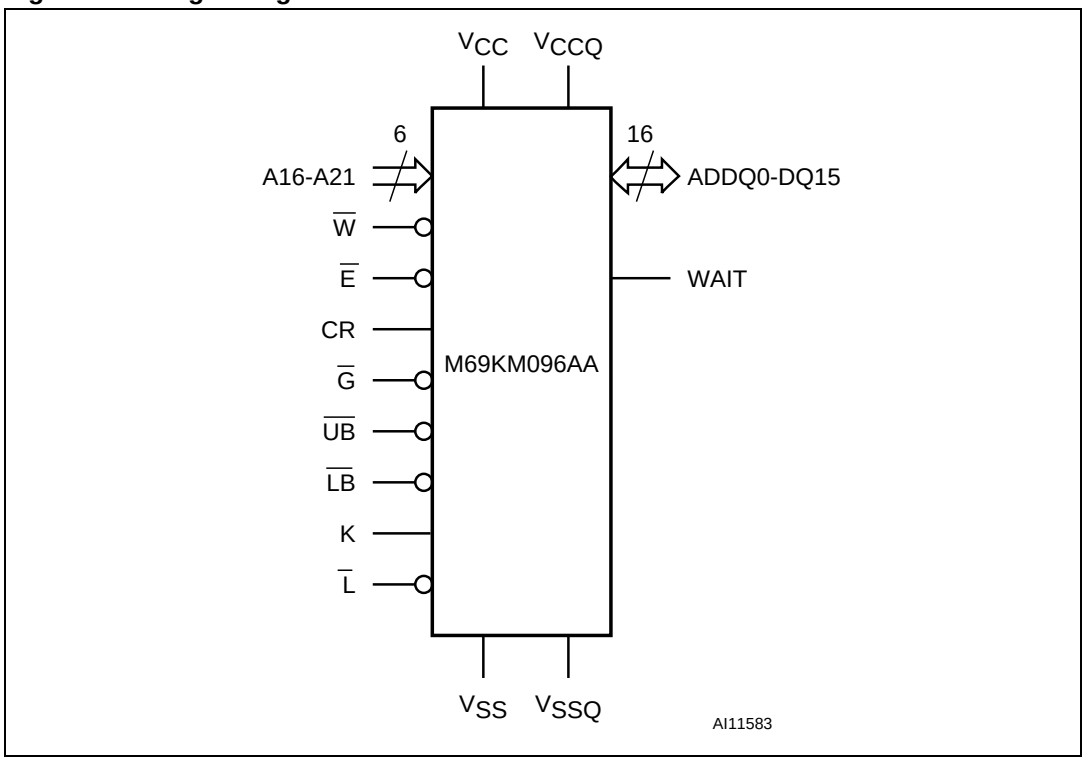
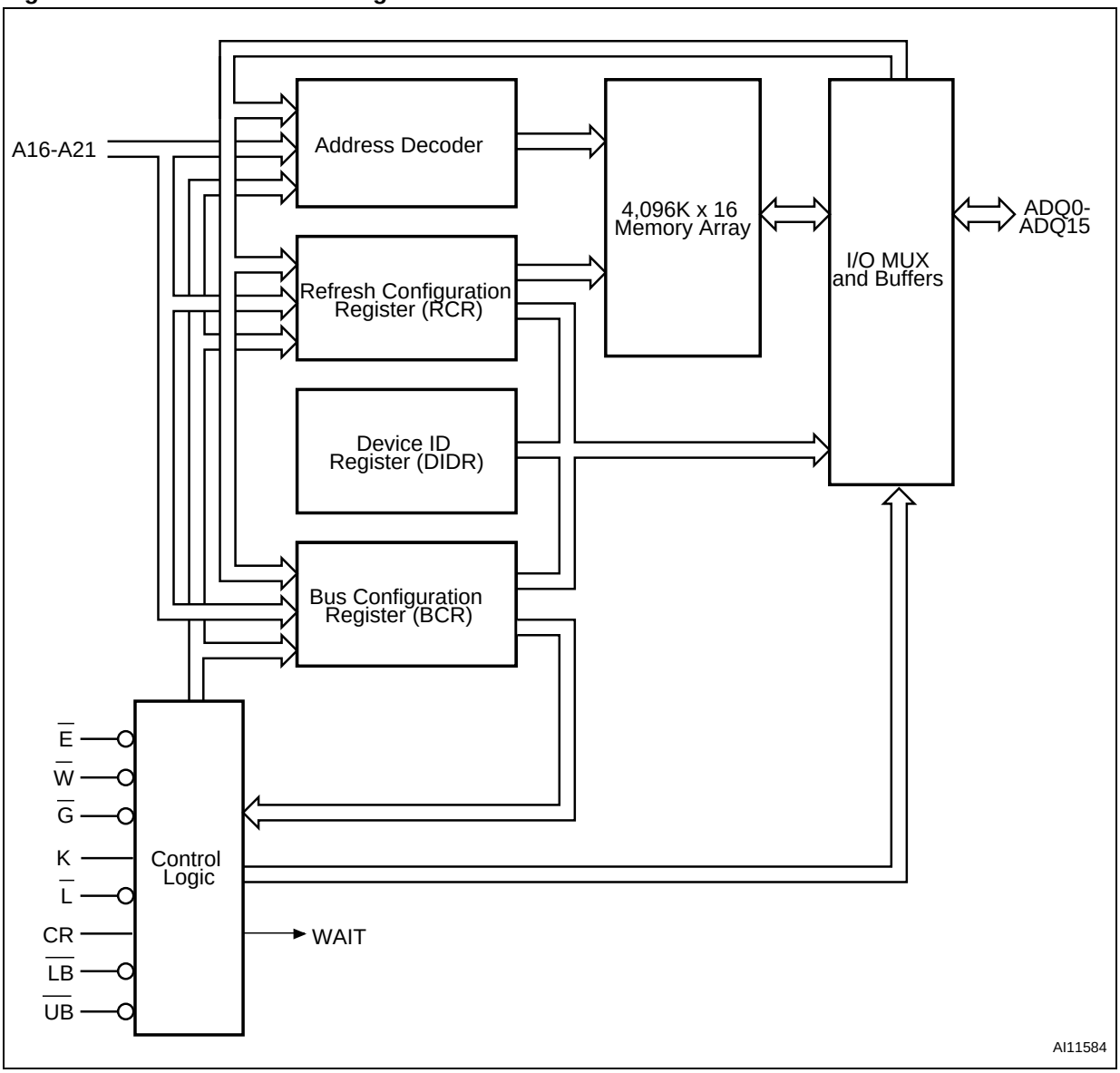


Table 1. Signal Names

A16-A21	Address Inputs
ADQ0-ADQ15	Address Inputs or Data Input/Outputs
$\overline{E}$	Chip Enable Input
CR	Configuration Register Enable Input
$\overline{G}$	Output Enable Input
$\overline{W}$	Write Enable Input
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
K	Clock Input
$\overline{L}$	Latch Enable Input
WAIT	Wait Output
V_{CC}	Core Supply Voltage
V_{CCQ}	Input/Output Buffers Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Buffers Ground

Figure 2. Functional block diagram



1. This functional block diagram illustrates simplified device operation.

2 Signal descriptions

The signals are summarized in *Figure 1: Logic Diagram*, and *Table 1: Signal Names*.

2.1 Address Inputs (A16-A21)

The Address Inputs A16-A21 are used in conjunction with ADQ0 to ADQ15, to select the cells in the memory array that are accessed during read and write operations.

2.2 Address Inputs or Data Input/Outputs (ADQ0-ADQ15)

ADQ0-ADQ15 support multiplexed address/data sequencing. They are used to input addresses to the memory array, or to program data in the memory array. Addresses are internally latched during Read and Write operations.

ADQO-ADQ15 are also used to define the value to be loaded into the BCR or the RCR, along with A16- A21 address Inputs.

2.3 Chip Enable ($\overline{E}$)

Chip Enable, $\overline{E}$, activates the device when driven Low (asserted). When de-asserted (V_{IH}), the device is disabled and goes automatically in low-power Standby mode or Deep Power-Down mode, according to the RCR settings.

2.4 Output Enable ($\overline{G}$)

When held Low, V_{IL}, the Output Enable, $\overline{G}$, enables the Bus Read operations of the memory.

2.5 Write Enable ($\overline{W}$)

Write Enable, $\overline{W}$, controls the Bus Write operation of the memory. When asserted (V_{IL}), the device is in write mode and write operations can be performed either to the configuration registers or to the memory array.

2.6 Upper Byte Enable ($\overline{UB}$)

The Upper Byte Enable, $\overline{UB}$, gates the data on the Upper Byte of the Address Inputs/ Data Inputs/Outputs (ADQ8-ADQ15) to or from the upper part of the selected address during a write or read operation.

2.7 Lower Byte Enable ($\overline{LB}$)

The Lower Byte Enable, $\overline{LB}$, gates the data on the Lower Byte of the Address Inputs/Data Input/Outputs (ADQ0-ADQ7) to or from the lower part of the selected address during a write or read operation.

If both $\overline{LB}$ and $\overline{UB}$ are disabled (High), the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{E}$ remains Low.

2.8 Clock Input (K)

The Clock, K, is an input signal to synchronize the memory to the microcontroller or system bus frequency during Synchronous Burst Read and Write operations. The Clock input signal increments the device internal address counter. The addresses are latched on the rising edge of the Clock K, when $\overline{L}$ is Low during Synchronous Bus operations.

Latency counts are defined from the first Clock rising edge after $\overline{L}$ falling edge to the first data input latched or the first data output valid.

The Clock input is required during all synchronous operations and must be kept Low during asynchronous operations.

2.9 Configuration Register Enable (CR)

When this signal is driven High, V_{IH}, bus read or write operations access either the value of the Refresh Configuration Register (RCR) or the Bus Configuration Register (BCR) according to the value of A19.

2.10 Latch Enable ($\overline{L}$)

In Synchronous mode, addresses are latched on the rising edge of the Clock K when the Latch Enable input, $\overline{L}$ is Low. In Asynchronous mode, addresses are latched on $\overline{L}$ rising edge.

2.11 Wait (WAIT)

The WAIT output signal provides data-valid feedback during Synchronous Burst Read and Write operations. The signal is gated by $\overline{E}$. Driving $\overline{E}$ High while WAIT is asserted may cause data corruption.

Once a read or write operation has been initiated, the WAIT signal goes active to indicate that the M69KM096AA device requires additional time before data can be transferred.

The WAIT signal also is used for arbitration when a Read or Write operation is launched while an on-chip refresh is in progress (see *Figure 5: Refresh Collision during Synchronous Burst Read in Variable Latency Mode*). Typically, the WAIT pin of the M69KM096AA can be connected to a shared WAIT signal used by the processor to coordinate transactions with multiple memories on the synchronous bus.

See *Section 3: Power-up* for details on the WAIT signal operation.

2.12 V_{CC} Supply Voltage

The V_{CC} Supply Voltage is the core supply voltage.

2.13 V_{CCQ} Supply Voltage

V_{CCQ} provides the power supply for the I/O pins. This allows all Outputs to be powered independently from the core power supply, V_{CC}.

2.14 V_{SS} Ground.

The V_{SS} Ground is the reference for all voltage measurements.

2.15 V_{SSQ} Ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{CCQ}. V_{SSQ} must be connected to V_{SS}.

3 Power-up

To guarantee correct operation, a specific Power-Up sequence must be followed to initialize the M69KM096AA. Power must be applied simultaneously to V_{CC} and V_{CCQ}. Once V_{CC} and V_{CCQ} have reached a stable level (see *Figure 28: Deep Power-Down Entry and Exit AC waveforms* and *Figure 27: Power-Up AC waveforms*), the device will require t_{VCHEL} to complete its self-initialization process. During the initialization period, the $\overline{E}$ signal must remain High. Once initialization has completed, the device is ready for normal operation.

Initialization will load the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR) with their default settings (see *Table 7: Bus Configuration Register Definition*, and *Table 11: Refresh Configuration Register Definition*).

4 Low-power modes

4.1 Standby

When the device is in Standby, the current consumption is reduced to the level necessary to perform the memory array refresh operation. The device will enter Standby when a read or write operation is completed, depending on the operating mode (asynchronous, synchronous).

For details on how to enter Standby, refer to *Table 2: Standard asynchronous operating modes*, *Table 3: Asynchronous Write Operations (NOR-Flash Synchronous Mode)* and *Table 4: Synchronous Read Operations (NOR-Flash Synchronous mode)*.

4.2 Deep Power-Down

Deep Power-Down (DPD) is used by the system memory microcontroller to disable the PSRAM device when its storage capabilities are not needed. All refresh operations are then disabled.

For the device to enter Deep Power-Down mode, bit 4 of the RCR must be set to ‘0’ and Chip Enable, $\overline{E}$, must go High, V_{IH}. When the Deep Power-Down is enabled, the data stored in the device may be corrupted and the BCR, the RCR and DIDR contents are saved.

The device exits from Deep Power-Down mode when the Chip Enable signal, $\overline{E}$, has been Low again for a minimum time of $t_{ELEH(DP)}$ (see *Table 22: Power-Up and Deep Power-Down AC characteristics* and *Figure 27: Power-Up AC waveforms*).

Bit 4 of the RCR will be automatically set to ‘1’. Once the Deep Power-Down is exited, the device will be available for normal operations after t_{VCHEL} (time to perform an initialization sequence) During this delay, the current consumption will be higher than the specified Standby levels, but considerably lower than the active current. The content of the registers will be restored after Deep Power-Down.

For details on how to enter Deep Power-Down, refer to *Table 2: Standard asynchronous operating modes*, *Table 3: Asynchronous Write Operations (NOR-Flash Synchronous Mode)* and *Table 4: Synchronous Read Operations (NOR-Flash Synchronous mode)*.

4.3 Partial Array Self Refresh

The Partial Array Self Refresh (PASR) performs a limited refresh of part of the PSRAM array. This mechanism enables the device to reduce the Standby current by refreshing only the part of the memory array that contains essential data. Different refresh options can be defined by setting the RCR0 to RCR2 bits of the RCR:

- Full array
- One eighth of the array
- One half of the array
- One quarter of the array
- None of the array

These memory areas can be located either at the top or bottom of the memory array.

The WAIT signal is used for arbitration when a read/write operation is launched while an on-chip refresh is in progress. If locations are addressed while they are undergoing refresh, the WAIT signal will be asserted for additional clock cycles, until the refresh has completed (see *Figure 5: Refresh Collision during Synchronous Burst Read in Variable Latency Mode*). When the refresh operation is completed, the read or write operation will be allowed to continue normally.

4.4 Automatic Temperature Compensated Self Refresh

The leakage current of DRAM capacitive storage elements increases with the temperature. At lower temperatures, the refresh rate can be decreased to minimize the Standby current.

The M69KM096AA is based on DRAM architecture, consequently it requires increasingly frequent refresh operations to maintain data integrity as the temperature increases. The Automatic Temperature Compensated Self Refresh mechanism (TCSR) that the devices feature, automatically adjusts the refresh rate depending on the operating temperature.

5 Standard Asynchronous operating modes

The M69KM096AA supports Asynchronous Read and Write modes (Random Read, Asynchronous Write).

The device is put in Asynchronous mode by setting bit 15 (BCR15) of the BCR to '1'.

During asynchronous operations, the WAIT signal should be ignored and the Clock input signal K should be held Low, V_{IL}.

Refer to *Table 2: Standard asynchronous operating modes* for a detailed description of asynchronous operating modes.

5.1 Asynchronous Read and Write modes

At Power-Up, the device defaults to Asynchronous Random Read mode (bit BCR15 set to '1'). This mode uses the industry standard control bus ($\overline{E}$, $\overline{G}$, $\overline{W}$, $\overline{LB}$, $\overline{UB}$). Read operations are initiated by bringing $\overline{E}$, $\overline{G}$ and $\overline{L}$ Low, V_{IL}, while keeping $\overline{W}$ High, V_{IH}, and driving the address onto the multiplexed address/data bus. $\overline{L}$ is then taken High, V_{IH}, to capture the address, and $\overline{G}$ is taken Low, V_{IL}. Valid data will be gated through the output buffers after the specific access time t_{ELQV} has elapsed.

Write operations occur when $\overline{E}$, $\overline{W}$ and $\overline{L}$ are driven Low, V_{IL} with the address on the multiplexed address/data bus. $\overline{L}$ is then taken High, V_{IH}, to capture the address, and the write data is driven onto the bus. During Asynchronous Random Write operations, the $\overline{G}$ signal is 'don't care' and $\overline{W}$ will override $\overline{G}$. The data to be written is latched on the rising edge of $\overline{E}$, $\overline{W}$, $\overline{LB}$ or $\overline{UB}$ (whichever occurs first). The write operation is terminated by de-asserting $\overline{E}$, $\overline{W}$, $\overline{LB}$ or $\overline{UB}$.

See *Figure 13*, and *Table 17* for details on Asynchronous Read AC waveforms and characteristics and *Figure 15*, and *Table 18* for details of Asynchronous Write AC waveforms and characteristics.

5.2 Configuration Registers Asynchronous Read and Write

Programming the registers (BCR and RCR) and reading the registers (BCR, RCR or DIDR) can be performed using the CR controlled method in standard Asynchronous mode.

Table 2. Standard asynchronous operating modes(1)

Asynchronous Modes	Power	$\overline{E}$	$\overline{L}$	$\overline{W}$	$\overline{G}$	$\overline{UB}$	$\overline{LB}$	CR	A19	A18	A16, A17, A20, A21	ADQ0-ADQ7	ADQ8-ADQ15
Word Read	Active (I_{CC})	V_{IL}	¯_/¯	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	Address In Valid			Address In/ Data Out Valid	
Lower Byte Read					V_{IL}	V_{IH}	V_{IL}	V_{IL}	Address In Valid			Address In/ Data Out Valid	High-Z
Upper Byte Read					V_{IL}	V_{IL}	V_{IH}	V_{IL}	Address In Valid			High-Z	Address In/ Data Out Valid
Word Write				V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Address In Valid			Address In/ Data In Valid	
Lower Byte Write						V_{IH}	V_{IL}	V_{IL}	Address In Valid			Address In/ Data In Valid	Data In Invalid
Upper Byte Write						V_{IL}	V_{IH}	V_{IL}	Address InValid			Data In Invalid	Address In/ Data In Valid
Read Configuration Register (CR controlled method)				V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	00(RCR) 10(BCR) X1(DIDR)		X	Address In/ BCR, RCR or DIDR Content Valid	
Program Configuration Register (CR Controlled)(2)			V_{IL}	V_{IL}	V_{IH}	X	X		00(RCR) 10(BCR) (3)		BCR/ RCR Data	Address In Valid	
Output Disable/No Operation	Active (I_{CC})		X	V_{IH}	X	X	X	V_{IL}	X	X	X	High-Z	
Deep Power-Down(4)	Deep Power-Down (I_{CCPD})	V_{IH}		X	X	X	X	X	X	X	X	High-Z	
Standby	Standby (I_{PASR})	V_{IH}		X	X	X	X	X	V_{IL}	X	X	High-Z	

1. The Clock signal, K, must remain Low in asynchronous operating mode.
2. BCR and RCR only.
3. A18 and A19 are used to select the BCR, the RCR or the DIDR.
4. The device enters Deep Power-Down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to '0'. The device remains in Deep Power-Down mode until $\overline{E}$ goes Low again and is held Low for $t_{ELEH(DP)}$.

6 Synchronous operating modes

The synchronous modes allow high-speed read and write operations synchronized with the clock.

The M69KM096AA supports two types of synchronous modes:

- **NOR-Flash**:- this mode greatly simplifies the interfacing with traditional burst-mode Flash memory microcontrollers.
- **Full Synchronous**: both read and write are performed in Synchronous mode.

All the options related to the synchronous modes can be configured through the Bus Configuration Register, BCR. In particular, the device is put in Synchronous mode, either NOR-Flash or Full Synchronous, by setting bit BCR15 of the Bus Configuration Register to '0'.

The device will automatically detect whether the NOR-Flash or the Full Synchronous mode is being used by monitoring the Clock, K, and the Latch Enable, $\overline{L}$, signals. If a rising edge of the Clock K is detected while $\overline{L}$ is held Low, V_{IL} (active), the device operates in Full Synchronous mode.

6.1 NOR-Flash Synchronous mode

In this mode, the device operates in synchronous mode for read operations, and in asynchronous mode for write operations.

Asynchronous write operations are performed at Word level, with $\overline{LB}$ and $\overline{UB}$ Low. The data is latched on $\overline{E}$, $\overline{W}$, $\overline{LB}$, $\overline{UB}$, whichever occurs first. RCR and BCR registers can be programmed in NOR-Flash Asynchronous Write mode, using the CR controlled method (see *Section 7.1: Programming and Reading Registers using the CR controlled method*). A Program Configuration Register operation can only be issued if the device is in idle state and no burst operations are in progress. NOR-Flash Asynchronous Write operations are described in *Table 3: Asynchronous Write Operations (NOR-Flash Synchronous Mode)*.

Synchronous read operations are also performed at Word level. They are controlled by the state of $\overline{E}$, $\overline{L}$, $\overline{G}$, $\overline{W}$, $\overline{LB}$ and $\overline{UB}$ signals when a rising edge of the clock signal, K, occurs. The initial Burst Read access latches the Burst start address. The number of Words to be output is controlled by bits 0 to 2 of the BCR. The first data will be output after a number of clock cycles, also called Latency. NOR-Flash Synchronous Burst Read operations are described in *Table 4: Synchronous Read Operations (NOR-Flash Synchronous mode)*.

When a Burst Write operation is initiated or when switching from NOR-Flash mode to Full Synchronous mode, the delay from $\overline{E}$ Low to Clock High, t_{ELKH}, should not exceed 20ns. However, when it is not possible to meet these specifications, special care must be taken to keep addresses stable after driving the Write Enable signal, $\overline{W}$, Low.

Write operations are considered as Asynchronous operations until the device detects a valid clock edge and hence the address setup time of t_{AVWL} must be satisfied (see *Figure 5: Refresh Collision during Synchronous Burst Read in Variable Latency Mode*).

6.2 Full Synchronous mode

In Full Synchronous mode, the device performs read and write operations synchronously. Synchronous Read and Write operations are performed at Word level. The initial Burst Read and Write access latches the Burst start address. The number of Words to be output or input during Synchronous Read and Write operations is controlled by bits 0 to 2 of the BCR. During Burst Read and Write operations, the first data will be output after a number of clock cycles defined by the Latency value.

Programming the registers (BCR and RCR) and reading the registers (BCR, RCR or DIDR) can be performed using the CR controlled method in Full Synchronous mode.

Full Synchronous operations are described in *Table 5: Full Synchronous mode*.

6.3 Synchronous Burst Read and Write

During Synchronous Burst Read or Write operations, addresses are latched on the rising edge of the Clock K when $\overline{L}$ is Low and data are latched on the rising edge of K. The Write Enable, $\overline{W}$, signal indicates whether the operation is going to be a read ($\overline{W}=V_{IH}$) or a write ($\overline{W}=V_{IL}$). The WAIT output will be asserted as soon as a Synchronous Burst operation is initiated and will be de-asserted to indicate when data are to be transferred to (or from) the memory array.

The Burst Length is the number of Words to be output or input during a Synchronous Burst Read or Write operation. It can be configured as 4, 8, 16 or 32 Words or continuous through bit BCR0 to BCR2 or the Burst Configuration Register.

The Latency defines the number of clock cycles between the beginning of a Burst Read operation and the first data output (counting from the first Clock edge where $\overline{L}$ was detected Low) or between the beginning of a Burst Write operation and the first data input. The Latency can be set through bits BCR13 to BCR11 of the Bus Configuration Register.

The latency can also be configured to fixed or variable by programming bit BCR14. By default, the Latency Type is set to variable. Synchronous Read operations are performed in both fixed and variable latency mode while Synchronous Write operations are only performed with fixed latency.

See *Figure 19*, *Figure 21*, and *Figure 24*, *Figure 25*, for details on Synchronous Read and Write AC waveforms, respectively.

6.3.1 Variable Latency

In Variable Latency mode, the latency programmed in the BCR is not guaranteed and is maintained only if there is no conflict with a refresh operation. The Latency set in the BCR is applicable only for an initial burst read access, when no refresh request is pending. For a given latency value, the Variable Latency mode allows higher operating frequencies than the Fixed Latency mode (see *Table 9: Variable Latency Counter Configuration* and *Figure 3: Variable Latency Mode, No Refresh Collision*).
Burst Write operations are always performed at fixed latency, even if BCR14 is configured to Variable Latency (see *Section 6.3.2: Fixed Latency*).

Monitoring of the WAIT signal is recommended for reliable operation in this mode. See *Figure 19*. and *Figure 25* for details on Synchronous Burst Read and Write AC waveforms in Variable Latency mode.

6.3.2 Fixed Latency

The latency programmed in the BCR is the real latency. The number of clock cycles is calculated by taking into account the time necessary for a refresh operation and the time necessary for an initial Burst access. This limits the operating frequency for a given latency value (see *Table 10: Fixed Latency Counter Configuration* and *Figure 4: Fixed Latency Mode*).

It is recommended to use the Fixed Latency mode if the microcontroller cannot monitor the WAIT signal.

6.3.3 Row Boundary Crossing

Row boundary crossings between adjacent rows may occur during Burst Read and Write operations. Row boundary crossings are not handled automatically by the PSRAM.

The microcontroller must stop the Burst operation at the row boundary and restart it at the beginning of the next row. Burst operations must be stopped by driving the Chip Enable signal, $\overline{E}$, High, after the WAIT signal falling edge.

$\overline{E}$ must transition within the first clock cycle after the last valid data output is sampled by the rising edge of the clock K.

Refer to *Figure 21* and *Figure 24* for details on how to manage row boundary crossings during burst operations.

6.3.4 Synchronous Burst Read Interrupt

Ongoing Burst Read operations can be interrupted to start a new Burst cycle by either of the following means:

- Driving $\overline{E}$ High, V_{IH}, and then Low, V_{IL} on the next clock cycle (recommended). If necessary, refresh cycles will be added during the new Burst operation to schedule any outstanding refresh. If Variable Latency mode is set, additional wait cycles will be added if a refresh operation is scheduled during the Synchronous Burst Read Interrupt. WAIT monitoring is mandatory for proper system operation.
- Starting a new Synchronous Burst Read operation without toggling $\overline{E}$.

An ongoing Burst Read operation can be interrupted only after the first valid data is output. When a new Burst access starts, I/O signals immediately become high impedance.

6.4 Synchronous Burst Write Interrupt

Ongoing Burst Write operations can be interrupted to start a new Burst cycle by either of the following means:

- Driving $\overline{E}$ High, V_{IH}, and then Low, V_{IL} on the next clock cycle (recommended),
- Starting a new Synchronous Burst Write without toggling $\overline{E}$. Considering that Burst Writes are always performed in Fixed Latency mode, refresh is never scheduled. A maximum Chip Enable, $\overline{E}$, low time (t_{ELEH}) must be respected for proper device operation.

An ongoing Burst Write can be interrupted only after the first data is input. When a new Burst access starts, I/O signals immediately become high impedance.

6.5 Synchronous Burst Read and Write Suspend

Synchronous Burst Read and Write operations can be suspended by halting the Clock K holding it Low, V_{IL}. The status of the I/O signals will depend on the status of Output enable input, $\overline{G}$. The device internal address counter is suspended and data outputs become high impedance t_{GHQZ} after the rising edge of the Output Enable signal, $\overline{G}$. It is prohibited to suspend the first data output at the beginning of a Synchronous Burst Read.

See *Figure 20* for details on the Synchronous Burst Read and Write Suspend mechanisms.

During Synchronous Burst Read and Synchronous Burst Write Suspend operations, the WAIT output will be asserted. Bit BCR8 of the Bus Configuration Register is used to configure when the transition of the WAIT output signal between the asserted and the de-asserted state occurs with respect to valid data available on the data bus.

Table 3. Asynchronous Write Operations (NOR-Flash Synchronous Mode)

Asynchronous Operations	Power	$\overline{K}$(1)	$\overline{E}$	$\overline{L}$	$\overline{W}$	$\overline{G}$	$\overline{UB}$, $\overline{LB}$	CR	A19	A18	A16, A17, A20, A21	ADQ0-ADQ15
Word Write(2)	Active (I_{CC})	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Address In Valid			Address In/Data In Valid
Program Configuration Register (CR Controlled)(3)			V_{IL}	V_{IL}	V_{IL}	X	X	V_{IH}	00(RCR) 10(BCR)		RCR/BCR Data	X
Output Disable/ No Operation(2)(4)	Active (I_{CC})		V_{IL}	X	X	X	X	X	V_{IL}			High-Z
Standby(5)(4)	Standby (I_{PASR})		V_{IH}	X	X	X	X	V_{IL}	X			High-Z
Deep Power-Down(6)	Deep Power-Down (I_{CCPD})		V_{IH}	X	X	X	X	X	X			High-Z

1. K must be held Low during Asynchronous Read And Write operations. It must also be kept Low for the device to consume Standby current during Standby and Deep Power-Down modes, and during Burst Suspend operations.
2. The device will consume active power in this mode whenever addresses are changed.
3. BCR and RCR only.
4. V_{IN} = 0V or V_{CCQ}; all signals must be stable in order to achieve standby current.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. The device enters Deep Power-Down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to '0'. The device remains in Deep Power-Down mode until $\overline{E}$ goes Low again and is held Low for $t_{ELEH(DP)}$.

Table 4. Synchronous Read Operations (NOR-Flash Synchronous mode)

Synchronous Operations	Power	K (1)	$\overline{E}$	$\overline{L}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$, $\overline{UB}$	WAIT (2)	CR	A19	A18	A16, A17, A20, A21	ADQ15-ADQ0
Initial Burst Read(3)(4)	Active (I_{CC})	↑	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Low-Z	V_{IL}	Address In Valid			X
Subsequent Burst Read(3)(4)(5)		↑	V_{IL}	V_{IH}	X	X	V_{IL}		V_{IL}	X			Address In/Data Out Valid
Read Configuration Register (CR controlled method)(3)(6)		↑	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}		V_{IH}	00(RCR) 10(BCR) X1(DIDR)		X	Address In/ BCR, RCR or DIDR Content Valid
Output Disable/No Operation(4)(7)	Active (I_{CC})	↑	V_{IL}	X	X	X	X		V_{IL}	X			High-Z
Standby(7)(8)	Standby (I_{PASR})	V_{IL}	V_{IH}	X	X	X	X	High-Z	V_{IL}	X			High-Z
Deep Power-Down(9)	Deep Power-Down (I_{CCPD})	V_{IL}	V_{IH}	X	X	X	X		X	X			High-Z

1. K must be held Low for the device to consume Standby current during Standby and Deep Power-Down modes, and during Burst Suspend operations.
2. The WAIT polarity is configured through bit 10 (BCR10) of the Bus Configuration Register.
3. The Burst mode is configured through bit 15 (BCR15) of the Bus Configuration Register.
4. The device will consume active power in this mode whenever addresses are changed.
5. Burst Read Interrupt and Suspend are described in dedicated paragraph of the *Section 6: Synchronous operating modes*.
6. The Configuration Register is output during the initial burst read. The following read operations are similar to subsequent burst read operations. $\overline{E}$ must be held Low for the equivalent of a single-word burst read (as indicated by the WAIT signal).
7. V_{IN} = 0V or V_{CCQ}; all signals must be stable in order to achieve standby current.
8. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
9. The device enters Deep Power-Down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to '0'. The device remains in Deep Power-Down mode until $\overline{E}$ goes Low again and is held Low for $t_{ELEH(DP)}$.

Table 5. Full Synchronous mode

Synchronous Mode	Power	K (1)	$\overline{E}$	$\overline{L}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$, $\overline{UB}$	WAIT (2)	CR	A19	A18	A16, A17, A20, A21	ADQ15-ADQ0
Initial Burst Read(3)(6)	Active (I_{CC})	⮥	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Low-Z	V_{IL}	Address In Valid			X
Subsequent Burst Read(3)(4)(6)		⮥	V_{IL}	V_{IH}	X	X	V_{IL}			X	X		Address In/Data Out Valid
Initial Burst Write(3)(6)		⮥	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X			Address In Valid			Address In/Data In Valid
Subsequent Burst Write(3)(6)		⮥	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}			X	X	X	Address In/Data In Valid
Program Configuration Register (CR Controlled)(3)(5)		⮥	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X		V_{IH}	00(RCR) 10(BCR)		RCR/BCR Data	X
Read Configuration Register (CR controlled method)(3)(5)		⮥	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}		V_{IH}	00(RCR) 10(BCR) X1(DIDR)		X	Address In/ BCR, RCR or DIDR Content Valid
No Operation(6)(8)	Active (I_{CC})	⮥	V_{IL}	X	V_{IH}	V_{IH}	X		V_{IL}	X			High-Z
Standby(7)(8)	Standby (I_{PASR})	V_{IL}	V_{IH}	X	X	X	X	High-Z	V_{IL}	X			High-Z
Deep Power-Down(9)	Deep Power-Down (I_{CCPD})	V_{IL}	V_{IH}	X	X	X	X		X	X			High-Z

1. K must be held Low for the device to consume Standby current during Standby and Deep Power-Down modes, and during Burst Suspend operations.
2. The WAIT polarity is configured through bit 10 (BCR10) of the Bus Configuration Register.
3. The Burst mode is configured through bit 15 (BCR15) of the Bus Configuration Register.
4. Burst Read Interrupt, Suspend, Terminate and Burst Write Interrupt, Suspend and Terminate are described in dedicated paragraph of the *Section 6: Synchronous operating modes*.
5. The Configuration Register is output during the initial burst operation (read or write). The following read or write operations are similar to subsequent burst operations. $\overline{E}$ must be held Low for the equivalent of a single-word burst operation (as indicated by the WAIT signal).
6. The device will consume active power in this mode whenever addresses are changed.
7. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
8. V_{IN} = 0V or V_{CCQ}; all signals must be stable in order to achieve standby current.
9. The device enters Deep Power-Down mode by driving the Chip Enable signal, $\overline{E}$, from Low to High, with bit 4 of the RCR set to '0'. The device remains in Deep Power-Down mode until $\overline{E}$ goes Low again and is held Low for $t_{ELEH(DP)}$.

Figure 3. Variable Latency Mode, No Refresh Collision

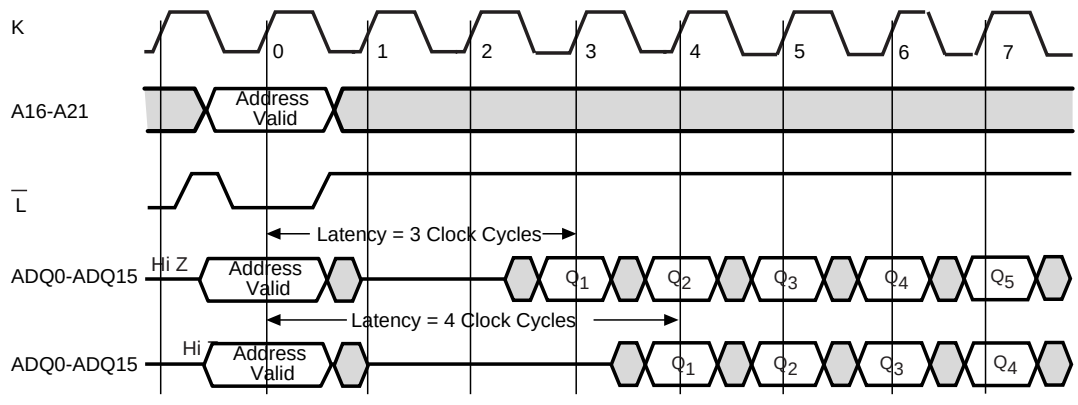
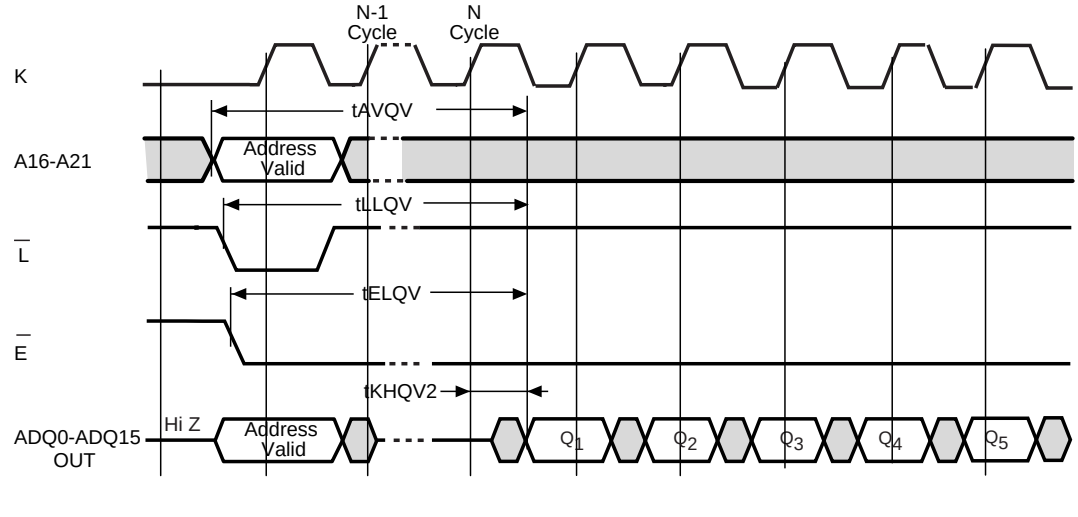
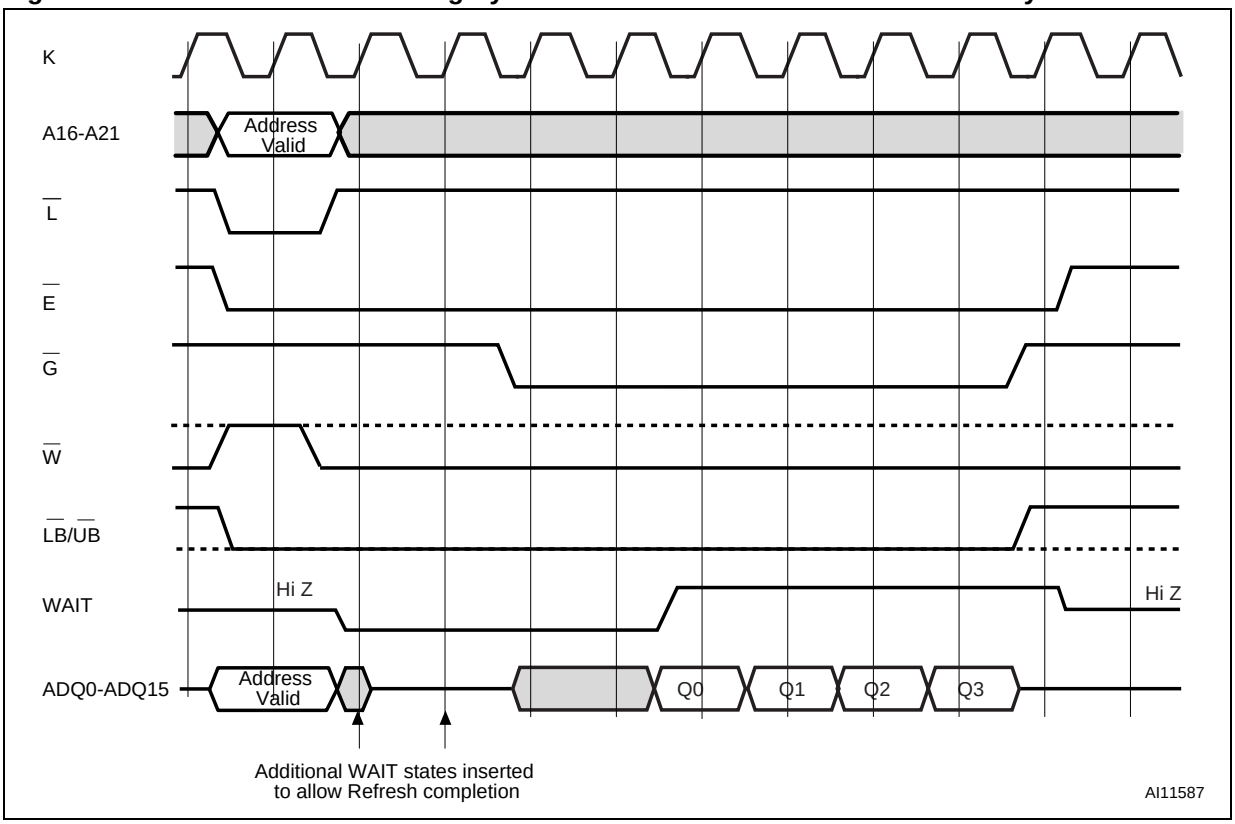


Figure 4. Fixed Latency Mode



1. See *Table 20: Synchronous Burst Read AC characteristics* for details on the synchronous read AC Characteristics shown in the above waveforms.

Figure 5. Refresh Collision during Synchronous Burst Read in Variable Latency Mode



1. Additional Wait states are inserted to allow Refresh completion.
The latency is set to 3 clock cycles (BCR13-BCR11 = 010). The WAIT must be active Low, V_{IL}, (BCR10 = 0) and asserted during delay (BCR8= 0).

7 Configuration Registers

The M69KM096AA features three registers:

- The Bus Configuration Register (BCR)
- The Refresh Configuration Register (RCR)
- The Device ID Register (DIDR)

BCR and RCR are user-programmable registers that define the device operating mode. They are automatically loaded with default settings during Power-Up, and selected by address bits A18 and A19 (see *Table 6: Register Selection*).

The DIDR is a read-only register that contains information about the device identification. It is selected by setting address bit A18 to '1' with A19 'don't care'.

The configuration registers can be programmed and read using two methods:

- The CR controlled method (or hardware method)
- The software method

7.1 Programming and Reading Registers using the CR controlled method

7.1.1 Read Configuration Register

The content of a register is read by issuing a read operation with Configuration Register Enable signal, CR, High, V_{IH}. Address bits A18 and A19 select the register to be read (see *Table 6: Register Selection*). The value contained in the register is then available on data bits DQ0 to DQ15. The BCR, the RCR and the DIDR can be read either in normal asynchronous or synchronous mode.

The CR pin has to be driven high prior to any access.

See *Table 4* and *Table 5* for a detailed description of Configuration register Read by the CR Controlled methods and *Figure 14* and *Figure 22*, CR Controlled Configuration Register Read waveforms in asynchronous and synchronous mode.

7.1.2 Program Configuration Register

BCR and RCR registers can be programmed by issuing a bus write operation, in asynchronous or synchronous mode (NOR-Flash or Full Synchronous), with Configuration Register Enable signal, CR, High, V_{IH}. Address bits A18 and A19 allow to select between BCR and RCR (see *Table 6: Register Selection*).

In synchronous mode, the values placed on address lines A0 to A15 are latched on the rising edge of $\overline{L}$, $\overline{E}$, or $\overline{W}$, whichever occurs first.

In asynchronous mode, a register is programmed by toggling $\overline{L}$ signal.

$\overline{LB}$ and $\overline{UB}$ are 'don't care'. The CR pin has to be driven high prior to any access.

Refer to *Table 3* and *Table 5* for a detailed description of Configuration Register Program by the CR Controlled method and to *Figure 17* and *Figure 26*, showing CR controlled Configuration Register Program waveforms in asynchronous and synchronous mode.

Table 6. Register Selection

Register	Read or Write Operation	A18	A19
RCR	Read/Write	0	0
BCR	Read/Write	0	1
DIDR	Read-only	1	X

7.2 Programming and Reading the registers using the software method

All registers (BCR, RCR, DIDR) can be read by issuing a Read Configuration Register sequence (see *Figure 7: Read Configuration Register (software method)*.

BCR and RCR can be programmed by issuing a Set Configuration Register sequence (see *Figure 6: Set Configuration Register (software method)*.

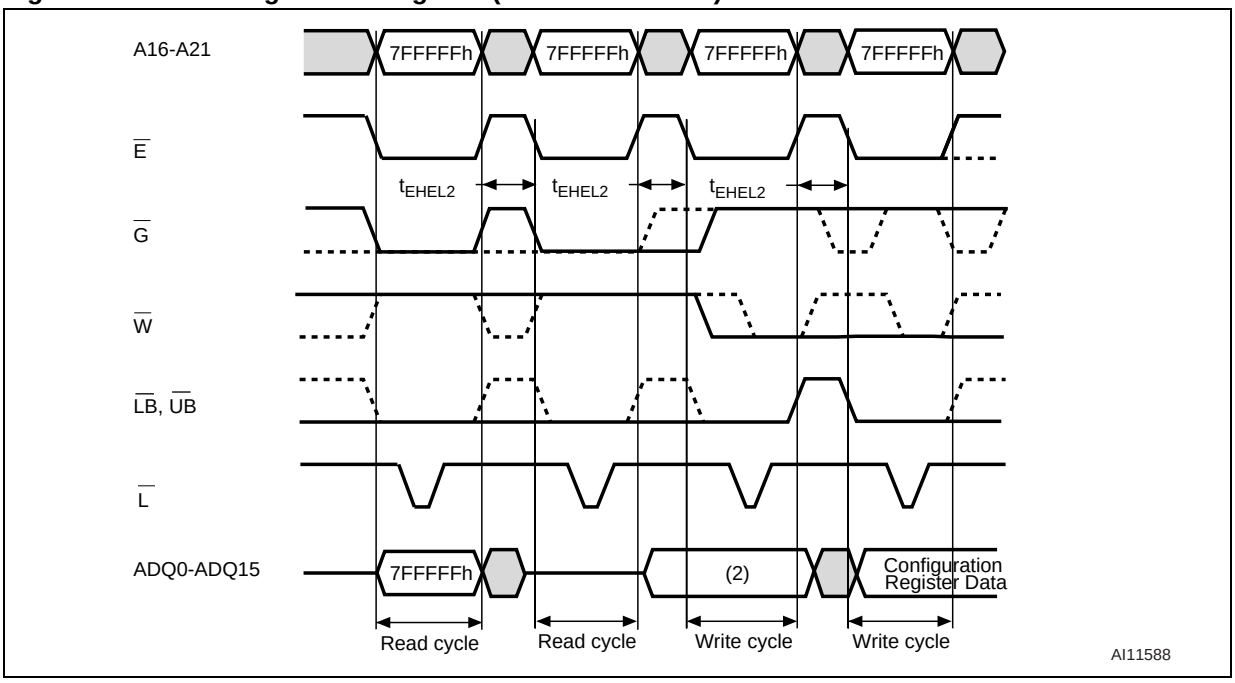
The timings will be identical to those described in *Table 17: Asynchronous Read AC characteristics*. The Configuration Register Enable input, CR, is ‘don’t care’.

Read Configuration Register and Set Configuration Register sequences both require 4 read and write cycles. These cycles are performed in asynchronous mode, whatever the device operating mode:

- 2 bus read and one bus write cycles to a unique address location, 7FFFFFh, indicate that the next operation will read or write to a configuration register. The data written during the third cycle must be ‘0000h’ to access the RCR, ‘0001h’ to access the BCR, and ‘0002h’ to access the DIDR during the next cycle.
- The fourth cycle reads from or writes to the configuration register.

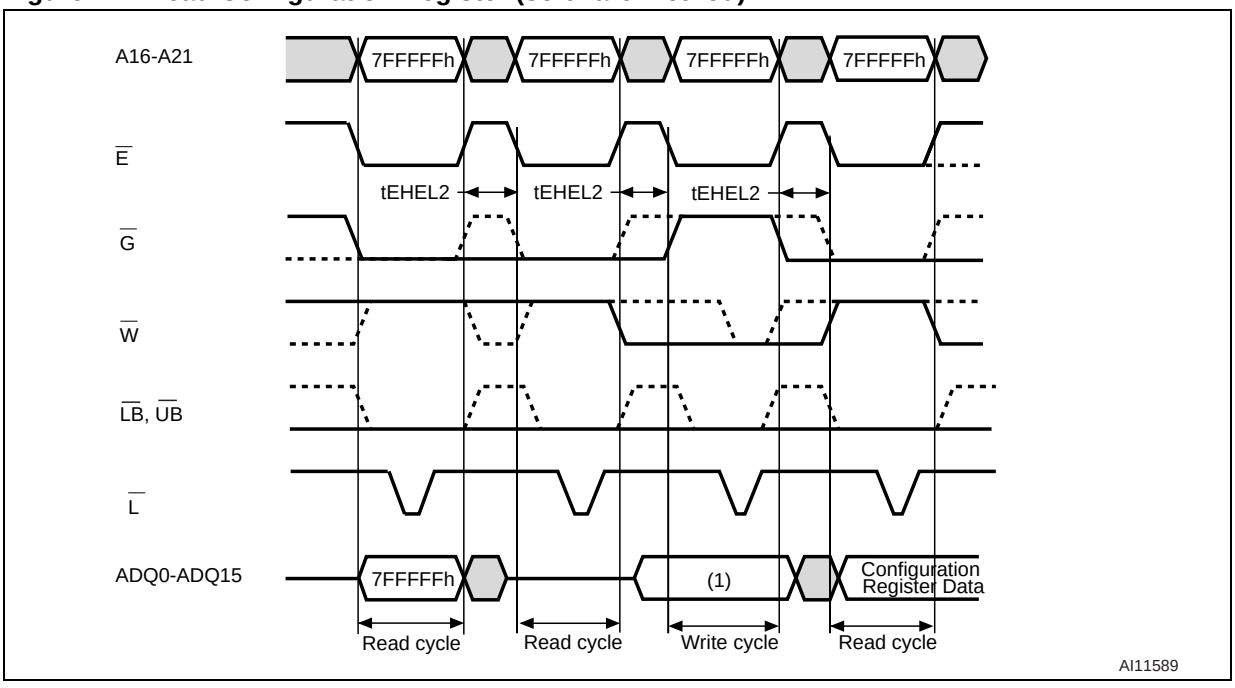
The timings for programming and reading the registers by the software method are identical to the asynchronous write and read timings.

Figure 6. Set Configuration Register (software method)



1. Only the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR) can be modified.
2. To program the BCR or the RCR on last bus write cycle, DQ0-DQ15 must be set to '0001h' and '0000' respectively.
3. The highest order address location is not modified during this operation.
4. The control signals $\overline{E}$, $\overline{G}$, $\overline{W}$, $\overline{LB}$ and $\overline{UB}$, must be toggled as shown in the above figure.

Figure 7. Read Configuration Register (software method)



1. To read the BCR, the RCR or the DIDR, on last bus read cycle, DQ0-DQ15 must be set to '0001h' and '0000', respectively.
2. The highest order address location is not modified during this operation.
3. The control signals $\overline{E}$, $\overline{G}$, $\overline{W}$, $\overline{LB}$ and $\overline{UB}$, must be toggled as shown in the above figure.

7.3 Bus Configuration Register

The Bus Configuration Register (BCR) defines how the PSRAM interacts with the system memory bus. All the device operating modes are configured through the BCR. Refer to *Table 7* for the description of the Bus Configuration Register Bits.

7.3.1 Operating Mode Bit (BCR15)

The Operating Mode bit allows the Synchronous mode or the Asynchronous mode (default setting) to be selected. Selecting the Synchronous mode will allow the device to operate either in NOR Flash mode or in full Synchronous Burst mode.

The device will automatically detect that the NOR Flash mode is being used by monitoring a rising edge of the Clock signal, K, when $\overline{L}$ is Low. If this should not be the case, the device operates in full Synchronous mode.

7.3.2 Latency Type (BCR14)

The Latency Type bit is used to configure the latency type. When the Latency Type bit is set to ‘0’, the device operates in variable latency mode (only available for Synchronous Read mode). When it is ‘1’, the fixed latency mode is selected and the latency is defined by the values of bits BCR13 to BCR11.

Refer to *Table 3* and *Table 4* for examples of fixed and variable latency configuration.

7.3.3 Latency Counter Bits (BCR13-BCR11)

The Latency Counter bits are used to set the number of clock cycles between the beginning of a read or write operation and the first data output or input.

The Latency Counter bits can only assume the values shown in *Table 7: Bus Configuration Register Definition* (see also *Figure 3* and *Figure 4*).

7.3.4 WAIT Polarity Bit (BCR10)

The WAIT Polarity bit indicates whether the WAIT output signal is active High or Low. As a consequence, it also determines whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state (see *Figure 9: WAIT Polarity*).

By default, the WAIT output signal is active High.

7.3.5 WAIT Configuration Bit (BCR8)

The system memory microcontroller uses the WAIT signal to control data transfer during Synchronous Burst Read and Write operations.

The WAIT Configuration bit is used to determine when the transition of the WAIT output signal between the asserted and the de-asserted state occurs with respect to valid data available on the data bus.

When the Wait Configuration bit is set to ‘0’, data is valid or invalid on the first Clock rising edge immediately after the WAIT signal transition to the de-asserted or asserted state.

When the Wait Configuration bit is set to ‘1’ (default settings), the WAIT signal transition occurs one clock cycle prior to the data bus going valid or invalid.

See *Figure 8: WAIT Configuration Example* for an example of WAIT configuration.

7.3.6 Driver Strength Bits (BCR5-BCR4)

The Driver Strength bits allow to set the output drive strength to adjust to different data bus loading. Normal driver strength (full drive) and reduced driver strength (half drive and a quarter drive) are available.

By default, outputs are configured at ‘half drive” strength.

7.3.7 Burst Wrap Bit (BCR3)

Burst Read operations can be confined inside the 4, 8, 16 or 32 Word boundary (wrap mode). If the wrap mode is not enabled, the device outputs data sequentially up to the end of the row, regardless of burst boundaries.

The Burst Wrap bit is used to select between ‘wrap’ and ‘no wrap’ mode.

7.3.8 Burst Length Bits (BCR2-BCR0)

The Burst Length bits set the number of Words to be output or input during a Synchronous Burst Read or Write operation. They can be set for 4 Words, 8 Words, 16 Words, 32 Words or Continuous Burst (default settings), where all the Words are output or input sequentially regardless of address boundaries (see also *Table 8: Burst Type Definition*).

Table 7. Bus Configuration Register Definition

Address Bits	Bus Configuration Register Bits	Name	Value	Description
ADQ15	BCR15	Operating Mode Bit	0	Synchronous Mode (NOR Flash or Full Synchronous Mode)
			1	Asynchronous Mode (Default)
ADQ14	BCR14	Latency Type	0	Variable Latency (Default)
			1	Fixed Latency
ADQ13-ADQ11	BCR13-BCR11	Latency Counter Bits	010	3 Clock Cycles
			011	4 Clock Cycles (Default)
			100	5 Clock Cycles
			101	6 Clock Cycles
			110	7 Clock Cycles
			Other Configurations Reserved(1)	
ADQ10	BCR10	WAIT Polarity Bit	0	WAIT Active Low
			1	WAIT Active High (default).See *Figure 9: WAIT Polarity*.
ADQ9	-	-	Must be set to '0'	Reserved(1)
ADQ8	BCR8	Wait Configuration Bit	0	WAIT Asserted During Delay (see *Figure 8: WAIT Configuration Example*).
			1	WAIT Asserted One Clock Cycle Before Delay (Default)
ADQ7-ADQ6	-	-	Must be set to '0'	Reserved(1)
ADQ5-ADQ4	BCR5-BCR4	Driver Strength Bits	00	Full Drive
			01	1/2 Drive (Default)
			10	1/4 Drive
			11	Reserved(1)
ADQ3	BCR3	Burst Wrap Bit	0	Wrap (within the Burst Length)
			1	No Wrap (default)
ADQ2-ADQ0	BCR2-BCR0	Burst Length Bit	001	4 Words
			010	8 Words
			011	16 Words
			100	32 Words
			111	Continuous Burst (default)
			Other Configurations Reserved(1)	

1. Programming the BCR with reserved value will force the device to use the default register settings.

Table 8. Burst Type Definition

Mode	Start Add	4 Words (Sequential) BCR2-BCR0 = 001b	8 Words (Sequential) BCR2-BCR0=010b	16 Words (Sequential) BCR2-BCR0=011b	32 Words (Sequential) BCR2-BCR0=100b	Continuous Burst BCR2-BCR0=111b
Wrap (BCR3='0')	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-...-14-15	0-1-2-3-...-30-31	0-1-2-3-..-511-.
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-...-14-15-0	1-2-3-...-30-31-0	1-2-3-4-...-510-511-
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-...-15-0-1	2-3-4-...-31-0-1	2-3-4-5-6-...-511-
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-...-15-0-1-2	3-4-5-...-31-0-1-2	3-4-5-...-511-
	4		4-5-6-7-0-1-2-3	4-5-...-15-0-1-2-3	4-5-6-...-31-0-1-2-3	4-5-...-511-
	5		5-6-7-0-1-2-3-4	5-6-7-...-15-0-1-...-4	5-6-7-..-31-0-1-..-4	5-6-7-...-511-
	6		6-7-0-1-2-3-4-5	6-7-8-...-15-0-1-...-5	6-7-8-...-31-0-1-...-5	6-7-8-...-511-
	7		7-0-1-2-3-4-5-6	7-8-9-...15-0-1-...-6	7-8-9-...-31-0-1-...-6	7-8-9-...-511-
	...	...	...	...	...	...
	14			14-15-0-1-2-...-13	14-15-...-31-0-...-13	14-...511-
	15			15-0-1-2-...-14	15-0-1-...-31-0-...-14	15-...511-
	...	...	...	...	...	...
	30				30-31-0-...-28-29	30-...-511-
	31				31-0-1-...-29-30	31-...-511-
No Wrap (BCR3='1')	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-...-14-15	0-1-2-3-...-30-31	0-1-2-3-..-511-.
	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-..-15-16	1-2-3-4-...-32	1-2-3-4-...-512-
	2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-...-17	2-3-4-...-33	2-3-4-5-...-513-
	3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-...-18	3-4-5-...-34	3-4-5-...-514-
	4		4-5-6-7-8-9-10-11	4-5-6-...-19	4-5-6-...-35	4-5-6-...-515-
	5		5-6-7-8-9-10-11-12	5-6-7-...-20	5-6-7-...-36	5-6-7-...-516-
	6		6-7-8-9-10-11-12-13	6-7-8-...-21	6-7-8-...-37	6-7-8-...-517-
	7		7-8-9-10-11-12-13-14	7-8-9-...-22	7-8-9-...-38	7-8-9-...-518-
	...	...				...
	14			14-15-...-29	14-15-16-...-46	14-...-525-
	15			15-16-17-...-30	15-16-17-...-47	15-...-526-
	...	...				...
	30				30-31-0-...-28-62	30-...-541-
	31				31-0-1-...-29-63	31-...-542-

Table 9. Variable Latency Counter Configuration

BCR13- BCR11	Latency Configuration Code	Latency		Maximum Clock Rate
		Normal	Refresh Collision	
010	2 (3 clocks cycles)	2	4	52 (19.2ns)
011	3 (4 clocks cycles) - default	3	6	83 (12ns)
Others	Reserved	-	-	-

Table 10. Fixed Latency Counter Configuration

BCR13- BCR11	Latency Configuration Code	Latency	Maximum Clock Rate
010	2 (3 clocks cycles)	2	33 (30ns)
011	3 (4 clocks cycles)-default	3	52 (19.2ns)
100	4 (5 clocks cycles)	4	66 (15ns)
101	5 (6 clocks cycles)	5	75 (13.3ns)
110	6 (7 clocks cycles)	6	83 (12ns
Others	Reserved	-	-

Figure 8. WAIT Configuration Example

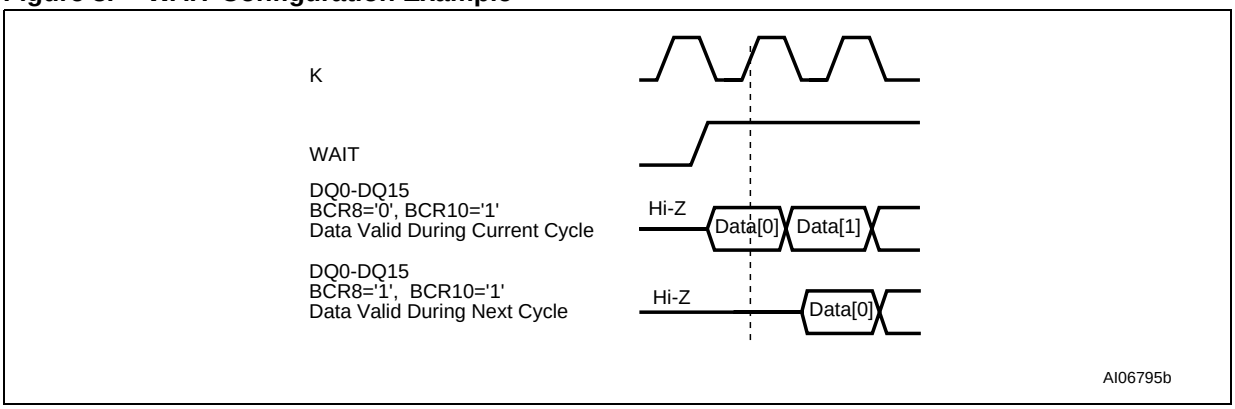
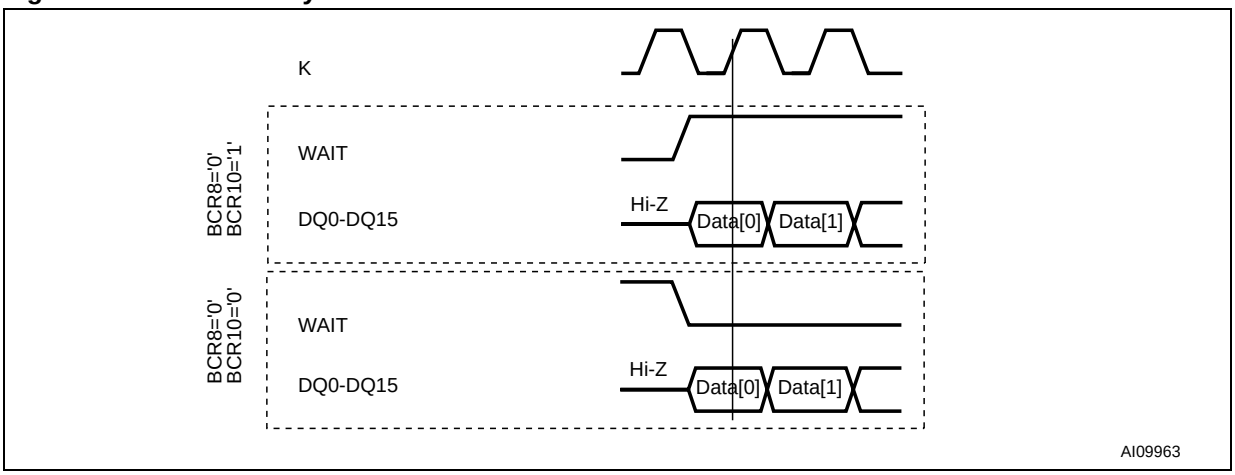


Figure 9. WAIT Polarity



7.4 Refresh Configuration Register

The role of the Refresh Configuration Register (RCR) is:

- to define how the self refresh of the PSRAM array is performed
- to select the Deep Power-Down mode

Refer to *Table 11* for the description of the Refresh Configuration Register Bits.

7.4.1 Deep Power-Down Bit (RCR4)

The Deep Power-Down bit enables or disables all refresh-related operations. Deep Power-Down mode is enabled when the RCR4 bit is set to '0', and remains enabled until this bit is set to '1'. When $\overline{E}$ goes high, the device enters Deep-Power Down mode and remains in this mode until the $\overline{E}$ mean time goes low and stays low for at least 10µs. At power-up, the Deep Power-Down mode is disabled.

See the *Section 4.2: Deep Power-Down* for more details.

7.4.2 Partial Array Refresh Bits (RCR2-RCR0)

The Partial Array Refresh bits allow refresh operations to be restricted to a portion of the total PSRAM array. The refresh options can be full array, one half, one quarter, one eighth or none of the array. These memory areas can be located either at the top or bottom of the memory array. By default, the full memory array is refreshed.

Table 11. Refresh Configuration Register Definition

Address Bits	Refresh Configuration Register Bits	Name	Value	Description
ADQ15-ADQ5	-	-	Must be set to '0'	Reserved
ADQ4	RCR4	Deep Power-Down Bit	0	Deep Power-Down Enabled
			1	Deep Power-Down Disabled (Default)
ADQ3	-	-	Must be set to '0'	Reserved
ADQ2-ADQ0	RCR2-RCR0	Partial Array Refresh Bits	000	Full Array Refresh (Default)
			001	Refresh of the Bottom Half of the Array
			010	Refresh of the Bottom Quarter of the Array
			011	Refresh of the Bottom Eighth of the Array
			100	None of the Array
			101	Refresh of the Top Half of the Array
			110	Refresh of the Top Quarter of the Array
			111	Refresh of the Top Eighth of the Array

7.5 Device ID Register

The Device ID Register (DIDR) is a read-only register that contains the Manufacturer code. It is preprogrammed by STMicroelectronics and cannot be modified by the user.

Refer to *Table 12* for the description of the Bus Configuration Register Bits.

Table 12. Device ID Register Definition

Address Bits	Device ID Register Bits	Name	Value	Description
ADQ15	DID15	Row Length	0	128 Words
			1	256 Words
ADQ14-ADQ11	DIDR14-DIDR11	Design Version	0000	A
			0001	B
			0010	C
			0011	D
			1111	P
			Other Configurations Reserved	
ADQ10-ADQ8	DIDR10-DIDR8	Device Density	000	16 Mbits
			001	32 Mbits
			010	64 Mbits
			011	128 Mbits
			100	256 Mbits
			Other Configurations Reserved	
ADQ7-ADQ5	DIDR7-DIDR5	PSRAM Generation	001	1.0
			010	1.5
			011	2.0
			Other Configurations Reserved	
ADQ4-ADQ0	DIDR4-DIDR0	Manufacturer ID	00001	Cypress
			00010	Infineon
			00011	Micron
			00100	Renesas
			01111	STMicroelectronics
			Other Configurations Reserved	

8 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 13. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	–30	+85	°C
T_{STG}	Storage Temperature	–55	150	°C
V_{CC}	Core Supply Voltage	–0.2	2.45	V
V_{CCQ}	Input/Output Buffer Supply Voltage	–0.2	2.45	V
V_{IO}	Input or Output Voltage	–0.2	2.45	V

9 DC and AC parameters

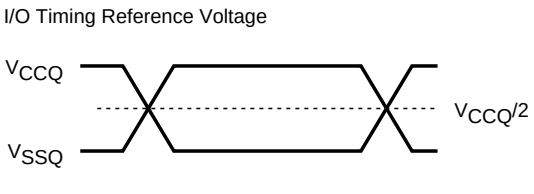
This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 14: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 14. Operating and AC measurement conditions(1)

Parameter	M69KM096AA		Unit
	Min	Max	
V_{CC} Supply Voltage	1.7	1.95	V
V_{CCQ} Input/Output Buffer Supply Voltage	1.7	1.95	V
Load Capacitance (C_L)	30		pF
Output Circuit Protection Resistance (R)	50		Ω
Input Pulse Voltages(2)(3)	0	V_{CC}	V
Input and Output Timing Ref. Voltages(2)(3)	$V_{CC}/2$		V
Input Rise Time t_r and Fall Time t_f(2)(3)		1	V/ns

1. All voltages are referenced to V_{SS}.
2. Referenced to V_{SS}.
3. V_{CC}=V_{CCQ}

Figure 10. AC Measurement I/O Waveform



1. Logic states ‘1’ and ‘0’ correspond to AC test inputs driven at V_{CCQ} and V_{SS} respectively. Input timings begin at $V_{CCQ}/2$ and output timings end at $V_{CCQ}/2$.

Figure 11. AC Input Transitions

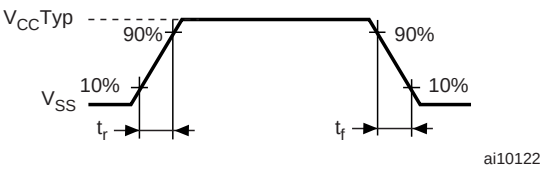


Figure 12. AC Measurement Load Circuit

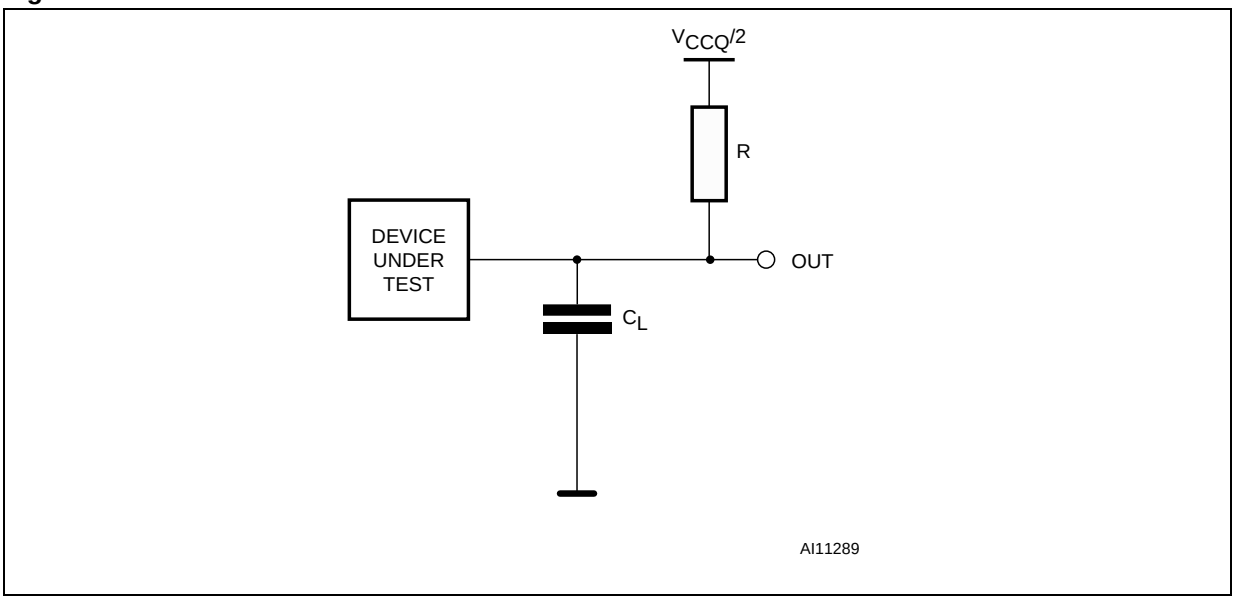


Table 15. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1MHz, V_{IN} = 0V	2	6	pF
C_{IO}	Data Input/Output Capacitance		3.5	6	pF

Table 16. DC characteristics

Symbol	Parameter	Refreshed Array	Test Conditions	Min.	Typ	Max.	Unit
V_{OH}(1)	Output High Voltage		I_{OH} = –0.2mA	$0.8V_{CCQ}$			V
V_{OL}(1)	Output Low Voltage		I_{OL} = 0.2mA			$0.2V_{CCQ}$	V
V_{IH}(2)	Input High Voltage			V_{CCQ} – 0.4		V_{CCQ} + 0.2	V
V_{IL}(3)	Input Low Voltage			–0.2		0.4	V
I_{LI}	Input Leakage Current		V_{IN} = 0 to V_{CCQ}			1	µA
I_{LO}	Output Leakage Current		$\overline{G}$ = V_{IH} or $\overline{E}$ = V_{IH}			1	µA
I_{CC1}(4)	Asynchronous Read/Write Random at t_{RC} min		V_{IN} = 0V or V_{CCQ}, I_{OUT} = 0mA, $\overline{E}$ = V_{IL}			25	mA
I_{CC2}(4)	Burst, Initial Read/Write Access		V_{IN} = 0V or V_{CCQ} I_{OUT} = 0mA, $\overline{E}$ = V_{IL}			30	mA
I_{CC3R}(4)	Continuous Burst Read		V_{IN} = 0V or V_{CCQ} I_{OUT} = 0mA, $\overline{E}$ = V_{IL}			25	mA
I_{CC3W}(4)	Continuous Burst Write		V_{IN} = 0V or V_{CCQ} I_{OUT} = 0mA, $\overline{E}$ = V_{IL}			30	mA

Table 16. DC characteristics (continued)

Symbol	Parameter	Refreshed Array	Test Conditions	Min.	Typ	Max.	Unit
I_{PASR}(4)	Partial Array Refresh Standby Current	Full Array	V_{IN} = 0V or V_{CCQ} $\overline{E}$ = V_{CCQ}			140	µA
		1/2 Array				120	µA
		1/4 Array				110	µA
		1/8 Array				105	µA
		None				95	µA
I_{SB}(5)	Standby Current		V_{IN} = 0V or V_{CCQ} $\overline{E}$ = V_{CCQ}			140	µA
I_{CCPD}	Deep-Power Down Current		V_{IN} = 0V or V_{CCQ}, V_{CC} = V_{CCQ} = 1.95V, T_A= +85°C		3	10	µA

1. BCR5-BCR4 = 01 (default settings).
2. Input signals may overshoot to V_{CCQ}+ 1.0V for periods of less than 2ns during transitions.
3. Output signals may undershoot to V_{SS} – 1.0V for periods of less than 2ns during transitions.
4. This parameter is specified with all outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected for the actual system.
5. I_{SB} maximum value is measured at +85°C with PAR set to Full Array. In order to achieve low standby current, all inputs must be driven either to V_{CCQ} or V_{SSQ}. I_{SB} might be slightly higher for up to 500ms after Power-up, or when entering Standby mode.

Figure 13. Asynchronous Random Read AC waveforms

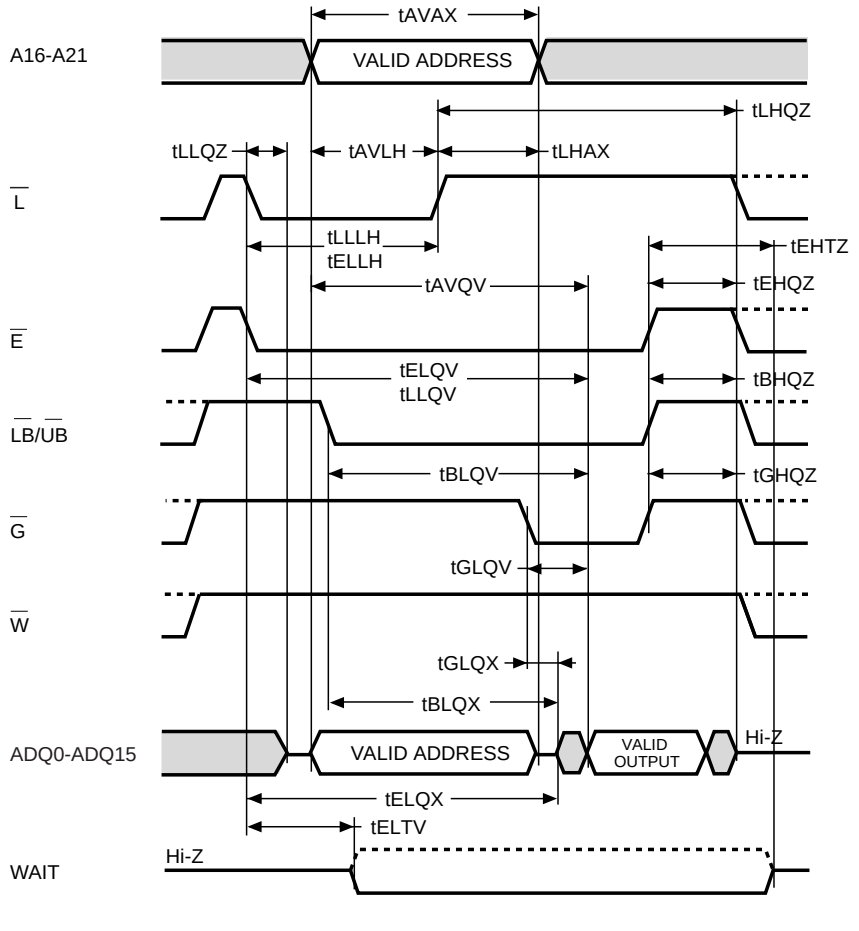
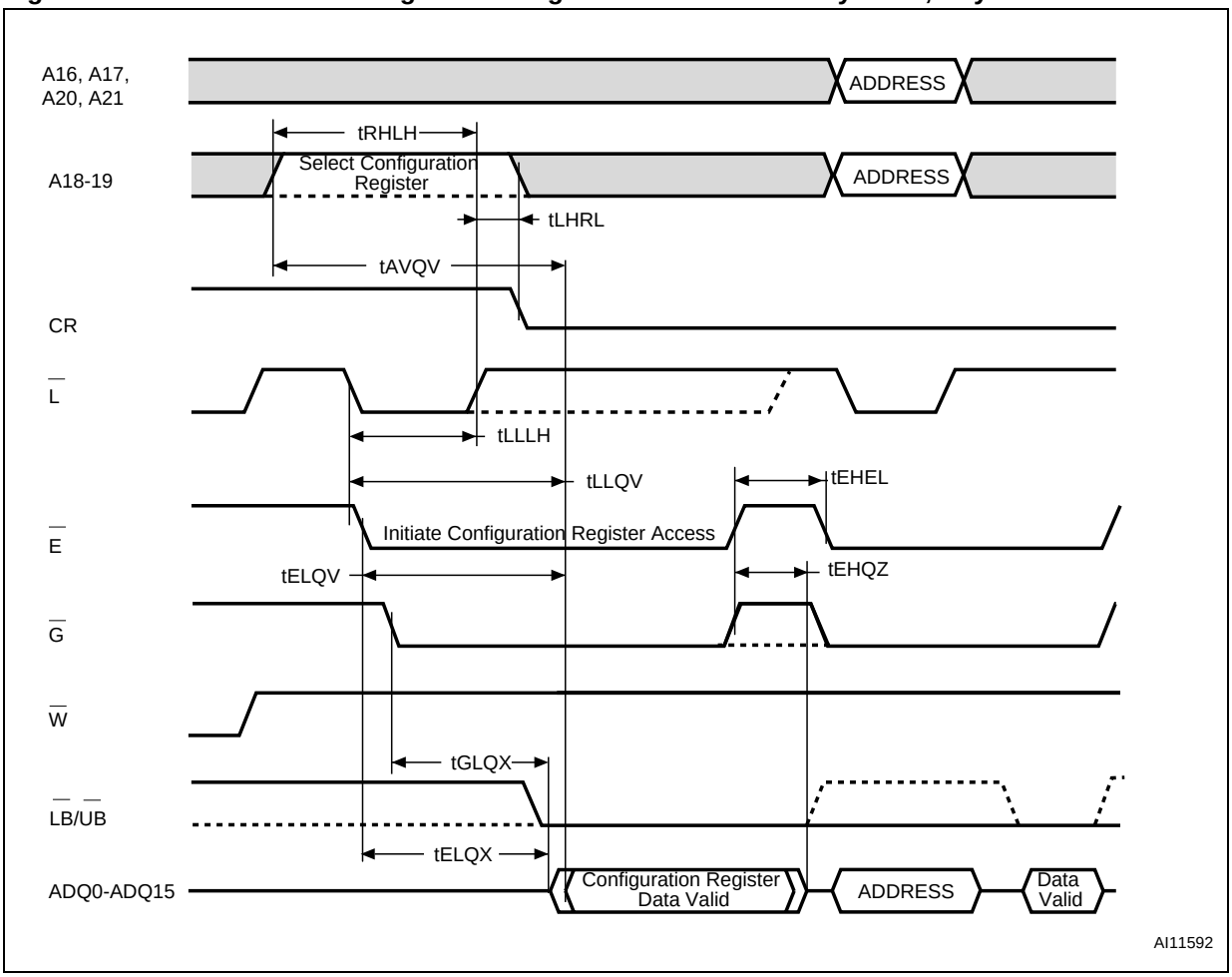


Figure 14. CR Controlled Configuration Register Read Followed by Read, Asynchronous Mode



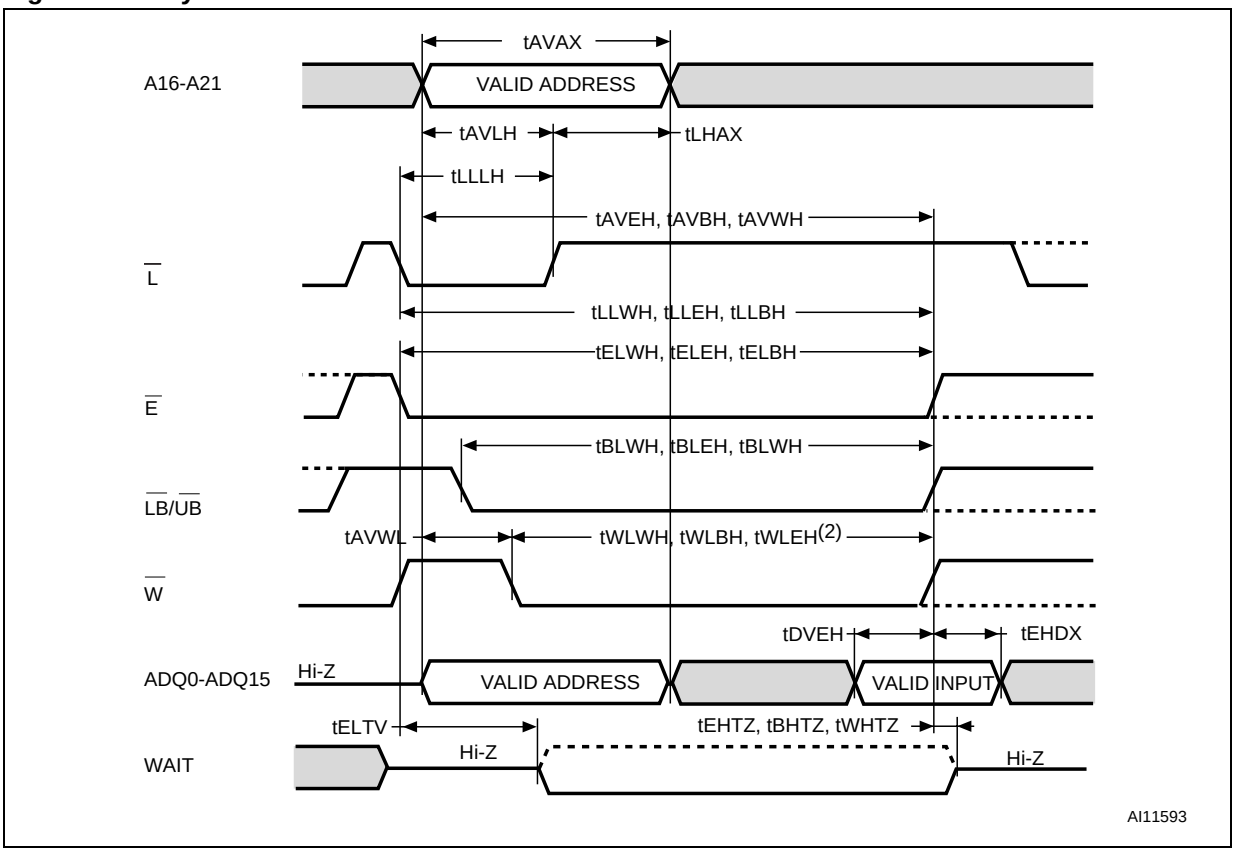
1. A18-A19 must be set to ‘00b’ to select RCR, ‘01b’ to select the BCR, and ‘1Xb’ to select the DIDR.

Table 17. Asynchronous Read AC characteristics(1)

Symbol	Alt.	Parameter	Min	Max	Unit
t_{AVQV}	t_{AA}	Address Valid to Output Valid		70	ns
t_{AVAX}	t_{RC}	Read Cycle Time	70		ns
t_{AVLH} t_{RHLH}	t_{AVS}	Address Valid to $\overline{L}$ High Configuration Register High to $\overline{L}$ High	5		ns
t_{BLQV}	t_{BA}	Upper/Lower Byte Enable Low to Output Valid		70	ns
t_{BHQZ}(2)	t_{BHZ}	Upper/Lower Byte Enable High to Output Hi-Z		8	ns
t_{BLQX}(3)	t_{BLZ}	Upper/Lower Byte Enable Low to Output Transition	10		ns
t_{ELTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	ns
t_{ELQV}	t_{CO}	Chip Enable Low to Output Valid		70	ns
t_{ELLH}	t_{CVS}	Chip Enable Low to $\overline{L}$ High	7		ns
t_{EHEL}	t_{CBPH}	Chip Enable High between Subsequent Asynchronous Operations	6		ns
t_{EHQZ}(2)	t_{HZ}	Output Enable High to Output Hi-Z Chip Enable High to Output Hi-Z		8	ns
t_{ELQX}(3)	t_{LZ}	Chip Enable Low to Output Transition	10		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		20	ns
t_{GHQZ}(2)	t_{OHZ}	Output Enable Low to Output Hi-Z		8	ns
t_{GLQX}(3)	t_{OLZ}	Output Enable Low to Output Transition	3		ns
t_{LLQV}	t_{AADV}	Latch Enable Low to Output Valid		70	ns
t_{LHAX} t_{LHRL}	t_{AVH}	Latch Enable High to Address Transition Latch Enable High to Configuration Register Low	2		ns
t_{LHQZ}	t_{AHZ}	Latch Enable High Output Low-Z	3		ns
t_{LLQZ}	t_{AHZ}	Latch Enable Low Output Hi-Z		8	ns
t_{LLLH}	t_{VP}	Latch Enable Low Pulse Width	5		ns

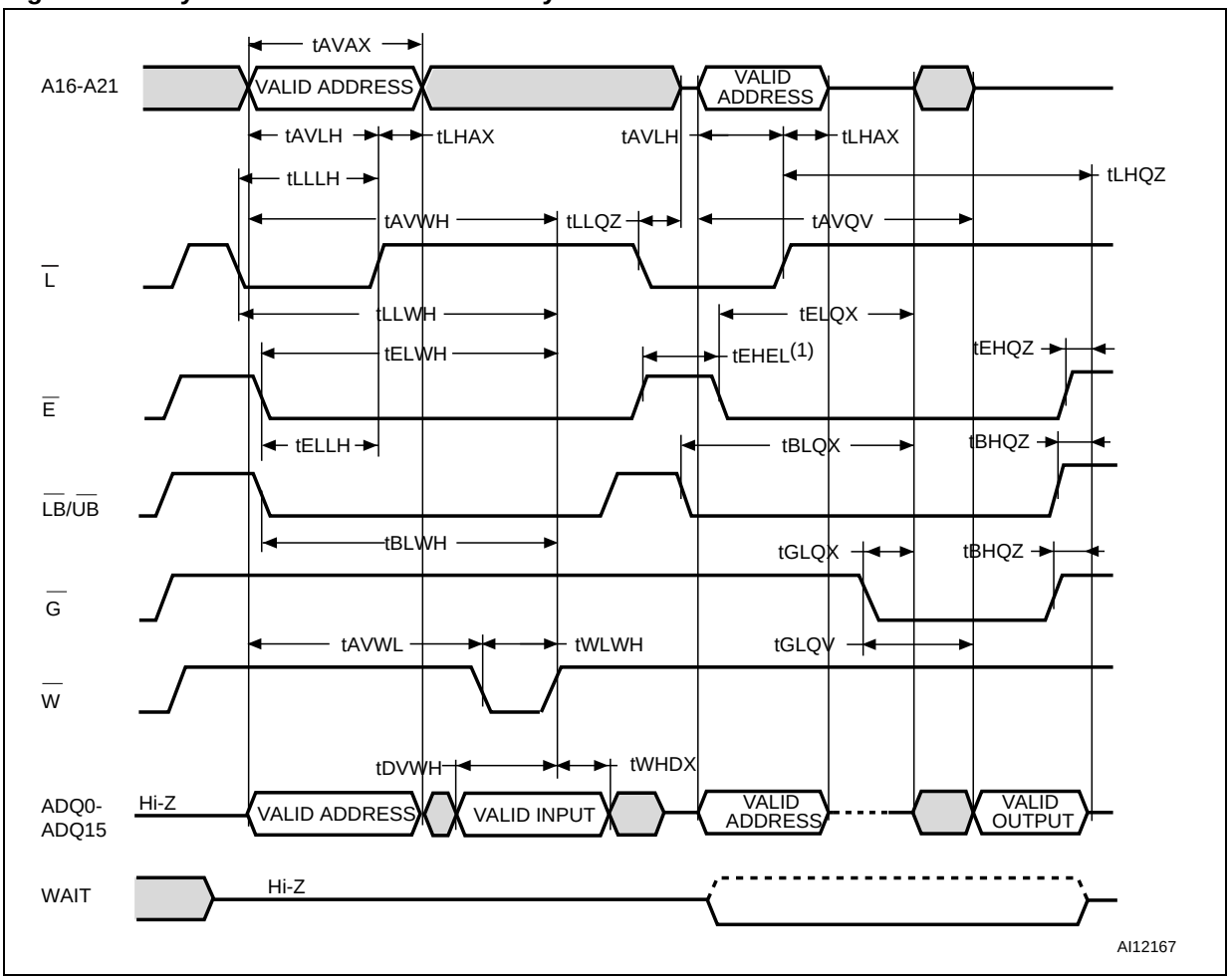
1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 12: AC Measurement Load Circuit*.
2. The Hi-Z timings measure a 100mV transition from either V_{OH} or V_{OL} to $V_{CCQ}/2$.
3. The Low-Z timings measure a 100mV transition from the Hi-Z ($V_{CCQ}/2$) level to either V_{OH} or V_{OL}.

Figure 15. Asynchronous Write AC waveforms



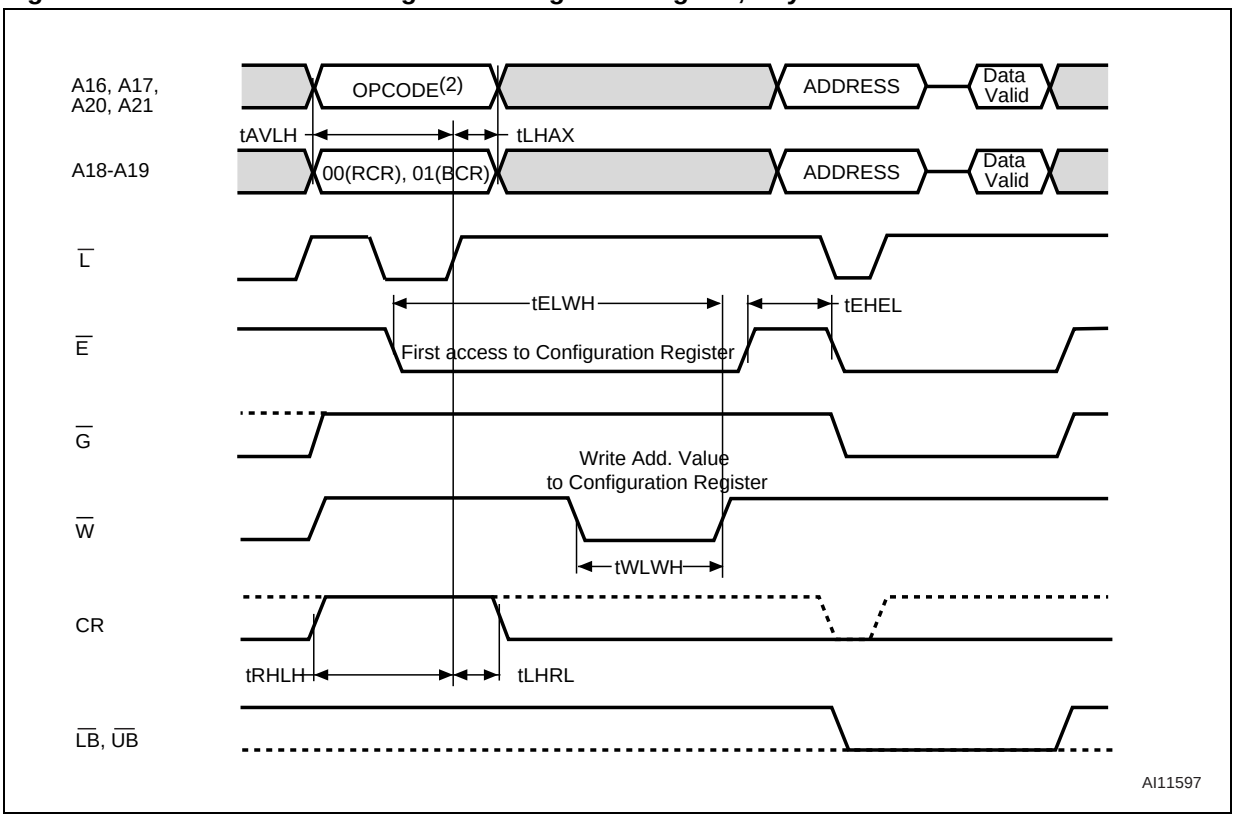
1. Data Inputs are Hi-Z if $\overline{E}$ is High, V_{IH}.
2. When $\overline{E}$ is Low, V_{IL} (device selected), $\overline{W}$ must not remain Low, for longer than t_{ELEH}.
3. The end of the Write operation is controlled by $\overline{E}$, $\overline{LB}$, $\overline{UB}$, or $\overline{W}$, whichever is de-asserted first.

Figure 16. Asynchronous Write followed by Read AC waveforms



1. When configured to operate in Synchronous mode (BCR[15] = 0), $\overline{E}$ must remain High, V_{IH}, for at least t_{ELEH} to schedule the appropriate refresh interval. Otherwise, t_{ELEH} is only required after $\overline{E}$ controlled write operations.

Figure 17. CR Controlled Configuration Register Program, Asynchronous mode



1. Only the content of the Bus Configuration Register (BCR) and Refresh Configuration Register (RCR) can be modified.
2. The Opcode is the value to be written the configuration register.
3. CR is latched on the rising edge of $\overline{L}$. There is no setup requirement of CR with respect to $\overline{E}$.

Table 18. Asynchronous Write AC characteristics(1)

Symbol	Alt.	Parameter	Min	Max	Unit
t_{AVBL}, t_{AVEL} t_{AVWL}, t_{LLWL}	t_{AS}	Address Set-up to Beginning of Write Operation	0		ns
t_{AVLH}, t_{RHLH}	t_{AVS}	Address Valid to Latch Enable High Configuration Register High to Latch Enable High	5		ns
t_{AVWH}, t_{AVEH} t_{AVBH}	t_{AW}	Address Set-up to End of Write Operation	70		ns
t_{AVAX}	t_{WC}	Write Cycle Time	70		ns
t_{BLBH}, t_{BLEH} t_{BLWH}	t_{BW}	Upper/Lower Byte Enable Low to End of Write Operation	70		ns
t_{ELTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	ns
t_{EHEL}	t_{CBPH}	Chip Enable High between Subsequent Asynchronous Operations	6		ns
t_{ELLH}	t_{CVS}	Chip Enable Low to $\overline{L}$ High	7		ns
t_{ELWH}, t_{ELEH} t_{ELBH}	t_{CW}	Chip Enable Low to End of Write Operation	70		ns
t_{EHDX} t_{WHDX} t_{BHDX}	t_{DH}	Input Hold from Write	0		ns
t_{ELWH}, t_{DVBH} t_{DVEH}, t_{DVWH}	t_{DW}	Input Valid to Write Setup Time	20		ns
t_{EHTZ}, t_{BHTZ}, t_{WHTZ}(2)	t_{HZ}	Chip Enable High to WAIT Hi-Z $\overline{LB}$/$\overline{UB}$ High to WAIT Hi-Z Write Enable High to WAIT Hi-Z		8	ns
t_{LLWH}, t_{LLEH}, t_{LLBH}	t_{VS}	Latch Enable Low to Write Enable High	70		ns
t_{LHAX}, t_{LHRL}	t_{AVH}	Latch Enable High to Address Transition or Latch Enable High to Configuration Register Low	2		ns
t_{LLLH}	t_{VP}	Latch Enable Low Pulse Width	5		ns
t_{WHQZ}	t_{OW}	End of Write to Input Low-Z	5		ns
t_{WLBH}, t_{WLEH} t_{WLWH}(3)	t_{WP}	Write Pulse Width	45		ns
t_{WHWL}	t_{WPH}	Write Enable Pulse Width High	10		ns

1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 12: AC Measurement Load Circuit*.
2. The Hi-Z timings measure a 100mV transition from either V_{OH} or V_{OL} to $V_{CCQ}/2$. The Low-Z timings measure a 100mV transition from the Hi-Z ($V_{CCQ}/2$) level to either V_{OH} or V_{OL}.
3. $\overline{W}$ Low time must be limited to t_{EHEL}.

Figure 18. Clock input AC waveform

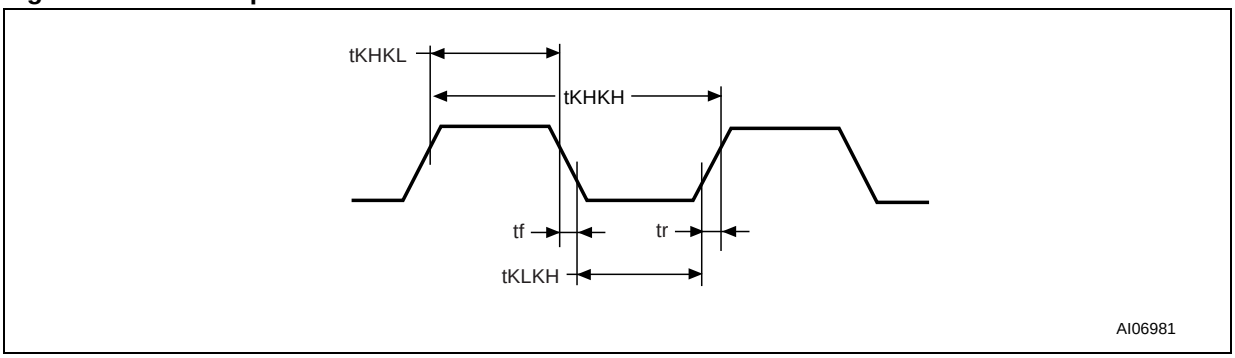
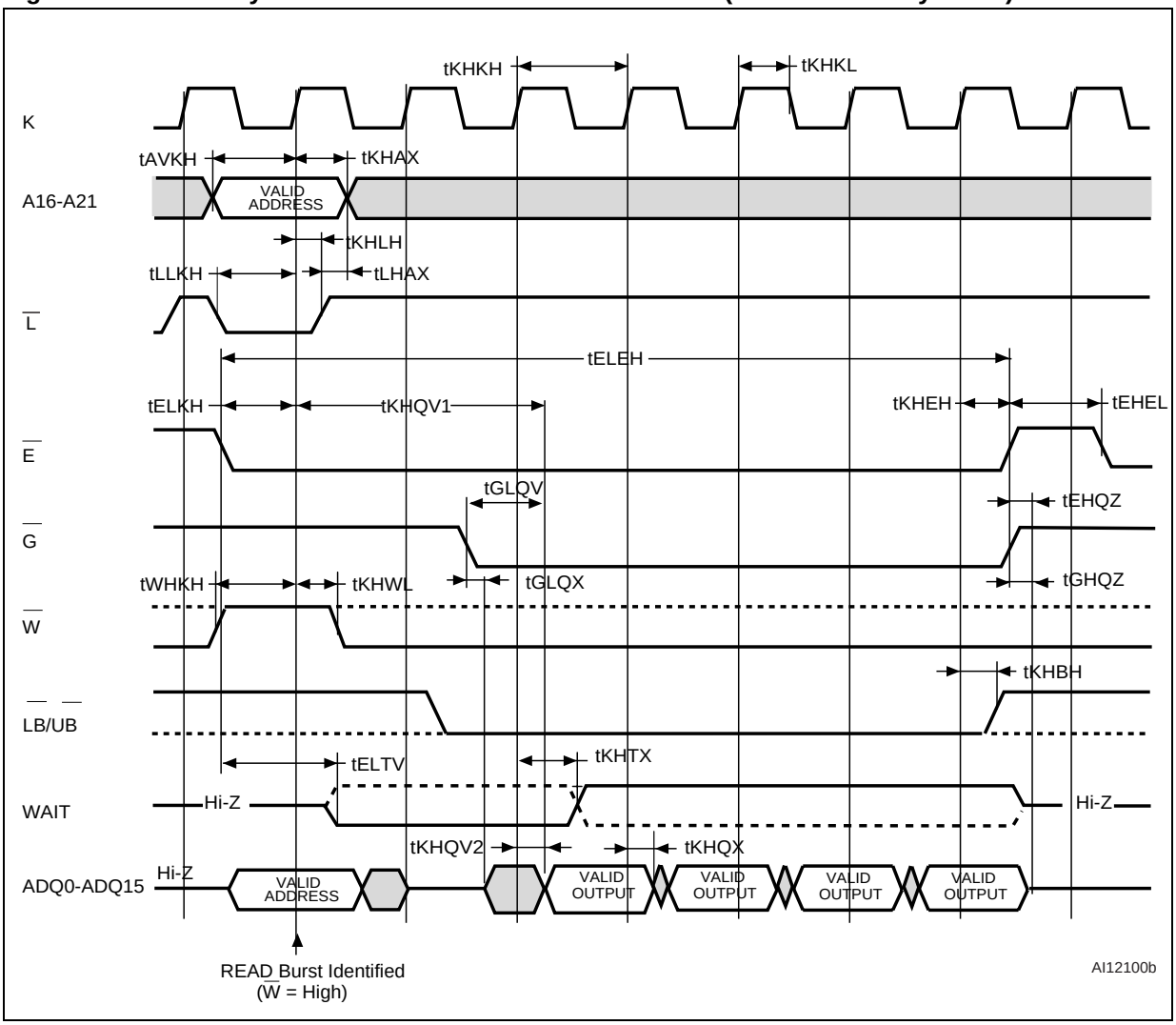


Table 19. Clock Related AC characteristics

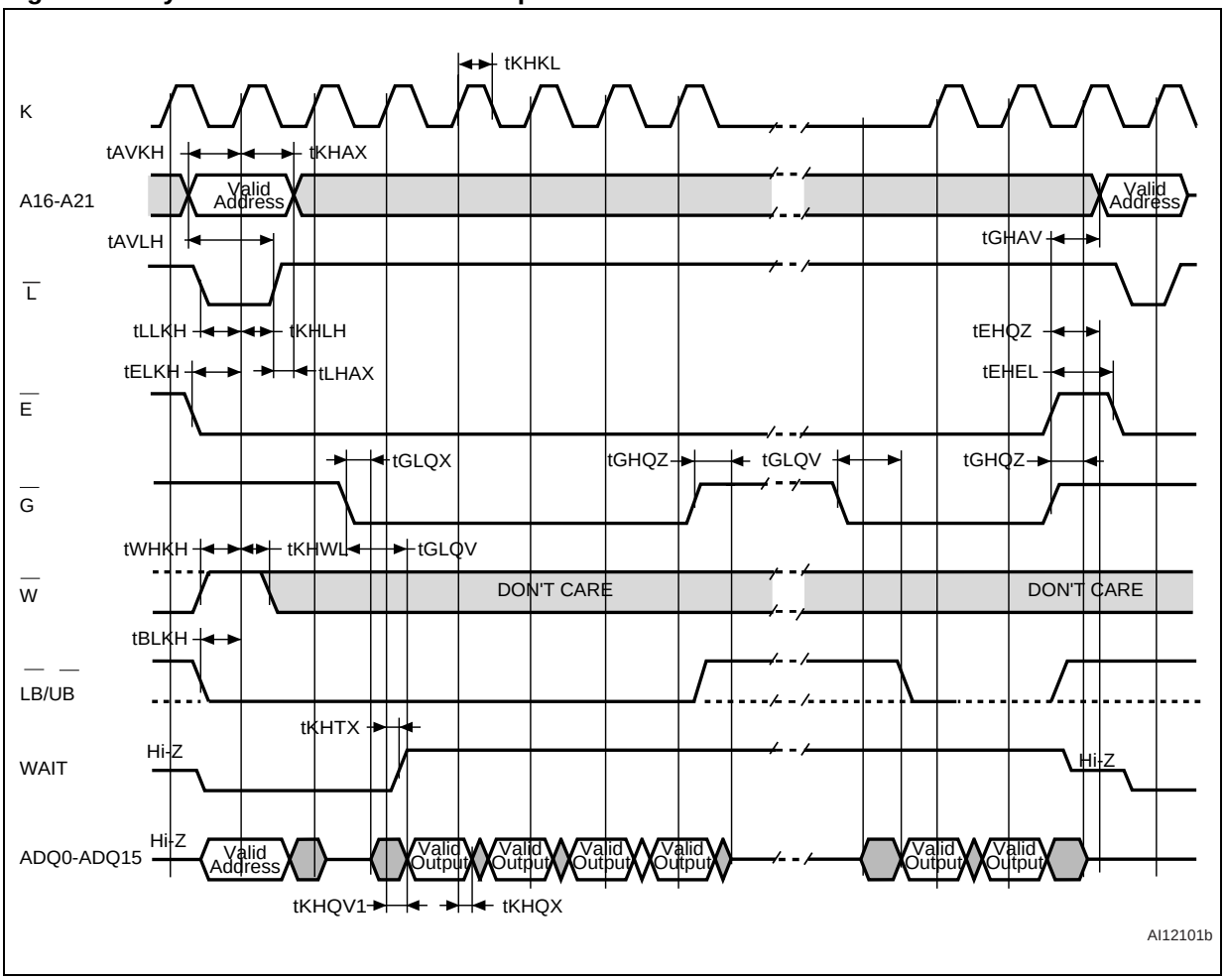
Symbol	Alt.	Parameter	M69KM096AA 83MHz		Unit
			Min	Max	
f_{CLK}	f_{CLK}	Clock frequency		83	MHz
t_{KHKH}	t_{CLK}	Clock Period	12		ns
t_{KHKL}, t_{KLKH}	t_{KP}	Clock High to Clock Low, Clock Low to Clock High	4		ns
t_R, t_F	t_{KHKL}	Clock Rise Time, Clock Fall Time		1.8	ns

Figure 19. 4-Word Synchronous Burst Read AC waveforms (Variable Latency Mode)



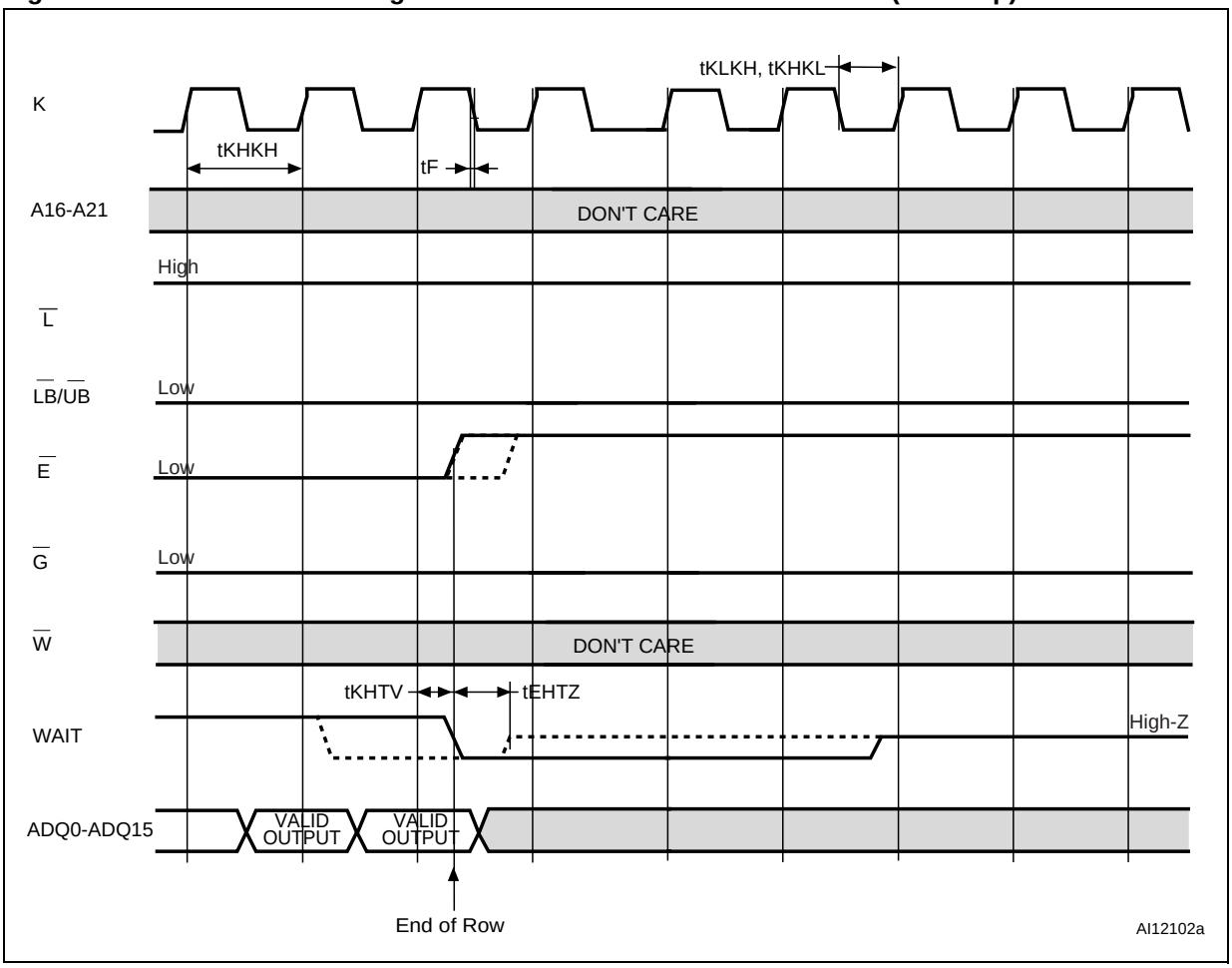
1. The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).

Figure 20. Synchronous Burst Read Suspend and Resume AC waveforms



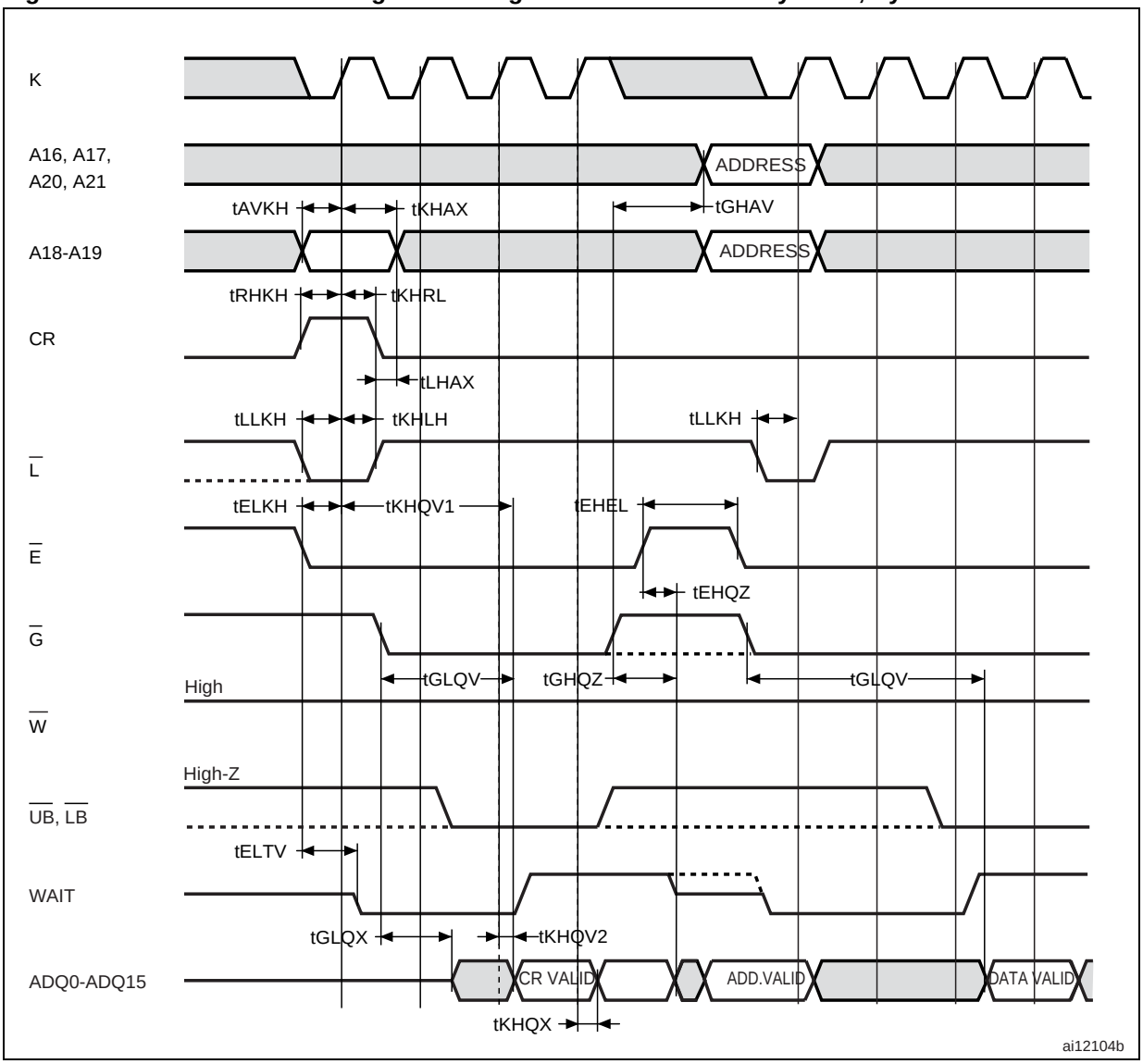
1. The latency Type (BCR14) can be set to fixed or variable during Burst Read Suspend operations.The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).
2. During Burst Read Suspend operations, the Clock signal must be stopped (Low).
3. $\overline{G}$ can be held Low, V_{IL}, during Burst Suspend operations. If so, data output remain valid.

Figure 21. Burst Read Showing End-of-Row Condition AC waveforms (No Wrap)



1. The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).

Figure 22. CR Controlled Configuration Register Read Followed by Read, Synchronous Mode



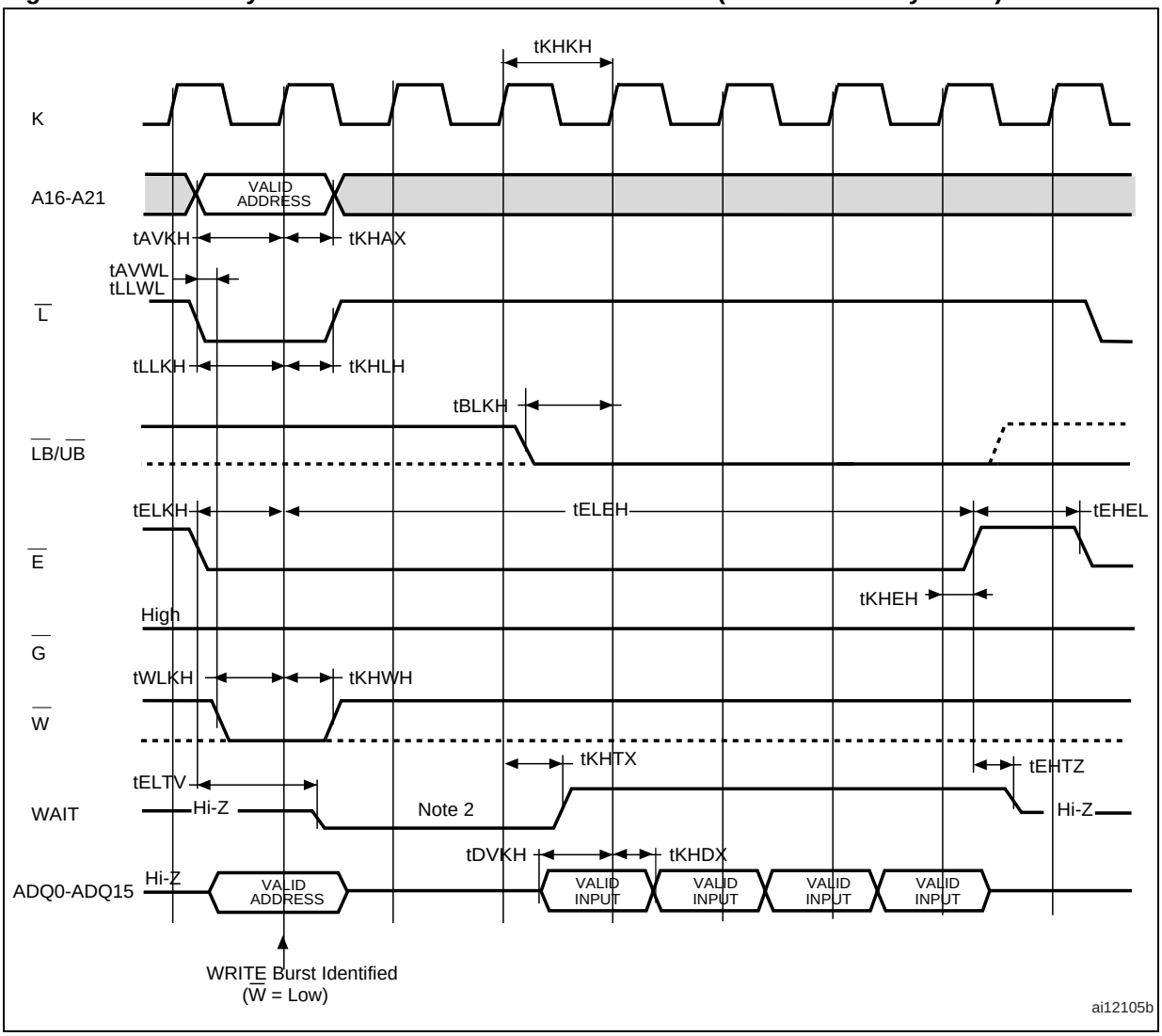
1. A18-A19 must be set to ‘00b’ to select RCR, ‘01b’ to select the BCR, and ‘1Xb’ to select the DIDR.

Table 20. Synchronous Burst Read AC characteristics(1)

Symbol	Alt.	Parameter	M69KM096AA		Unit
			83MHz		
			Min	Max	
t_{AVQV}	t_{AA}	Address Valid to Output Valid (Fixed Latency)		70	ns
t_{AVKH}, t_{RHKH} t_{QVKH}, t_{LLKH} t_{BLKH}, t_{WHKH}	t_{SP}	Set-up Time to Active Clock Edge	3		ns
t_{EHEL}(2)	t_{CBPH}	Chip Enable High between Subsequent Operations in Full-Synchronous or NOR-Flash mode.	6		ns
t_{ELEH}(2)	t_{CEM}	Chip Enable Pulse Width		4	µs
t_{ELTV}, t_{LLTV}	t_{CEW}	Chip Enable Low to WAIT Valid Latch Enable Low to WAIT Valid	1	7.5	ns
t_{ELQV}	t_{CO}	Chip Enable Low to Output Valid		70	ns
t_{ELKH}	t_{CSP}	Chip Enable Low to Clock High	4		ns
t_{EHQZ}, t_{EHTZ}(3)	t_{HZ}	Chip Enable High to Output Hi-Z or WAIT Hi-Z		8	ns
t_{GLQV}	t_{BOE}	Delay From Output Enable Low to Output Valid in Burst mode		20	ns
t_{GHQZ}(3)	t_{OHZ}	Output Enable High to Output Hi-Z		8	ns
t_{GLQX}(4)	t_{OLZ}	Output Enable Low to Output Transition	3		ns
t_{KHQV1}	t_{ABA}	Burst to Read Access Time (Variable Latency)		46	ns
t_{KHQV2}	t_{ACLK}	Clock High to Output Delay		9	ns
t_{KHAX}, t_{KHBH} t_{KHWL}, t_{KHEH} t_{KHLH}, t_{KHQX}	t_{HD}	Hold Time from Active Clock Edge	3		ns
t_{LLQV}	t_{AADV}	Latch Enable Low to Output Valid (Fixed Latency)		70	ns
t_{KHTX}, t_{KHTV}	t_{KHTL}	Clock High to WAIT Valid		9	ns
t_{LHAX}	t_{AVH}	Address hold from Latch Enable High (fixed latency)	2		ns
t_{GHAV}	t_{OHZS}	Output Enable High to Address valid	8		ns

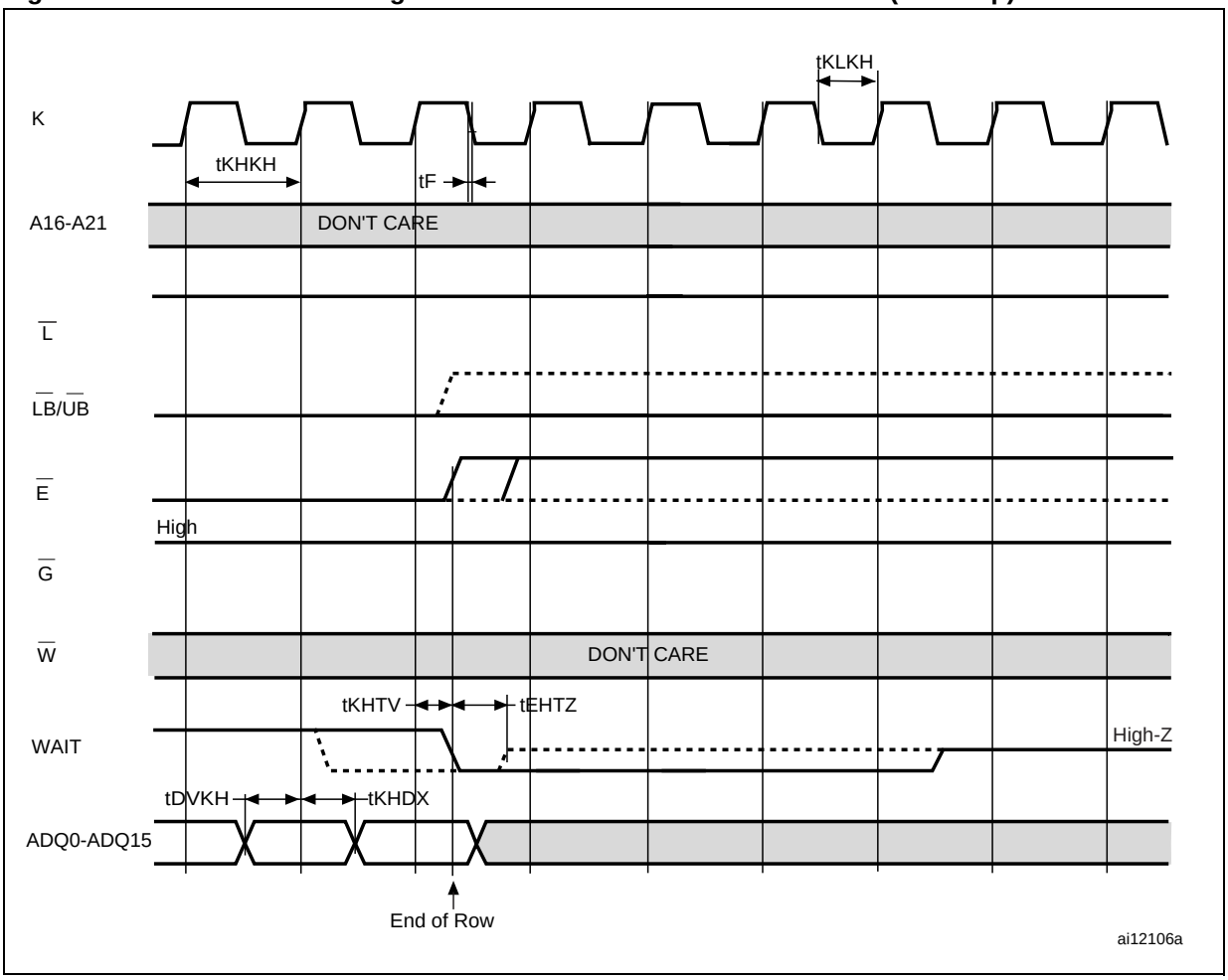
1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 12: AC Measurement Load Circuit*.
2. A refresh opportunity must be offered every t_{ELEH}. A refresh opportunity is possible either if $\overline{E}$ is High during the rising edge of K; or if $\overline{E}$ is High for longer than 15ns.
3. The Hi-Z timings measure a 100mV transition from either V_{OH} or V_{OL} to $V_{CCQ}/2$.
4. The Low-Z timings measure a 100mV transition from the Hi-Z ($V_{CCQ}/2$) level to either V_{OH} or V_{OL}.

Figure 23. 4-Word Synchronous Burst Write AC waveforms (Variable Latency Mode)



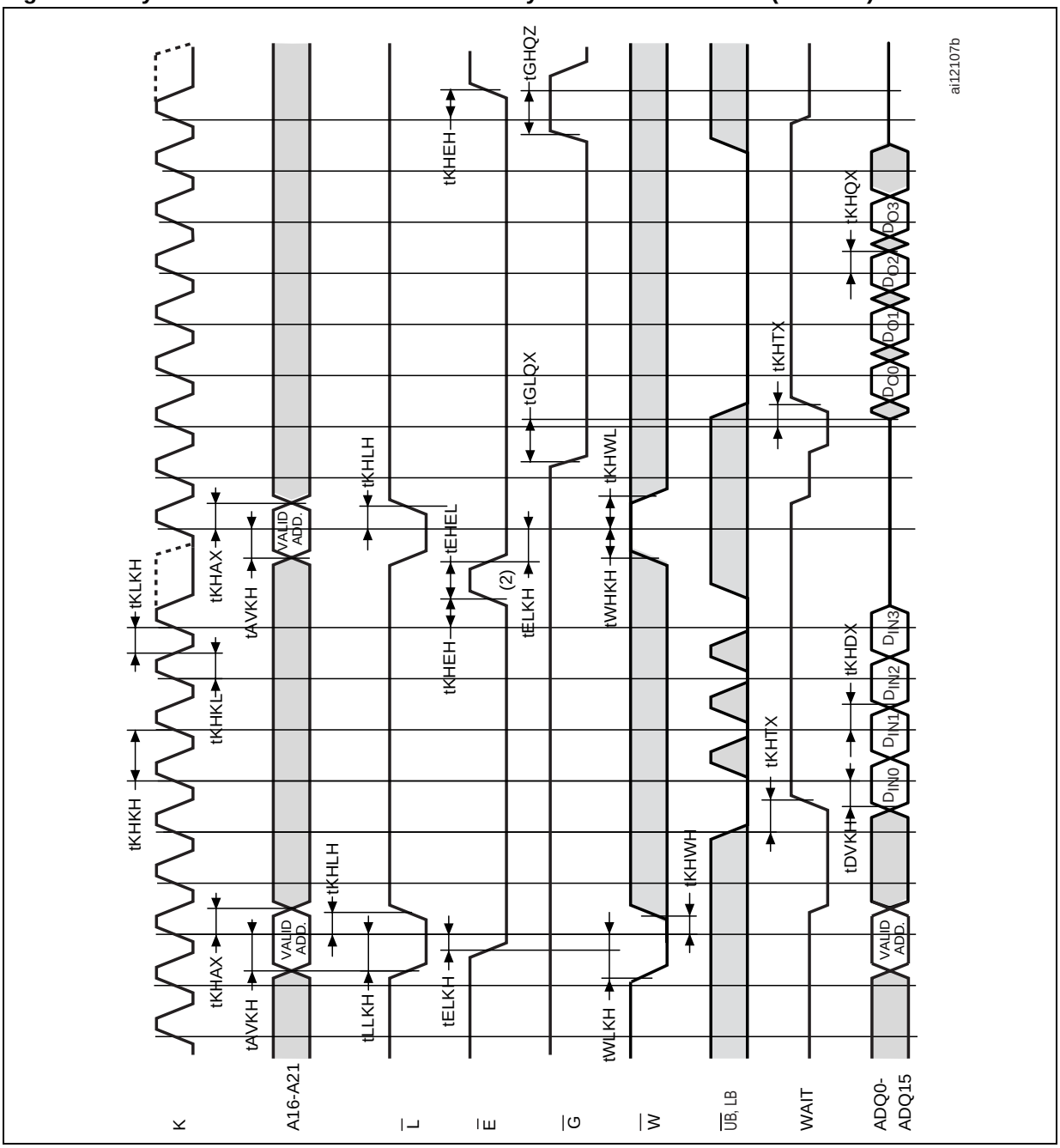
1. The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and asserted during delay (BCR8=0).
2. The WAIT signal must remain asserted for LC clock cycles (LC Latency code), whatever the Latency mode (fixed or variable).
3. t_{AVLL} and t_{LLWL}, are required if t_{ELKH}> 20ns.

Figure 24. Burst Write Showing End-of-Row Condition AC waveforms (No Wrap)



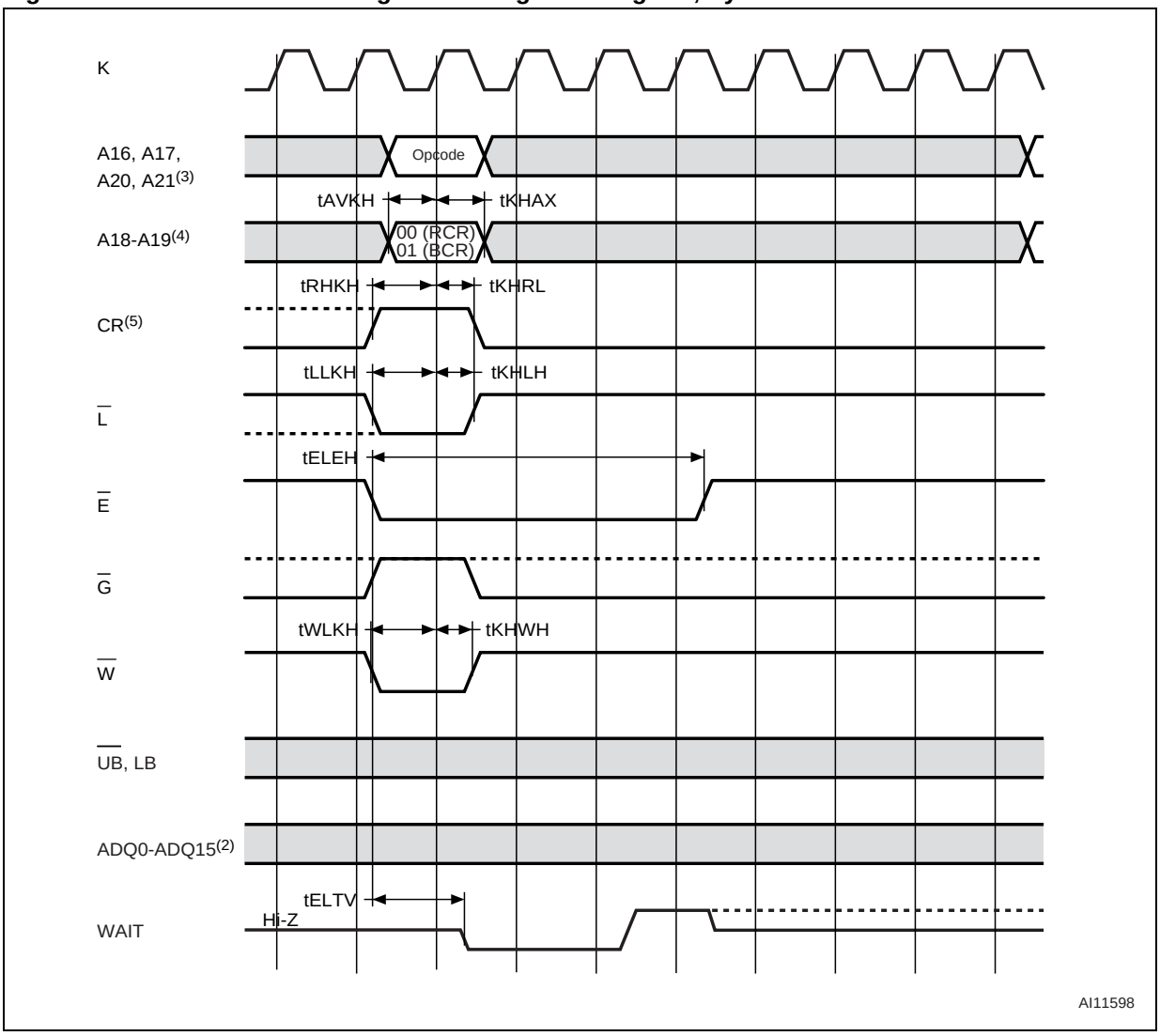
1. The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).

Figure 25. Synchronous Burst Write Followed by Read AC waveforms (4 Words)



1. The Latency type can set to fixed or variable mode. The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).
2. $\overline{E}$ can remain Low between the Burst Read and Burst Write operation, but it must not be held Low for longer than t_{ELEH}.

Figure 26. CR Controlled Configuration Register Program, Synchronous Mode



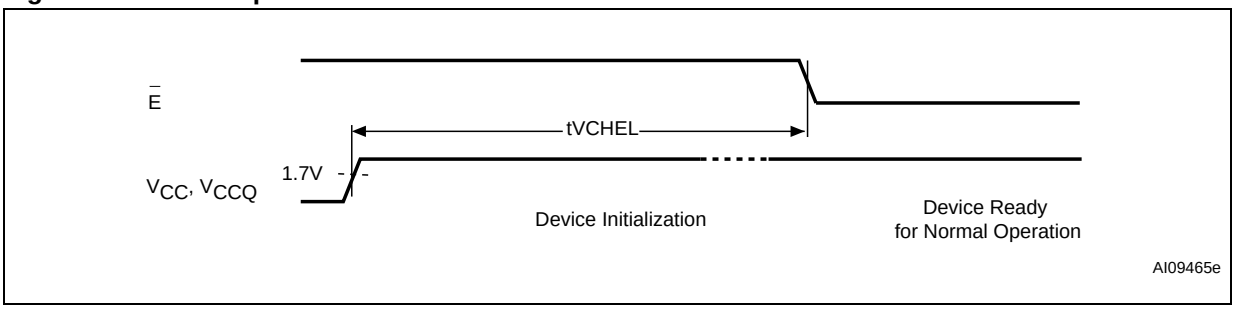
1. Only the Configuration Register (BCR) and the Refresh Configuration Register (RCR) can be modified.
2. Data Inputs/Outputs are not used.
3. The Opcode is the value to be written in the Configuration Register.
4. A19 gives the Configuration Register address.
5. CR initiates the Configuration Register Access.

Table 21. Synchronous Burst Write AC characteristics(1)

Symbol	Alt.	Parameter	M69KM096AA 83MHz		Unit
			Min	Max	
t_{AVWL} t_{LLWL}(2)	t_{AS}	Address Set-up to Beginning of Write Operation	0		ns
t_{AVKH} t_{DVKH} t_{WLKH} t_{LLKH} t_{BLKH} t_{WHKH} t_{WHWL}	t_{SP}	Set-up Time to Active Clock Edge	3		ns
t_{LHAX}	t_{AVH}	Latch Enable High to Address Transition (Fixed Latency)	2		ns
t_{EHEL}(3)	t_{CBPH}	Chip Enable High between Subsequent Operations in Full-Synchronous or NOR-Flash mode.	6		ns
t_{ELEH}(3)	t_{CEM}	Maximum Chip Enable Low Pulse		4	µs
t_{ELTV} t_{LLTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	ns
t_{ELKH}	t_{CSP}	Chip Enable Low to Clock High	4		ns
t_{EHDZ} t_{EHTZ}(4)	t_{HZ}	Chip Enable High to Input Hi-Z or WAIT Hi-Z		8	ns
t_{KHAX} t_{KHRL} t_{KHLH} t_{KHDX} t_{KHEH} t_{KHBH} t_{KHWH}	t_{HD}	Hold Time from Active Clock Edge	3		ns
t_{KHTV} tKHTX	t_{KHTL}	Clock High to WAIT Valid or Low		9	ns

1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 12: AC Measurement Load Circuit*.
2. t_{AVWL} and t_{LLWL}, are required if t_{ELKH}> 20ns.
3. A refresh opportunity must be offered every t_{ELEH}. A refresh opportunity is possible either if $\overline{E}$ is High during the rising edge of K; or if $\overline{E}$ is High for longer than 15ns.
4. The Hi-Z timings measure a 100mV transition from either V_{OH} or V_{OL} to $V_{CCQ}/2$.

Figure 27. Power-Up AC waveforms



1. Power must be applied to V_{CC} prior to or at the same time as V_{CCQ}.

Figure 28. Deep Power-Down Entry and Exit AC waveforms

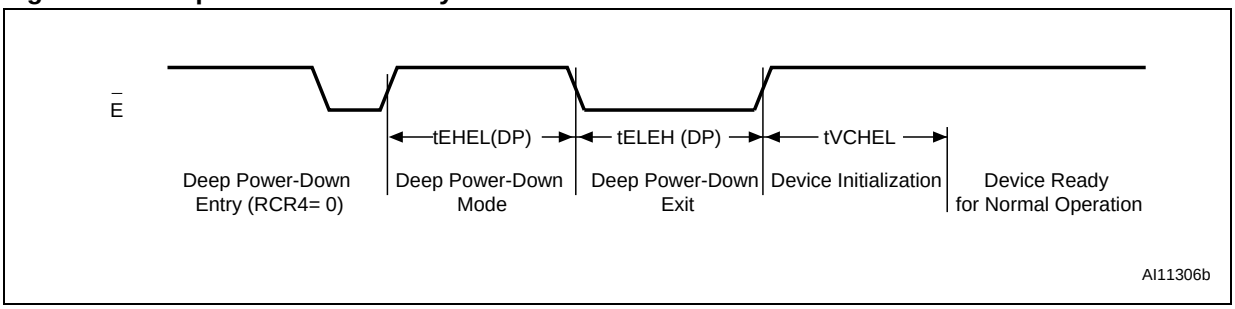


Table 22. Power-Up and Deep Power-Down AC characteristics

Symbol	Alt.	Parameter	Min	Max	Unit
t_{VCHEL}	t_{PU}	Initialization delay after Power-Up or Deep Power-Down Exit	150		µs
$t_{EHEL(DP)}$	t_{DPD}	Deep Power-Down Entry to Deep Power-Down Exit	10		µs
$t_{ELEH(DP)}$	t_{DPDX}	Chip Enable Low to Deep Power-Down Exit	10		µs

10 Part numbering

Table 23. Ordering Information Scheme

Example: M69KM096AA C W 8

Device Type

M69 = PSRAM

Mode

K = Bare Die

Operating Voltage

M= V_{CC} = 1.7 to 1.95V, x16, Multiplexed I/O, PSRAM

Array Organization

096 = 64 Mbit (4 Mbit x16)

Option 1

A = 1 Chip Enable

Silicon Revision

A = A Die

Maximum Clock Frequency

C = 83MHz

Package

W = Unsawn Wafer

Operating Temperature

8 = –30 to 85 °C

The notation used for the device number is as shown in *Table 23*. Not all combinations are necessarily available. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest STMicroelectronics Sales Office.

11 Revision history

Table 24. Document Revision History

Date	Rev.	Revision Details
15-Dec-2005	0.1	First Issue.
29-May-2006	1	80MHz clock frequency changed to 83MHz, and 104MHz removed. t_{EHEL} and t_{LHQZ} minimum values, and t_{LLQZ} maximum value updated in *Table 17: Asynchronous Read AC characteristics*. t_{EHEL} minimum values updated in *Table 18: Asynchronous Write AC characteristics*. t_{LHAX} and t_{GHAV} added in *Table 20: Synchronous Burst Read AC characteristics*. t_{LHAX} added in *Figure 19*. t_{LHAX} and t_{GHAV} added in *Figure 20* and *Figure 22*. t_{KHLL} removed from *Table 21: Synchronous Burst Write AC characteristics*, *Figure 23* and *Figure 25*. t_{PU} changed to t_{VCHEL} in *Table 22: Power-Up and Deep Power-Down AC characteristics*, *Figure 27* and *Figure 28*. Wafer and Die specifications section removed. Maximum clock frequency identifier changed from ‘80’ to ‘C’ in *Table 23: Ordering Information Scheme*.
6-Jul-2006	2	Updated *Section 6.3.3: Row Boundary Crossing on page 18*, *Figure 21: Burst Read Showing End-of-Row Condition AC waveforms (No Wrap) on page 48*, *Figure 23: 4-Word Synchronous Burst Write AC waveforms (Variable Latency Mode) on page 51*, *Figure 24: Burst Write Showing End-of-Row Condition AC waveforms (No Wrap) on page 52*, Hold Time from Active Clock Edge value in *Table 20: Synchronous Burst Read AC characteristics* and *Table 21: Synchronous Burst Write AC characteristics*.

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