

PSMN023-80LS

N-channel QFN3333 80 V 23 mΩ standard level MOSFET

Rev. 2 — 18 August 2010

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in QFN3333 package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and power supply equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Small footprint for compact designs
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	-	34	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	65	W
T_j	junction temperature		-55	-	150	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 100\text{ °C}$; see Figure 12	-	-	38	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; see Figure 13	-	19	23	mΩ

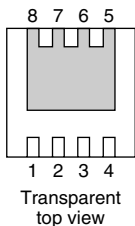
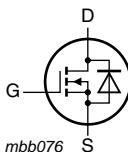


Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 30\text{ A};$	-	4.8	-	nC
$Q_{G(tot)}$	total gate charge	$V_{DS} = 40\text{ V};$ see Figure 14 ; see Figure 15	-	21	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ $I_D = 34\text{ A}; V_{sup} \leq 80\text{ V};$ $R_{GS} = 50\text{ }\Omega; \text{ unclamped}$	-	-	37	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>Transparent top view</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
5,6,7,8	D	drain		
mb	D	mounting base; connected to drain		

SOT873-1 (QFN3333)

3. Ordering information

Table 3. Ordering information

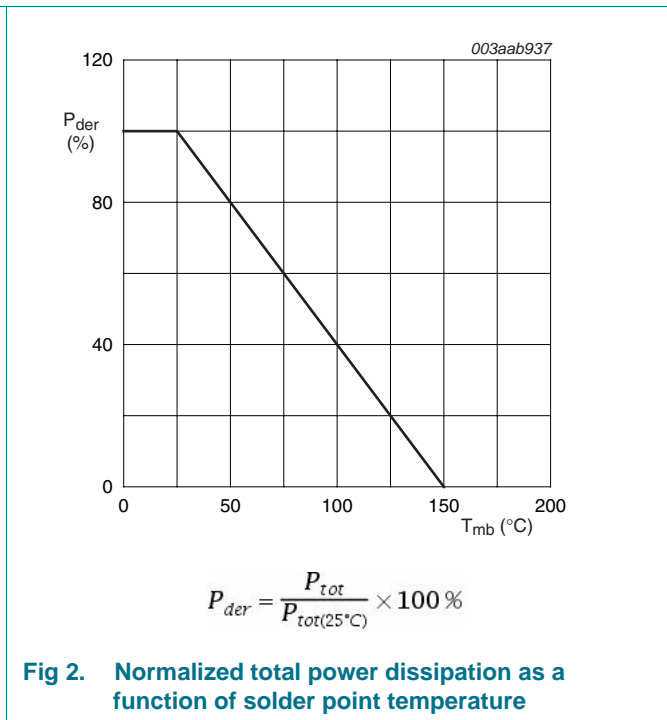
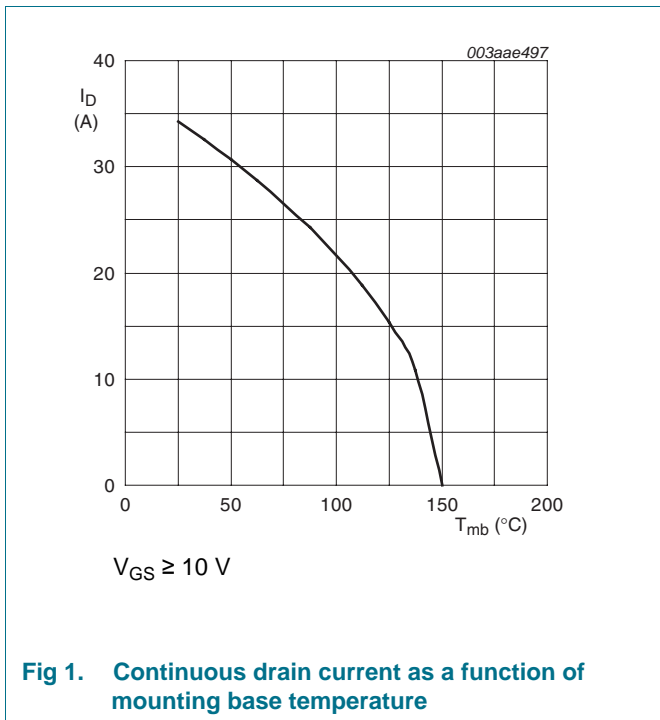
Type number	Package		Version
	Name	Description	
PSMN023-80LS	QFN3333	plastic thermal enhanced very thin small outline package; no leads; 8 terminals	SOT873-1

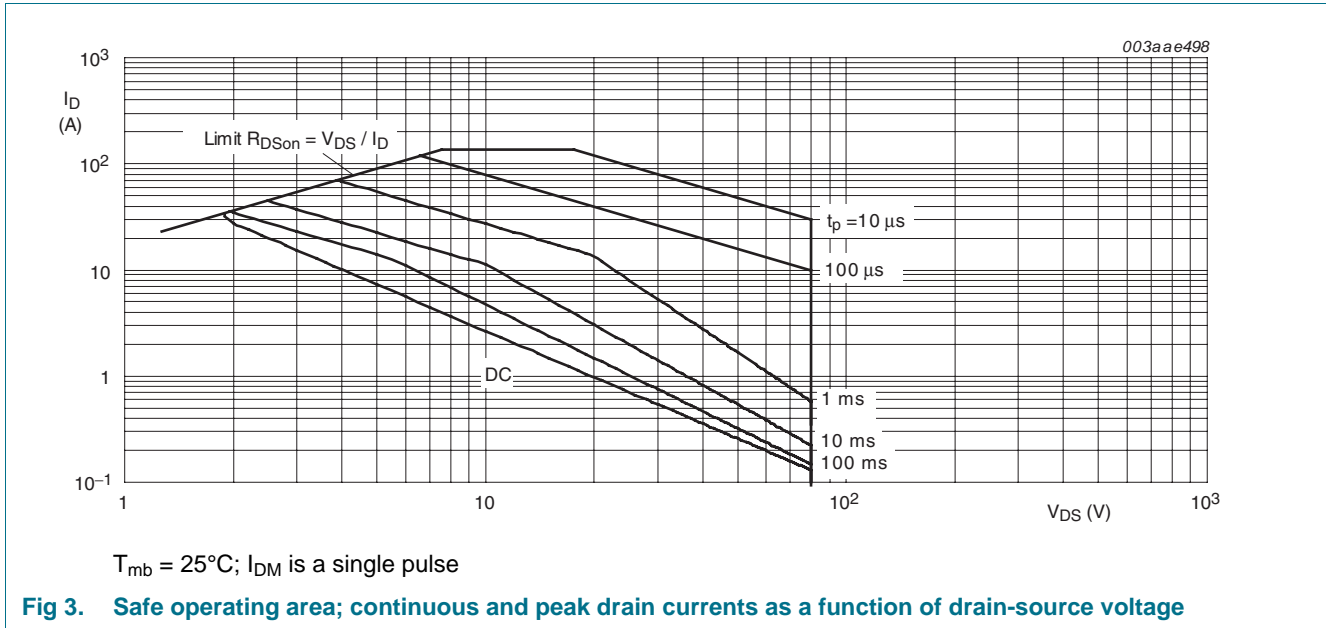
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	80	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	80	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	-	22	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	-	34	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 3	-	137	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	65	W
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	34	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	137	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(initial)} = 25 °C; I _D = 34 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; unclamped	-	37	mJ



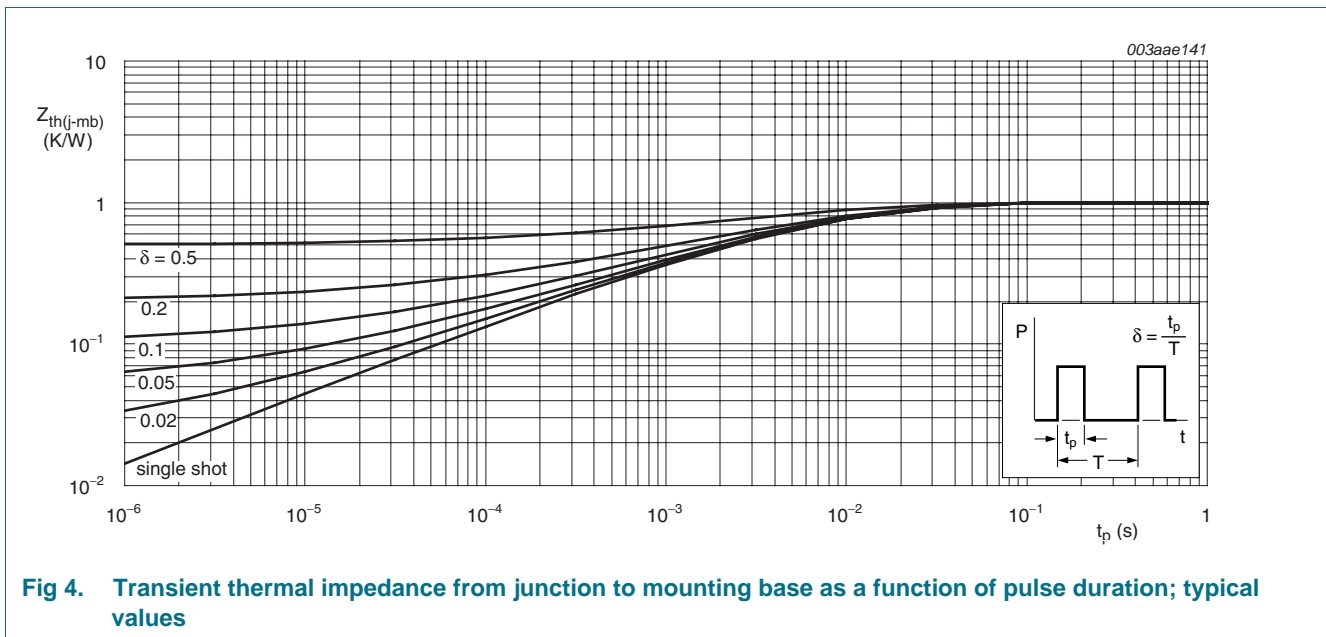


5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	1	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	53	60	K/W

[1] $R_{th(j-a)}$ is guaranteed by design and assumes that the device is mounted on a 40mm x 40mm x 70μm copper pad at 20°C ambient temperature. In practice $R_{th(j-a)}$ will be determined by the customer’s PCB characteristics



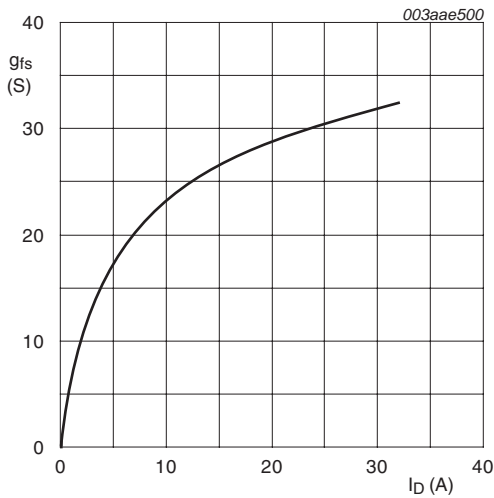
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	73	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10	-	-	4.7	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	2.3	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.1	2	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	50	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 12	-	39.9	48.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12	-	-	38	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	19	23	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14	-	18.4	-	nC
		$I_D = 30 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	21	-	nC
Q_{GS}	gate-source charge		-	6.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	3.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	2.7	-	nC
Q_{GD}	gate-drain charge		-	4.8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 30 \text{ A}; V_{DS} = 40 \text{ V};$ see Figure 14 ; see Figure 15	-	5	-	V
C_{iss}	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 16	-	1295	-	pF
C_{oss}	output capacitance		-	125	-	pF
C_{rss}	reverse transfer capacitance		-	69	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.33 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega$	-	10.5	-	ns
t_r	rise time	$V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; R_{G(ext)} = 4.7 \text{ } \Omega$	-	8	-	ns
$t_{d(off)}$	turn-off delay time	$V_{DS} = 40 \text{ V}; R_L = 1.33 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 4.7 \text{ } \Omega$	-	20.5	-	ns
t_f	fall time		-	5.4	-	ns

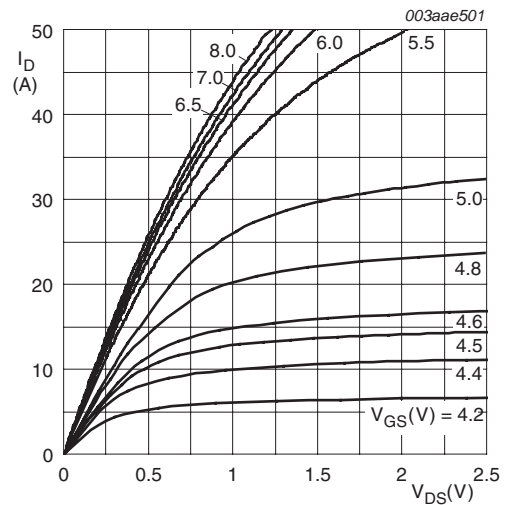
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}$; $di_S/dt = 100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	36	-	ns
Q_r	recovered charge	$V_{DS} = 40\text{ V}$	-	53	-	nC



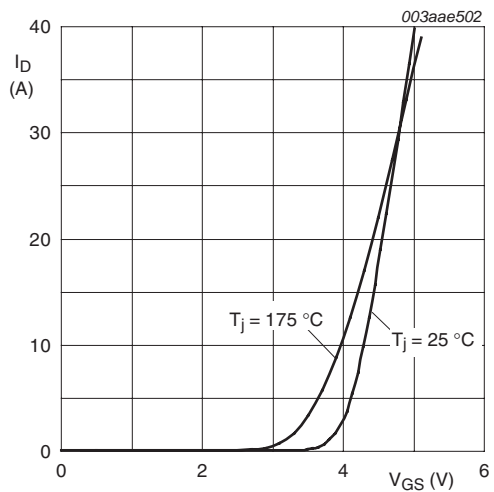
$T_j = 25\text{ °C}$; $V_{DS} = 10\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



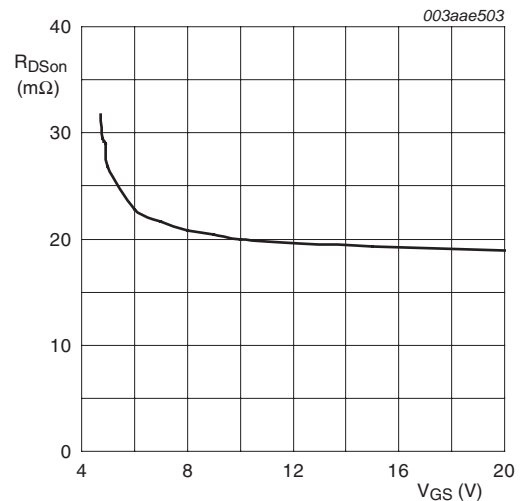
$T_j = 25\text{ °C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$T_j = 25\text{ °C}$; $I_D = 10\text{ A}$

Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

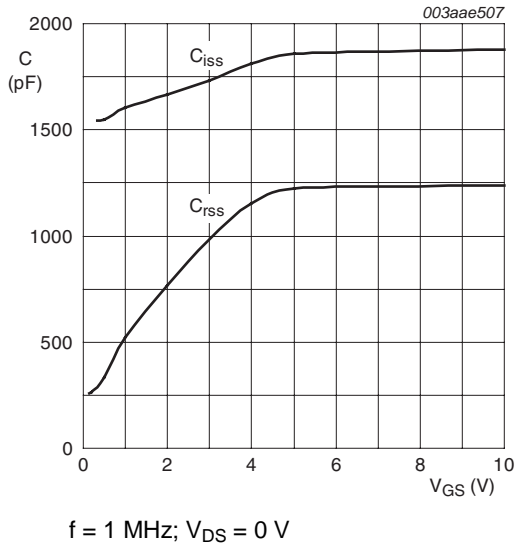


Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

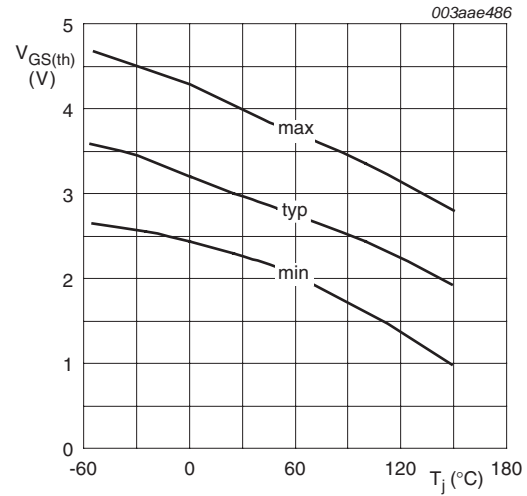


Fig 10. Gate-source threshold voltage as a function of junction temperature

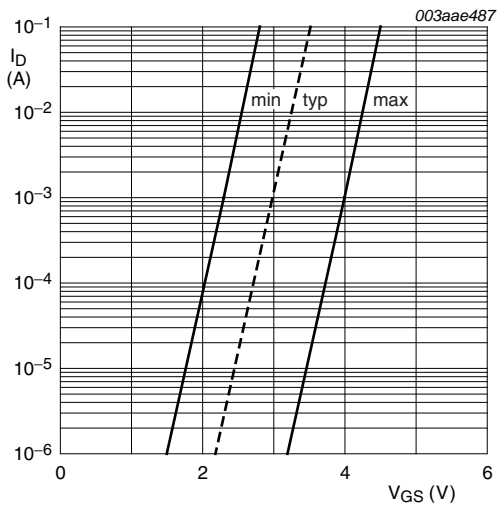


Fig 11. Sub-threshold drain current as a function of gate-source voltage

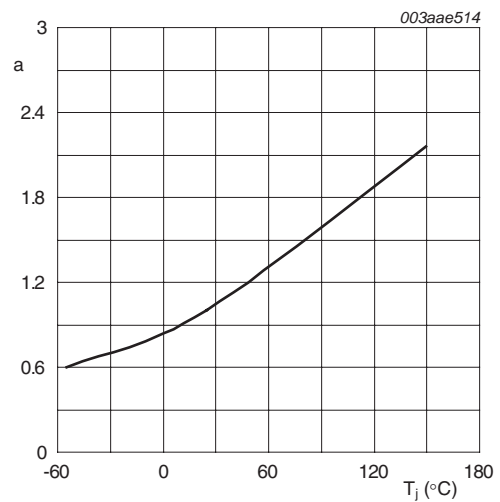
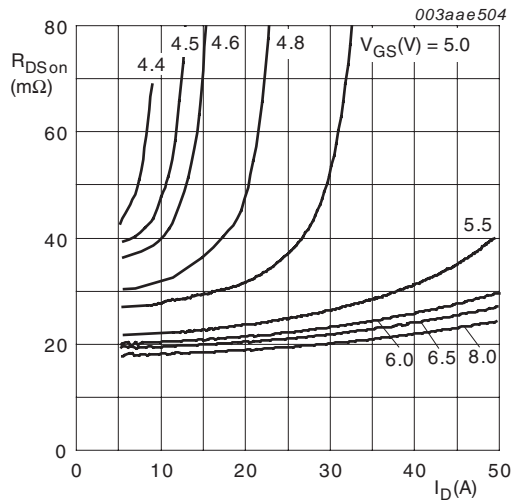


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

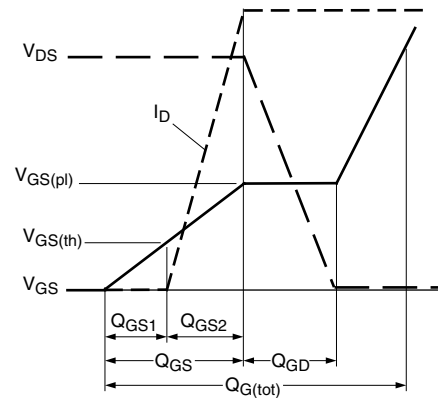
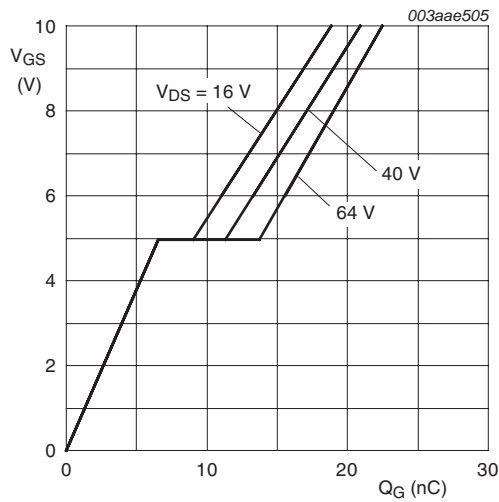
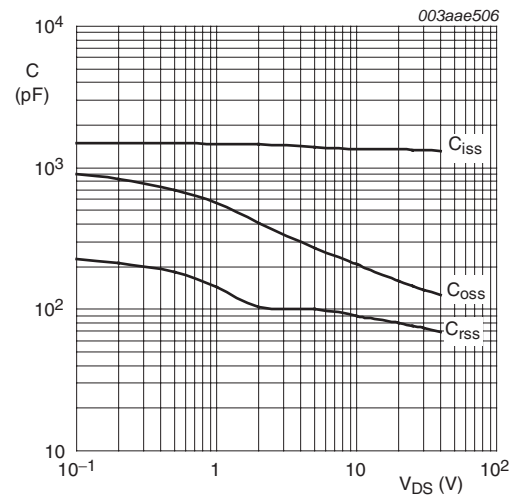


Fig 14. Gate charge waveform definitions



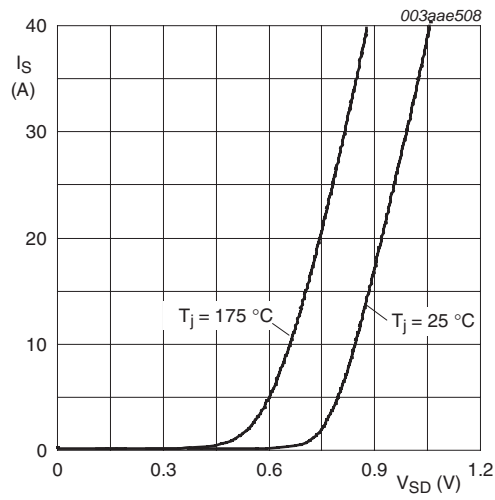
$T_j = 25^\circ\text{C}; I_D = 30 \text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

QFN3333: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3.3 x 3.3 x 1.0 mm

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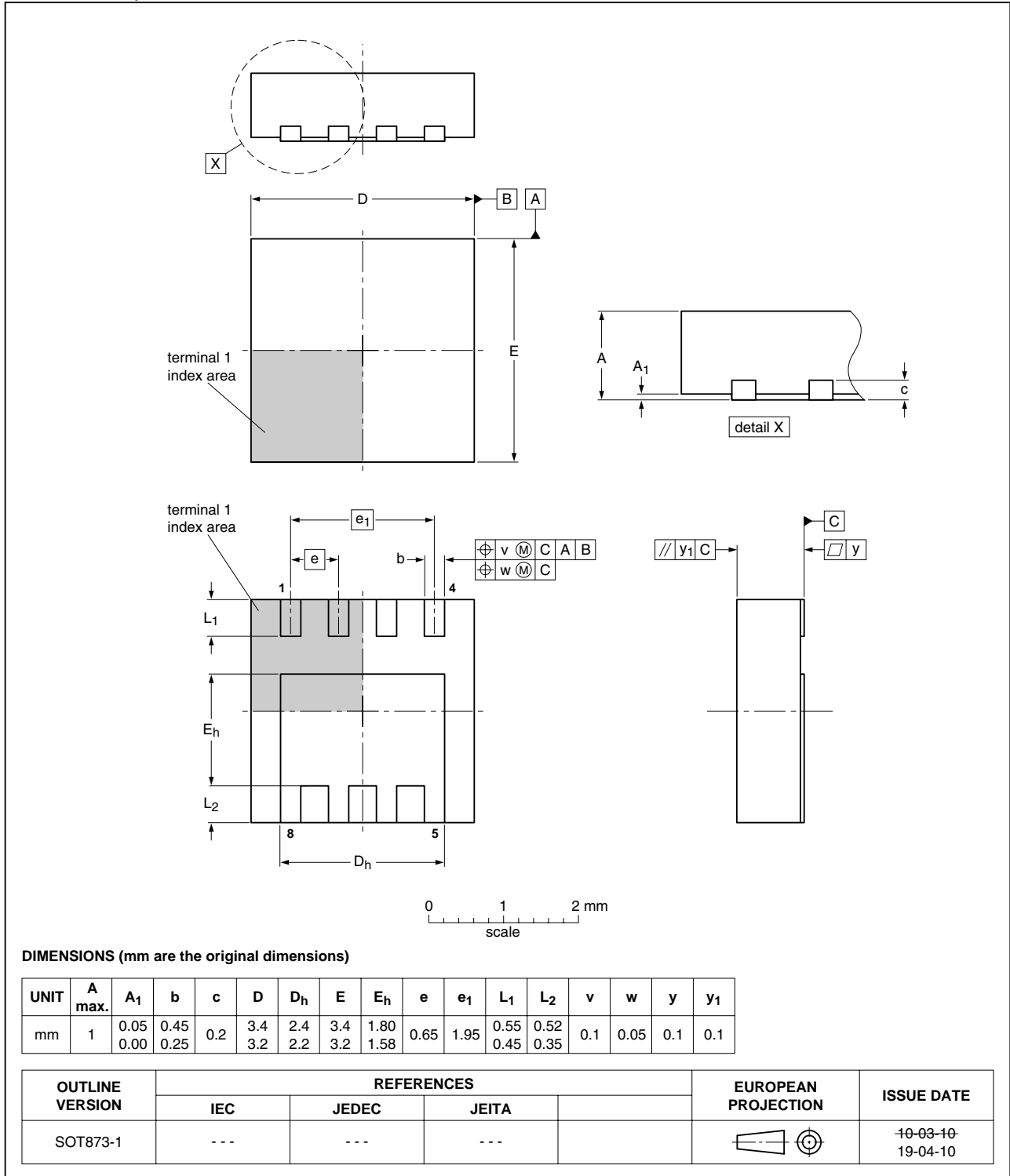


Fig 18. Package outline SOT873-1 (QFN3333)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN023-80LS v.2	20100818	Product data sheet	-	PSMN023-80LS v.1
Modifications:	• Status changed from objective to product.			
PSMN023-80LS v.1	20100624	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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