v03.1010

HMC672LC3C

14 Gbps, AND / NAND / OR / NOR Gate

Typical Applications

The HMC672LC3C is ideal for:

- 16 G Fiber Channel
- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 14 Gbps
- Digital Logic Systems up to 14 GHz
- NRZ-to-RZ Conversion

Features

Supports High Data Rates: up to 14 Gbps

Differential or Single-Ended Operation

Fast Rise and Fall Times: 24 / 22 ps

Low Power Consumption: 180 mW typ.

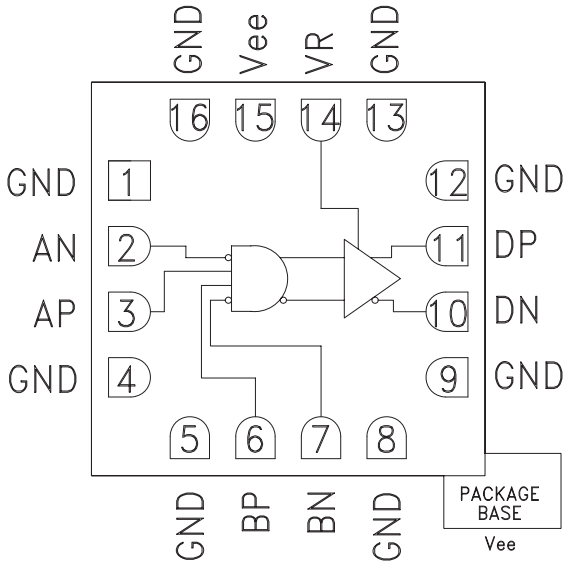
Programmable Differential Output
Voltage Swing: 400 - 1100 mVp-p

Propagation Delay: 60 ps

Single Supply: -3.3 V

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC672LC3C is a AND/NAND/OR/NOR function designed to support data transmission rates of up to 14 Gbps, and clock frequencies as high as 14 GHz. The HMC672LC3C may be easily configured to provide any of the following logic functions: AND, NAND, OR and NOR.

All differential inputs to the HMC672LC3C are CML and terminated on-chip with 50 Ohms to the positive supply, GND, and may be DC or AC coupled. Outputs can be connected directly to a 50 Ohm ground-terminated system or drive devices with CML logic input. The HMC672LC3C also features an ouput level control pin, VR, which allows for loss compensation or signal level optimization. The HMC672LC3C operates from a single -3.3 V supply and is available in ROHS-compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vee = -3.3 V, VR = 0 V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			55		mA
Maximum Data Rate			14		Gbps
Maximum Clock Rate			14		GHz
Clock Bandwidth, 3 dB	200 mVp-p Input		12.2		GHz
Input Voltage Range		-1.5		0.5	V
Input Differential Range		0.1		2.0	Vp-p
Input Return Loss	Frequency <14 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVp-p
	Differential, peak-to-peak		1100		mVp-p
Output High Voltage			-10		mV
Output Low Voltage			-560		mV

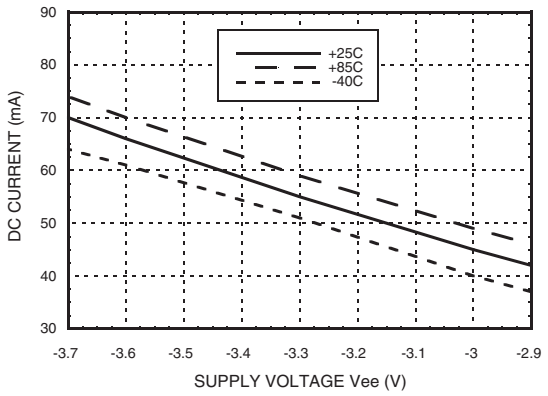
Electrical Specifications (continued)

Parameter	Conditions	Min.	Typ.	Max	Units
Output Rise / Fall Time	Differential, 20% - 80%		24 / 22		ps
Output Return Loss	Frequency <14 GHz		10		dB
Small Signal Gain			27		dB
Random Jitter Jr	rms [1]			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [2]		2		ps, p-p
Propagation Delay, td			60		ps
Off Isolation	Conditions:<13GHz, Port B=Low Voltage		50		dB
VR Pin Current	VR = 0.0 V		2		mA
VR Pin Current	VR = +0.4 V			3.5	mA

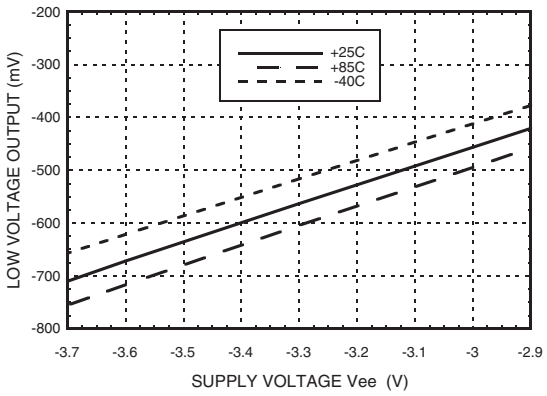
[1] Upper limit of random jitter, JR, determined by measuring and integrating output phase noise with a sinusodal input at 5, 10, and 13.5 GHz over temperature

[2] Deterministic jitter calculated by simultaneously measuring the jitter of a 200 mV, 12.5 GHz, 2^{15}-1 PRBS input, and a single-ended output

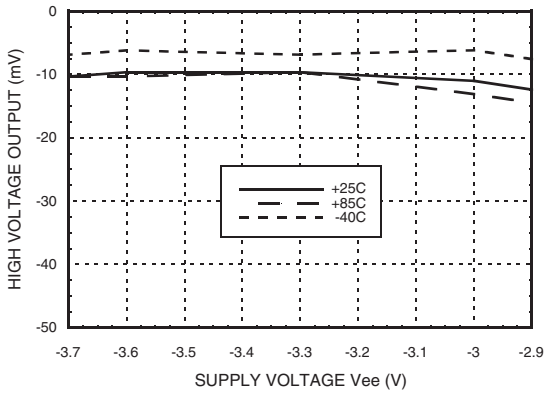
DC Current vs. Supply Voltage [1][2]



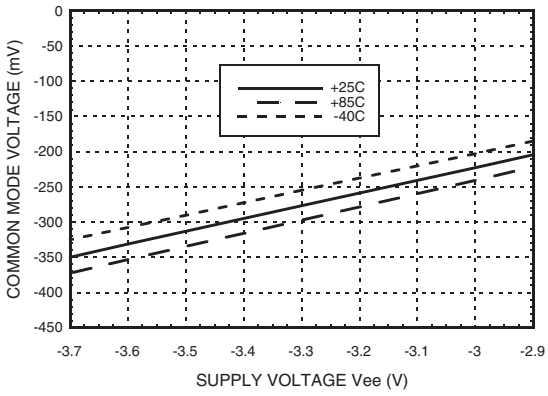
Output Low Voltage vs. Supply Voltage [1][2]



Output High Voltage vs. Supply Voltage [1][2]

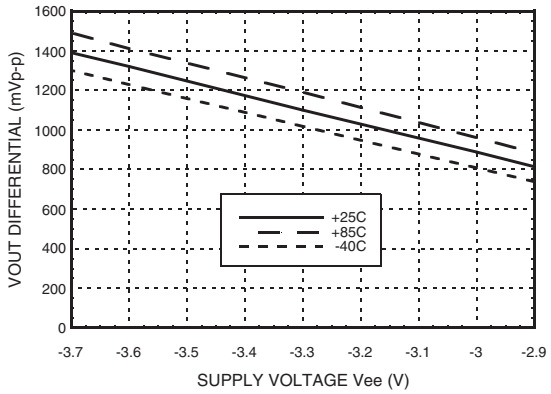


Common Mode Voltage vs. Supply Voltage [1][2]

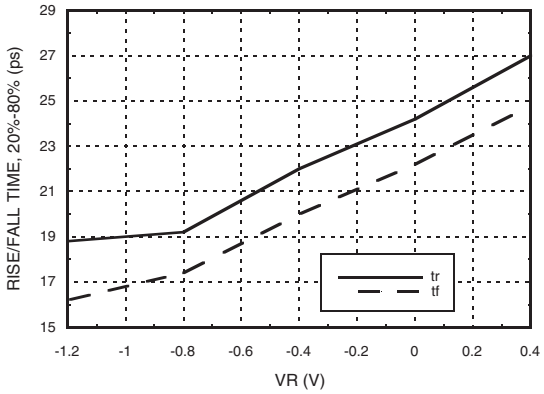


[1] VR = 0.0 V [2] Frequency = 1 GHz [3] Vee = -3.3 V

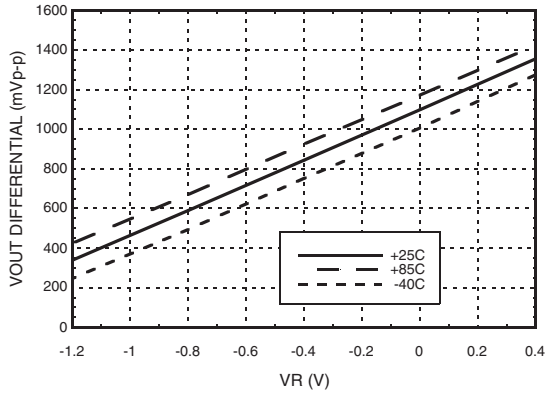
Output Differential Voltage vs. Supply Voltage [1][2]



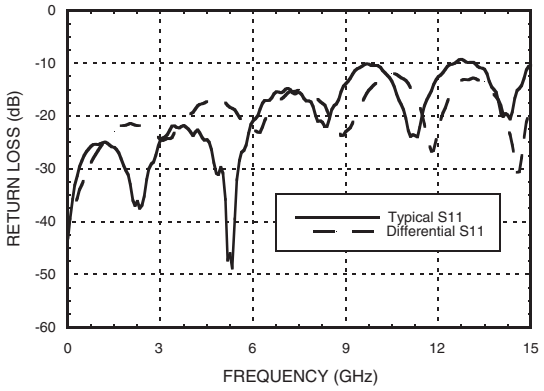
Rise / Fall Time vs. VR [3][4]



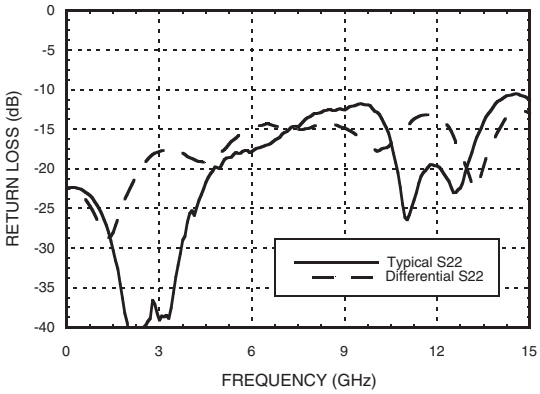
Output Differential Voltage vs. VR [2][4]



Input Return Loss vs. Frequency

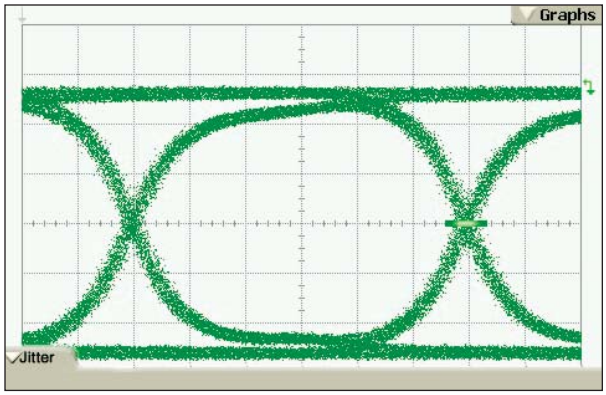


Output Return Loss vs. Frequency



[1] VR = 0.0 V [2] Frequency = 1 GHz [3] Frequency = 5 GHz [4] Vee = -3.3 V

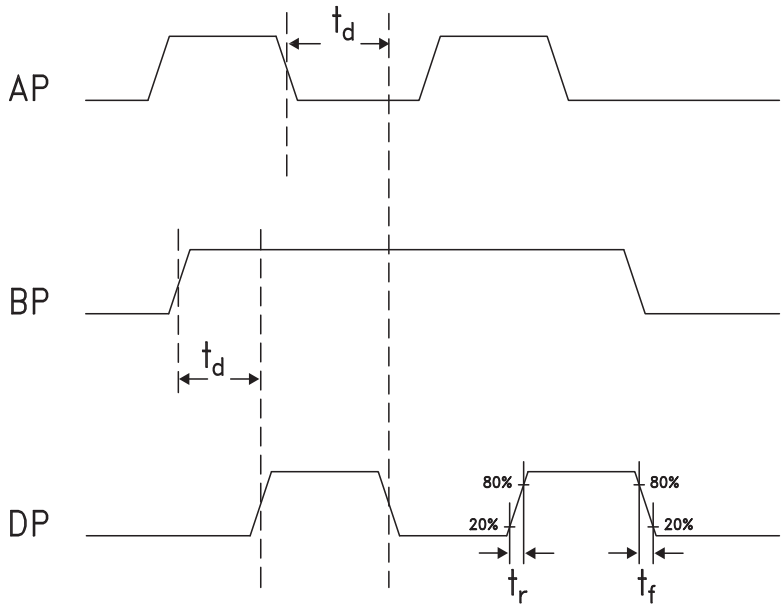
Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4901B Serial BERT
Eye diagram data presented on an Infinium DCA 86100A
Rate = 10.0 GB/s
Pseudo Random Code = 2^{15} -1
Vin = 400 mVp-p differential

[2] Vertical Scale = 100 mV/Div

Timing Diagram



Truth Table

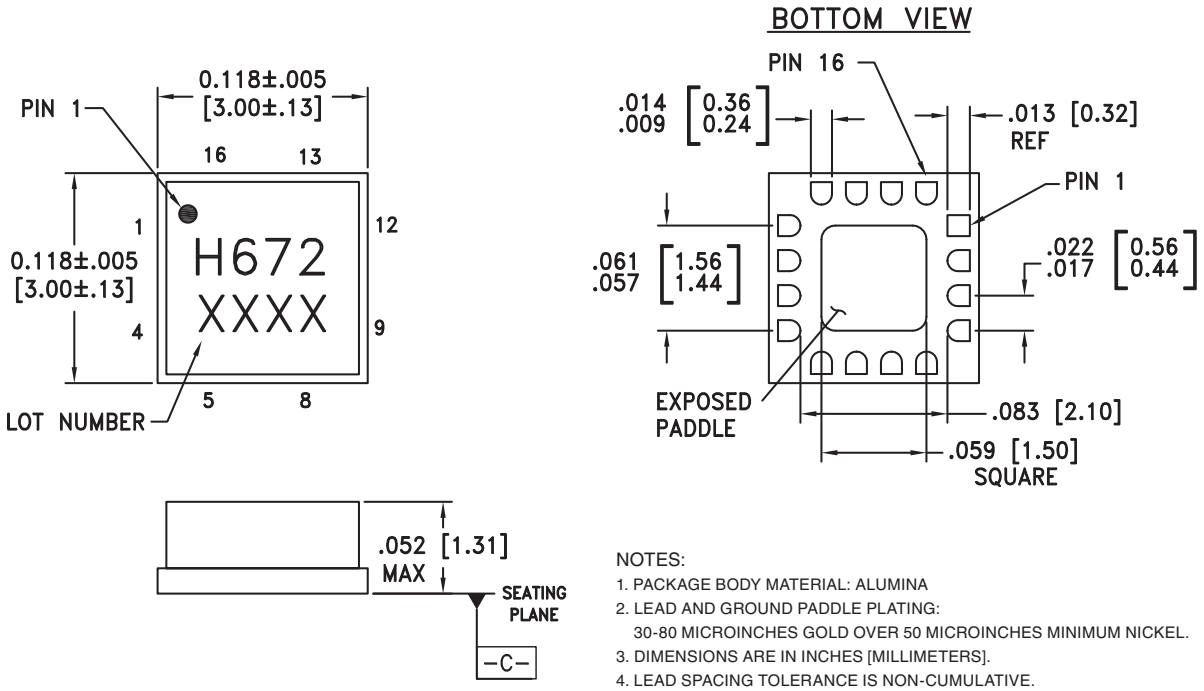
Input		Outputs
A	B	D
L	L	L
L	H	L
H	L	L
H	H	H
Notes: A = AP - AN B = BP - BN D = DP - DN	H - Positive voltage level L - Negative voltage level	

Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75 V to +0.5 V
Input Signals	-2 V to +0.5 V
Output Signals	-1.5 V to +1 V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worst case junction to package paddle	59 °C/W
Maximum Junction Temperature	125 °C
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

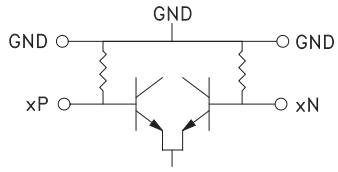
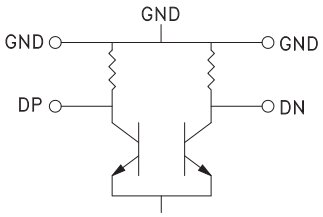
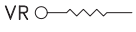
Outline Drawing



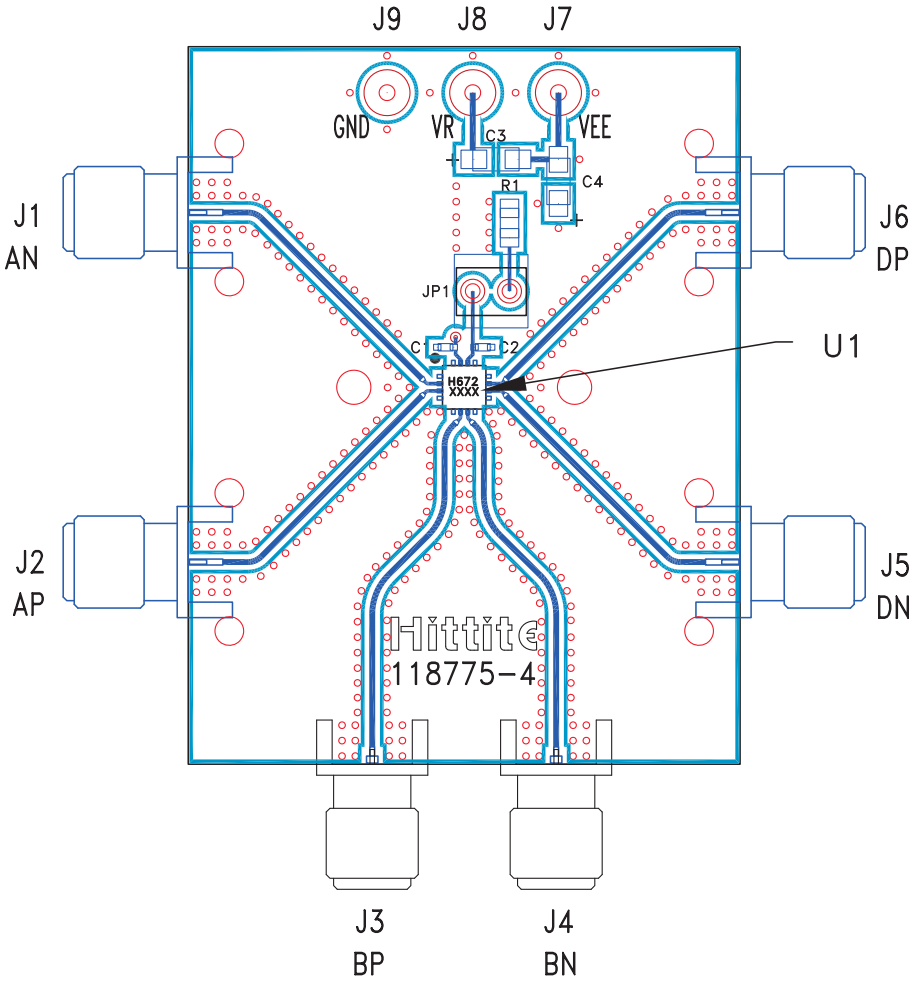
NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3, 6, 7	AN, AP, BP, BN	Differential Clock / Data Inputs: Current Mode Logic (CML) referenced to positive supply.	
10, 11	DN, DP	Differential Clock / Data Outputs: Current Mode Logic (CML) referenced to positive supply.	
13, 16	GND	Supply Ground	
14	VR	Output level control. Output level may be adjusted by either applying a voltage to VR per “Output Differential vs. VR” plot.	
15, Package Base	Vee	Negative Supply	

Evaluation PCB



List of Materials for Evaluation PCB 118777 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J14	DC Pin
JP1	0.1" Header with Shorting Jumper
C1, C2	100 pF Capacitor, 0402 Pkg.
C3, C4	4.7 µF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC672LC3C High Speed Logic, AND / NAND / OR / NOR
PCB [2]	118775 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

Application Circuit