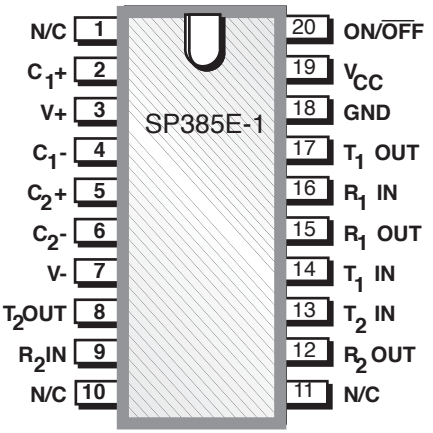
True +3V or +5V RS-232 Line Driver/Receiver

FEATURES

- Operates from 3.3V or 5V Power Supply
- Meets True EIA/TIA-232-F Standards from a +3.0V to +5.5V Power Supply
- Meets EIA-562 Specifications at $V_{CC} \geq$ 2.7V
- Two Drivers and Receivers
- Operates with 0.1µF Capacitors
- High Data Rate — 120kbps Under Load
- Low Power Shutdown ≤1µA
- 3-State TTL/CMOS Receiver Outputs
- Low Power CMOS — <1mA Operation
- Improved ESD Specifications:
  ±15kV Human Body Model
  ±15kV IEC1000-4-2 Air Discharge
  ±8kV IEC1000-4-2 Contact Discharge

20 PIN SSOP

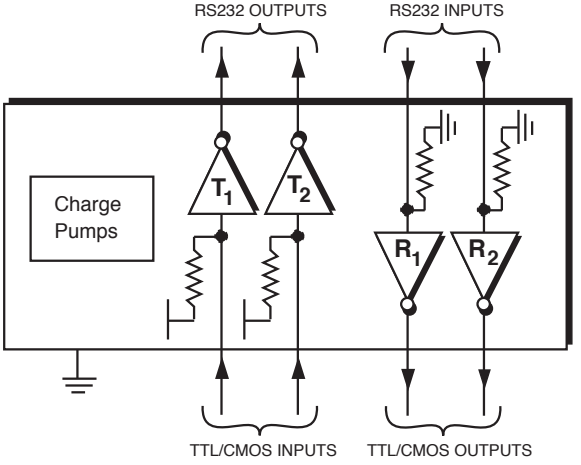


Now Available in Lead Free Packaging

DESCRIPTION

Sipex's SP385-1 is an enhanced version of the **Sipex** SP200 family of RS232 line drivers/receivers. The **SP385E-1** offers +3.3V operation for EIA-562 and EIA-232 applications. The **SP385E-1** maintains the same performance features offered in its predecessors. The **SP385E-1** is available in plastic SOIC or SSOP packages operating over the commercial and industrial temperature ranges. The **SP385E-1** is pin compatible to the LTC1385 EIA-562 transceiver, except the drivers in the **SP385E-1** can only be disabled with the ON/OFF pin.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} ..... +6V
V^+ ..... (Vcc-0.3V) to +13.2V
V^- 13.2V

Input Voltages
T_{IN} ..... -0.3 to (Vcc +0.3V)
R_{IN} ..... ±15V

Output Voltages
T_{OUT} ..... (V+, +0.3V) to (V-, -0.3V)
R_{OUT} ..... -0.3V to (Vcc +0.3V)

Short Circuit Duration
T_{OUT} ..... Continuous

Power Dissipation
CERDIP 675mW
(derate 9.5mW/°C above +70°C)
Plastic DIP 375mW
(derate 7mW/°C above +70°C)
Small Outline 375mW
(derate 7mW/°C above +70°C)

ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V ± 10%; cap on (V+) and (V-) = 1.0µF, C1 = C2 = 0.1µF; T_{MIN} to T_{MAX} unless otherwise noted.

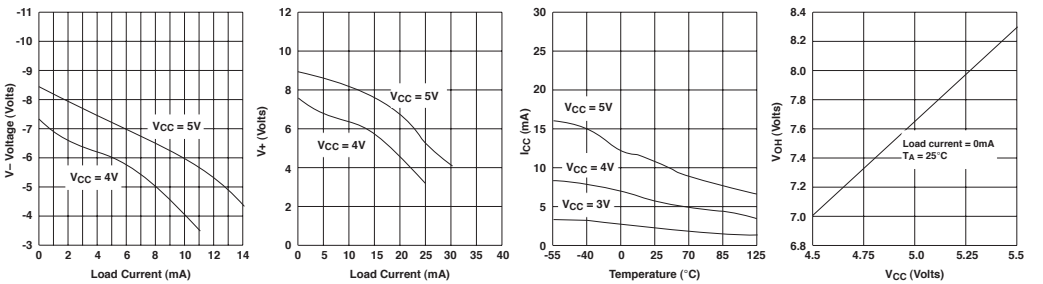
PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TTL INPUT					
Logic Threshold					
Low			0.8	Volts	T_{IN} ; ON/$\overline{OFF}$ Vcc = 3.3V
High	2.0			Volts	T_{IN} ; ON/$\overline{OFF}$ Vcc = 3.3V
Logic Pullup Current		0.01	200	µA	T_{IN} = 0V
Maximum Data Rate	120			kbps	C_L = 2500pF, R_L= 3kΩ
TTL OUTPUT					
TTL/CMOS Output					
Voltage, Low			0.4	Volts	I_{OUT} = 1.6mA; Vcc = 3.3V
Voltage, High	V_{CC}-0.6			Volts	I_{OUT} = -1.0mA
Leakage Current; T_A = +25°C		0.05	±10	µA	ON/$\overline{OFF}$=0V, 0 ≤ V_{OUT} ≤ V_{CC}
EIA-562 OUTPUT					
Output Voltage Swing	±3.7	±4.2		Volts	All transmitter outputs loaded with 3kΩ to ground
Power-Off Output Resistance	300			Ω	V_{CC} = 0V; V_{OUT} = ±2V
Output Short Circuit Current		±35		mA	Infinite duration
EIA-562 INPUT					
Voltage Range	-15		+15	Volts	
Voltage Threshold					
Low	0.6	1.2		Volts	V_{CC} = 3.3V, T_A = +25°C
High		1.5	2.4	Volts	V_{CC} = 3.3V, T_A = +25°C
Hysteresis		0.5	1.0	Volts	V_{CC} = 3.3V, T_A = +25°C
Resistance	3	5	7	kΩ	V_{IN} = 15V to –15V
DYNAMIC CHARACTERISTICS					
Driver Propagation Delay		1.0		µs	TTL to RS-562
Receiver Propagation Delay		0.3		µs	RS-562 to TTL
Instantaneous Slew Rate			30	V/µs	C_L = 10pF, R_L= 3kΩ - 7kΩ; T_A = +25°C
Transition Region Slew Rate		10		V/µs	C_L = 2500pF, R_L= 3kΩ; measured from +2V to -2V or -2V to +2V
Output Enable Time		200		ns	
Output Disable Time		200		ns	
POWER REQUIREMENTS					
V_{CC} Power Supply Current		0.5	6	mA	No load, T_A= +25°C; V_{CC} = 3.3V
		8		mA	All transmitters R_L = 3kΩ T_A = +25°C
Shutdown Supply Current		0.010	5	µA	V_{CC} = 3.3V, T_A = +25°C

ELECTRICAL CHARACTERISTICS

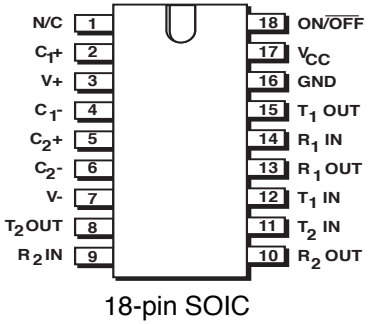
V_{CC} = +3.3V ± 10%; cap on (V+) and (V-) = 1.0μF, C1 = C2 = 0.1μF; T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TTL INPUT					
Logic Threshold					
Low			0.8	Volts	T_{IN} ; ON/$\overline{OFF}$
High	2.4			Volts	T_{IN} ; ON/$\overline{OFF}$
Logic Pullup Current		0.01	200	μA	T_{IN} = 0V
Maximum Data Rate	120			kbps	C_L = 2500pF, R_L= 3kΩ
TTL OUTPUT					
TTL/CMOS Output					
Voltage, Low			0.4	Volts	I_{OUT} = 1.6mA; Vcc = +5V
Voltage, High	V_{CC}-0.6			Volts	I_{OUT} = -1.0mA
Leakage Current; T_A = +25°C		0.05	±10	μA	$\overline{EN}$ = V_{CC}, 0V ≤ V_{OUT} ≤ V_{CC}
EIA-232 OUTPUT					
Output Voltage Swing	±5	±9		Volts	All transmitter outputs loaded with 3kΩ to ground.
Power-Off Output Resistance	300			Ω	V_{CC} = 0V; V_{OUT} = ±2V
Output Short Circuit Current		±35		mA	Infinite duration
EIA-562 INPUT					
Voltage Range	-15		+15	Volts	
Voltage Threshold					
Low	0.8	1.5		Volts	V_{CC} = 5V, T_A = +25°C
High		1.8	2.4	Volts	V_{CC} = 5V, T_A = +25°C
Hysteresis		0.5	1.0	Volts	V_{CC} = 5V, T_A = +25°C
Resistance	3	5	7	kΩ	V_{IN} = 15V to –15V
DYNAMIC CHARACTERISTICS					
Propagation Delay, RS-232 to TTL		1		μs	TTL to RS-562
Instantaneous Slew Rate			30	V/μs	C_L = 10pF, R_L= 3kΩ - 7kΩ; T_A =+25°C
Transition Region Slew Rate		10		V/μs	C_L = 2500pF, R_L= 3kΩ; measured from +3V to -3V or -3V to +3V
Output Enable Time		200		ns	
Output Disable Time		200		ns	
POWER REQUIREMENTS					
V_{CC} Power Supply Current		0.5	15	mA	No load, T_A= +25°C; V_{CC} = 5V
		25		mA	All transmitters R_L = 3kΩ; T_A = +25°C
Shutdown Supply Current		1	10	μA	V_{CC} = 5V, T_A = +25°C

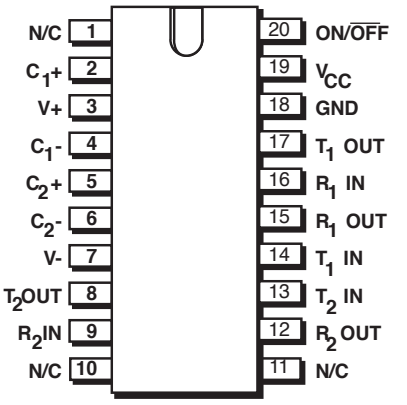
PERFORMANCE CURVES



PINOUT

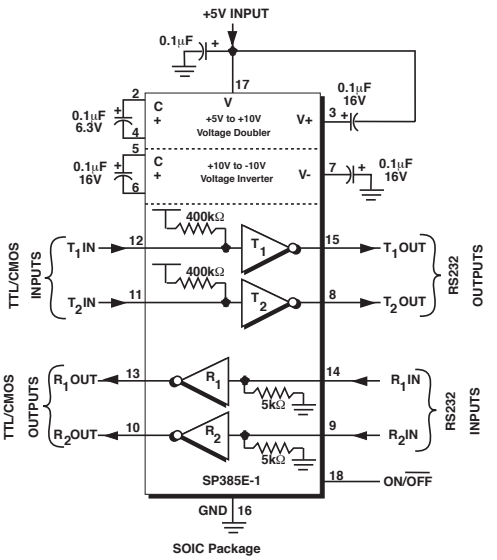


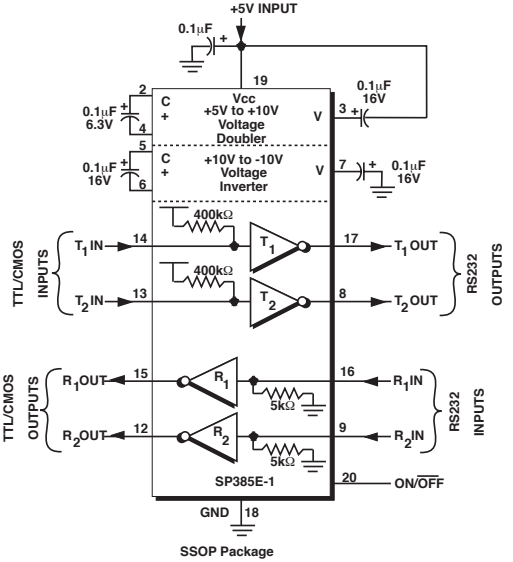
18-pin SOIC



20-pin SSOP

TYPICAL OPERATING CIRCUIT





FEATURES...

The **Sipex SP385E-1** is a +3V to +5V EIA-232/ EIA-562 line transceiver. It is a pin-for-pin alternative for the SP310A and will operate in the same socket with 0.1µF capacitors, either polarized or non–polarized, in +3V supplies. The **SP385E-1** offers the same features such as 120kbps guaranteed transmission rate, increased drive current for longer and more flexible cable configurations, low power dissipation and overall ruggedized construction for commercial and industrial environments. The **SP385E-1** also includes a shutdown feature that tri-states the drivers and the receivers.

The **SP385E-1** includes a charge pump voltage converter which allows it to operate from a single +3.3V or +5V supply. These converters double the V_{CC} voltage input in order to generate the EIA-232 or EIA-562 output levels. For +5V operation, the **SP385E-1** driver outputs adhere to all EIA-232-F and CCITT V.28 specifications. While at +3.3V operation, the outputs adhere to EIA-562 specifications. Due to **Sipex's** efficient charge pump design, the charge pump levels and the driver outputs are less noisy than other 3V EIA-232 transceivers.

The **SP385E-1** has a single control line which simultaneously shuts down the internal DC/DC converter and puts all transmitter and receiver outputs into a high impedance state.

The **SP385E-1** is available in 18-pin plastic SOIC and 20-pin plastic SSOP packages for operation over commercial and industrial temperature ranges. Please consult the factory for surface-mount packaged parts supplied on tape-on-reel as well as parts screened to MIL-M-38510.

The **SP385E-1** is ideal for +3.3V battery applications requiring low power operation. The charge pump strength allows the drivers to provide ±4.0V signals, plenty for typical EIA-562 applications since the EIA-562 receivers have input sensitivity levels of less than ±3V.

THEORY OF OPERATION

The **SP385E-1** device is made up of three basic circuit blocks — 1) a driver/transmitter, 2) a receiver and 3) a charge pump.

Driver/Transmitter

The drivers are inverting level transmitters, that convert TTL or CMOS logic levels to ±5.0V EIA/ TIA-232 levels inverted relative to the input logic levels. Typically the RS-232 output voltage swing is ±5.5V with no load and at least ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of ±3.7V with supply voltages as low as 2.7V.

The instantaneous slew rate of the transmitter output is internally limited to a maximum of 30V/ µs in order to meet the standards [EIA 232-D 2.1.7, Paragraph (5)]. However, the transition region slew rate of these enhanced products is typically 10V/µs. The smooth transition of the loaded output from V_{OL} to V_{OH} clearly meets the monotonicity requirements of the standard [EIA 232-D 2.1.7, Paragraphs (1) & (2)].

Receivers

The receivers convert RS-232 input signals to inverted TTL signals. Since the input is usually from a transmission line, where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines.

The input thresholds are 0.8V minimum and 2.4V maximum, again well within the ±3V RS-232 requirements. The receiver inputs are also protected against voltages up to ±15V. Should an input be left unconnected, a 5kΩ pull-down resistor to ground will commit the output of the receiver to a high state.

In actual system applications, it is quite possible for signals to be applied to the receiver inputs before power is applied to the receiver circuitry. This occurs for example when a PC user attempts to print only to realize the printer wasn't turned on. In this case an RS-232 signal from the PC will appear on the receiver input at the printer. When the printer power is turned on, the receiver will operate normally. All of these enhanced devices are fully protected.

CHARGE PUMP

The charge pump is a **Sipex**–patented design (5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

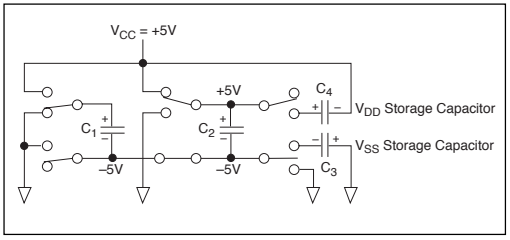


Figure 1. Charge Pump — Phase 1

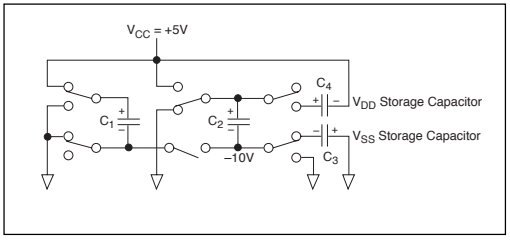


Figure 2. Charge Pump — Phase 2

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is l0V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground, and transfers the generated l0V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V^+ and V^- are separately generated from V_{CC}; in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

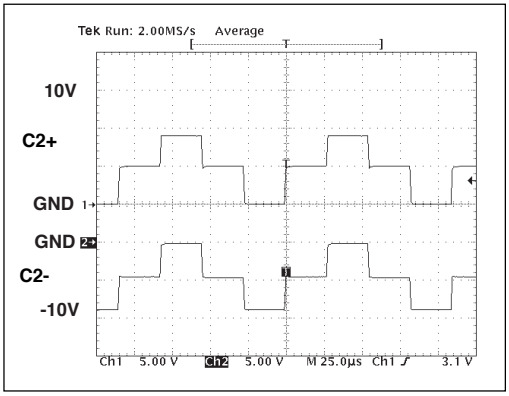


Figure 3. Charge Pump Waveforms

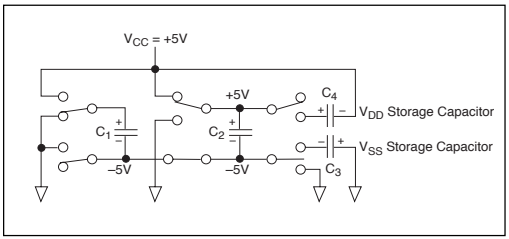


Figure 4. Charge Pump — Phase 3

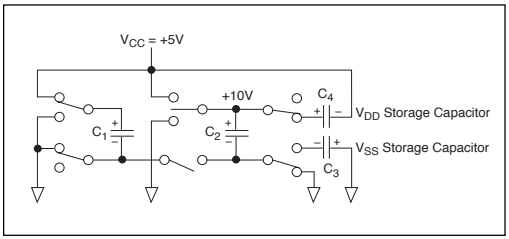


Figure 5. Charge Pump — Phase 4

Shutdown (ON/OFF)

The **SP385E-1** has a shut-down/standby mode to conserve power in battery-powered systems. To activate the shutdown mode, which stops the operation of the charge pump, a logic "0" is applied to the appropriate control line. The shutdown mode is controlled on the **SP385E-1** by a logic "0" on the ON/OFF control line (pin 18 for the SOIC and pin 20 for the SSOP packages); this puts the transmitter outputs in a tri-state mode.

ESD Tolerance

The **SP385E-1** device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15KV without damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) IEC1000-4-2 Air-Discharge
c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 6*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on *Figure 7*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of

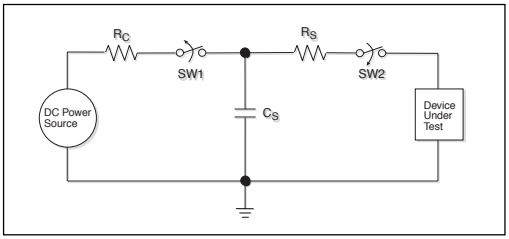


Figure 6. ESD Test Circuit for Human Body Model

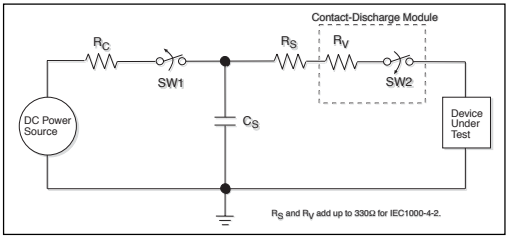


Figure 7. ESD Test Circuit for IEC1000-4-2

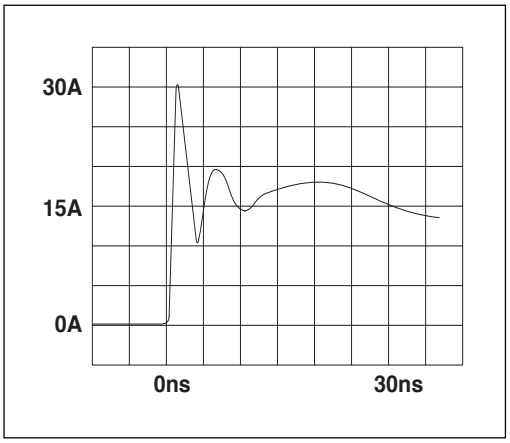


Figure 8. ESD Test Waveform for IEC1000-4-2

the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise timeis constant since energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

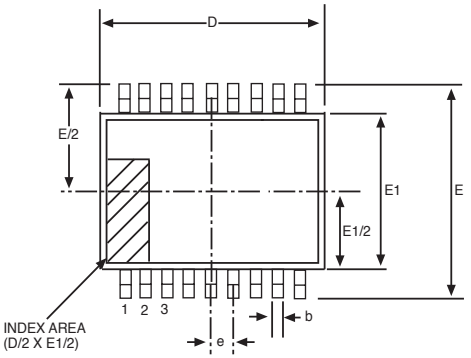
The circuit models in *Figures 6 & 7* represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

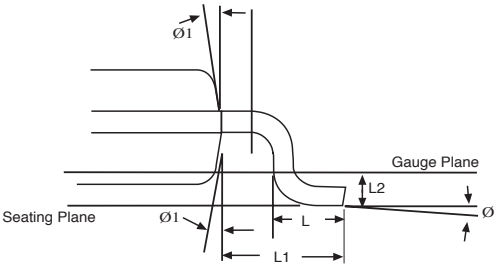
The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

SP385E-1 Family	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

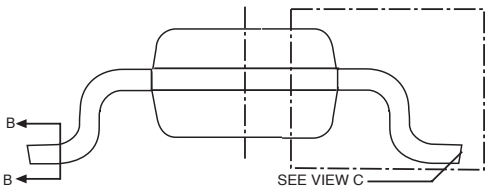
Table 1. Transceiver ESD Tolerance Levels

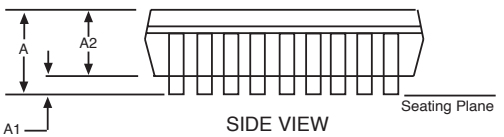


TOP VIEW



VIEW C

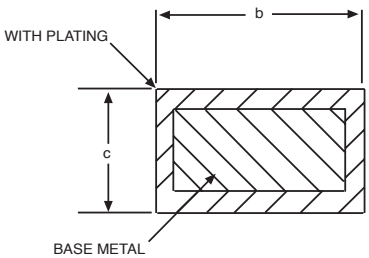




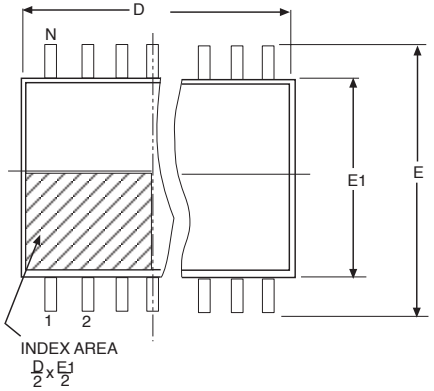
SIDE VIEW

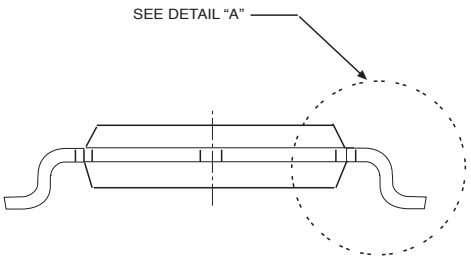
18 Pin WSOIC JEDEC MS-013 (AB) Variation			
SYMBOL	MIN	NOM	MAX
A	2.350	-	2.650
A1	0.100	-	0.300
A2	2.050	-	2.550
b	0.310	-	0.510
c	0.200	-	0.330
D	11.55 BSC		
E	10.30 DSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.400	-	1.270
L1	1.04 REF		
L2	0.25 BSC		
ø	0º	-	8º
ø1	5º	-	15º

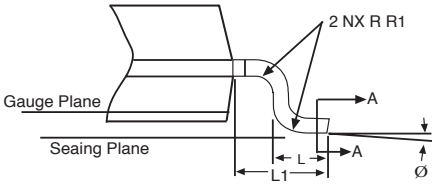
Note: Dimensions in (mm)



SECTION B-B



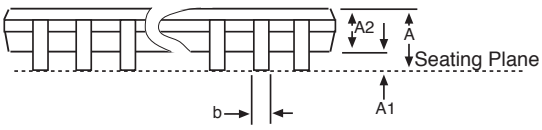


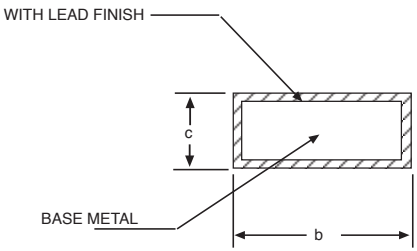


DETAIL A

20 Pin SSOP JEDEC MO-153 (AE) Variation			
SYMBOL	MIN	NOM	MAX
A	-	-	2
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	6.9	7.2	7.5
E	7.4	7.8	8.2
E1	5	5.3	5.6
L	0.55	0.75	0.95
L1	1.25 REF		
ø	0º	4º	8º

Note: Dimensions in (mm)





Section A-A

20 PIN SSOP

ORDERING INFORMATION

Part Number	Temperature Range	Package
SP385ECA-1	0°C to +70°C	20–pin SSOP
SP385ECA-1/TR	0°C to +70°C	20–pin SSOP
SP385EEA-1	–40°C to +85°C	20–pin SSOP
SP385EEA-1/TR	–40°C to +85°C	20–pin SSOP
SP385ECT-1	0°C to +70°C	18–pin WSOIC
SP385ECT-1/TR	0°C to +70°C	18–pin WSOIC
SP385EET-1	–40°C to +85°C	18–pin WSOIC
SP385EET-1/TR	–40°C to +85°C	18–pin WSOIC

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP385EEA-1/TR = standard; SP385EEA-1-L/TR = lead free

/TR = Tape and Reel

Pack quantity is 1,500 for WSOIC and SSOP.

CLICK HERE TO ORDER SAMPLES

Sipex Corporation

ANALOG EXCELLENCE

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