μPD75048/75P056
General-Purpose 4-Bit Microcomputers With EEPROM and A/D Converter

Description

The μPD75048 is a single-chip CMOS microcomputer containing CPU, ROM, EEPROM, RAM, I/O ports, several timer/counters, A/D converter, vectored interrupts, subsystem clock, and serial interface.

The instruction set allows the user to manipulate RAM data and I/O ports in 1-, 4-, and 8-bit units. The devices are ideally suited for controlling devices which require EEPROM, such as meters requiring individual calibration.

Features

- 103 instructions
  - Bit manipulation
  - 4-bit and 8-bit transfer
  - GETI instruction, to convert one 2-byte or two 1-byte instructions into a single 1-byte instruction
  - 1-byte relative branch instruction
- Fast execution time (@ 4.19 MHz)
  - High-speed cycle: 0.95 μs
  - Lower-voltage cycles: 1.91 and 15.3 μs
- 8064 bytes of program ROM: μPD75048
- 16256 bytes of program ROM: μPD75P056
- 1024 x 4 bits of EEPROM
- 512 x 4 bits of RAM
  - Allows operation on 1, 4, or 8 bits
- Bit sequential buffer
  - 16-bit, bit manipulation memory
- Eight 4-bit registers
- Accumulators
  - 1-bit (CY)
  - 4-bit (A)
  - 8-bit (XA)
- 48 I/O lines
  - 12 N-channel open drain; can withstand 10 V
  - 12 outputs directly drive LEDs
  - 43 lines can have an on-chip pullup/pulldown resistor
- One external event input
- Four timers
  - 8-bit basic interval timer
  - 8-bit timer/event counter
  - 14-bit watch timer
  - 16-bit multifunction timer/event counter which can be used as an 8-bit timer/event counter, PWM output, 16-bit free-running timer, or 16-bit counter for an integrating A/D converter
- A/D converter
  - 8-channel, 8-bit
- Four zero cross detection pins
- 8-bit serial interface
  - SBI mode
  - 2- or 3-wire mode: data transfer can be full duplex or receive only, and can be MSB or LSB first
- Vectored interrupts
  - Three external interrupts
  - Four internal interrupts
  - Nine inputs which each generate one interrupt request
- Standby modes
  - HALT mode: stops CPU only
  - STOP mode: stops main clock generator
- Operates with oscillator or ceramic resonator
- OTP version: μPD75P056
- CMOS operation, with V_{DD} from 2.7 to 6.0 V

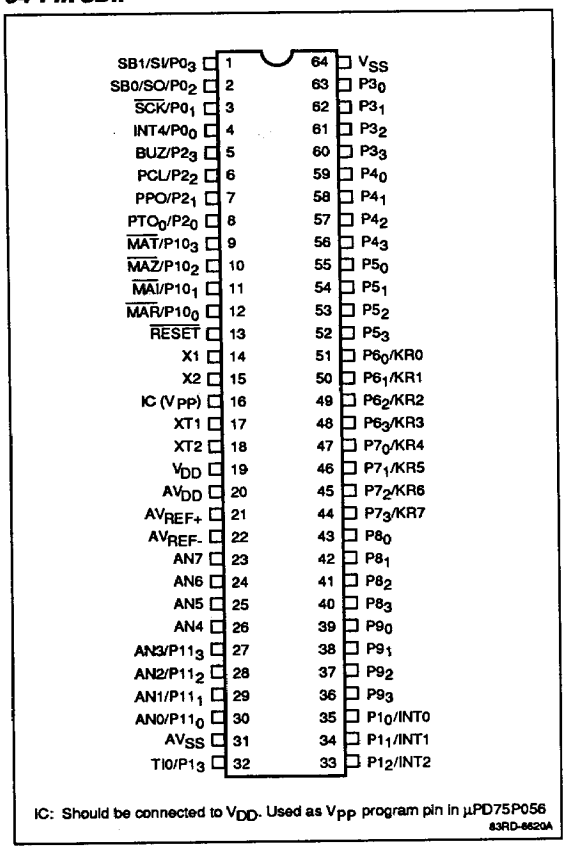
Ordering Information

Part Number	Package Type	ROM
μPD75048CW-xxx	64-pin plastic SDIP	Mask ROM
μPD75048GC-xxx-AB8	64-pin plastic QFP	Mask ROM
μPD75P056CW*	64-pin plastic SDIP	OTP
μPD75P056GC-AB8*	64-pin plastic QFP	OTP

*Under Development

Pin Configurations

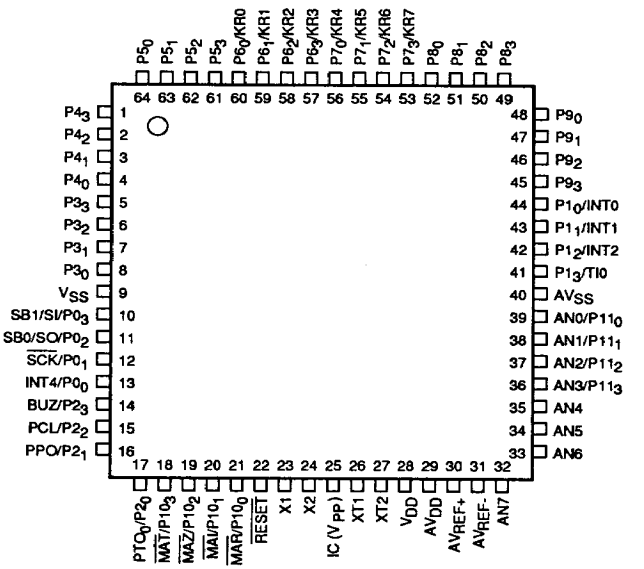
64-Pin SDIP



IC: Should be connected to V_{DD}. Used as V_{PP} program pin in μPD75P056

83RD-8620A

64-Pin QFP



IC: Should be connected to V_{DD}. Used as V_{PP} programming pin in μPD75P056

83RD-66218

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Pin Identification

Symbol	Function
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/$\overline{SCK}$	Port 0 input; serial clock
$P0_2$/SO/SB0	Port 0 input; serial out; serial interface
$P0_3$/SI/SB1	Port 0 input; serial in; serial interface
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/TI0	Port 1 input; timer 0 input
$P2_0$/PTO0	Port 2 I/O; timer/event counter output
$P2_1$/PPO	Port 2 I/O; multifunction timer output
$P2_2$/PCL	Port 2 I/O; clock output
$P2_3$/BUZ	Port 2 I/O; buzzer output
$P3_0$-$P3_3$	Port 3 I/O
$P4_0$-$P4_3$	Port 4 I/O
$P5_0$-$P5_3$	Port 5 I/O
$P6_0$/KR0	Port 6 I/O; key scan input 0
$P6_1$/KR1	Port 6 I/O; key scan input 1
$P6_2$/KR2	Port 6 I/O; key scan input 2
$P6_3$/KR3	Port 6 I/O; key scan input 3
$P7_0$/KR4	Port 7 I/O; key scan input 4
$P7_1$/KR5	Port 7 I/O; key scan input 5
$P7_2$/KR6	Port 7 I/O; key scan input 6
$P7_3$/KR7	Port 7 I/O; key scan input 7
$P8_0$-$P8_3$	Port 8 I/O
$P9_0$-$P9_3$	Port 9 I/O
$P10_0$/$\overline{MAR}$	Port 10 I/O; multifunction timer/event counter output
$P10_1$/$\overline{MAI}$	Port 10 I/O; multifunction timer/event counter output
$P10_2$/$\overline{MAZ}$	Port 10 I/O; multifunction timer/event counter output
$P10_3$/$\overline{MAT}$	Port 10 I/O; multifunction timer/event counter input
$P11_0$/AN0	Port 11 I/O; A/D converter input 0
$P11_1$/AN1	Port 11 I/O; A/D converter input 1
$P11_2$/AN2	Port 11 I/O; A/D converter input 2
$P11_3$/AN3	Port 11 I/O; A/D converter input 3
AN4-AN7	A/D converter inputs 4-7
AV_{DD}	A/D converter positive power supply
AV_{SS}	A/D converter ground
AV_{REF+} AV_{REF-}	A/D converter reference voltages
IC (V_{PP})	Internally connected (Programming voltage for μPD75P056)
X1, X2	Main clock inputs
XT1, XT2	Subsystem clock inputs
$\overline{RESET}$	Reset input
V_{DD}	Positive power supply
V_{SS}	Ground

PIN FUNCTIONS

$P0_0$/INT4, $P0_1$/$\overline{SCK}$, $P0_2$/SO/SB0, $P0_3$/SI/SB1

These pins can be used as 4-bit input port 0. Or, $P0_0$ can also be used for vectored interrupt 4, which interrupts on either the leading edge or the trailing edge of the signal. $P0_1$-$P0_3$ may also be used for the serial interface in the SBI or 2- or 3-wire mode. SI is the serial input, SO is the serial output, and $\overline{SCK}$ is the serial clock. Reset causes these pins to default to the port 0 input mode.

$P1_0$/INT0, $P1_1$/INT1, $P1_2$/INT2, $P1_3$/TI0

These pins can be used as 4-bit input port 1. Or, $P1_0$ and $P1_1$ can also be used for edge-triggered interrupts INT0 and INT1. $P1_2$ can be used for INT2, which is also an edge-triggered input, but one which generates an interrupt request and does not cause an interrupt. $P1_3$ can be used as an input clock to the timer/event counter to count external events. Reset causes these pins to default to the port 1 input mode.

$P2_0$/PTO0, $P2_1$/PPO, $P2_2$/PCL, $P2_3$/BUZ

These pins can be used as 4-bit I/O port 2. When used as an output, the data is latched. When used as an input port, the port outputs are three-state. $P2_0$ can also be used as the output of the timer/event counter flip flop (TOUT); $P2_1$ can also be used as the output for the multifunction timer/event counter T flip flop; $P2_2$ can be used as the output (PCL) of the clock generator; and $P2_3$ can be used to output square waves for a buzzer. Reset causes these pins to default to the port 2 input mode.

$P3_0$-$P3_3$

These pins are used for I/O port 3. Each bit in this port can be independently programmed to be either an input or an output. This port has latched outputs, and can directly drive LEDs. A reset signal causes this port to default to the input mode.

$P4_0$-$P4_3$, $P5_0$-$P5_3$

Port 4 and port 5 are identical 4-bit I/O ports which can be combined together to function as a single 8-bit port. Latched outputs will directly drive LEDs. Outputs are N-channel open drain, and can withstand up to 10 volts; pullup resistor mask options are available for these ports. A reset signal causes these ports to default to the input mode.

$P6_0$/KR0, $P6_1$/KR1, $P6_2$/KR2, $P6_3$/KR3 $P7_0$/KR4, $P7_1$/KR5, $P7_2$/KR6, $P7_3$/KR7

Ports 6 and 7 are 4-bit I/O ports with latched outputs. Each pin of port 6 can be independently programmed to be either an input or an output, while port 7 can be programmed to be either all inputs or all outputs. Alternately, these pins may be used to detect the falling edge of inputs KR0-KR3 (port 6) and KR4-KR7 (port 7). A reset signal causes these ports to default to the input mode.

$P8_0$-$P8_3$, $P9_0$-$P9_3$

Ports 8 and 9 are identical 4-bit I/O ports. Outputs are latched. A reset signal causes these ports to default to the input mode.

$P10_0$/$\overline{MAR}$, $P10_1$/$\overline{MAI}$, $P10_2$/$\overline{MAZ}$, $P10_3$/$\overline{MAT}$

These pins are used for I/O Port 10. Outputs are N-channel open drain which can withstand up to 10 volts. $P10_0$-$P10_2$ can also be used as the $\overline{MAR}$, $\overline{MAI}$, and $\overline{MAZ}$ outputs from the multifunction timer/event counter's A/D control logic. $P10_3$ can be used as the input $\overline{MAT}$ to the multifunction timer/event counter's A/D control logic. A reset signal causes this port to default to the input mode.

$P11_0$/AN0, $P11_1$/AN1, $P11_2$/AN2, $P11_3$/AN3

These pins are used for I/O Port 11, or can alternately be used as A/D converter inputs AN0-AN3. A reset signal causes this port to default to the input mode.

AN4-AN7

A/D converter inputs AN4-AN7.

AV_{DD}

A/D converter positive power supply.

AV_{SS}

A/D converter analog ground.

AV_{REF+}, AV_{REF-}

A/D converter positive and negative reference voltages.

IC/V_{PP}

This pin should be connected to V_{DD} when using the μPD75048. For the μPD75P056, this pin is used as the programming voltage input during the EPROM write/verify cycles. When the device is not being programmed, this pin should be connected to V_{DD}.

X1, X2

These pins are the main system clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

XT1, XT2

These pins are the subsystem clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

$\overline{RESET}$

This is the reset input, and it is active low.

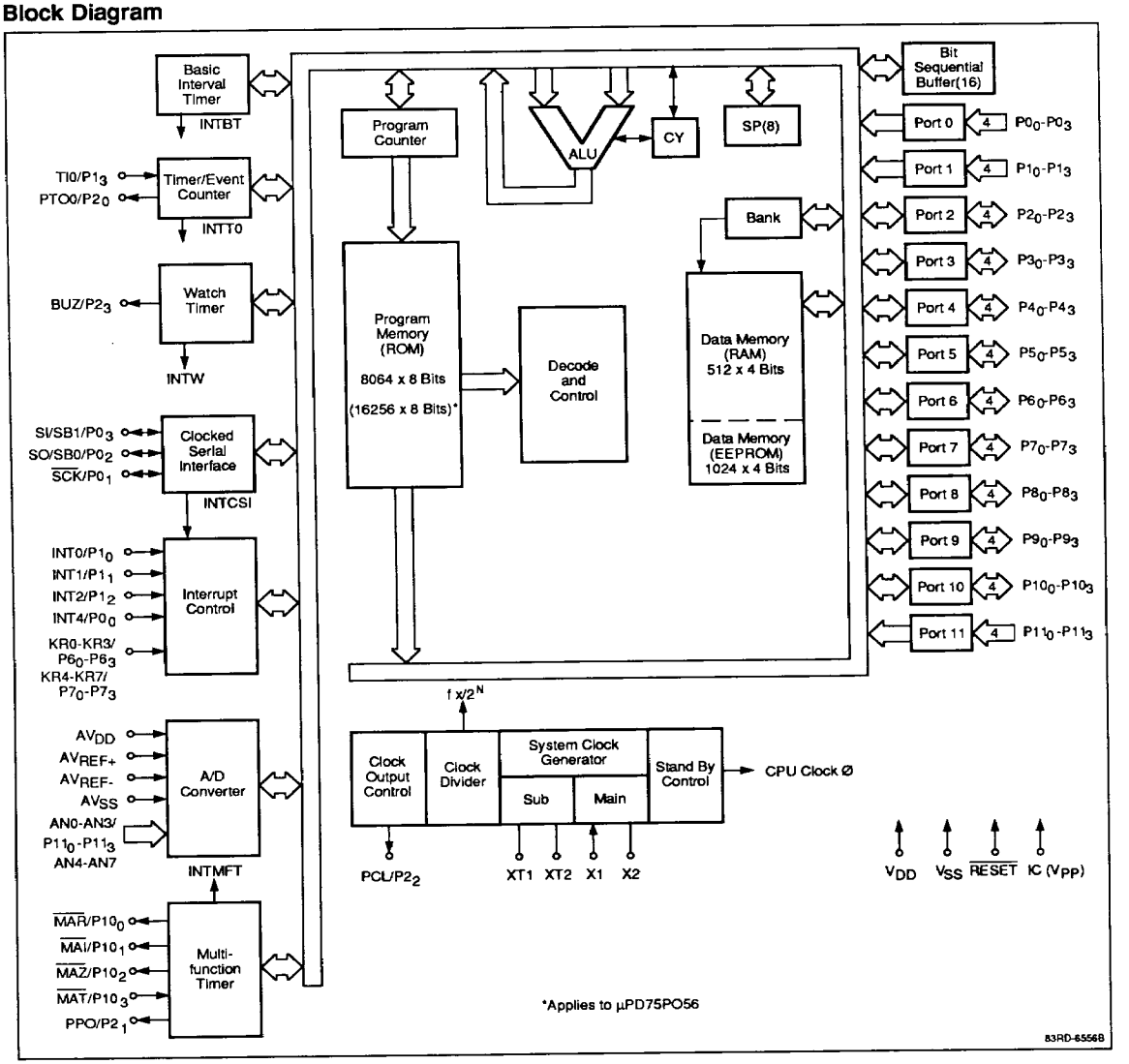
V_{DD}

The system positive power supply pin.

V_{SS}

System ground.

Block Diagram



Specifications

ROM	8064 bytes (μPD75048) 16256 bytes (μPD75P056)
RAM	512 x 4 bits
EEPROM	1024 x 4 bits
General-purpose registers	4 bits x 8 or 8 bits x 4
Instruction cycle	0.95 μs/1.91 μs/15.3 μs (with main system clock operating at 4.19 MHz)
	122 μs (with subsystem clock operating at 32 kHz)
I/O Ports	48 total lines. There are 12 N-channel open-drain I/O ports, each tolerating as much as 10 volts. (Pullup resistor mask-option is available in the μPD75048 only). The remaining 36 lines are standard CMOS, including 12 input ports and 24 I/O ports. Of these, 27 have software-selectable pullup resistors, and four have software-selectable pulldown resistors.
A/D converter	8-bit x 8-channel
	Low-voltage operation possible (V_{DD} = 2.7 to 6.0 V)
Timer/Counter	Three. These include an 8-bit timer/event counter, an 8-bit basic interval timer, and a clock timer.
Multifunction timer	This can be used as an 8-bit timer/event counter, PWM output, 16-bit free-running timer, or 16-bit counter for an integrating A/D converter.
Serial interface	NEC standard serial bus interface (SBI)
	Clock serial interface
External interrupts	Three vector interrupts, one test input.
Internal interrupts	Six vector interrupts, one test input.
Bit sequential buffer	16-bit, on-chip
Clock output (PCL)	CPU clock ϕ: 524 kHz, 262 kHz, 65.6 kHz (with main system clock operating at 4.19 MHz)
Buzzer output (BUZ)	2 kHz, 4 kHz, 32 kHz (with subsystem clock operating at 32.768 kHz)
Package	64-pin plastic SDIP (750 mil)
	64-pin plastic QFP (14 x 14 mm)
Operating voltage	V_{DD} = 2.7 to 6.0 V EEPROM target specification V_{DD} = 2.7 to 6.0 V

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