HYUNDAI

32Mx72 bits
PC100 SDRAM Registered DIMM

based on 16Mx8 SDRAM with LVTTL, 4 banks & 4K Refresh

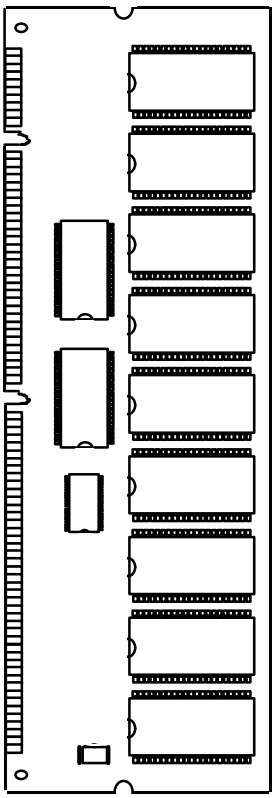
GMM27333230ANTG

Description

The GMM27333230ANTG is a 32M x 72bits Synchronous Dynamic RAM MODULE which is assembled 18 pieces of 16M x 8bits Synchronous DRAMs in 54 pin TSOP II, 2 pieces of 16 bits Register in 48 pin TSSOP, one clock distribution PLL in 24 pin SOP and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM27333230ANTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM27333230ANTG provides common data inputs and outputs.

GMM27333230ANTG (Double Side)



Features

* PC100/PC66 Compatible
  -8(125MHz)
  -7K(PC100,2-2-2)/-7J(PC100,3-2-2)/-10K(PC66)
* 3.3V +/- 0.3V Power supply
* Maximum Clock frequency
  100 / 125 MHz
* LVTTL Interface
* Burst read/write operation and burst read/ single write operation capability
* Programmable burst length ;
  1, 2, 4, 8, Full page
* Programmable burst sequence
  Sequential / Interleave
* Full Page burst length capability
  Sequential burst
  Burst stop capability
* Programmable $\overline{CAS}$ Latency ; 2, 3
* CKE power down mode
* Input / Output data masking
* 4096 Refresh Cycles / 64ms
* Auto refresh / Self refresh Capability
* Serial Presence Detect with EEPROM

Pin Name

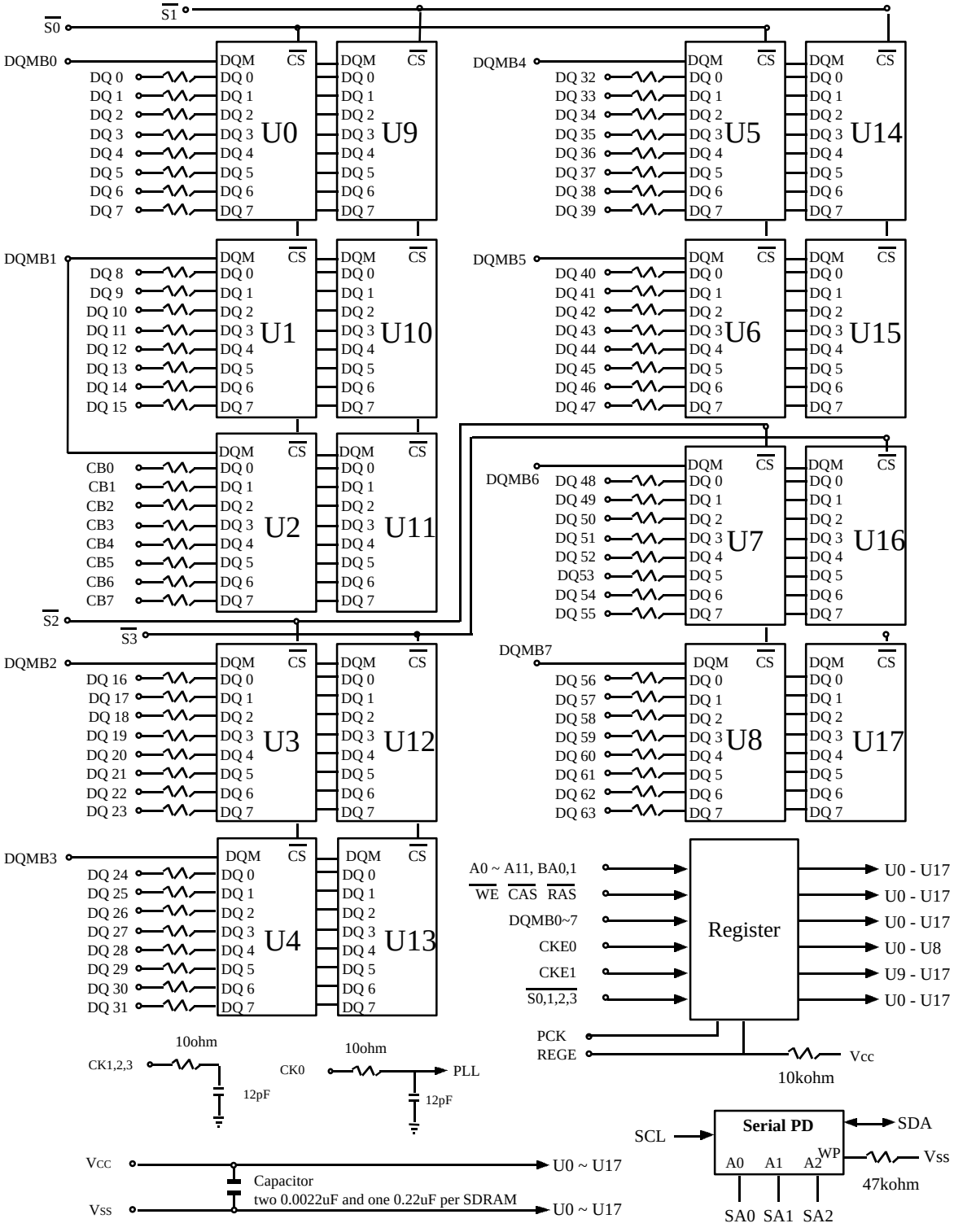
CK0, 1, 2, 3	Clock input
$\overline{CKE}$0,1	Clock Enable
$\overline{S}$0~3	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
REGE	Register Enable
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
WP	Write Protect for SPD
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	29	DQMB1	57	DQ18	85	V_{SS}	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	V_{CC}	87	DQ33	115	$\overline{RAS}$	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{CC}	34	A2	62	*V_{REF}, NC	90	V_{CC}	118	A3	146	*V_{REF}, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	V_{CC}	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	V_{CC}	101	DQ45	129	$\overline{S3}$	157	V_{CC}
18	V_{CC}	46	DQMB2	74	DQ28	102	V_{CC}	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	V_{CC}	77	DQ31	105	CB4	133	V_{CC}	161	DQ63
22	CB1	50	NC	78	V_{SS}	106	CB5	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	CK2	107	V_{SS}	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	V_{CC}	54	V_{SS}	82	SDA	110	V_{CC}	138	V_{SS}	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	V_{CC}	112	DQMB4	140	DQ49	168	V_{CC}

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0,1 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0,1,2,3}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A9 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs. Data is not latched in the register.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. -Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. -Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
REGE	If REGE input is high, permits the DIMM to operate in `registered mode`. If REGE input is low, permits the DIMM to operate in `buffered mode`.
NC	No Connection pins.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to Vcc+0.5 (<= 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	C	
Storage temperature	Tstg	-55 to +125	C	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1,3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.6V for pulse width <= 3ns

3. V_{IL} (min) = -2.0V for pulse width <= 3ns

Registered DIMM Operation

1. All control and address signals are registered on-DIMM register and hence delayed by one cycle in arriving at the SDRAMs. But data is not registered in the register.

2. CAS latency defines the delay from when a READ command is registered on a rising clock edge to when the data from that READ command becomes available at the outputs. Do not confuse DIMM CAS latency with the SDRAM CAS latency which is one clock less.

DC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ}= 0 V)

Parameter	Symbol	- 8	- 7K	- 7J	- 10K	Unit	Test conditions	Notes
		Max	Max	Max	Max			
Operating current	I_{CC1}	1200			1100	mA	Burst length= 1 t_{RC} = min	1, 2, 3
Standby current in power down	I_{CC2P}	40				mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)	I_{CC2PS}	20				mA	CKE=V_{IL}, t_{CK}= Infinity	6
Standby current in non power down ($\overline{CAS}$ Latency=2)	I_{CC2N}	300				mA	CKE,CS = V_{IH}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)	I_{CC2NS}	280				mA	CKE,CS = V_{IH}, t_{CK} = Infinity	4
Active standby current in power down	I_{CC3P}	100				mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)	I_{CC3PS}	85				mA	CKE = V_{IL}, t_{CK} = Infinity	2,6
Active standby current in non power down	I_{CC3N}	550				mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)	I_{CC3NS}	500				mA	CKE,CS = V_{IH}, t_{CK} = Infinity	2,8
Burst operating current (CL= 2)	I_{CC4}	1300	1300	1000	1000	mA	t_{CK} = min BL = 4	1,2,3
Burst operating current (CL= 3)	I_{CC4}	1400	1300	1300	1300	mA		
Refresh current	I_{CC5}	2300	2300	2200	1900	mA	t_{RC} = min	3
Self refresh current	I_{CC6}	40				mA	V_{IH} >=V_{CC} - 0.2 V_{IL} <=0.2V	7

Parameter	Symbol	- 8, - 7K, -7J, -10K		Unit	Test conditions	Notes
		Min	Max			
Input leakage current	I_{LI}	-1	1	uA	0<=Vin<=V_{CC}	
Output leakage current	I_{LO}	-1.5	1.5	uA	0<=Vout <=V_{CC} DQ = disable	
Output high voltage	V_{OH}	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After Power down mode, CLK operating current.
6. After Power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25C, V_{CC}, V_{CCQ} = 3.3V +/- 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A11, BA0,1)	-	TBD	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 3
C_{I3}	Input capacitance (CK0~CK3)	-	TBD	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$~$\overline{S3}$)	-	TBD	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	TBD	pF	1, 3
$C_{I/O}$	I/O capacitance (DQ0 ~ 63)	-	TBD	pF	1, 2 ,3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = VIH to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	-8		-7K		-7J		-10K		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	12	-	10	-	15	-	15	-	ns	1
	(CL=3)	t_{CK}	8	-	10	-	10	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	6	-	6	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	6	-	8		
Data-out hold time		t_{OH}	3	-	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedance		t_{LZ}	2	-	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedance (CL = 2,3)		t_{HZ}	-	6	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	68	-	70	-	70	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	48	120000	50	120000	50	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	20	-	20	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	20	-	20	-	30	-	ns	1

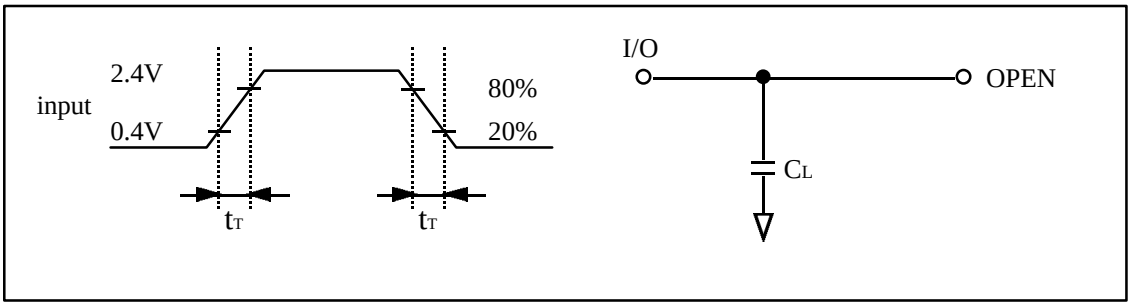
AC Characteristics (Ta = 0 to 70C, V_{CC}, V_{CCQ} = 3.3 V +/- 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	- 8		- 7K		- 7J		- 10K		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	8	-	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	16	-	20	-	20	-	20	-	ns	1
Refresh period	t_{REF}	-	64	-	64	-	64	-	64	ms	
PLL Stabilization time	t_{STAB}	200	-	200	-	200	-	200	-	us	6

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V. If t_T is longer than 1ns,transition time compensation should be considered.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (min)defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.
5. t_{CES} define CKE setup time to CKE rising edge except Power down exit command.
6. The on-DIMM PLL must be given enough clock cycles to stabilize (t_{STAB}) before any operation can be guaranteed.

Test Condition

Input and output-timing reference levels: 1.4V
Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-8		-7K		-7J		-10K		Notes
frequency(MHz)			125	83	100	100	100	66	100	66	
t_{CK} (ns)			8	12	10	10	10	15	10	15	
Active command to column command (same bank)		l_{RCD}	3	2	2	2	2	2	3	2	1
Active command to active command (same bank)		l_{RC}	9	6	7	7	7	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to Precharge command (same bank)		l_{RAS}	6	4	5	5	5	4	6	4	1
Precharge command to active command (same bank)		l_{RP}	3	2	2	2	2	2	3	2	1
Write recovery or last data-in to Precharge command (same bank)		l_{RWL}	1	1	1	1	1	1	1	1	1
Active command to active command (different bank)		l_{RRD}	2	2	2	2	2	2	2	2	1
Self refresh exit time		l_{SREX}	1	2	1	1	1	2	2	2	
Last data in to active command (Auto Precharge, same bank)		l_{APW}	4	3	3	3	3	3	5	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input		l_{SEC}	9	6	7	7	7	6	9	6	= [l_{RC}]
Precharge command to high impedance	(CL=2)	l_{HZP}	-	2	2	2	-	2	-	2	
	(CL=3)	l_{HZP}	3	3	3	3	3	3	3	3	
Last data out to active command (auto Precharge) (same bank)		l_{APR}	1	1	1	1	1	1	1	1	
Last data out to Precharge (early Precharge)	(CL=2)	l_{EP}	-	-1	- 1	- 1	-	-1	-	-1	
	(CL=3)	l_{EP}	-2	-2	- 2	- 2	- 2	- 2	- 2	- 2	
Column command to column command		l_{CCD}	1	1	1	1	1	1	1	1	
Write command to data in latency		l_{WCD}	0	0	0	0	0	0	0	0	
DQM to data in		l_{DID}	0	0	0	0	0	0	0	0	
DQM to data out		l_{DOD}	2	2	2	2	2	2	2	2	
CKE to CLK disable		l_{CLE}	1	1	1	1	1	1	1	1	
Register set to active command		l_{RSA}	1	1	1	1	1	1	1	1	
$\overline{CS}$ to command disable		l_{CDD}	0	0	0	0	0	0	0	0	
Power down exit to command input		l_{PEC}	1	1	1	1	1	1	1	1	

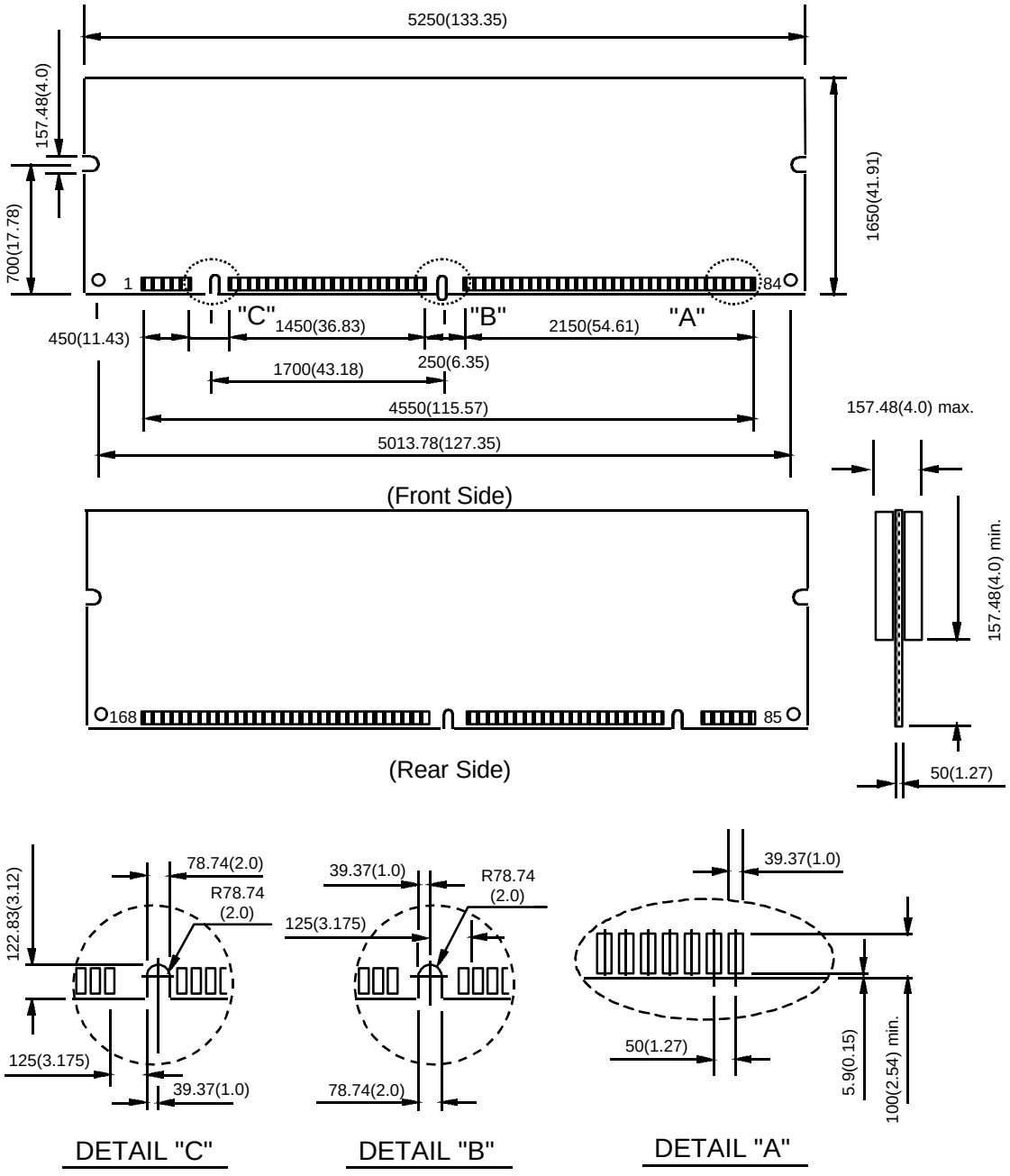
Relationship Between Frequency and Minimum Latency

Parameter		Symbol	- 8		- 7K		- 7J		- 10K		Notes
frequency(MHz)			125	83	100	100	100	66	100	66	
t_{CK} (ns)			8	12	10	10	10	15	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	1	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	2	2	
Burst stop to output high impedance	(CL=2)	l_{BSH}	-	2	2	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	0	0	

Notes : 1. l_{RCD} to l_{RRD} are recommended value.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions +/-5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

SDRAM Memory Module EEPROM Data Information

GMM27333230ATG-7J 00.05.09

Byte	Function described	Function support	HEX Code	DEC Code	BIN Code	Note
0	Define # bytes written into serial memory at module mfgr	128 Bytes	80	128	10000000	
1	Total # bytes of SPD memory device	256 Bytes	08	008	00001000	
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	SDRAM	04	004	00000100	
3	# Row addresses on this assembly	12	0C	012	00001100	
4	# Column addresses on this assembly	11	0B	011	00001011	
5	# Module banks on this assembly	1	01	001	00000001	
6	Data width of this assembly...	72 bit	48	072	01001000	
7	...Data width continuation	N/A	00	000	00000000	
8	Voltage interface standard of this assembly	LVTTL	01	001	00000001	
9	SDRAM cycletime	10.0 ns	A0	160	10100000	
10	SDRAM access from clock	6.0 ns	60	096	01100000	
11	DIMM configuration type (Non-parity, Parity, ECC)	ECC	02	002	00000010	
12	Refresh rate/type	Normal(15.625us)	80	128	10000000	
13	DRAM/SDRAM width, primary DRAM/SDRAM	x4	04	004	00000100	
14	Error checking SDRAM data width	x4	04	004	00000100	
15	Minimum clock delay, back to back random column address(tCCD)	1 ns	01	001	00000001	
16	Burst lengths supported	Full Page Supported	8F	143	10001111	
17	# Banks on each SDRAM device	4 banks	04	004	00000100	
18	CAS # latency	2&3	06	006	00000110	
19	CS # latency	0	01	001	00000001	
20	Write latency	0	01	001	00000001	
21	SDRAM module attributes	Register(w/ PLL)	16	022	00010110	
22	SDRAM device attributes : General	Support All(VCC:10%)	0F	015	00001111	
23	Minimum clock cycle time at CL X-1	15.0 ns	F0	240	11110000	
24	Maximum data access time from clock at CL X-1	8.0 ns	80	128	10000000	
25	Minimum clock cycle time at CL X-2	N/A	00	000	00000000	
26	Maximum data access time from clock at CL X-2	N/A	00	000	00000000	
27	Minimum row precharge time(tRP)	20 ns	14	020	00010100	
28	Minimum row active to row active delay(tRRD)	20 ns	14	020	00010100	
29	Minimum RAS to CAS delay(tRCD)	20 ns	14	020	00010100	
30	Minimum RAS pulse width(tRAS)	50 ns	32	050	00110010	
31	Module bank density	256 MBytes	40	064	01000000	
32	Command and address signal input setup time(tAS)	2.0 ns	20	032	00100000	
33	Command and address signal input hold time(tAH)	1.0 ns	10	016	00010000	
34	Data signal input setup time(tDS)	2.0 ns	20	032	00100000	
35	Data signal input hold time(tDH)	1.0 ns	10	016	00010000	
36-61	Superset information (may be used in future)	TBD	00	000	00000000	
62	SPD revision	Rev 1.2	12	018	00010010	
63	Checksum for bytes 0-62		C8	200	11001000	
64	Manufacturers JEDEC ID code per JEP-106F	HME	E0	224	11100000	1st Group
65-71	.... Continuation Manufacturers JEDEC ID Code		00	000	00000000	
72	Manufacturing location	Korea	52	082	01010010	82d(free)
73	Manufacturer's part number	GMM27333230ATG-7J	47	071	01000111	G
74	=== Allowed characters include 0-9, A-Z and 'space' ===		4D	077	01001101	M
75			4D	077	01001101	M
76			32	050	00110010	2
77			37	055	00110111	7
78			33	051	00110011	3
79			33	051	00110011	3
80			33	051	00110011	3
81			32	050	00110010	2
82			33	051	00110011	3
83			30	048	00110000	0
84			41	065	01000001	A
85			54	084	01010100	T
86			47	071	01000111	G
87			2D	045	00101101	-
88			37	055	00110111	7
89			4A	074	01001010	J
90			20	32	00100000	blank
91	Revision Code	Rev 0	00	000	00000000	
92	Revision Code		00	000	00000000	
93	Date Code	WW	14	020	00010100	20 ww
94		YY	00	000	00000000	0 year
95-98	Assembly serial number	Binary incremental	00	000	00000000	98byte start
99-125	Manufacturer specific data	N/A	00	000	00000000	
126	Intel specification for frequency		64	100	01100100	
127	Intel specfication details for 100Mhz Support	CK0_CL3	8D	141	10001101	
128-135	System integrator's ID		00	000	00000000	
136-150	System integrator's P/N		00	000	00000000	
151-152	System integrator's D/C		00	000	00000000	
153-165	System integrator's S/N		00	000	00000000	
166	Checksum for bytes 128-165		00	000	00000000	
167-189	Top level system serial no.		00	000	00000000	
190-221	Open		00	000	00000000	
222	Checksum for bytes 167-221		00	000	00000000	
223-253	Open		00	000	00000000	
254	Checksum for Bytes 223-253		00	000	00000000	
255	Checksum for bytes 0-128		00	000	00000000	

Source : Intel Rev. 1.2B

SDRAM Memory Module EEPROM Data Information

GMM27333230ATG-7K 00.05.09

Byte	Function described	Function support	HEX Code	DEC Code	BIN Code	Note
0	Define # bytes written into serial memory at module mfgr	128 Bytes	80	128	10000000	
1	Total # bytes of SPD memory device	256 Bytes	08	008	00001000	
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	SDRAM	04	004	00000100	
3	# Row addresses on this assembly	12	0C	012	00001100	
4	# Column addresses on this assembly	11	0B	011	00001011	
5	# Module banks on this assembly	1	01	001	00000001	
6	Data width of this assembly...	72 bit	48	072	01001000	
7	...Data width continuation	N/A	00	000	00000000	
8	Voltage interface standard of this assembly	LVTTL	01	001	00000001	
9	SDRAM cycletime	10.0 ns	A0	160	10100000	
10	SDRAM access from clock	6.0 ns	60	096	01100000	
11	DIMM configuration type (Non-parity, Parity, ECC)	ECC	02	002	00000010	
12	Refresh rate/type	Normal(15.625us)	80	128	10000000	
13	DRAM/SDRAM width, primary DRAM/SDRAM	x4	04	004	00000100	
14	Error checking SDRAM data width	x4	04	004	00000100	
15	Minimum clock delay, back to back random column address(tCCD)	1 ns	01	001	00000001	
16	Burst lengths supported	Full Page Supported	8F	143	10001111	
17	# Banks on each SDRAM device	4 banks	04	004	00000100	
18	CAS # latency	2&3	06	006	00000110	
19	CS # latency	0	01	001	00000001	
20	Write latency	0	01	001	00000001	
21	SDRAM module attributes	Register(w/ PLL)	16	022	00010110	
22	SDRAM device attributes : General	Support All(VCC:10%)	0F	015	00001111	
23	Minimum clock cycle time at CL X-1	10.0 ns	A0	160	10100000	
24	Maximum data access time from clock at CL X-1	6.0 ns	60	096	01100000	
25	Minimum clock cycle time at CL X-2	N/A	00	000	00000000	
26	Maximum data access time from clock at CL X-2	N/A	00	000	00000000	
27	Minimum row precharge time(tRP)	20 ns	14	020	00010100	
28	Minimum row active to row active delay(tRRD)	20 ns	14	020	00010100	
29	Minimum RAS to CAS delay(tRCD)	20 ns	14	020	00010100	
30	Minimum RAS pulse width(tRAS)	50 ns	32	050	00110010	
31	Module bank density	256 MBytes	40	064	01000000	
32	Command and address signal input setup time(tAS)	2.0 ns	20	032	00100000	
33	Command and address signal input hold time(tAH)	1.0 ns	10	016	00010000	
34	Data signal input setup time(tDS)	2.0 ns	20	032	00100000	
35	Data signal input hold time(tDH)	1.0 ns	10	016	00010000	
36-61	Superset information (may be used in future)	TBD	00	000	00000000	
62	SPD revision	Rev 1.2	12	018	00010010	
63	Checksum for bytes 0-62		58	088	1011000	
64	Manufacturers JEDEC ID code per JEP-106F	HME	E0	224	11100000	1st Group
65-71	.... Continuation Manufacturers JEDEC ID Code		00	000	00000000	
72	Manufacturing location	Korea	52	082	01010010	82d(free)
73	Manufacturer's part number	GMM27333230ATG-7K	47	071	01000111	G
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81			32	050	00110010	2
82			33	051	00110011	3
83			30	048	00110000	0
84			41	065	01000001	A
85			54	084	01010100	T
86			47	071	01000111	G
87			2D	045	00101101	-
88			37	055	00110111	7
89			4B	075	01001011	K
90			20	32	00100000	blank
91	Revision Code	Rev 0	00	000	00000000	
92	Revision Code		00	000	00000000	
93	Date Code	WW	14	020	00010100	20 ww
94		YY	00	000	00000000	0 year
95-98	Assembly serial number	Binary incremental	00	000	00000000	98byte start
99-125	Manufacturer specific data	N/A	00	000	00000000	
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128-135	System integrator's ID		00	000	00000000	
136-150	System integrator's P/N		00	000	00000000	
151-152	System integrator's D/C		00	000	00000000	
153-165	System integrator's S/N		00	000	00000000	
166	Checksum for bytes 128-165		00	000	00000000	
167-189	Top level system serial no.		00	000	00000000	
190-221	Open		00	000	00000000	
222	Checksum for bytes 167-221		00	000	00000000	
223-253	Open		00	000	00000000	
254	Checksum for Bytes 223-253		00	000	00000000	
255	Checksum for bytes 0-128		00	000	00000000	

Source : Intel Rev. 1.2B