

FEATURES

- ❑ 16K x 4 Static RAM with Common I/O
- ❑ Auto-Powerdown™ Design
- ❑ Advanced CMOS Technology
- ❑ High Speed — to 8 ns maximum
- ❑ Low Power Operation
Active: 210 mW typical at 35 ns
Standby: 500 μW typical
- ❑ Data Retention at 2 V for Battery Backup Operation
- ❑ Plug Compatible with IDT 7188/7198, Cypress CY7C164/166
- ❑ Package Styles Available:
 - 22/24-pin Plastic DIP
 - 22/24-pin Sidebrazed, Hermetic DIP
 - 22/24-pin CerDIP
 - 24-pin Plastic SOIC
 - 24-pin Plastic SOJ
 - 22-pin Ceramic LCC
 - 28-pin Ceramic LCC

DESCRIPTION

The L7C164, L7C165, and L7C166 are high-performance, low-power CMOS static RAMs. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C164 has a single active-low Chip Enable. The L7C165 has two Chip Enables and a separate Output Enable. The L7C166 has a single Chip Enable and an Output Enable. These devices are available in seven speeds with maximum access times from 8 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 210 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption

automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C164, L7C165, and L7C166 consume only 30 μW (typical) at 3 V, allowing effective battery backup operation.

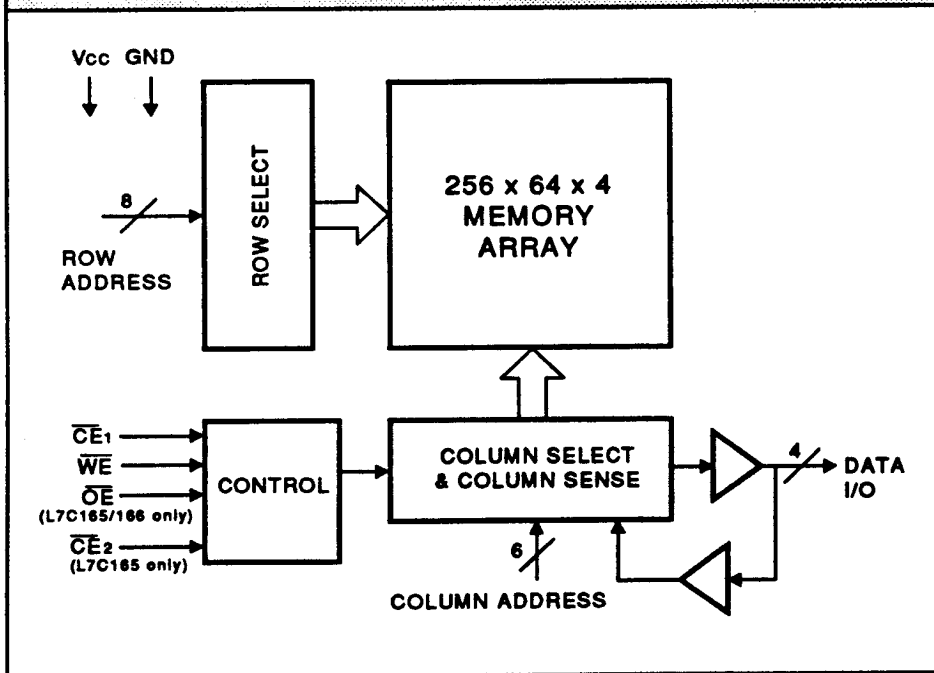
The L7C164, L7C165, and L7C166 provide asynchronous (unlocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A0 through A13. For the L7C164 and L7C166, reading from a designated location is accomplished by presenting an address and driving CE1 low while WE remains high. For the L7C165, both CE1 and CE2 must be low. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when CE or OE is high or WE is low.

Writing to an addressed location is accomplished when the active-low CE and WE inputs are low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C164, L7C165, and L7C166 can withstand an injection current of up to 200 mA on any pin without damage.

L7C164/165/166 BLOCK DIAGRAM



MAXIMUM RATINGS Above which useful life may be impaired (Notes 1, 2)

Storage temperature	-65°C to +150°C
Operating ambient temperature	-55°C to +125°C
Vcc supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ Vcc ≤ 5.5 V
Active Operation, Military	-55°C to +125°C	4.5 V ≤ Vcc ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ Vcc ≤ 5.5 V
Data Retention, Military	-55°C to +125°C	2.0 V ≤ Vcc ≤ 5.5 V

ELECTRICAL CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	IOH = -4.0 mA, Vcc = 4.5 V	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA			0.4	V
VIH	Input High Voltage		2.0		Vcc + 0.3	V
VIL	Input Low Voltage	(Note 3)	-3.0		0.8	V
IIX	Input Current	GND ≤ VIN ≤ Vcc	-10		+10	μA
IOZ	Output Leakage Current	GND ≤ VOUT ≤ Vcc, CE = Vcc	-10		+10	μA
IOS	Output Short Current	VOUT = GND, Vcc = Max (Note 4)			-350	mA
ICC2	Vcc Current, TTL Inactive	(Notes 5, 7)		15	30	mA
ICC3	Vcc Current, CMOS Standby	(Note 8)		100	500	μA
ICC4	Vcc Current, Data Retention	Vcc = 3.0 V (Note 9)		10	250	μA
CIN	Input Capacitance	Ambient Temp = 25°C, Vcc = 5.0 V			5	pF
COU	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

Symbol	Parameter	Test Condition	L7C164/165/166-							Unit
			35	25	20	15	12	10	8	
ICC1	Vcc Current, Active	(Notes 5, 6)	55	75	96	120	145	170	210	mA



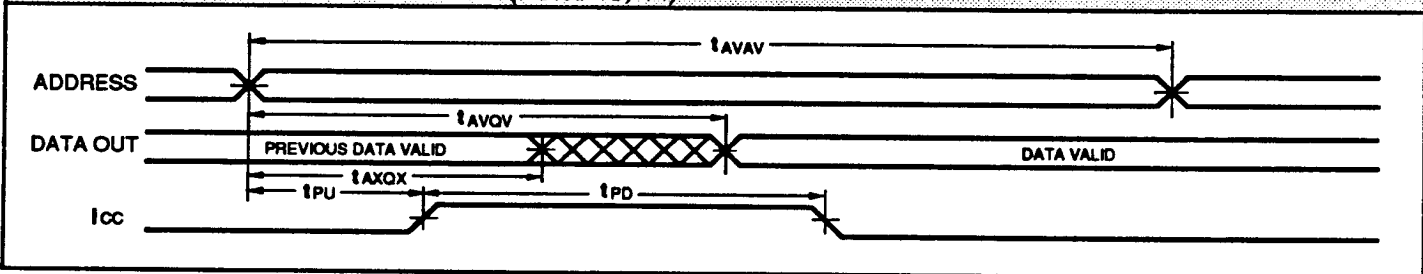
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SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

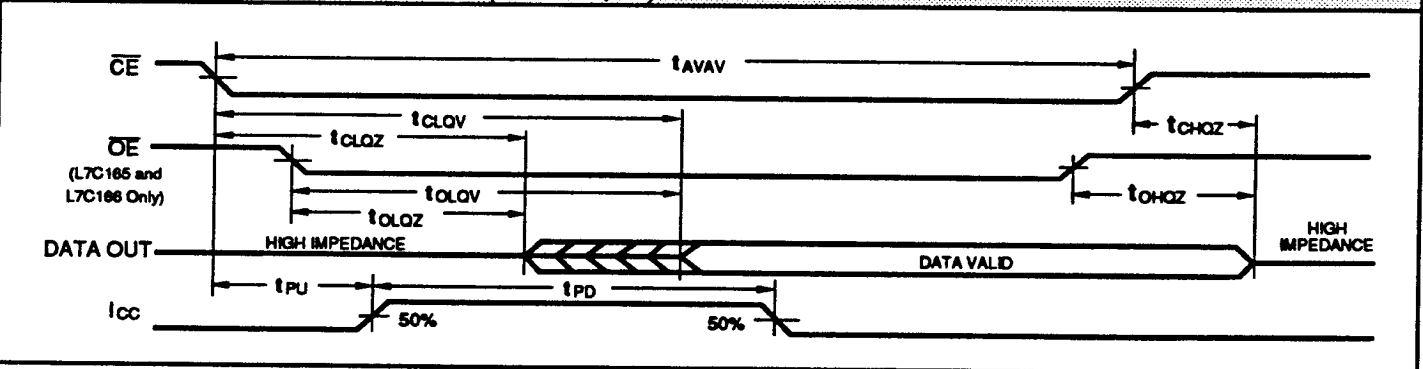
READ CYCLE (Notes 11, 12, 22, 23, 24)

Symbol	Parameter	L7C164/165/166-													
		35		25		20		15		12		10		8	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Read Cycle Time	35		25		20		15		12		10		8	
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
tAXQX	Address Change to Output Change	3		3		3		3		3		3		3	
tCLOV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
tCLOZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
tOLOV	Output Enable Low to Output Valid		15		12		10		8		6		4		4
tOLOZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0		0	
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		4
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	

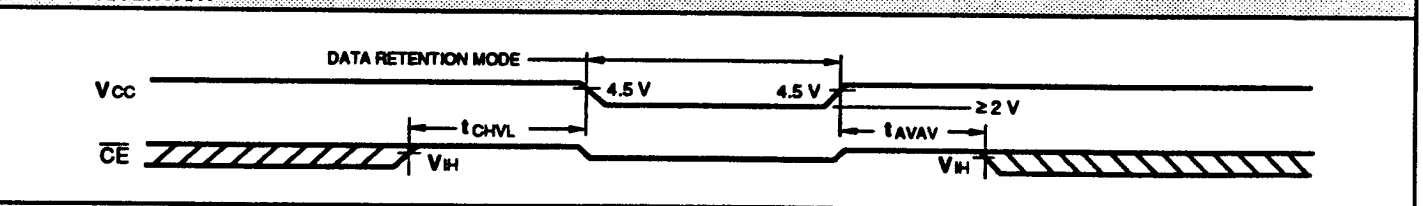
READ CYCLE — ADDRESS CONTROLLED (Notes 13, 14)



READ CYCLE — CE/OE CONTROLLED (Notes 13, 15)



DATA RETENTION

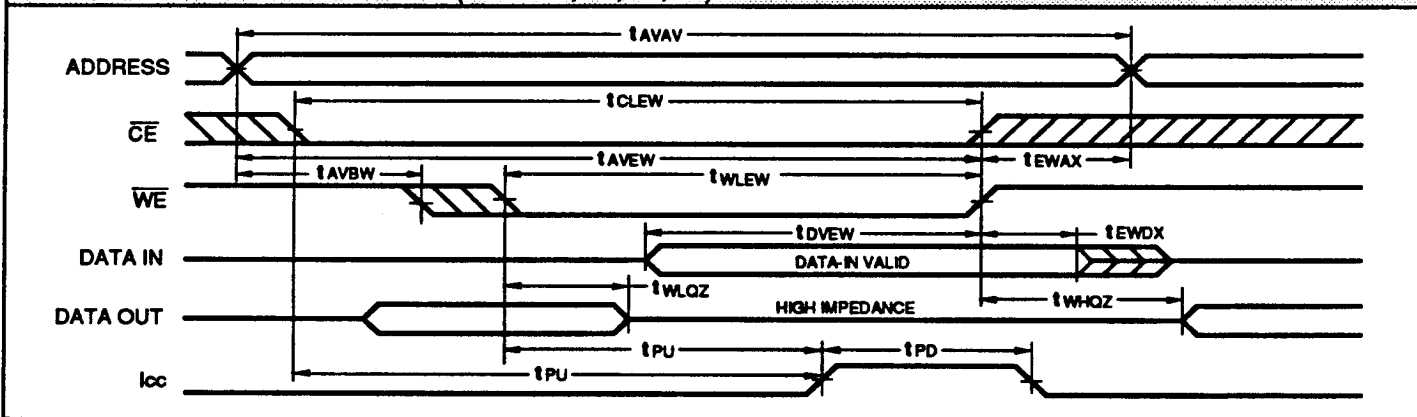


SWITCHING CHARACTERISTICS Over Operating Range (ns)

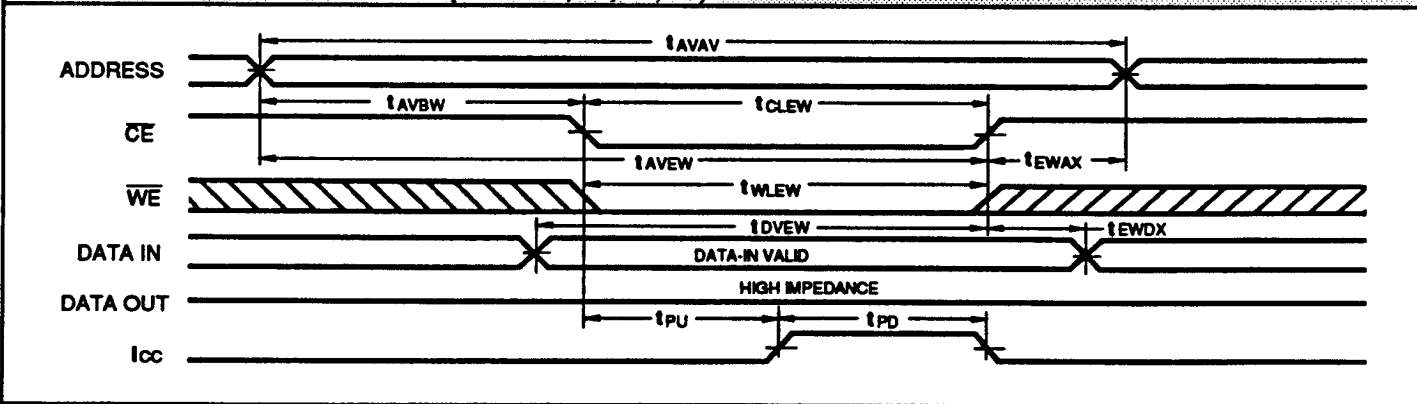
WRITE CYCLE (Notes 11, 12, 22, 23, 24)

Symbol	Parameter	L7C164/165/166-													
		35		25		20		15		12		10		8	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12		10		8	
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0	
tAVEV	Address Valid to End of Write Cycle	25		15		15		12		10		8		8	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5	
tDVEV	Data Valid to End of Write Cycle	15		10		10		7		6		5		4	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0	
tWLOZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3

WRITE CYCLE — WE CONTROLLED (Notes 16, 17, 18, 19)



WRITE CYCLE — CE CONTROLLED (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at -0.6 V. A current in excess of 100 mA is required to reach -2 V. The device can withstand indefinite operation with inputs as low as -3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of $+5.0$ V, an ambient temperature of $+25^{\circ}\text{C}$ and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{\text{CE}}^* \leq \text{VIL}$, $\overline{\text{WE}} \geq \text{VIH}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{\text{CE}}^* \geq \text{VIH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{\text{CE}}^* = \text{VCC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{\text{CE}}^*$ must be $\geq \text{VCC} - 0.2$ V. For all other inputs $\text{VIN} \geq \text{VCC} - 0.2$ V or $\text{VIN} \leq 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and

IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{\text{WE}}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{\text{CE}}^*$ low).

15. All address lines are valid prior to or coincident with the $\overline{\text{CE}}^*$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{\text{CE}}^*$ low and $\overline{\text{WE}}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{\text{WE}}$ goes low before or concurrent with $\overline{\text{CE}}^*$ going low, the output remains in a high impedance state.

18. If $\overline{\text{CE}}^*$ goes high before or concurrent with $\overline{\text{WE}}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

- Falling edge of $\overline{\text{CE}}^*$.
- Falling edge of $\overline{\text{WE}}$ ($\overline{\text{CE}}^*$ active).
- Transition on any address line ($\overline{\text{CE}}^*$ active).
- Transition on any data line ($\overline{\text{CE}}^*$ and $\overline{\text{WE}}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ± 200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{\text{CE}}^*$ or $\overline{\text{WE}}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 μF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

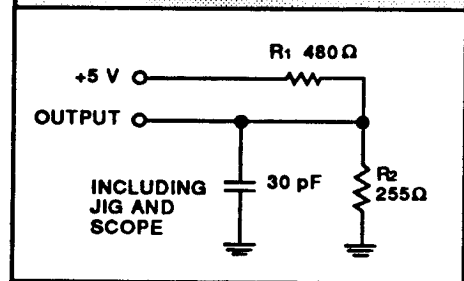


FIGURE 1b.

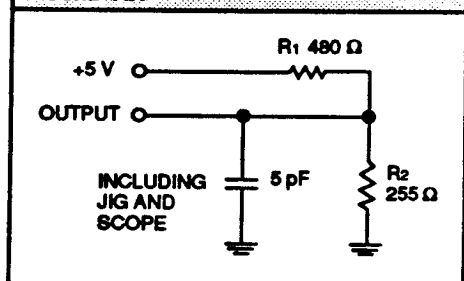
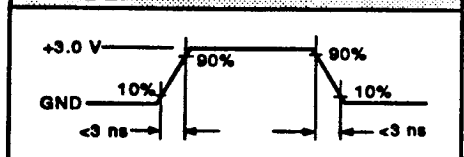


FIGURE 2.



* For the L7C165, $\overline{\text{CE}}^*$ refers to the logical AND of $\overline{\text{CE}}_1$ and $\overline{\text{CE}}_2$.

LOGIC

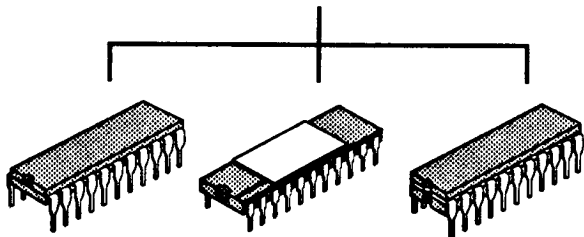
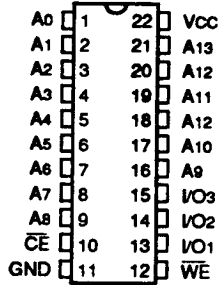
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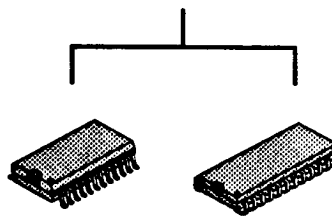
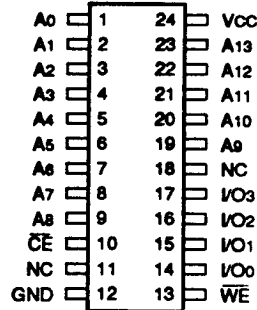
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L7C164 — ORDERING INFORMATION

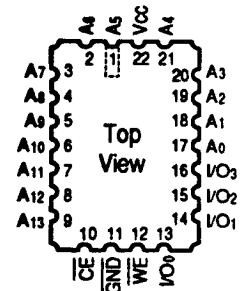
**22-pin
(0.3" wide)**



24-pin



**22-pin
(290 x 490)**



Speed	Plastic DIP (P8)	Sidebraze Hermetic DIP (D8)	CerDIP (C3)	Plastic SOIC (.300" - U1)	Plastic SOJ (.300" - W1)	Ceramic Leadless Chip Carrier (K4)
0°C to +70°C — COMMERCIAL SCREENING						
35 ns	L7C164PC35	L7C164DC35	L7C164CC35	L7C164UC35	L7C164WC35	L7C164KC35
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25	" " 25
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20	" " 20
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15	" " 15
12 ns	" " 12	" " 12	" " 12	" " 12	" " 12	" " 12
10 ns	" " 10	" " 10	" " 10	" " 10	" " 10	" " 10
8 ns	" " 8	" " 8	" " 8	" " 8	" " 8	" " 8
-55°C to +125°C — COMMERCIAL SCREENING						
35 ns		L7C164DM35	L7C164CM35			L7C164KM35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
-55°C to +125°C — EXTENDED SCREENING						
35 ns		L7C164DME35	L7C164CME35			L7C164KME35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
-55°C to +125°C — MIL-STD-883 COMPLIANT						
35 ns		L7C164DMB35	L7C164CMB35			L7C164KMB35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						



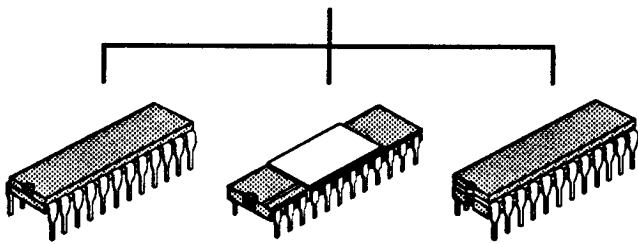
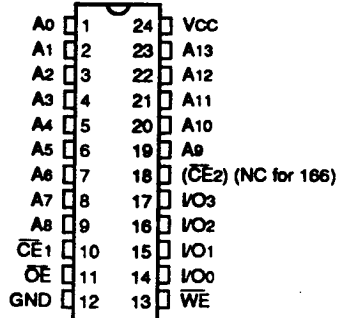
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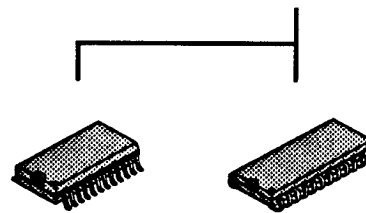
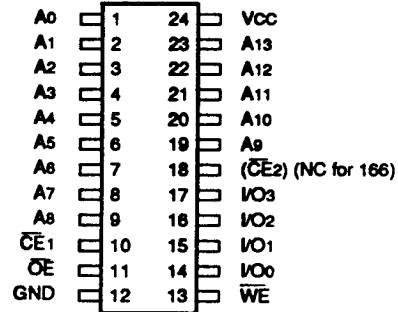
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L7C165/166 — ORDERING INFORMATION

**24-pin
(0.3" wide)**



24-pin



Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic SOIC (.300" - U1)	Plastic SOJ (.300" - W1)					
0°C to +70°C — COMMERCIAL SCREENING										
35 ns	L7C165PC or L7C166PC	L7C165DC or L7C166DC	L7C165CC or L7C166CC	L7C165UC or L7C166UC	L7C165WC or L7C166WC					
25 ns						35	25	35	25	35
20 ns						25	20	20	20	20
15 ns						20	15	15	15	15
12 ns						15	12	12	12	12
10 ns						12	10	10	10	10
8 ns	10	8	8	8	8					
-55°C to +125°C — COMMERCIAL SCREENING										
35 ns		L7C165DM or L7C166DM	L7C165CM or L7C166CM							
25 ns				35	35					
20 ns				25	25					
15 ns				20	20					
12 ns				15	15					
10 ns				12	12					
8 ns		10	10							
-55°C to +125°C — EXTENDED SCREENING										
35 ns		L7C165DME or L7C166DME	L7C165CME or L7C166CME							
25 ns				35	35					
20 ns				25	25					
15 ns				20	20					
12 ns				15	15					
10 ns				12	12					
8 ns		10	10							
-55°C to +125°C — MIL-STD-883 COMPLIANT										
35 ns		L7C165DMB or L7C166DMB	L7C165CMB or L7C166CMB							
25 ns				35	35					
20 ns				25	25					
15 ns				20	20					
12 ns				15	15					
10 ns				12	12					
8 ns		10	10							



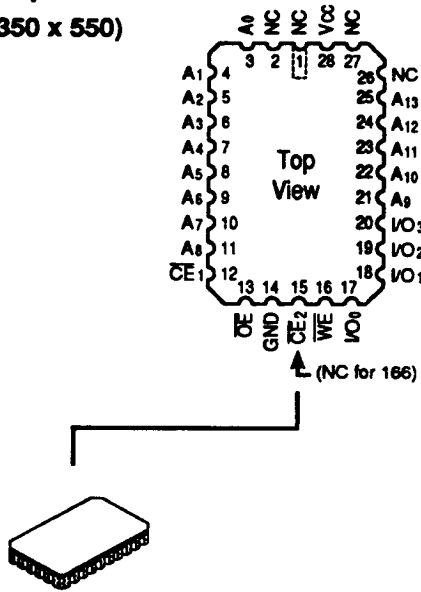
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L7C165/166 — ORDERING INFORMATION

28-pin
(350 x 550)



Speed	Ceramic Leadless Chip Carrier (K5)					
0°C to +70°C — COMMERCIAL SCREENING						
35 ns	L7C165KC or L7C166KC	35				
25 ns		25				
20 ns		20				
15 ns		15				
12 ns		12				
10 ns	10					
8 ns	8					
-55°C to +125°C — COMMERCIAL SCREENING						
35 ns	L7C165KM or L7C166KM	35				
25 ns		25				
20 ns		20				
15 ns		15				
12 ns		12				
10 ns	10					
8 ns						
-55°C to +125°C — EXTENDED SCREENING						
35 ns	L7C165KME or L7C166KME	35				
25 ns		25				
20 ns		20				
15 ns		15				
12 ns		12				
10 ns	10					
8 ns						
-55°C to +125°C — MIL-STD-883 COMPLIANT						
35 ns	L7C165KMB or L7C166KMB	35				
25 ns		25				
20 ns		20				
15 ns		15				
12 ns		12				
10 ns	10					
8 ns						