



DESCRIPTION

PT2258 is a 6-Channel Electronic Volume Controller IC utilizing CMOS Technology specially designed for the new generation of AV Multi-Channel Audio System. PT2258 provides an I²C Control Interface, an attenuation range of 0 to -79 dB at 1 dB/step, low noise, high channel separation. Housed in 20-pin, DIP or SO Package, PT2258's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

FEATURES

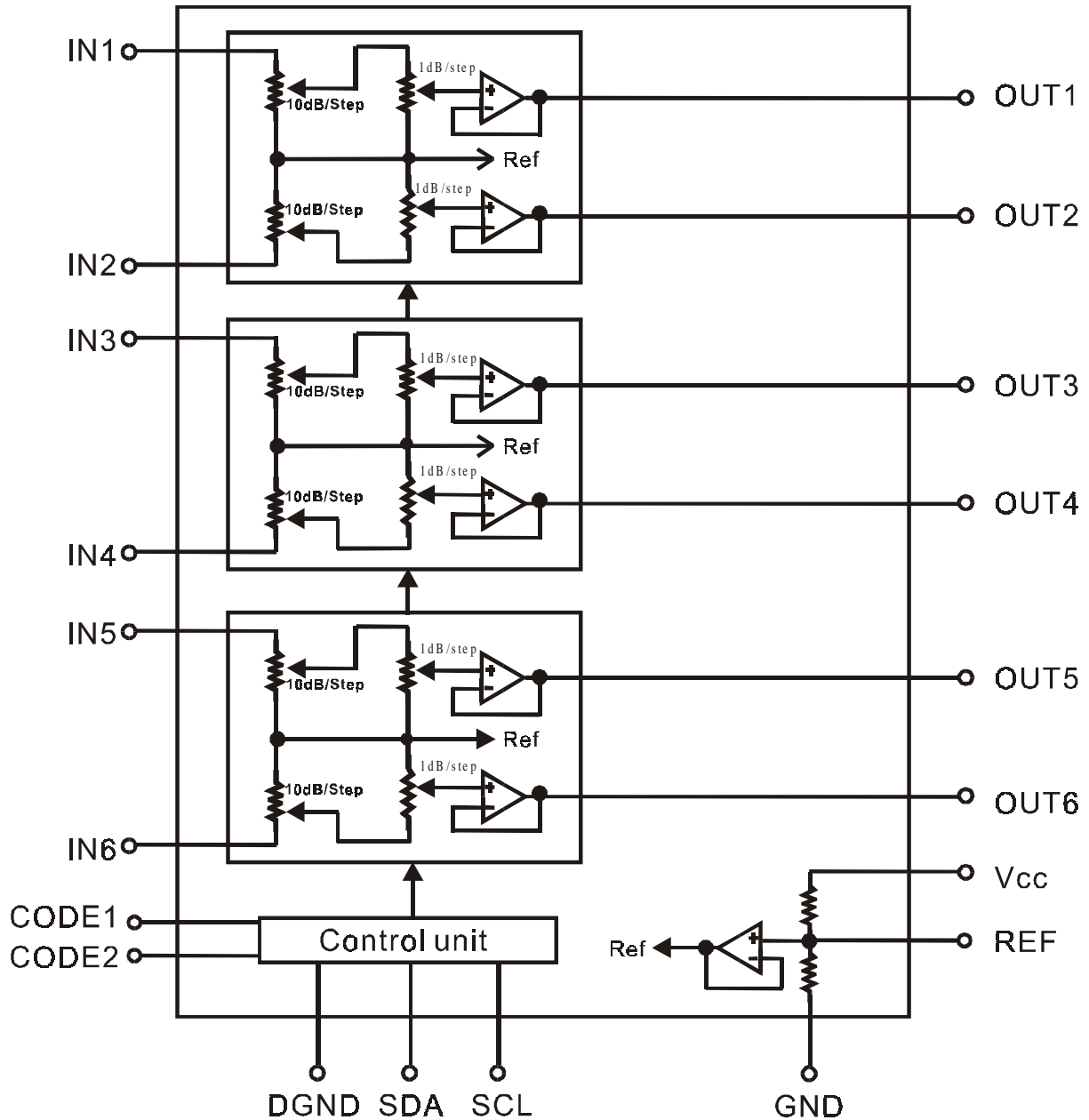
- CMOS Technology
- Low Power Consumption
- Least External Components
- Attenuation Range: 0 to -79 dB at 1dB/step
- Operating Voltage: 5 to 9 V
- Low Noise, S/N Ratio>100dB (A-weighting)
- High Channel Separation
- I²C Bus Control Interface
- Selectable Address
- 6-Channel Outputs
- Available in 20-pin, DIP or SO Package

APPLICATIONS

- AV Surround Audio Equipment
- Car Audio
- Mini Compo
- Computer Multi-Media Speaker
- Other Audio Equipments

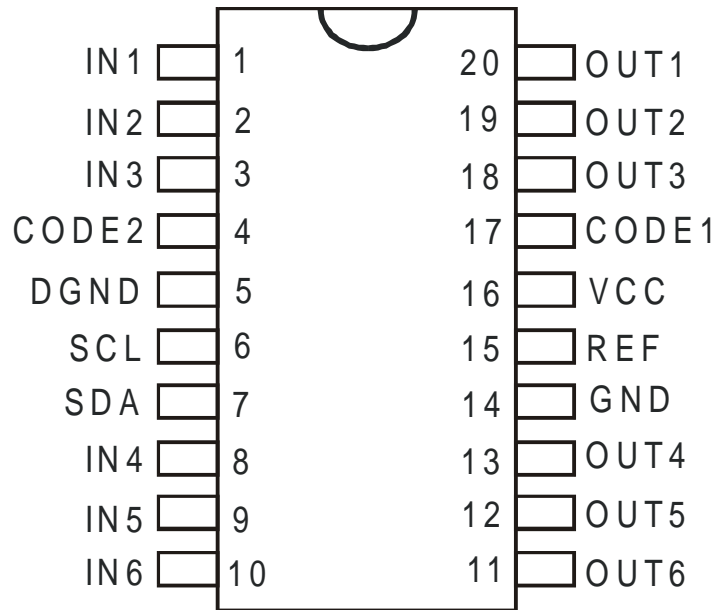


BLOCK DIAGRAM





PIN CONFIGURATION



PT2258



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
IN1	I	Channel Input No. 1. Connect a Capacitor to Audio Source	1
IN2	I	Channel Input No. 2 Connect a Capacitor to Audio Source	2
IN3	I	Channel Input No. 3 Connect a Capacitor to Audio Source	3
CODE2	-	Refer to Address Code Section	4
DGND	-	Digital Ground	5
SCL	I	I ² C Clock Input	6
SDA	I	I ² C Data Input	7
IN4	I	Channel Input No. 4 Connect a Capacitor to Audio Source	8
IN5	I	Channel Input No. 5 Connect a Capacitor to Audio Source	9
IN6	I	Channel Input No. 6 Connect a Capacitor to Audio Source	10
OUT6	O	Channel Output No. 6 Connect a Capacitor to the Next Stage	11
OUT5	O	Channel Output No. 5 Connect a Capacitor to the Next Stage	12
OUT4	O	Channel Output No. 4 Connect a Capacitor to the Next Stage	13
GND	-	Ground	14
REF	-	Reference Voltage= 1/2 Vcc Connect a Capacitor to the Ground	15
VCC	-	Power Supply Input	16
CODE1	-	Refer to the Address Code Section	17
OUT3	O	Channel Output No. 3 Connect a Capacitor to the Next Stage	18
OUT2	O	Channel Output No. 2 Connect a Capacitor to the Next Stage	19
OUT1	O	Channel Output No. 1 Connect a Capacitor to the Next Stage	20



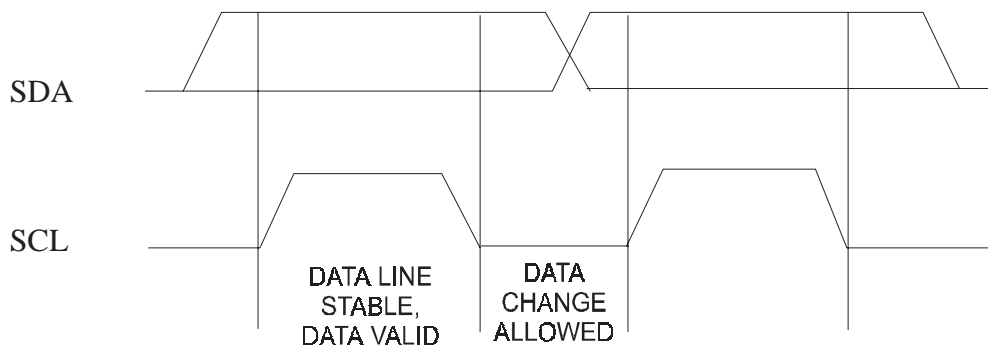
FUNCTIONAL DESCRIPTION

Bus Interface

Data are transmitted to and from the microprocessor to the PT2258 via the SDA and SCL. The SDA and SCL make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

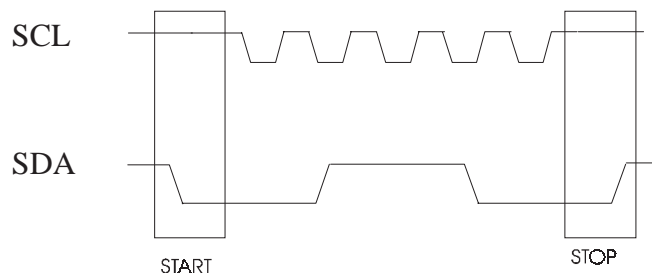
Data Validity

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW States of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.



Start and Stop Conditions

A Start Condition is activated when 1) the SCL is set to HIGH and 2) SDA shifts from HIGH to LOW State. The Stop Condition is activated when 1) SCL is set to HIGH and 2) SDA shifts from LOW to HIGH State. Please refer to the timing diagram below.



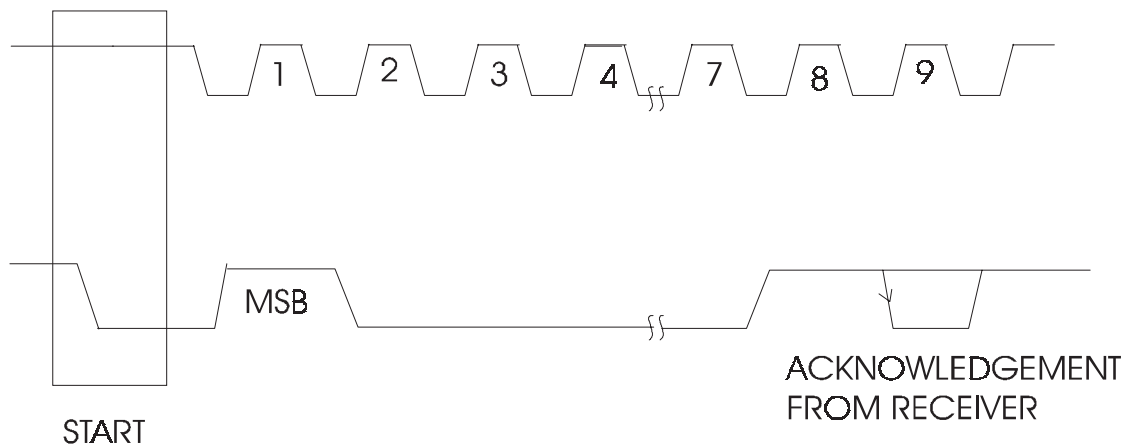


Byte Format

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

Acknowledge

During the Acknowledge Clock Pulse, the master (μ P) puts a resistive HIGH level on the SDA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge Clock Pulse so that the SDA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

Transmission without Acknowledge

If you want to avoid the acknowledge detection of the audio processor, a simpler μ P transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.



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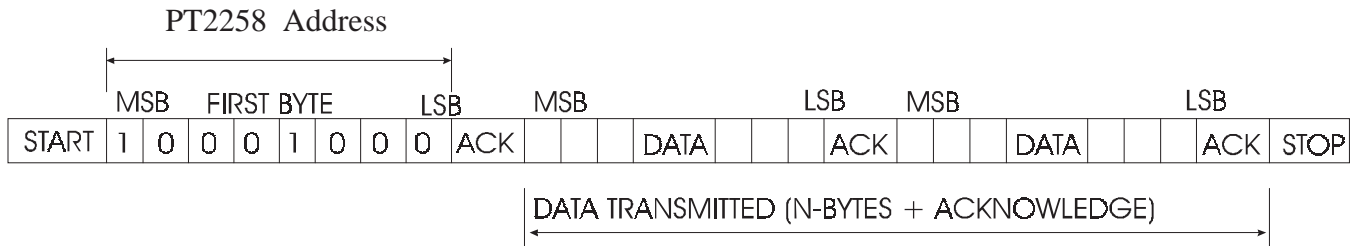
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Interface Protocol

The interface protocol consists of the following:

- A Start Condition
- A Chip Address Byte including the PT2258 address. The 8th Bit of the Byte must be “0”. PT2258 must always acknowledge the end of each transmitted byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition

Please refer to the diagram below:



Note: ACK = ACKNOWLEDGE
 MAX. CLOCK SPEED = 100KBITS/S

Software Specification

PT2258 ADDRESS CODE

PT2258 Address Code depends on the state of CODE1 (Pin No. 17) and CODE2 (Pin No.4). If CODE1 or CODE2 is connected to Vcc, then CODE1 or CODE2 is set to “1”. If CODE1 or CODE2 is connected to the Ground, it is set to “0”. Please refer to the information below:

Condition 1: When CODE1=“1” and CODE2=“1”:

CODE1	CODE2
1	1

Then, the PT2258 Address Code is (8CH):

1	0	0	0	1	1	0	0
MSB							LSB



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Condition 2: When CODE1="1" and CODE2="0":

CODE1	CODE2
1	0

Then, the PT2258 Address Code is (88H):

1	0	0	0	1	0	0	0
MSB							LSB

Condition 3: When CODE1="0" and CODE2="1":

CODE1	CODE2
0	1

Then, the PT2258 Address Code is (84H):

1	0	0	0	0	1	0	0
MSB							LSB

Condition 4: When CODE1="0" and CODE2="0":

CODE1	CODE2
0	0

Then, the PT2258 Address Code is (80H):

1	0	0	0	0	0	0	0
MSB							LSB



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Data Bytes Description

FUNCTION BITS

MSB							LSB	FUNCTION
1	1	1	0	A3	A2	A1	A0	6-Channel, -1dB/step
1	1	0	1	0	B2	B1	B0	6-Channel, -10dB/step
0	0	0	1	A3	A2	A1	A0	Channel No. 3, -1dB/step
0	0	0	0	0	B2	B1	B0	Channel No. 3, -10dB/step
0	0	1	1	A3	A2	A1	A0	Channel No. 4, -1dB/step
0	0	1	0	0	B2	B1	B0	Channel No. 4, -10dB/step
0	1	0	1	A3	A2	A1	A0	Channel No. 2, -1dB/step
0	1	0	0	0	B2	B1	B0	Channel No. 2, -10dB/step
0	1	1	1	A3	A2	A1	A0	Channel No. 5, -1dB/step
0	1	1	0	0	B2	B1	B0	Channel No. 5, -10dB/step
1	0	0	1	A3	A2	A1	A0	Channel No. 1, -1dB/step
1	0	0	0	0	B2	B1	B0	Channel No. 1, -10dB/step
1	0	1	1	A3	A2	A1	A0	Channel No. 6, -1dB/step
1	0	1	0	0	B2	B1	B0	Channel No. 6, -10dB/step
1	1	1	1	1	0	0	M	6-Channel, MUTE When M=1, MUTE=ON When M=0, MUTE=OFF



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ATTENUATION UNIT BIT

A3/---	A2/B2	A1/B1	A0/B0	ATTENUATION VALUE (dB)
0	0	0	0	0/0
0	0	0	1	-1/-10
0	0	1	0	-2/-20
0	0	1	1	-3/-30
0	1	0	0	-4/-40
0	1	0	1	-5/-50
0	1	1	0	-6/-60
0	1	1	1	-7/-70
1	0	0	0	-8/---
1	0	0	1	-9/---

where: Ax=-1dB/step, Bx=-10dB/step

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
Vs	Supply Voltage	12	V
Tamb	Ambient Temperature	-20 to +75	°C
Tstg	Storage Temperature	-40 to +125	°C



ELECTRICAL CHARACTERISTICS

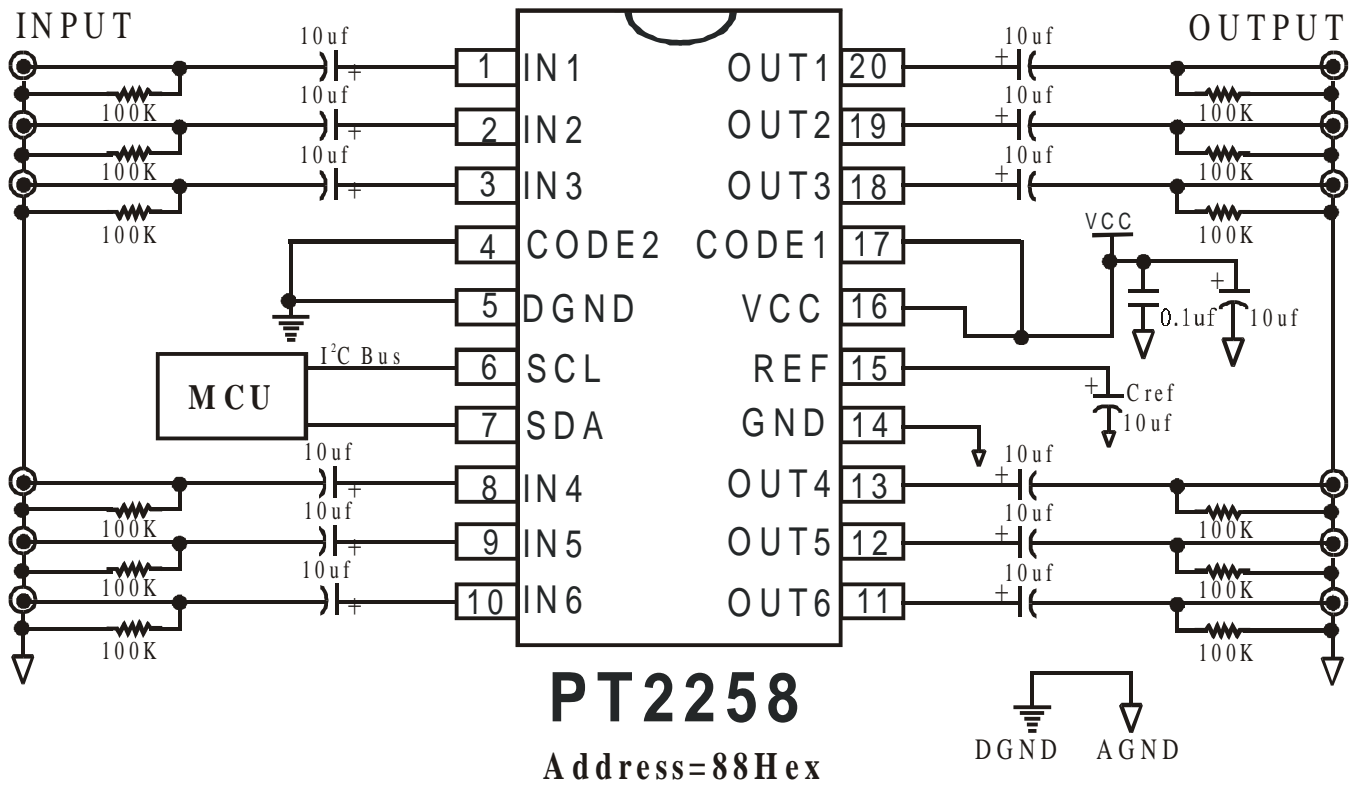
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply Voltage		5	9	10	V
Is	Supply Current			8		mA
RIN	Input Impedance	FL,FR,CTR SUB,SL,SR	27	30	35	KΩ
VCL	Maximum Input Voltage	Volume=0dB THD=1%		2.8	3.0	Vrms
Sc	Channel Separation		90	100	110	dB
CRANGE	Volume Control Range			79		dB
AVMAX	Maximum Attenuation			-79		dB
Astep	Attenuation Step			1		dB
EA	Attenuation Error	Volume=0~-50dB	-1.0	0	+1.0	dB
AMUTE	Mute Attenuation	A-weighting	90	95	98	dB
THD	Total Harmonic Distortion	Volume=0dB Input,200mVrms	0.003	0.005	0.01	%
Noise	Output Noise	A-weighting		3	5	μV
S/N	Signal-to-Noise Ratio	0dB=1Vrms A-weighting	100	105	110	dB
Ro	Output Impedance			600	900	Ω
Go	Output Gain		-0.5	0	+0.5	dB
Vomax	Maximum Output	FL,FR,CENTER SUB,SL,SR THD=1%	2.3	2.6	2.9	Vrms

I²C BUS SECTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIL	Bus Low Input Level			2.4	2.5	V
VIH	Bus High Input Level		2.8	3.0		V
TINIT	Bus Initialization	Cref=10μF		250	300	mS



APPLICATION CIRCUIT



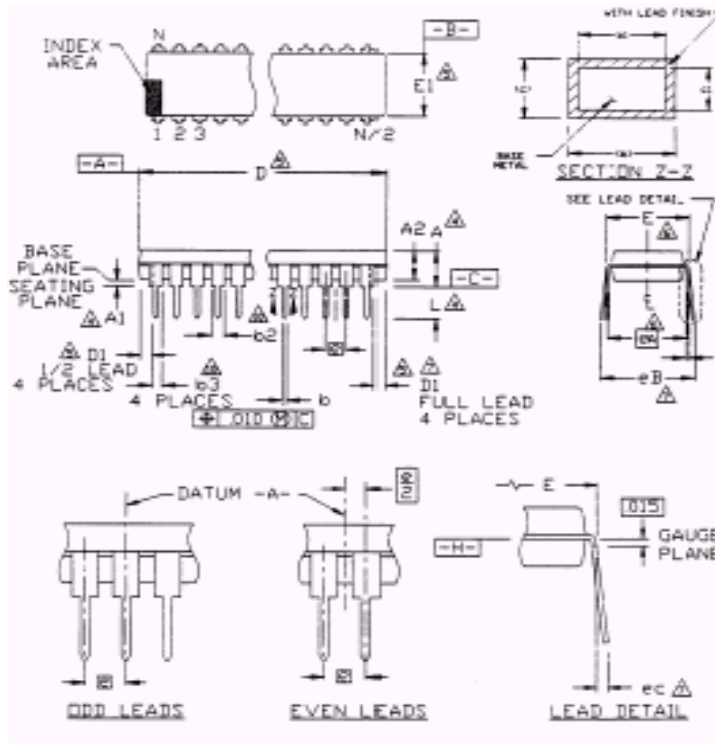
ORDER INFORMATION

Valid Part Number	Package Type
PT2258	20 Pins, DIP Package (300 mil)
PT2258-S	20 Pins, SO Package (300 mil)



PACKAGE INFORMATION

20-Pin, DIP Package (300 mil)



Symbols	Dimensions in Inches		
	Min.	Nom.	Max.
A			0.210
A1	0.015		
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.980	1.030	1.060
D1	0.005		
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e		0.100 bsc	
eA		0.300 bsc.	
eB			0.430
eC	0.000		0.060
L	0.115	0.130	0.150



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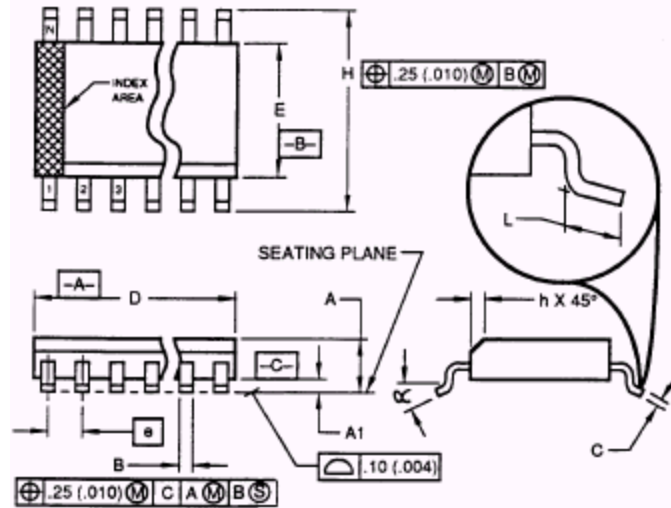
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- Notes:
1. All dimensions are in INCHES.
 2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
 3. Dimension "A", "A1" and "L" are measured with the package seated in JEDEC Seating Plane Gauge GS-3
 4. "D", "D1" and "E1" dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
 5. "E" and "eA" measured with the leads constrained to be perpendicular to datum -C-.
 6. "eB" and "eC" are measured at the lead tips with the leads unconstrained.
 7. N is the number of terminal positions (N=20)
 8. Pointed or rounded lead tips are preferred to ease insertion.
 9. "b2" and "b3" maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
 10. Distance between leads including Dambar protrusions to be 0.005 inch minimum.
 11. Datum plane -H- coincident with the bottom of lead, where lead exits body.
 12. Refer to JEDEC MS-001, Variation AD.



20-Pin, SO Package (300 mil)



Symbols	Dimensions in Millimeter		
	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	12.60		13.00
E	7.40		7.60
e		1.27 bsc.	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°

- Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
 3. Dimension "E" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
 4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
 5. "L" is the length of the terminal for soldering to a substrate.
 6. "N" is the number of terminal positions. (N=20)
 7. The lead width "B" as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
 8. Controlling dimension: MILLIMETER.
 9. Refer to JEDEC MS-013 Variation AC