MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

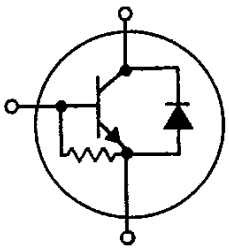
MJ12005D

Designers Data Sheet

NPN HORIZONTAL DEFLECTION TRANSISTOR WITH INTEGRATED DAMPER DIODE

. . . specifically designed for use in large-screen color-deflection circuits.

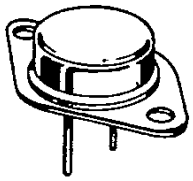
- Collector-Emitter Voltage — V_{CEX} = 1500 Vdc
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 20 A, 400 V
- Switching Times with Inductive Loads — t_f = 0.4 μs (Typ) @ I_C = 5.0 A
- C-E Diode Forward Voltage Specified

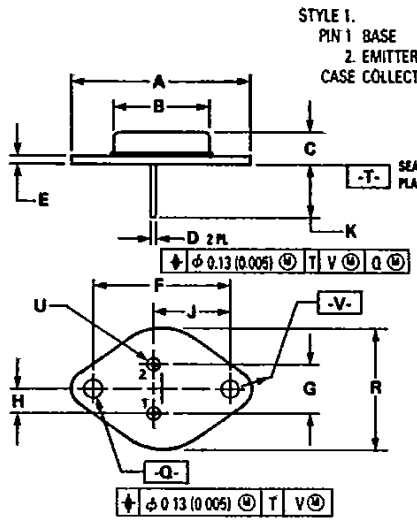


8.0 AMPERE

NPN SILICON POWER TRANSISTORS

1500 VOLTS
100 WATTS





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA
(TO-3)

MAXIMUM RATINGS

Rating	Symbol	MJ12005D	Unit
Collector-Emitter Voltage	V_{CEO}	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Emitter Current — Continuous	I_E	12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	100 40 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

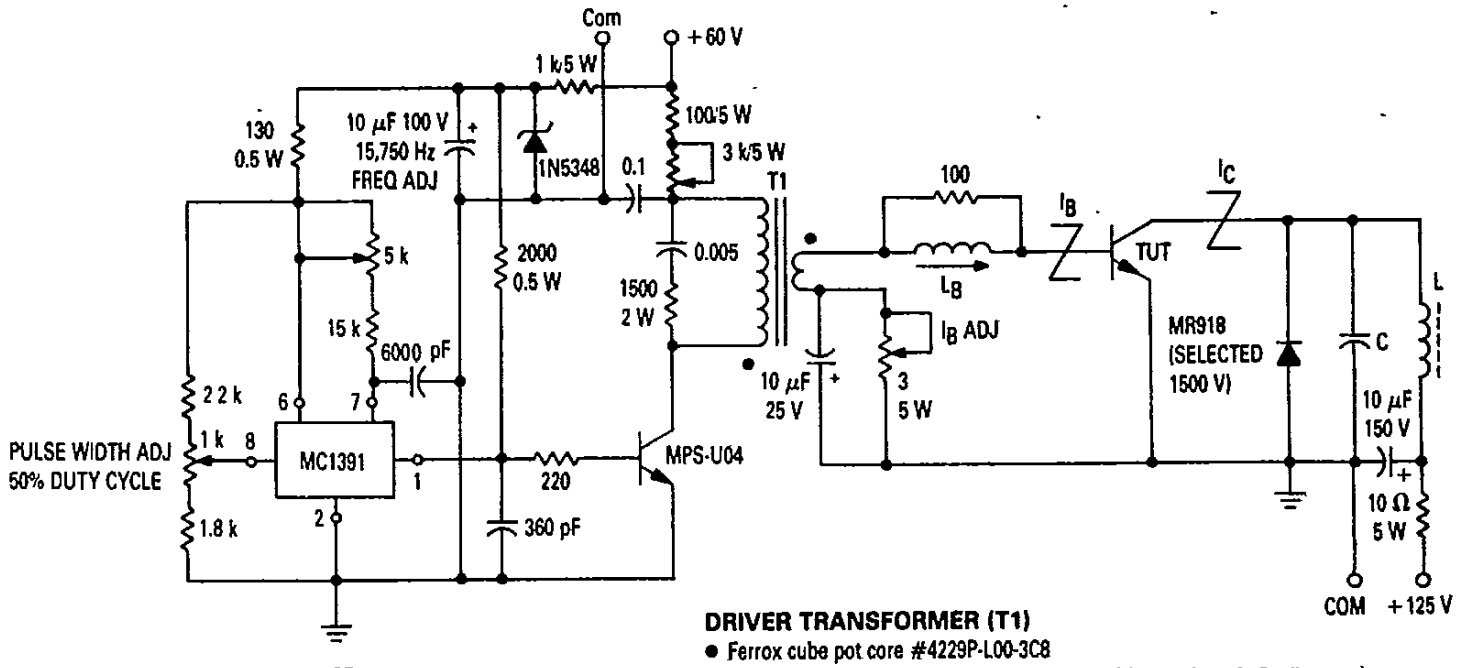
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves—representing boundaries on device characteristics—are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	—	—	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	—	—	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	—	200	mAdc
ON CHARACTERISTICS (1)					
Diode Forward Voltage (I_F = 8.0 Amps)	$V_{F(VEC)}$	—	—	2.5	Vdc
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 2.5 Adc)	$V_{CE(sat)}$	— —	— —	5.0 5.0	Vdc
Base Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 2.5 Adc)	$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	—	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	150	—	pF
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 5.0 Adc, I_{B1} = 1.5 Adc, L_B = 8.0 μH, See Figure 1) T_C = 25°C T_C = 100°C	t_f	— —	0.4 0.6	1.0 —	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

FIGURE 1 — SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
5.0	0.57	0.018
7.0	0.45	0.025

DRIVER TRANSFORMER (T1)

- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance Lp = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when I_{B1} h_{FE} = I_{CM}, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the I_{B1} h_{FE} = I_{CM} point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation I_{B1} h_{FE} = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

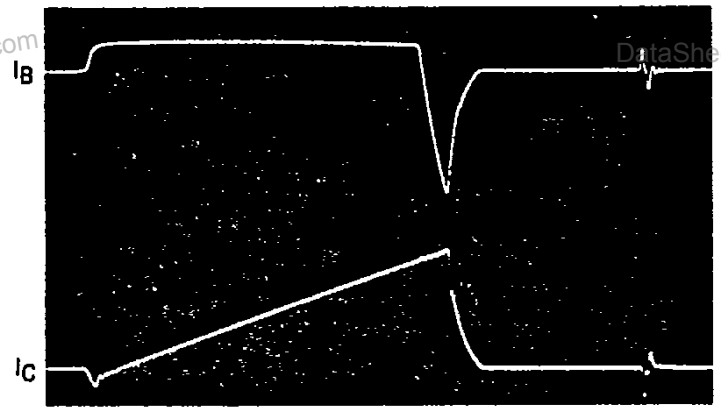
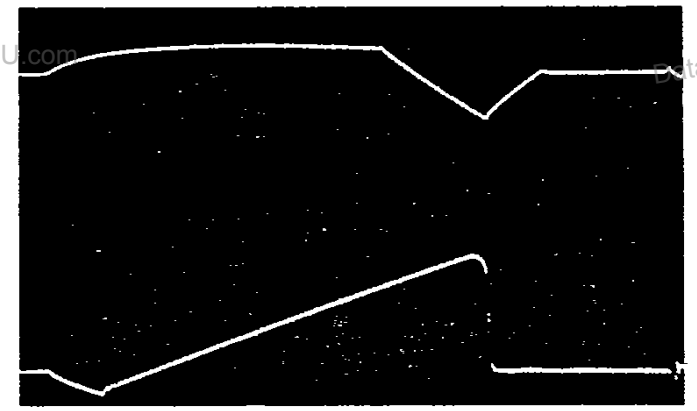


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 — OPTIMIZING DRIVE @ 5.0 A

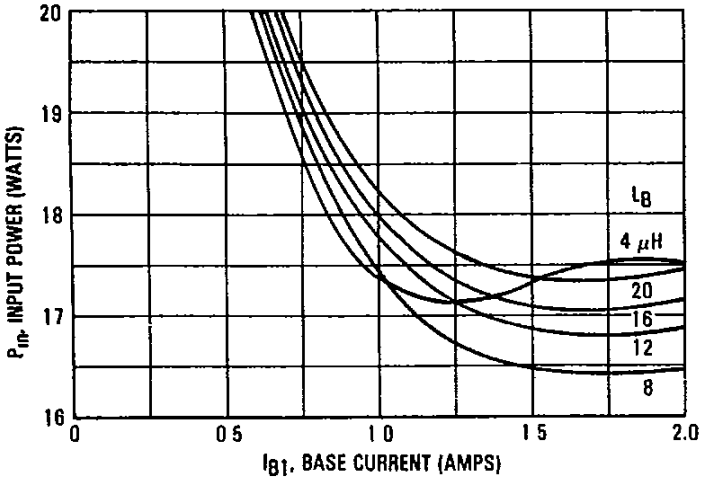


FIGURE 5 — OPTIMIZING DRIVE @ 7.0 A

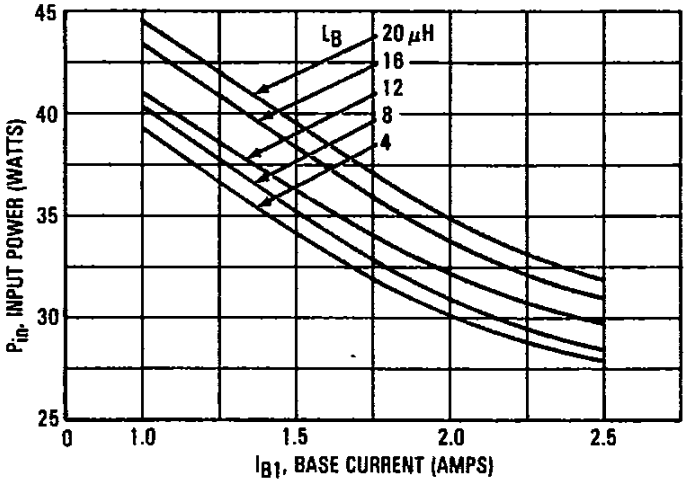


FIGURE 6 — SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 5.0 A, I_B = 1.5 A, L_B = 8.0 μH

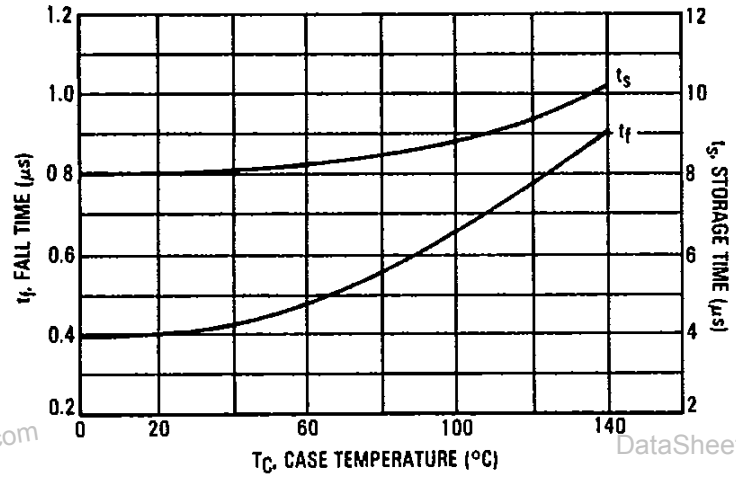


FIGURE 7 — SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 7.0 A, I_B = 2.0 A, L_B = 4.0 μH

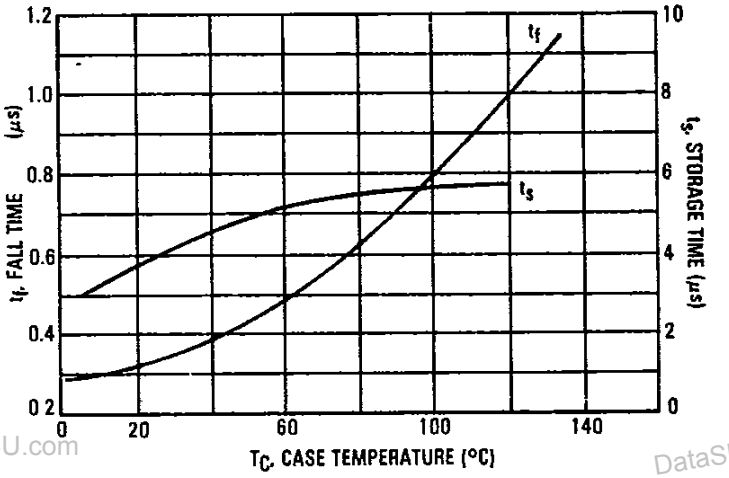


FIGURE 8 — OPTIMUM DRIVE CONDITIONS

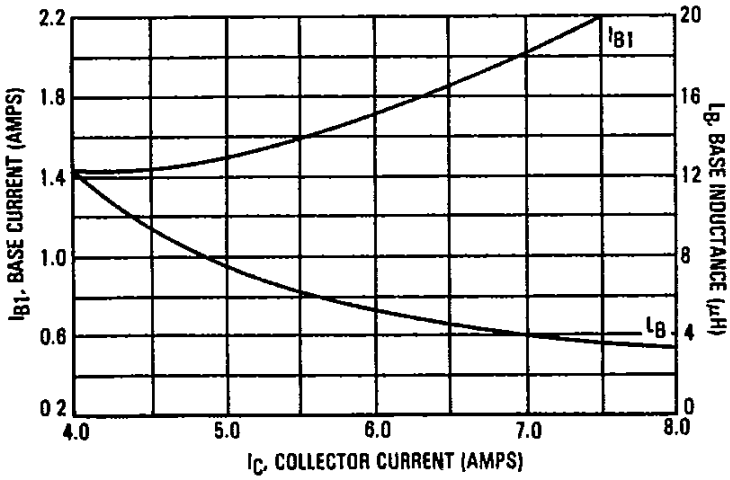


FIGURE 9 — SWITCHING BEHAVIOR versus I_{CM} AT 25°C

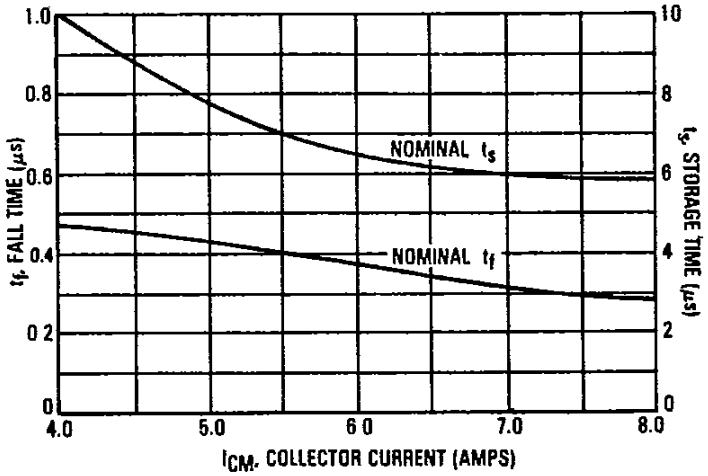


FIGURE 10 — THERMAL RESPONSE

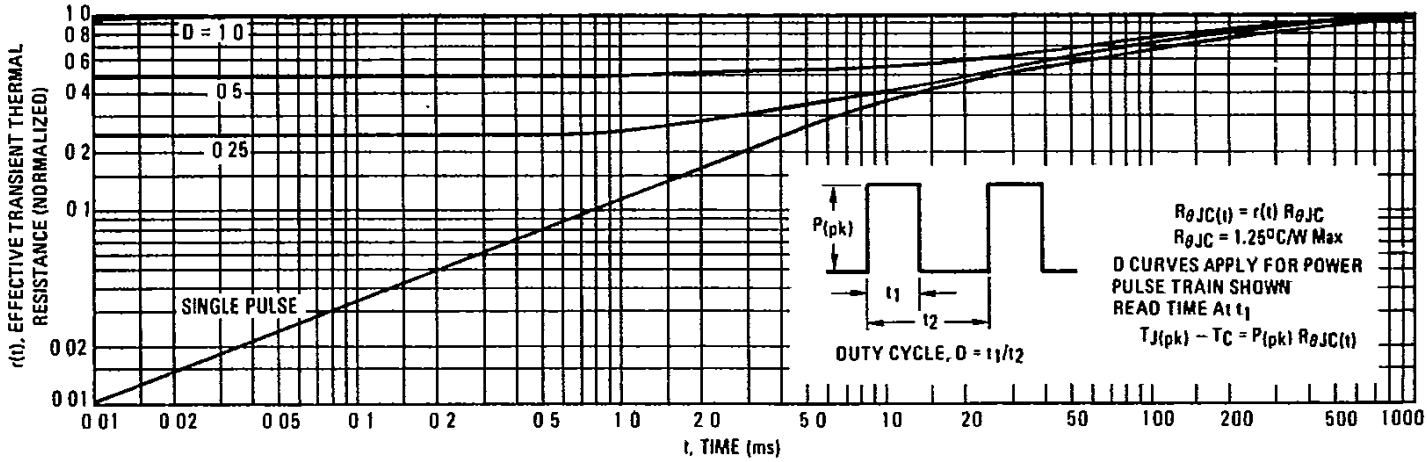


FIGURE 11 — COLLECTOR SATURATION REGION

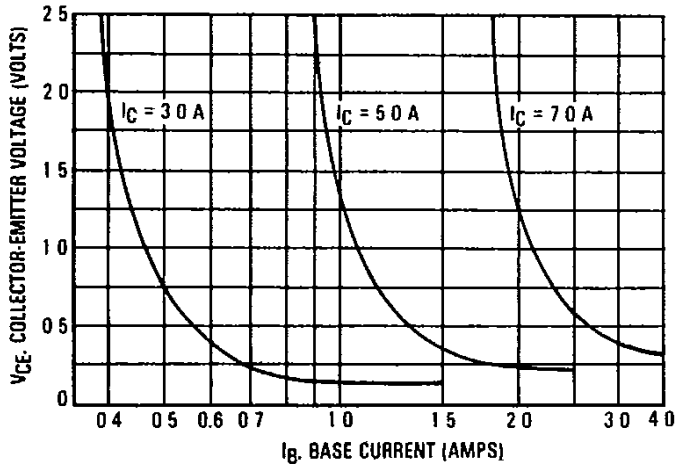


FIGURE 12 — DC CURRENT GAIN versus COLLECTOR CURRENT

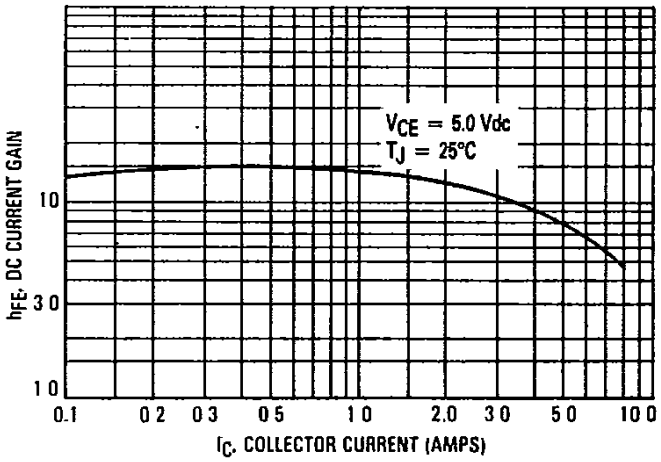


FIGURE 13 — "ON" VOLTAGES

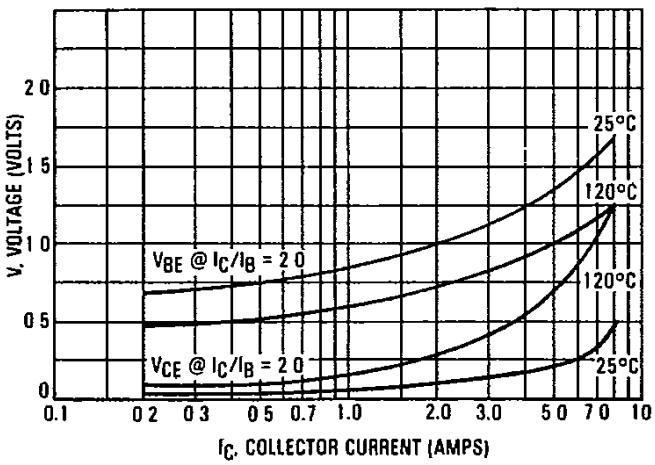
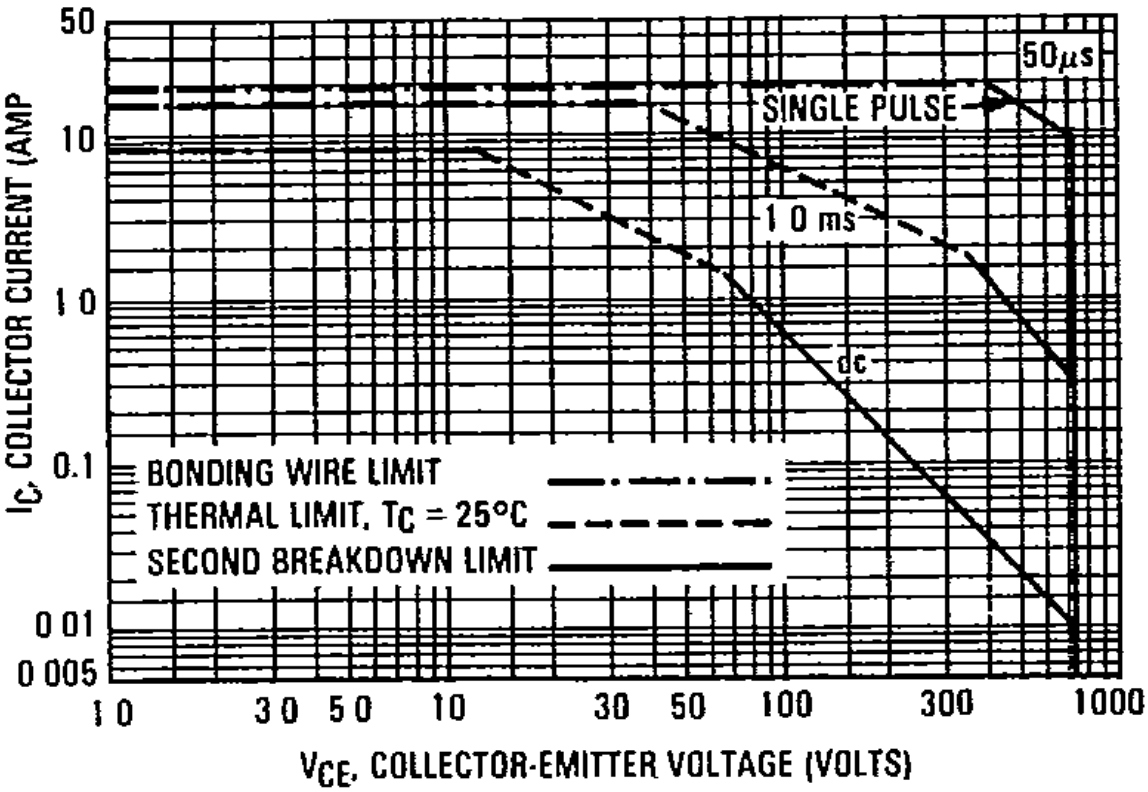


FIGURE 14 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA



NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without falling.