

MB86961/MB86961A



UNIVERSAL INTERFACE FOR 10BASE-T (TWISTED-PAIR) ETHERNET

DATASHEET

JANUARY 1995
Revised 3/97

Note: All descriptions apply to both MB86961 and MB86961A unless otherwise noted.

FEATURES

- Combines Manchester encoder/decoder and twisted pair transceiver functions
- Full-duplex capability (MB86961A only)
- Direct interface to all popular Ethernet controllers
- Direct interface to AUI and 10BASE-T outputs
- Manual or automatic AUI /10BASE-T selection
- Integrated pulse shaper and Tx/Rx filters
- Selectable 100Ω/150Ω termination permits operation with shielded or unshielded twisted pair cable
- Reverse-polarity detection for receiver with automatic correction
- On-chip jabber logic, SQE test and link test with enable/disable option
- Remote signaling of link down and jabber conditions
- Programmable receive threshold for extended range
- Power down mode for minimum power dissipation
- Output drivers for receive, transmit, collision and link test pass LED indicators
- Low power CMOS technology, single 5 volt power supply
- TP loopback disable for external loopback testing (MB86961A only)
- 44-pin PLCC and 48-pin PQFP packages

Additional features in MB86961A only

- Automatic shut-down of unused port to reduce power consumption
- TP external loopback enable for testing

GENERAL DESCRIPTION

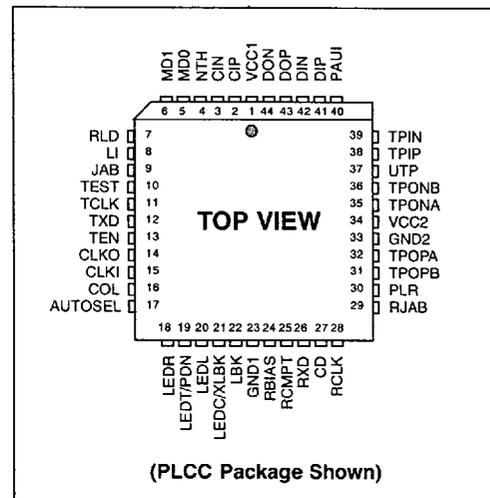
The MB86961(A) Universal Interface for 10BASE-T (Twisted-Pair) Ethernet is fully compliant with the IEEE 802.3 specifications for AUI (Attachment Unit Interface) and 10BASE-T (Twisted-Pair) interfaces and provides the electrical interface between an Ethernet controller and the

DB15 (AUI) and RJ45 (10BASE-T) connections to an Ethernet local area network. Functions provided by the MB86961(A) include Manchester encoding and decoding of the serial data stream, level conversion, collision detection, signal quality error (SQE) and link integrity testing, jabber control, loopback, and automatic correction of polarity reversal on the twisted-pair input.

Pulse shaping and filtering functions are performed by the MB86961(A) to eliminate the need for external filtering components and thus reduce overall system cost. The device also provides outputs for receive, transmit, collision and link test LEDs and provides compatibility with both shielded and unshielded twisted pair cables. The receive threshold can be reduced to allow an extended range between nodes in low noise environments. Its wide range of features and its ability to interface to virtually all popular controllers make the MB86961(A) the ideal device for twisted pair Ethernet applications.

The MB86961(A) is part of a complete family of Ethernet devices available from Fujitsu. It is fabricated in a low-power CMOS technology and is supplied in a 44-pin PLCC and 48-pin PQFP packages.

PIN CONFIGURATION



PIN ASSIGNMENT - 44-PIN PLCC

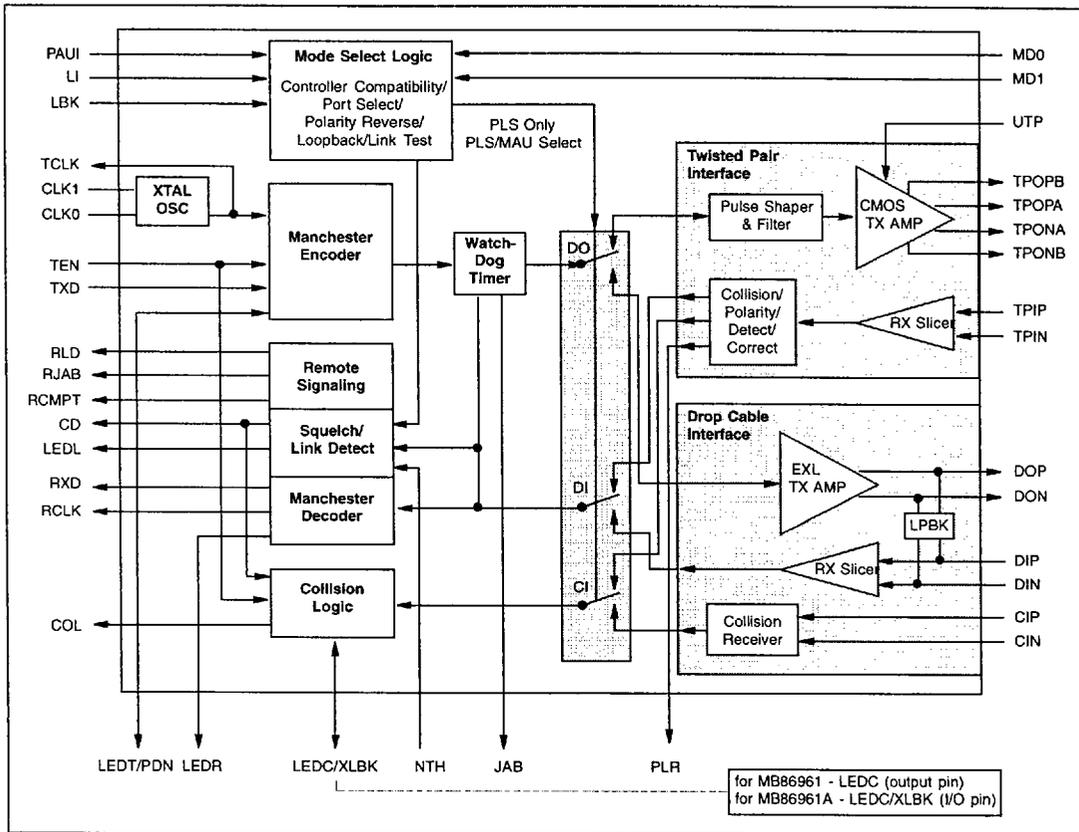
PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	VCC1	—	12	TXD	I	23	GND1	—	34	VCC2	—
2	CIP	I	13	TEN	I	24	RBIAS	I	35	TPONA	O
3	CIN	I	14	CLKO	O	25	RCMPT	O	36	TPONB	O
4	NTH	I	15	CLKI	I	26	RXD	O	37	UTP	I
5	MD0	I	16	COL	O	27	CD	O	38	TPIP	I
6	MD1	I	17	AUTOSEL	I	28	RCLK	O	39	TPIN	I
7	RLD	O	18	LEDR	O	29	RJAB	O	40	PAUI	I
8	LI	I	19	LEDT/PDN	I/O	30	PLR	O	41	DIP	I
9	JAB	O	20	LEDL	I/O	31	TPOPB	O	42	DIN	I
10	TEST	I	21	LEDC/XLBK	I/O	32	TPOPA	O	43	DOP	O
11	TCLK	O	22	LBK	I	33	GND2	—	44	DON	O

PIN ASSIGNMENT - 48-PIN PQFP

PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	PAUI	I	13	RLD	O	25	LEDR	O	37	RJAB	O
2	DIP	I	14	LI	I	26	LEDT/PDN	I/O	38	PLR	O
3	DIN	I	15	JAB	O	27	LEDL	I/O	39	TPOPB	O
4	DOP	O	16	TEST	I	28	LEDC/XLBK	I/O	40	TPOPA	O
5	DON	O	17	TCLK	O	29	LBK	I	41	GND	—
6	NC	—	18	TXD	I	30	GND	—	42	VCC	—
7	VCC	—	19	VCC	—	31	NC	—	43	VCC	—
8	CIP	I	20	TEN	I	32	RBIAS	I	44	TPONA	O
9	CIN	I	21	CLKO	I	33	RCMPT	O	45	TPONB	O
10	NTH	I	22	CLK1	O	34	RXD	O	46	UTP	I
11	MD0	I	23	COL	O	35	CD	O	47	TPIP	I
12	MD1	I	24	AUTOSEL	I	36	RCLK	O	48	TPIN	I

ORDERING CODE

PACKAGE STYLE	PACKAGE CODE	V _{CC} = +V ± 5%
44-Pin Plastic Leaded Chip Carrier	LCC-44P-M02	MB86961(A)PD-G
48-Pin Plastic Quad Flat Package	FPT-48P-M02	MN86961(A)PF-G



SIGNAL DESCRIPTIONS

Symbol	Type	Description
AUTOSEL	I	AUTOMATIC PORT SELECT: When AUTOSEL=1, automatic port selection is enabled (the MB86981(A) defaults to the AUI port only if TP link integrity=Fail). When AUTOSEL=0, manual port selection is enabled (the PAUI pin determines the active port).
CD	O	CARRIER DETECT: An output to notify the controller of activity on the network.
CIP CIN	I I	AUI COLLISION PAIR: Differential input pair connected to the AUI transceiver CI circuit. The input is collision signaling or SQE.
CLKO CLKI	O I	CRYSTAL OSCILLATOR: A 20MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI.
COL	O	COLLISION DETECT: Output which drives the collision detect input of the controller.
DIP DIN	I I	AUI RECEIVE PAIR: Differential input pair from the AUI transceiver DI circuit. The input is Manchester encoded.
DOP DON	O O	AUI TRANSMIT PAIR: A differential output driver pair for the AUI transceiver cable. The output is Manchester encoded.
JAB	O	JABBER INDICATION: Output goes high to indicate Jabber state.
LBK	I	LOOPBACK: When LBK=1, forced loopback is enabled. When LBK=0, normal loopback is enabled.
LEDC/XLBK	O	COLLISION LED: Open drain driver for the collision indicator. Output is pulled low during collision. For MB86961A only, if externally tied low, the MB86961A only disables the internal TP loopback and collision detection circuits in anticipation of external TP loopback or full-duplex operation. MB86961A is ready for loopback testing 16 ms after this pin goes low. No delay is needed when the pin goes high.
LEDL	I/O	LINK LED: Open drain driver for link integrity indicator. Output pulled low during link test pass. If externally tied low, internal circuitry is forced to "Link Pass" state and the MB86961 (A) will continue to transmit link test pulses.
LEDR	O	RECEIVE LED: Open drain driver for the receive indicator LED. Output is pulled low during receive.
LEDT/ PDN	O I	TRANSMIT LED/POWER DOWN: Open drain driver for the transmit indicator. Output is pulled low during transmit. If externally tied low, the MB86961 (A) goes to power down state.
LI	I	LINK TEST ENABLE: When LI=0, the Link Integrity Test function is disabled. When LI=1, the Link Integrity Test function is enabled.
MDO MD1	I I	MODE SELECT: Mode select pins which determine controller compatibility mode. See Table 1.
NTH	I	NORMAL THRESHOLD: When NTH=1, the normal TP squelch threshold is in effect. When NTH=0, the normal TP squelch threshold is reduced by 4.5 dB.
PAUI	I	PORT/AUI SELECT: In Manual Port Select mode (AUTOSEL=0), PAUI selects the active port. When PAUI=1, the AUI port is selected, When PAUI=0, the TP port is selected. In Auto Port Select mode, PAUI is ignored.
PLR	O	POLARITY REVERSE: Output goes high to indicate reversed polarity.
RBIAS	I	BIAS CONTROL: A bias resistor at this pin controls the bias of the operating circuit.
RCLK	O	RECEIVE CLOCK: A recovered 10 MHz clock which is synchronous with the received data and connected to the controller receive clock input.

SIGNAL DESCRIPTIONS (Continued)

Symbol	Type	Description
RCMPT	O	REMOTE COMPATIBILITY: Output goes high to signal the controller that the remote port is compatible with the MB86961 (A) remote signaling features.
RJAB	O	REMOTE JABBER: Output goes high to signal the controller that the remote port is in Jabber condition.
RLD	O	REMOTE LINK DOWN: Output goes high to signal to the controller that the remote port is in link down condition.
RXD	O	RECEIVE DATA: Output signal connected directly to the receive data input of the controller.
TCLK	O	TRANSMIT CLOCK: A 10 MHz clock output. This clock signal is directly connected to the transmit clock input of the controller.
TEN	I	TRANSMIT ENABLE: Enables data transmission and starts the watchdog timer. Synchronous with TCLK (see Figures 14, 20, 26, and 32 for details).
TEST	I	TEST: Input for factory test of the device. Leave open for normal operation.
TPIP TPIN	O O	RECEIVE TWISTED-PAIR: A differential input pair from the twisted-pair cable. Receive filter is integrated in-chip. No external filters are required.
TPOPA/B TPONA/B	O O	TRANSMIT TWISTED PAIR: Two differential driver pair outputs (A and B) to the twisted-pair cable. The output is pre-equalized, no external filter is required. Two pairs are used to provide compatibility with both 10 Ω load cable and 150 Ω load cable.
TXD	I	TRANSMIT DATA: Input signal containing NRZ data to be transmitted on the network. TXD is connected directly to the transmit data output of the controller.
UTP	I	UTP/STP: When UTP=0, 150 Ω termination for shielded TP is selected. When UTP=1, 100 Ω termination for unshielded TP is selected.
VCC1, VCC2	—	POWER INPUTS: +5V power supply inputs.
GND1 GND2	— —	GROUND RETURNS 1 & 2: Grounds

APPLICATIONS

Figure 1 shows the MB86961 (A) in a typical application, interfacing between a controller and the RJ45 connector of the twisted-pair network. Figures 2 through 5 show detailed diagrams of various MB86961 (A) applications.

AUTO PORT SELECT LOOPBACK CONTROL PIN

With MD0 and MD1 both tied high, the MB86961 (A) logic and framing are set to Mode 4 (compatible with National NS8390 controllers).

The AUTOSEL pin is tied high, allowing the MB86961 (A) to automatically select the active port. The high at LI enables Link Testing.

The UTP and NTH pins are both tied high selecting the standard receiver threshold and 100Ω termination for unshielded TP cable. (See Figure 2.)

MANUAL PORT SELECT LINK TEST FUNCTION

With MD0 low and MD1 tied high, the MB86961 (A) logic and framing are set to Mode 3 (compatible with Fujitsu MB86950 an MB86960 controllers). As in Figure 2, the LI pin is tied high, enabling Link Testing, and the UTP and NTH pins are both tied high, selecting the standard receiver threshold and 100 Ω termination for unshielded TP cable. However, in this application AUTO-

SEL is tied low, allowing external port selection through the PAUI pin. The remote status output are inverted and used to drive LED indicators. (See Figure 3.)

TWISTED-PAIR ONLY

Figure 4 shows the MB86961 (A) is a typical twisted-pair only application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ45 connector. (The AUI port is not used.) With MD0 tied high and MD1 grounded, the MB86961(A) logic and framing are set to Mode 2 (compatible with Intel 82586 controllers). The LI pin externally controls the link test function. The UTP and NTH pins are both tied high, selecting the reduced receiver threshold and 150Ω termination for shielded TP cable. The switch at LEDT/PDN manually controls the power down mode. (See Figure 4.)

AUI ENCODER/DECODER ONLY

In this application, the DTE is connected to the coaxial network through the AUI. AUTOSEL and PAUI are both tied to ground, manually selecting the AUI port. The twisted-pair port is not used. With MD1 and MD0 both grounded, the MB86961 (A) logic and framing are set to Mode 1 (compatible with AMD AM7990 controllers). The LI pin is tied low, disabling the link test function. The LBK input controls loopback. A 20 MHz crystal connected across CLKI and CLK0 provides the required clock signal. (See Figure 5.)

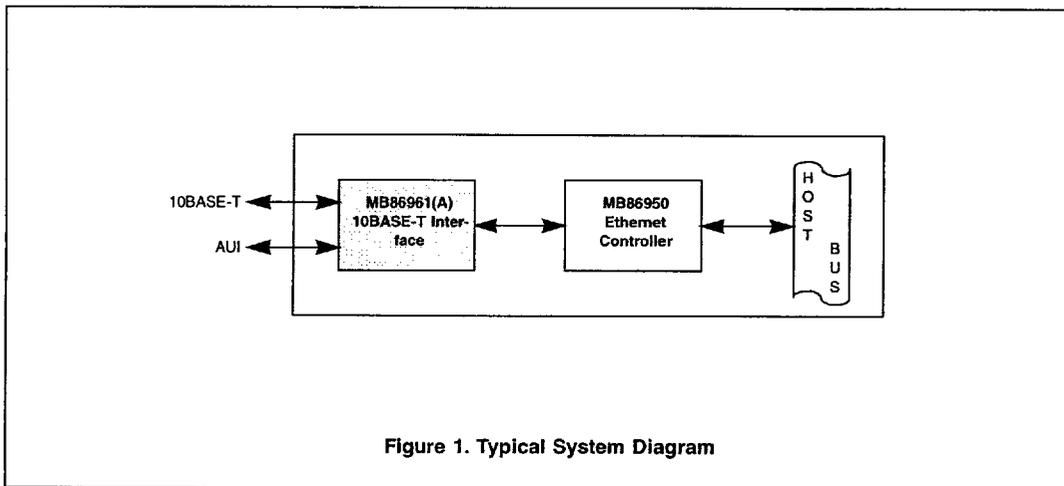
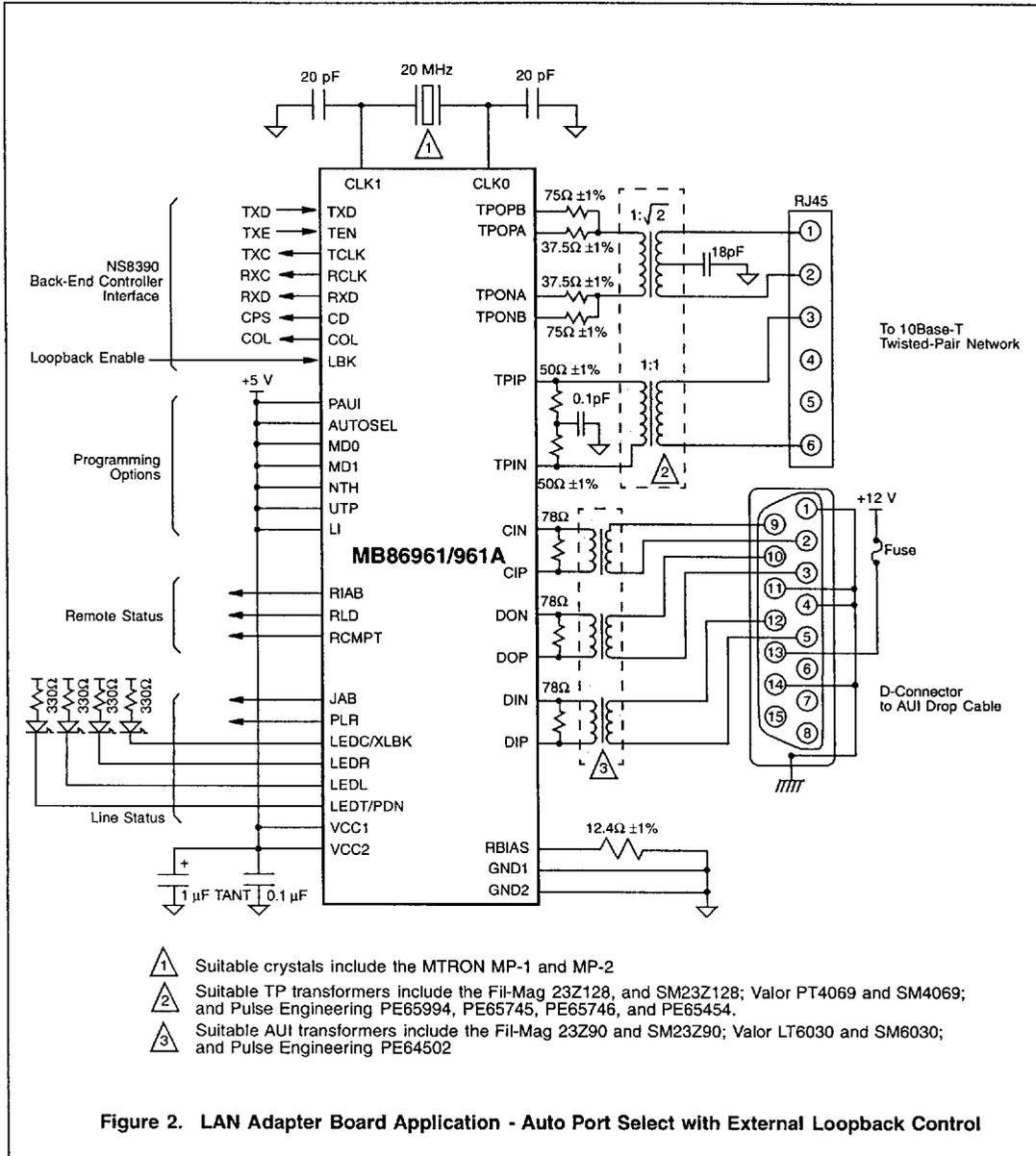
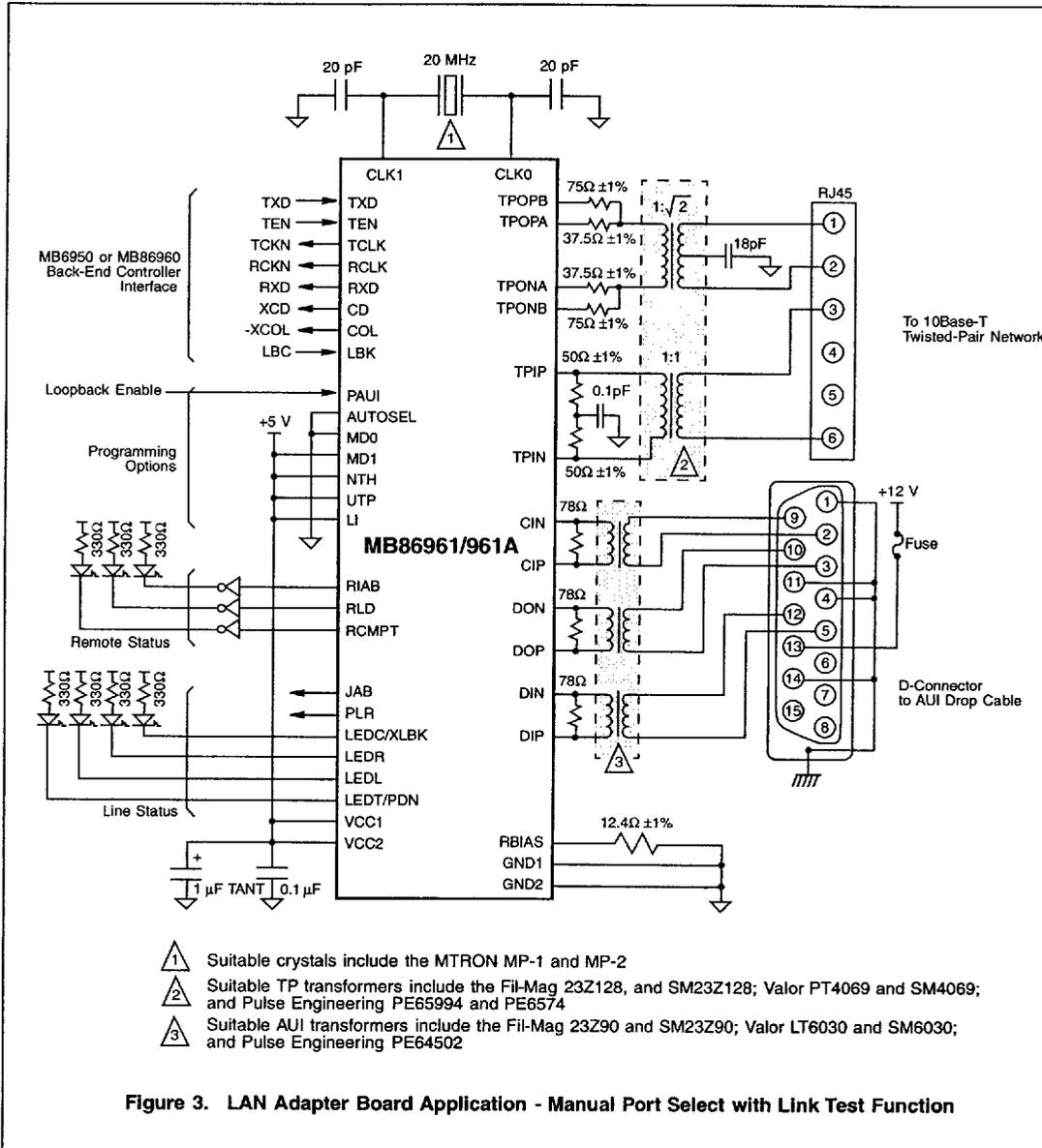
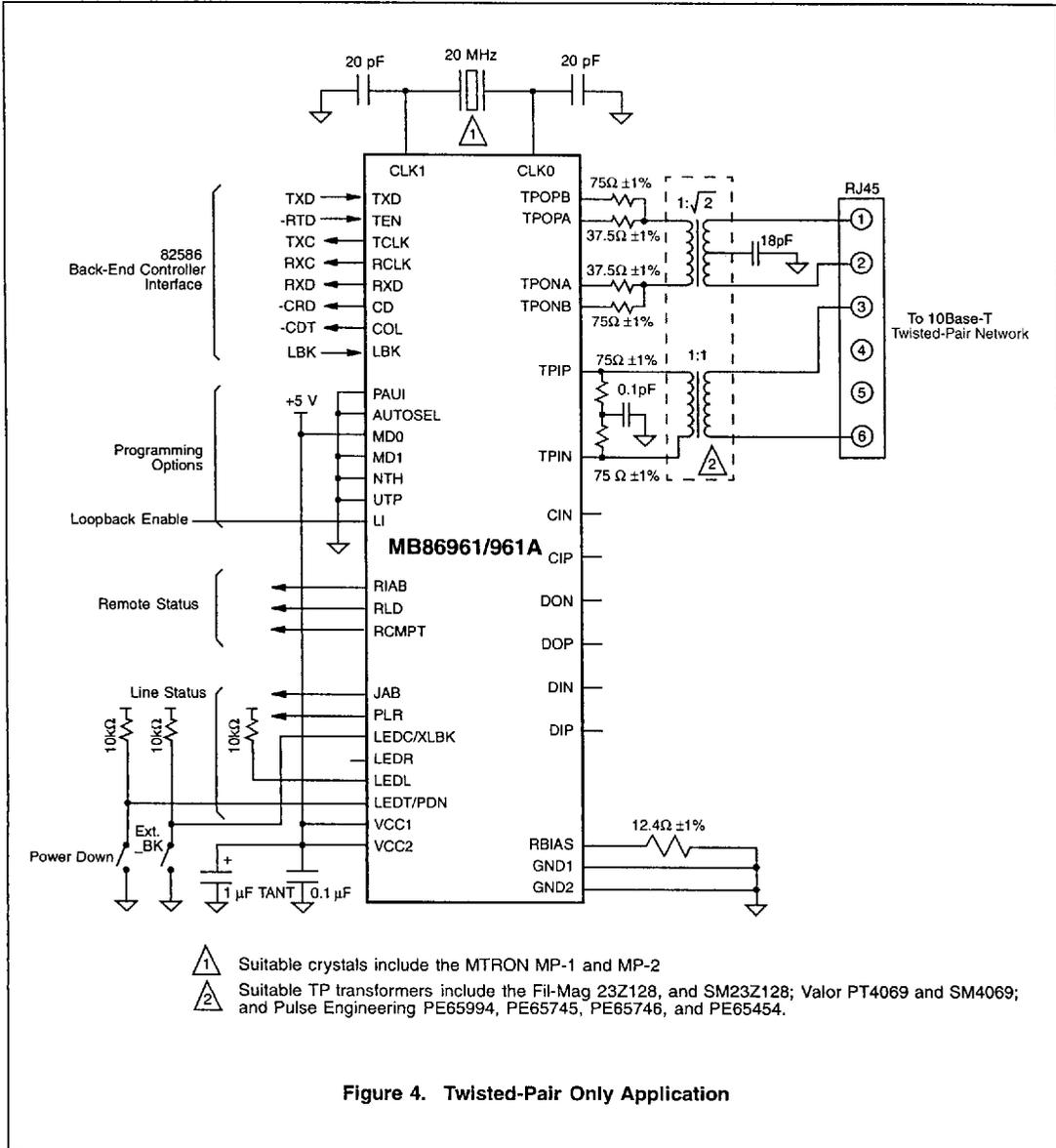
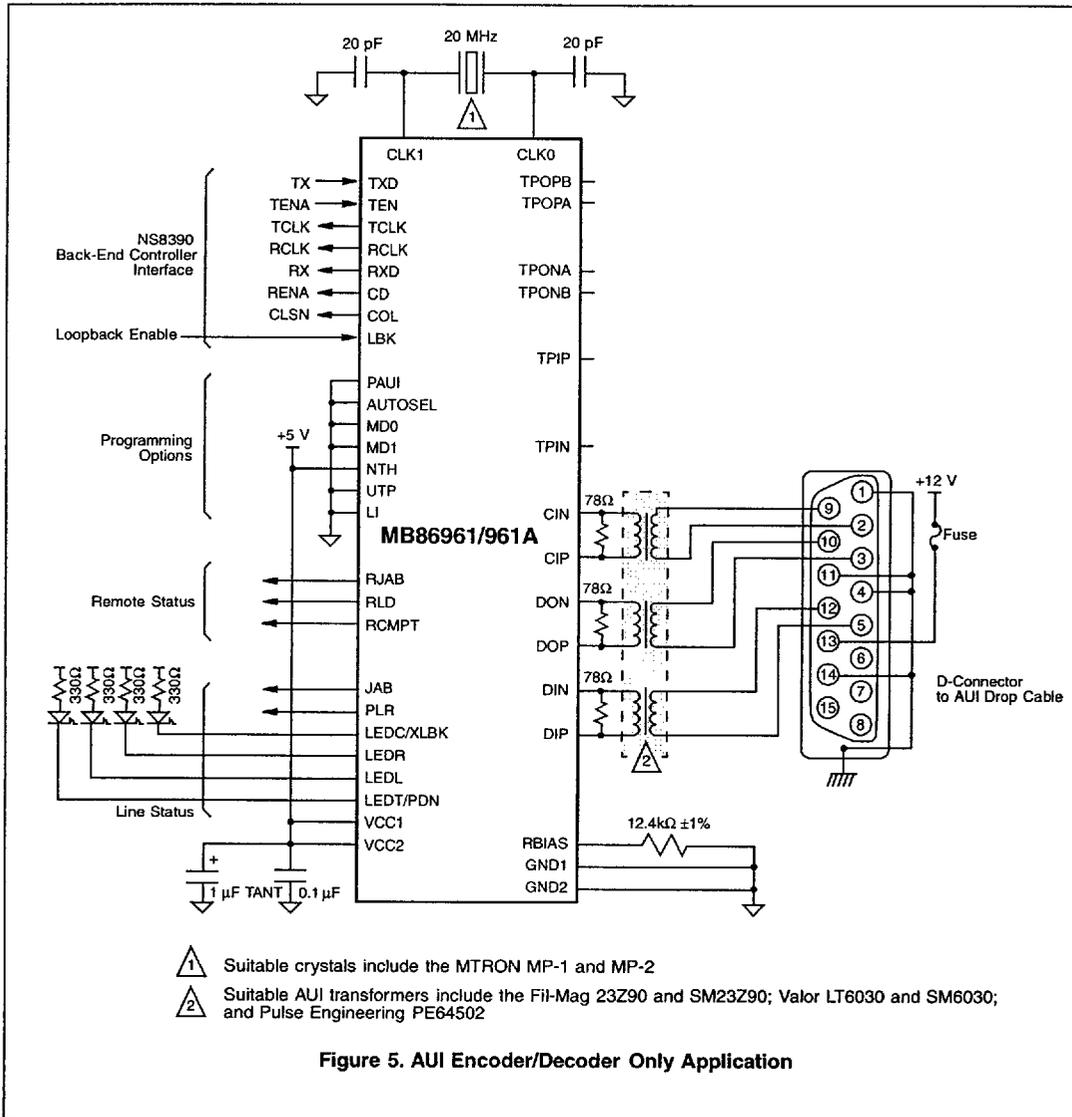


Figure 1. Typical System Diagram









FUNCTIONAL DESCRIPTION

The MB86961(A) Universal Ethernet Interface Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as a PLS-only device (for use with 10BASE2 or 10BASE5 coaxial cable networks) or as an Integrated PLS/MAU (for use with 10BASE-T twisted-pair networks).

The MB86961(A) interfaces a back-end controller to either an AUI drop cable or twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The AUI interface comprises three circuits: Data output (DO), Data Input (DI) and Collision (CI). The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the three basic interfaces, the MB86961(A) contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back end controller side of the interface. The MB86961(A) Transmit function refers to data transmitted by the back end to the AUI cable (PLS-Only mode) or to the twisted-pair network (Integrated PLS/MAU mode). The MB86961(A) Receive function refers to data received by the back end from the AUI cable (PLS-Only) or from the twisted-pair network (Integrated PLS/MAU mode). In the integrated PLS/MAU mode, the MB86961(A) performs all required MAU functions defined by the IEEE 802.3 10BASE-T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback. In the PLS-Only mode, the MB86961(A) receives incoming signals from the AUI DI circuit with up to 18ns of jitter and drives the AUI DO circuit.

CONTROLLER COMPATIBILITY MODES

The MB86961(A) is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Intel, Fujitsu and National Semiconductor. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins MD0 and MD1 determine controller compatibility modes as listed in Table 1.

Table 1. MB86961(A) Compatibility Modes

MD1	MD0	Mode
0	0	Mode 1: Compatible with Advanced Micro Devices AM7990 controllers
0	1	Mode 2: Compatible with Intel 82586 controllers
1	0	Mode 3: Compatible with Fujitsu MB86950 and MB86960 controllers
1	1	Mode 4: Compatible with National Semiconductor 8390 controllers

- Mode 1: Figures 12-17
- Mode 2: Figures 18-23
- Mode 3: Figures 24-29
- Mode 4: Figures 30-35

The related timing specifications are provided in the electrical characteristics section of this data sheet.

TRANSMIT FUNCTION

The MB86961(A) receives NRZ data from the controller at the TXD input (see MB86961(A) block diagram), and passes it through a Manchester encoder. The encoded data is then transferred to either the AUI cable (the DO circuit) or the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in Figure 6. The TPO output is pre-distorted and prefiltered to meet the 10BASE-T jitter template. No external filters are required. During idle periods, the MB86961(A) transmits link integrity test pulses on the TPO circuit if LI is enabled and integrated PLS/MAU mode is selected. The MB86961(A) can be programmed for either shielded TP (150 Ω) or unshielded TP (100Ω) through the UTP pin.

JABBER CONTROL FUNCTION

Figure 7 is a state diagram of the MB86961(A) Jabber control function. The MB86961(A) on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loop-back functions, and activates the JAB pin. Once the MB86961(A) is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

SQE FUNCTION

In the integrated PLS/MAU mode, the MB86961(A) supports the signal quality error (SQE) function as shown in Figure 8. After every successful transmission on the 10BASE-T network, the MB86961(A) transmits the SQE signal to the DTE for 10±5 bit times over the internal CI Circuit.

RECEIVE FUNCTION

The MB86961(A) receive function acquires timing and data from the twisted-pair network (the TPI circuit) or from the AUI (the DI Circuit). Valid received signals are passed through the on-chip filters and Manchester

decoder and output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively. No external filters are required.

An internal intelligent squelch function discriminates noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signal at the TPI or the DI circuit inputs falls below 75% of the threshold level (unsquelched) for eight bit times (typical), the MB86961(A) receive function enters the idle state. If the polarity of the TPI circuit is reversed, the MB86961(A) detects the polarity reversal and reports it via the PLR output. The MB86961(A) automatically corrects reversed polarity.

POLARITY REVERSE FUNCTION

The MB86961(A) polarity reverse function uses both link pulses and end-of-frame data to determine the polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the MB86961(A) enters the link fail state and no valid

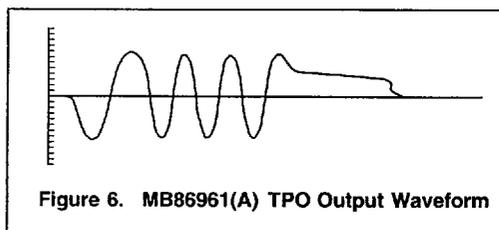


Figure 6. MB86961(A) TPO Output Waveform

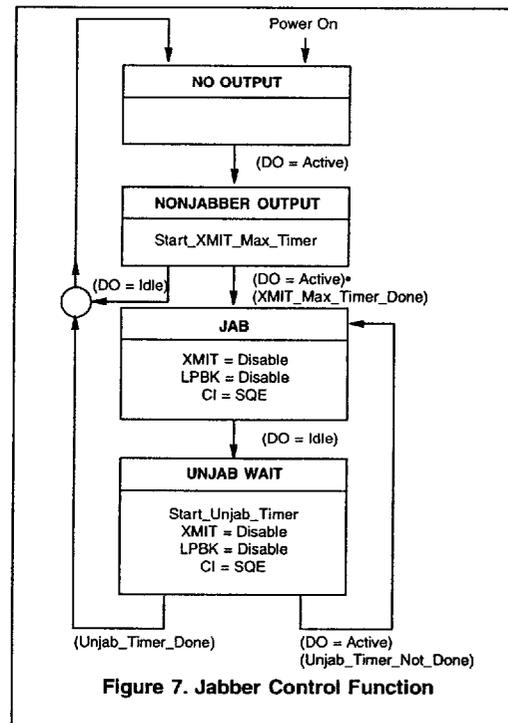


Figure 7. Jabber Control Function

data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. If Link Integrity Testing is disabled, polarity detection is based only on received data. Polarity correction is always enabled.

COLLISION DETECTION FUNCTION

The collision detection function operates on the twisted-pair side of the interface. A collision is defined as the

simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The MB86961(A) reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 9 is a state diagram of the MB86961(A) collision detection function. Refer to Electrical Characteristics for collision detection and COL/CI output timing.

LOOPBACK FUNCTION

The MB86961(A) provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the MB86961(A) from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the back-end. The “normal” loopback function is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Normal loopback is also disabled during link fail and jabber states.

The MB86961A also provides three additional loopback functions. An external loopback mode, useful for system-level testing, is controlled by pin 21 (LEDC). When LEDC is tied low, the MB86961A disables the collision detection and internal loopback circuits to allow external loopback or full-duplex operation. (This function is not implemented in the MB86961(A)). The MB86961(A) provides additional loopback functions controlled by pin 22 (LBK). When the TP port is selected and LBK=1, TP loopback is “forced,” overriding collisions on the TP circuit. When LBK=0, normal loopback is in effect.

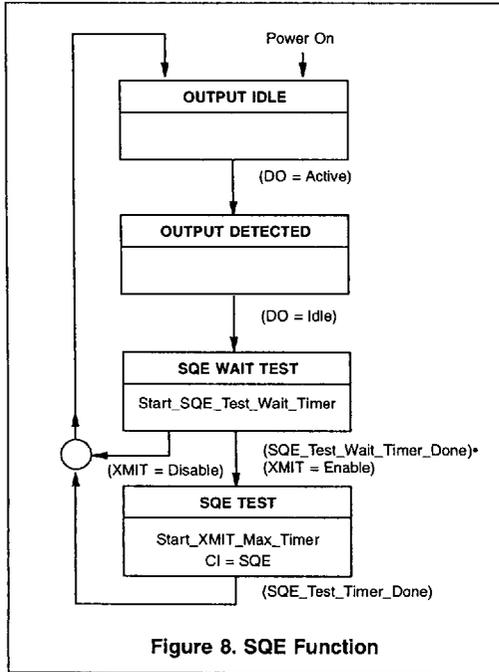


Figure 8. SQE Function

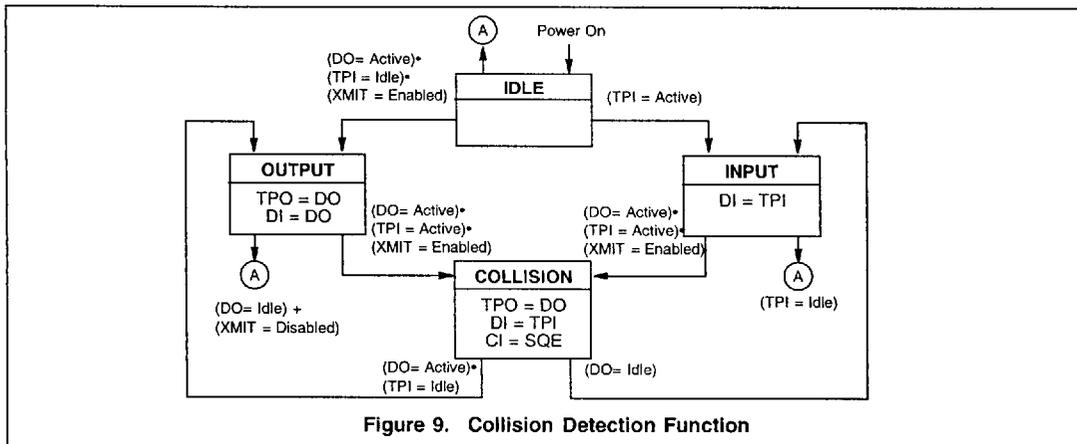


Figure 9. Collision Detection Function

When the AUI port is selected and LBK=1, data transmitted by the back-end is internally looped back from the TXD pin through the Manchester encoder/decoder to the RXD pin. When LBK=0, no AUI loopback occurs.

LINK INTEGRITY TEST

Figure 10 is a state diagram of the MB86961(A) Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when pin 8 (LI) is tied

high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50-150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The MB86961(A) ignores any link integrity pulse with an interval less than 2-7 ms. The MB86961(A) will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

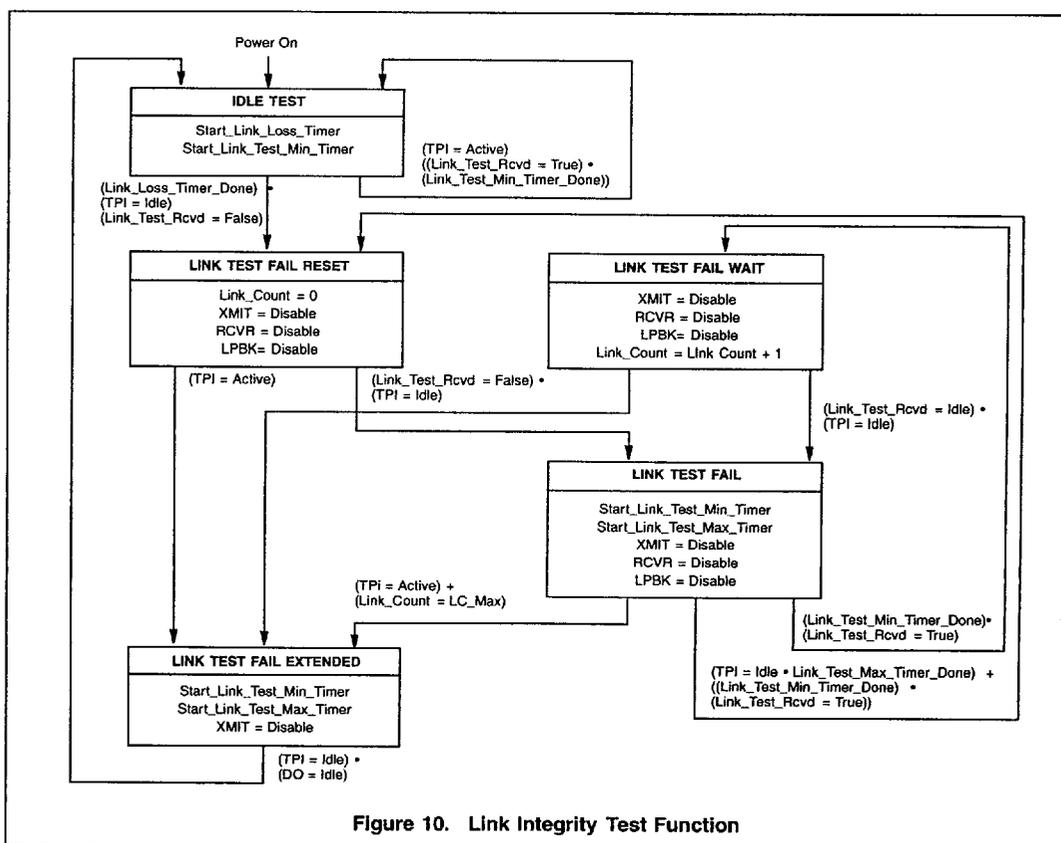
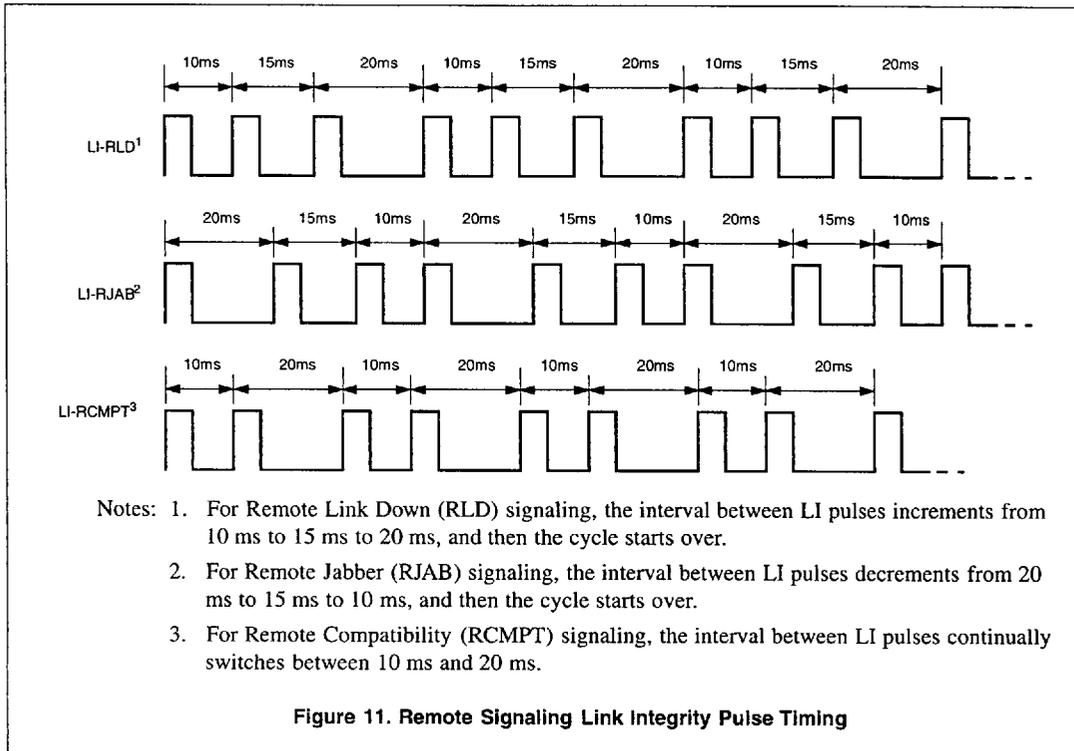


Figure 10. Link Integrity Test Function

REMOTE SIGNALING

The MB86961(A) transmits standard link pulses which meet the 10BASE-T specification. However, the MB86961(A) encodes additional status information into the link pulse by varying the link pulse timing. This is referred to as remote signaling. Using alternate pulse intervals, the MB86961(A) can signal three local condi-

tions: link down, jabber, and remote signaling capability. Figure 11 shows the interval variations used to signal local status to the other end of the line. The MB86961(A) also recognizes these alternate pulse intervals when received from a remote unit. Remote status conditions are reported to the controller over the RLD, RJAB and RCMPT output pins.



ELECTRICAL CHARACTERISTICS

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Conditions	Min.	Max.	Units
V _{CC}	Supply voltage		-0.3	6	V
T _{OP}	Operating temperature		0	70	°C
T _{ST}	Storage temperature		-65	150	°C

Note: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3. INPUT/OUTPUT CHARACTERISTICS ($\bar{T}_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, V_{CC} = 5 V $\pm 5\%$)

Symbol	Parameter	Condition	Min.	Typ. ¹	Max.	Units	
V _{IL}	Input low voltage ¹		—	—	0.8	V	
V _{IH}	Input high voltage ²		2.0	—	—	V	
V _{OL}	Output low voltage	I _{OL} = 1.6 mA for MB86961	—	—	0.4	V	
		I _{OL} = 3.2 mA for MB86961(A)	—	—	0.4	V	
		I _{OL} < 10 mA	—	—	10	%V _{CC}	
V _{OH}	Output high voltage	I _{OH} = 40 mA	2.4	—	—	V	
		I _{OH} < 10 mA	90	—	—	%V _{CC}	
I _{CC}	Supply current	Normal mode	—	90	—	mA	
		Power-down mode	—	5	—	mA	
t _R	Output rise time	CMOS	TCLK and RCLK	—	3	—	ns
		TTL	TCLK and RCLK	—	2	—	ns
t _F	Output fall time	CMOS	TCLK and RCLK	—	3	—	ns
		TTL	TCLK and RCLK	—	2	—	ns

Notes: 1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

2. Limited functional test patterns are performed at these input levels. The majority of functional tests are performed at levels 0V and 3V.

Table 4. AUI ELECTRICAL CHARACTERISTICS ($\bar{T}_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, V_{CC} = 5 V $\pm 5\%$)

Symbol	Parameter	Condition	Min.	Typ. ¹	Max.	Units
I _{IL}	Input low current		—	—	-700	mA
I _{IH}	Input high current		—	—	500	mA
V _{OD}	Differential output voltage		±550	—	±1200	mV
V _{DS}	Differential squelch threshold		—	220	—	mV

Note: Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Table 5. TP ELECTRICAL CHARACTERISTICS ($\bar{T}_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Parameter	Condition	Min.	Typ. ¹	Max.	Units
Z _{OUT}	Transmit output impedance		—	5	—	W
V _{OD}	Peak differential output voltage	Load=100 Ω at TPOP and TPON	—	3.5	—	V
t _{JIT}	Transmit timing jitter addition	0 line length ¹	—	—	±8	ns
t _{JIT}	Transmit timing jitter addition	After line model specified by IEEE 802.3 for 10BASE-T	—	—	±3.5	ns
Z _{IN}	Receive input impedance	Between TPIP/TPIN, CIP/CIN and DIP/DIN	—	20	—	kΩ
V _{DS}	Differential squelch threshold		—	420	—	mV
V _{DSL}	Lower squelch threshold		—	250	—	mV

Notes: 1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
 2. Parameter is guaranteed by design, not subject to production testing.

Table 6. SWITCHING CHARACTERISTICS ($\bar{T}_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Jabber Timing						
t _{JAB}	Maximum transmit time		20	—	150	ms
t _{UJAB}	Unjab time		250	—	750	ms
Link Integrity Timing						
t _{LL}	Time link loss		55	—	66	ms
t _{LP1}	Time between Link Integrity Pulses		8	—	24	ms
t _{LP2}	Interval for valid receive Link integrity Pulses		4.1	—	65	ms
General						
t _{RST}	Receive start-up delay ¹		0	—	500	ns
t _{TST}	Transmit start-up delay ¹		0	—	200	ns
t _{LST}	Loopback start-up delay ¹		0	—	500	ns

Note: Parameter is guaranteed by design; not subject to production testing.

Table 7. RCLK/Start-of-Packet Timing

Symbol	Parameter	Min.	Typ. ¹	Max.	Units	
t _{DATA}	Decoder acquisition time	AUI	—	900	—	ns
		TP	—	1300	—	ns
t _{CD}	CD turn-on delay	AUI	—	50	—	ns
		TP	—	400	—	ns
t _{RDS}	Receive data setup from RCLK	Mode 1	40	—	—	ns
		Modes 2, 3 and 4	30	—	—	ns
t _{RDH}	Receive data hold from RCLK	Mode 1	10	—	—	ns
		Modes 2, 3 and 4	30	—	—	ns

Note: Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Table 8. RCLK/End-of-Packet Timing

Symbol	Parameter	Type	Mode 1	Mode 2	Mode 3	Mode 4	Units
t _{RCH}	RCLK hold after CD low	Min.	0	1	27	5	bt
t _{RD}	RCV data throughput delay	Typ.	300	275	275	275	ns
t _{CDOFF}	CD turn off delay	Typ.	400	375	375	375	ns
t _{IFG}	Receive block out	Typ.	2	50	27	5	bt

Notes: 1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
 2. CD Turn off delay measured from middle of last bit, so timing specification is unaffected by the value of the last bit.

Table 9. Transmit Timing

Symbol	Parameter	Min.	Typ. ¹	Max.	Units
t _{EHCH}	TEN setup from TCLK	—	30	—	ns
t _{DSCH}	TXD setup from TCLK	—	30	—	ns
t _{CHEL}	TEN hold after TCLK	—	5	—	ns
t _{CHDU}	TXD hold after TCLK	—	5	—	ns

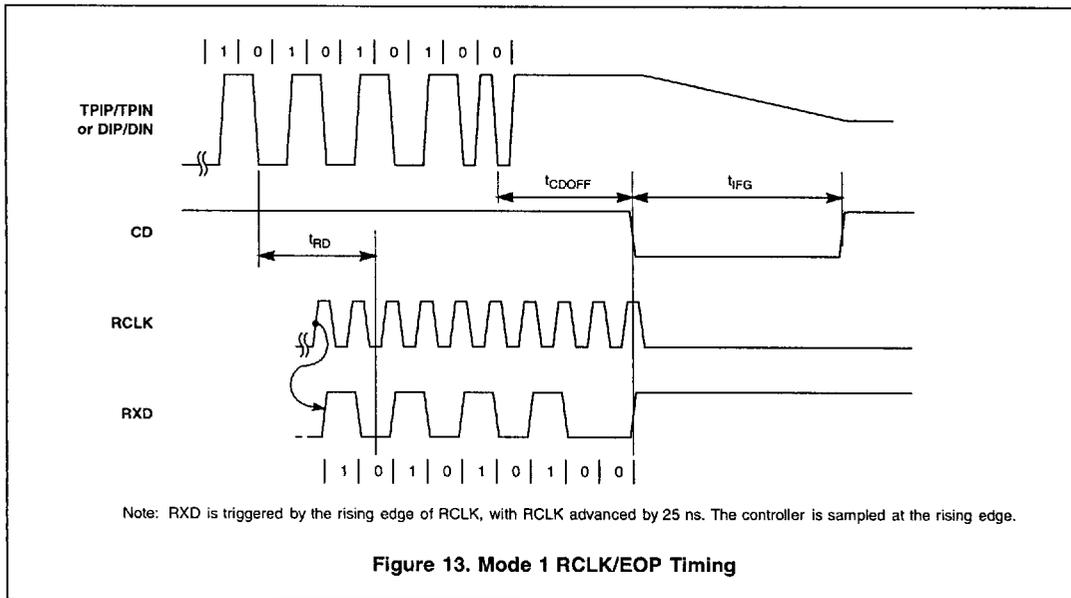
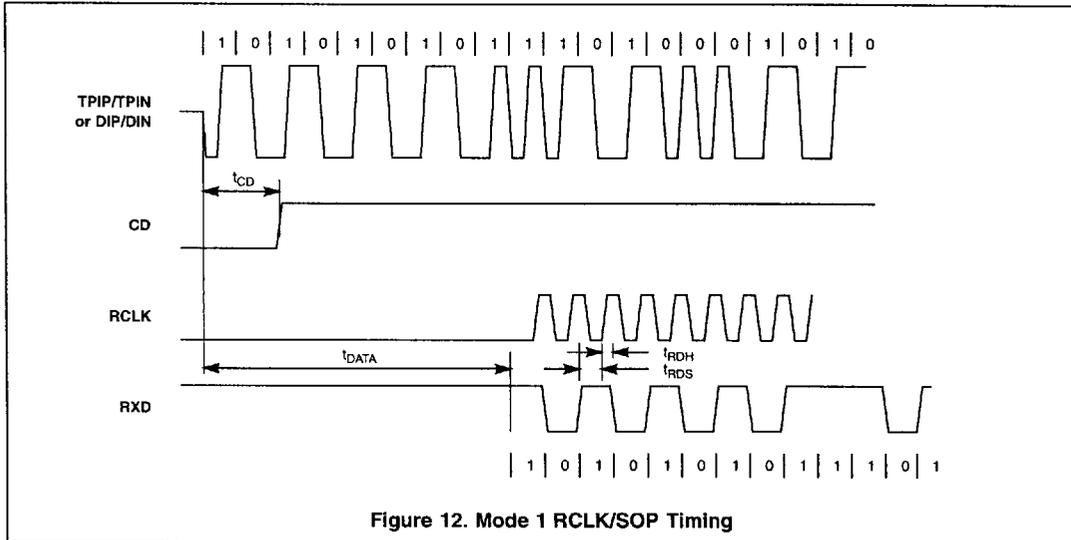
Note: Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

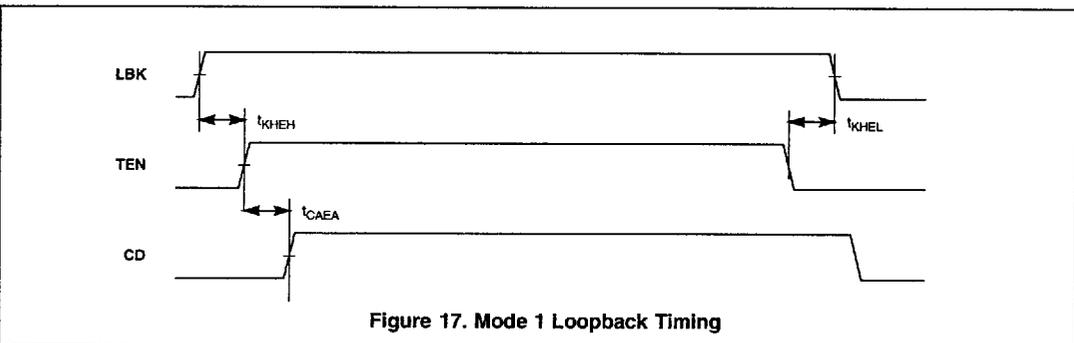
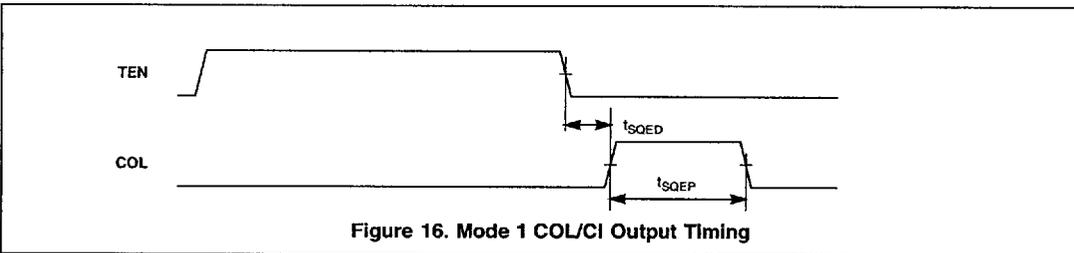
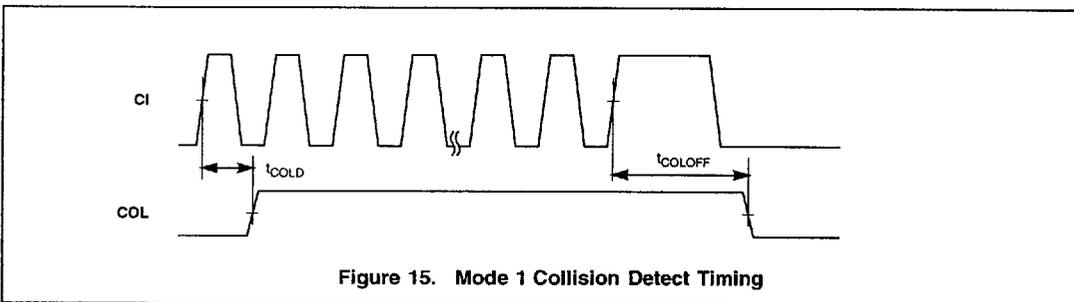
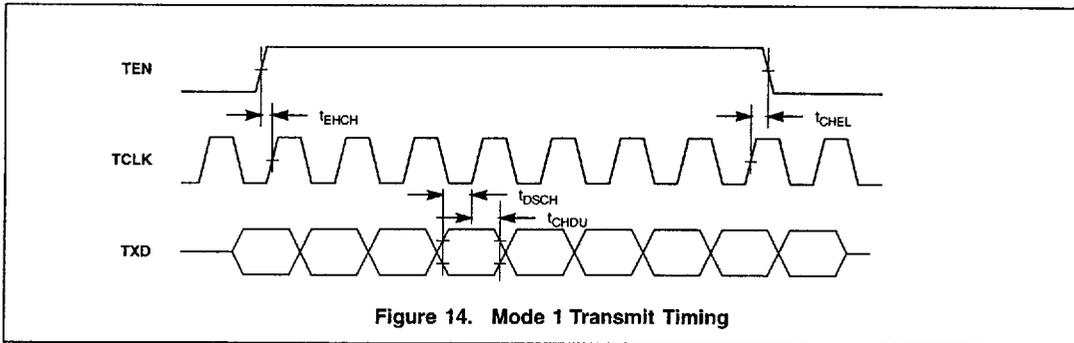
Table 10. Collision Detection, COL/CI Output and Loopback Timing

Symbol	Parameter	Min.	Typ. ¹	Max.	Units
t _{COLD}	COL turn on delay	—	50	—	ns
t _{COLOFF}	COL turn off delay	—	160	—	ns
t _{SQED}	SQE Delay	0.65	—	1.6	ms
t _{SQEP}	SQE Pulse Duration	500	—	1500	ns
t _{KHEH}	LBK setup from TEN	—	25	—	ns
t _{KHEL}	LBK hold after TEN	—	0	—	ns

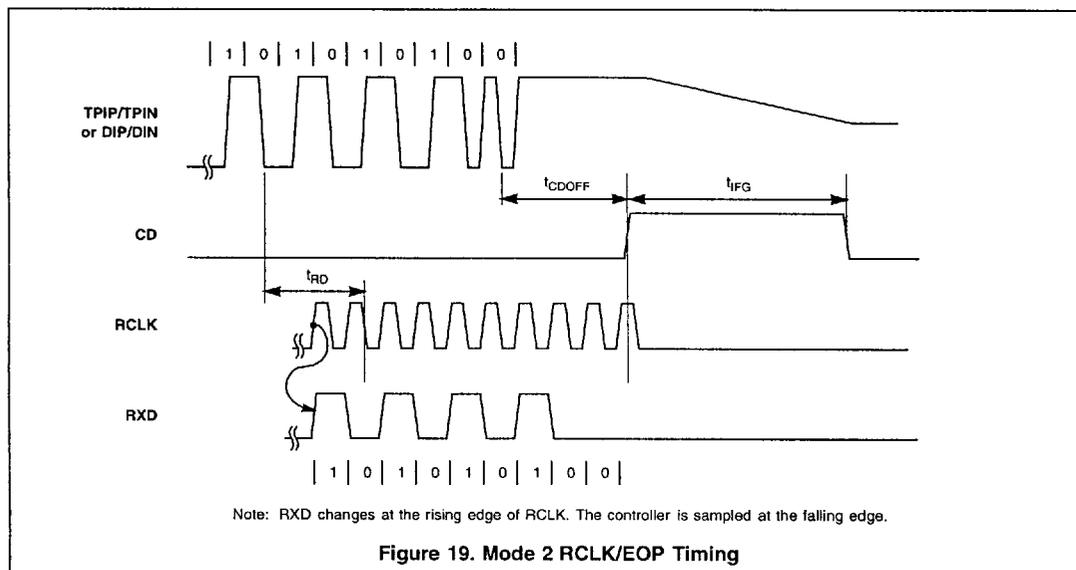
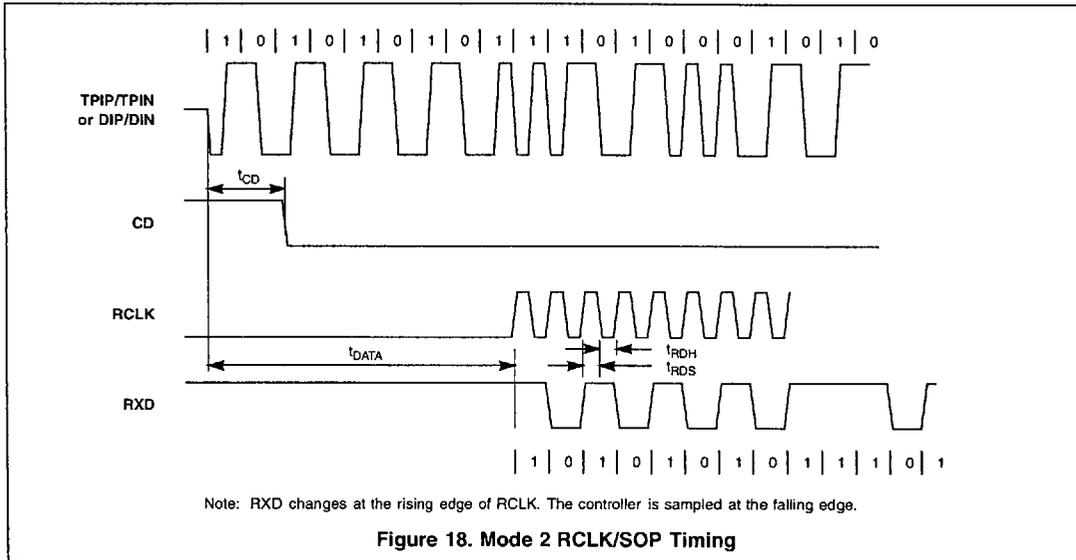
Note: Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

MODE 1 (MD1=0, MD0=0) TIMING DIAGRAMS — FIGURES 12 - 17





MODE 1 (MD1=0, MD0=0) TIMING DIAGRAMS — FIGURES 18 - 23



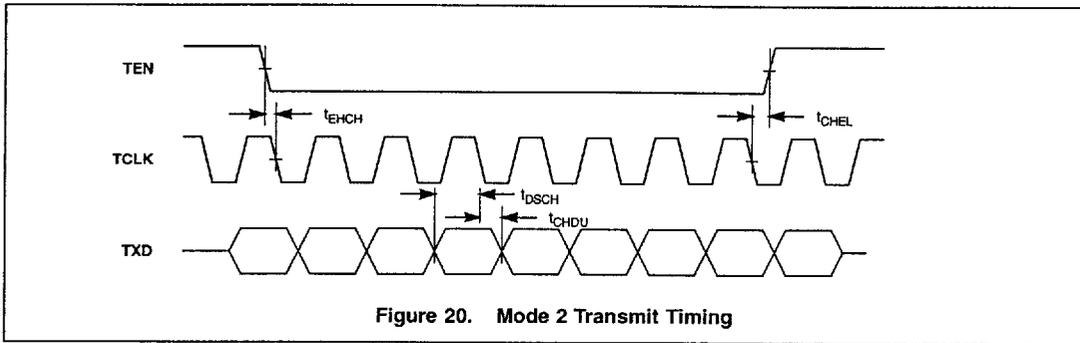


Figure 20. Mode 2 Transmit Timing

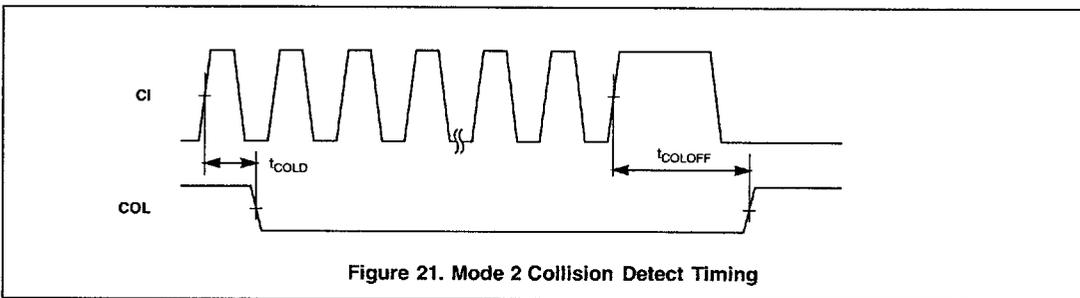


Figure 21. Mode 2 Collision Detect Timing

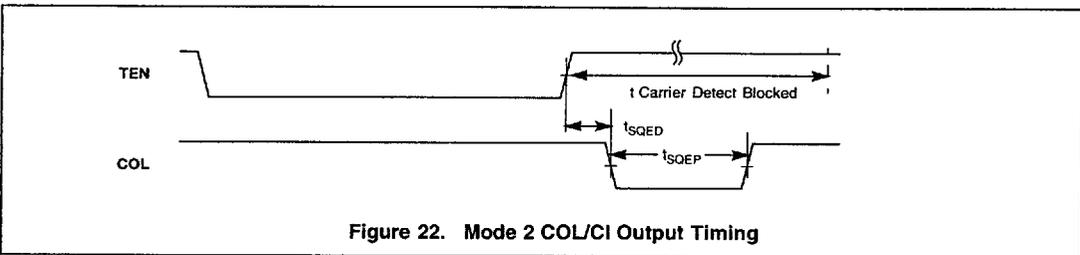


Figure 22. Mode 2 COL/CI Output Timing

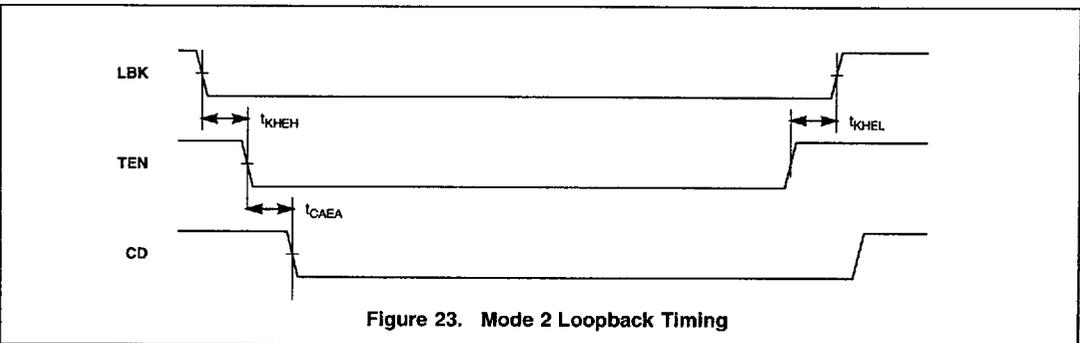
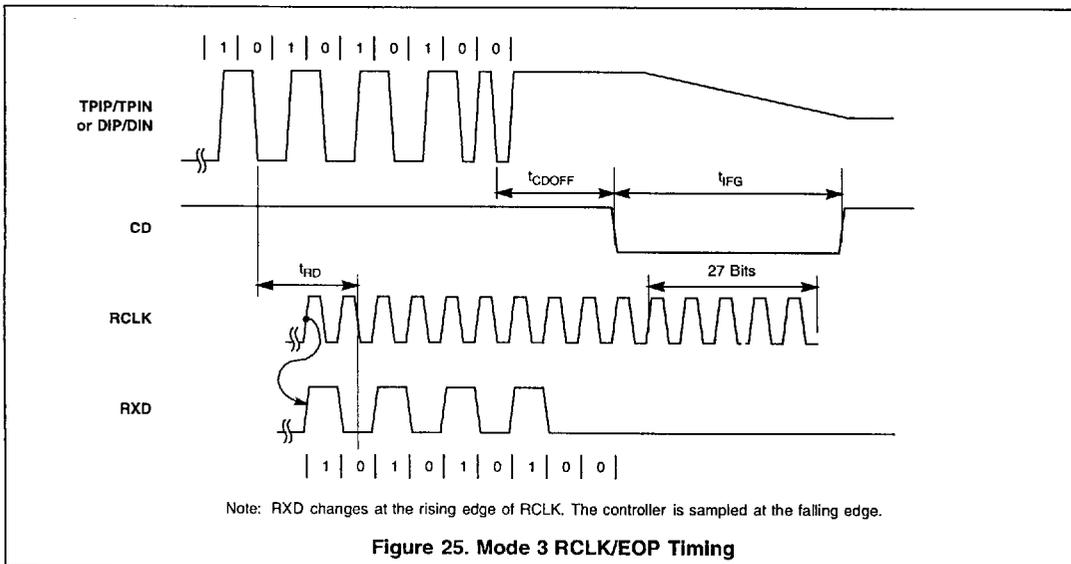
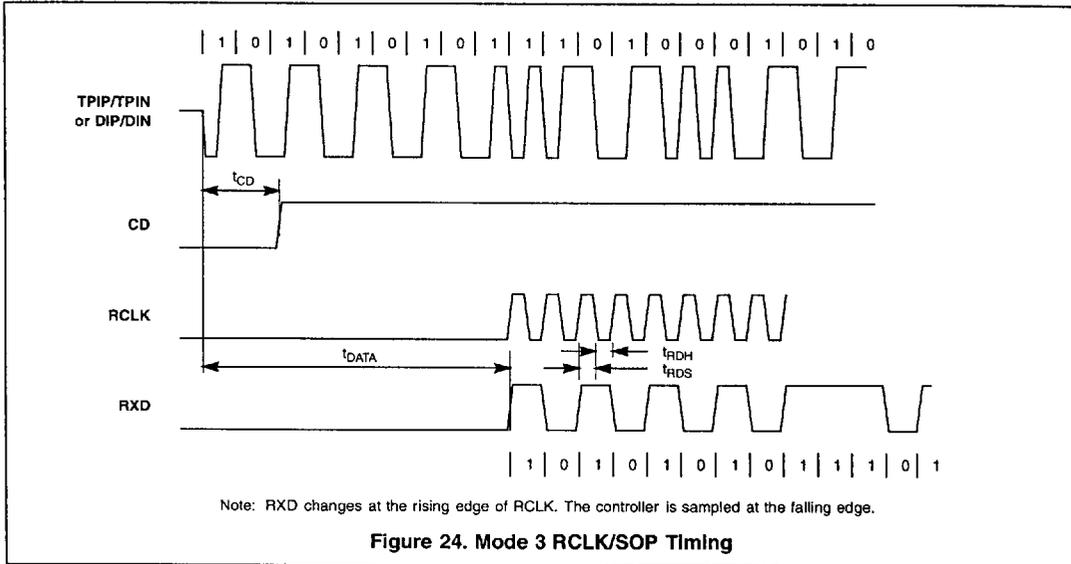
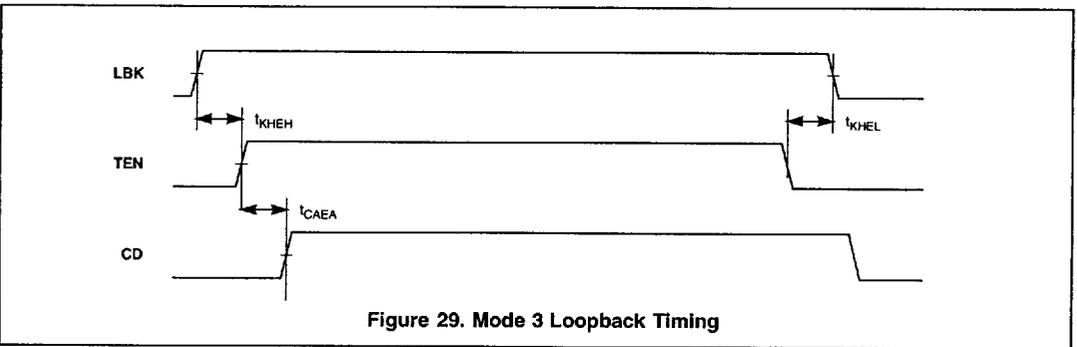
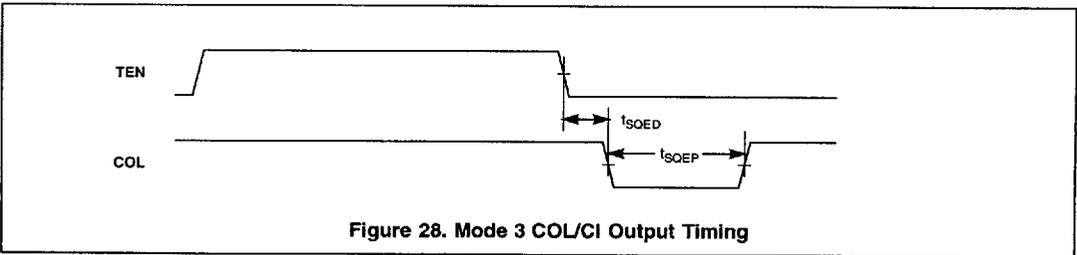
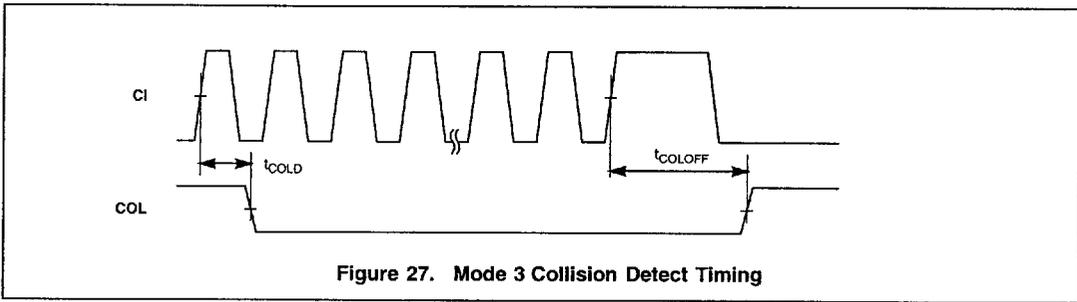
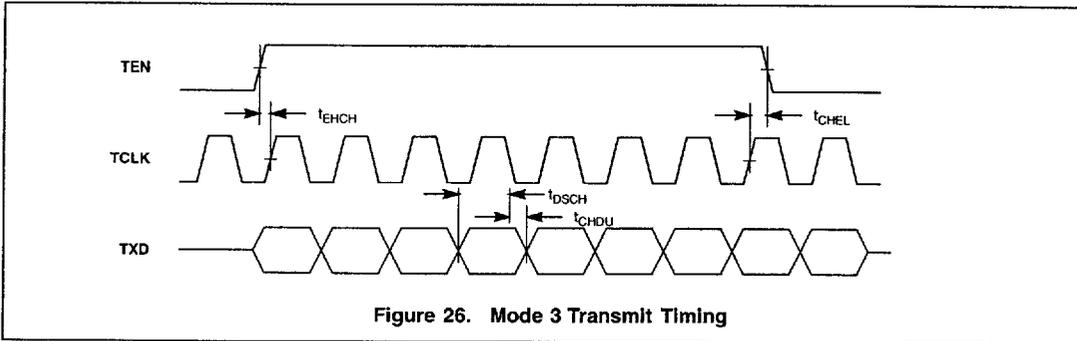


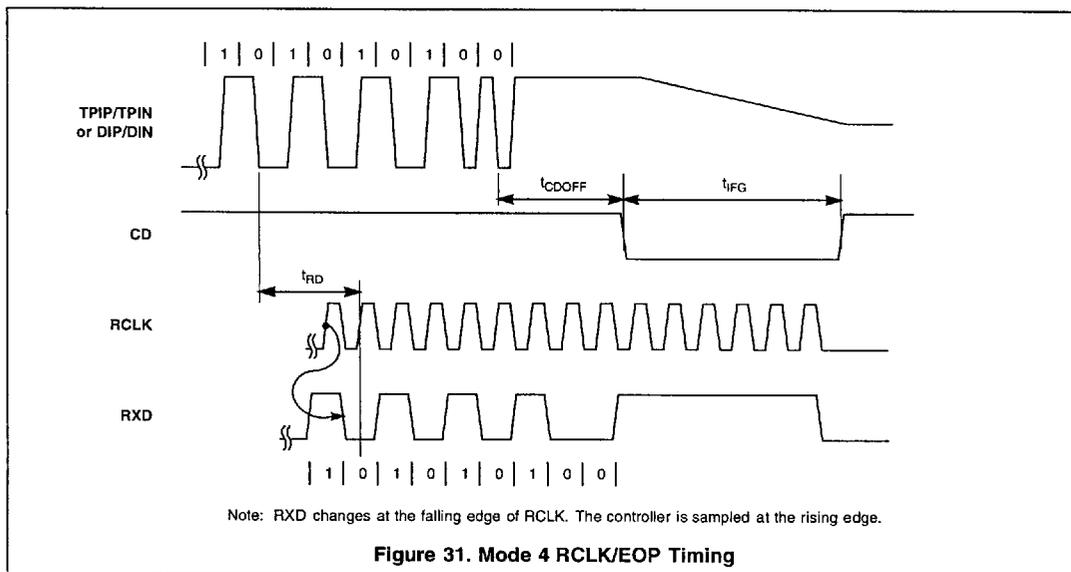
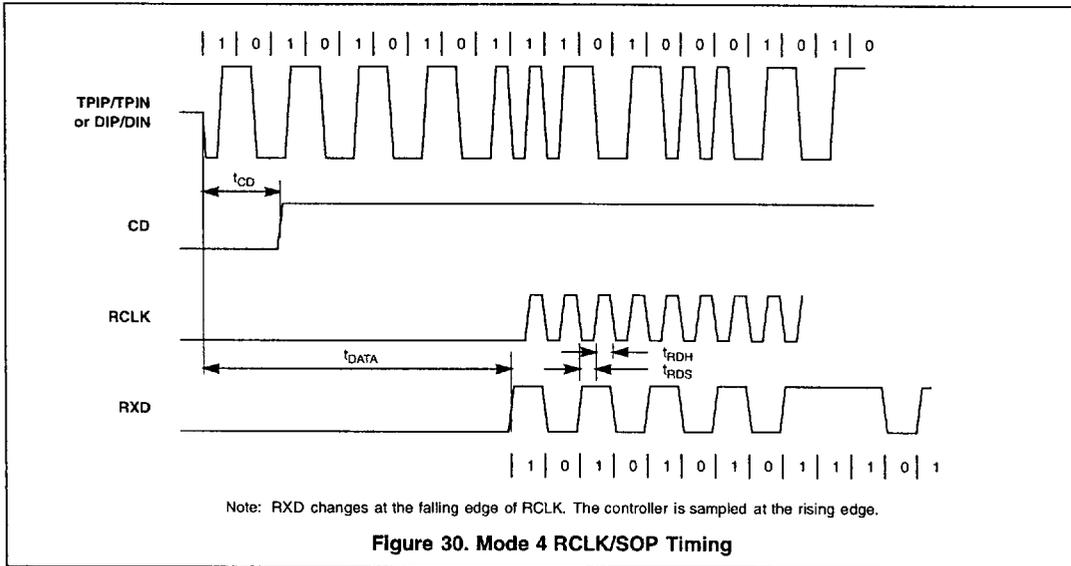
Figure 23. Mode 2 Loopback Timing

MODE 1 (MD1=0, MD0=0) TIMING DIAGRAMS — FIGURES 24 - 29





MODE 1 (MD1=0, MD0=0) TIMING DIAGRAMS — FIGURES 30 - 35



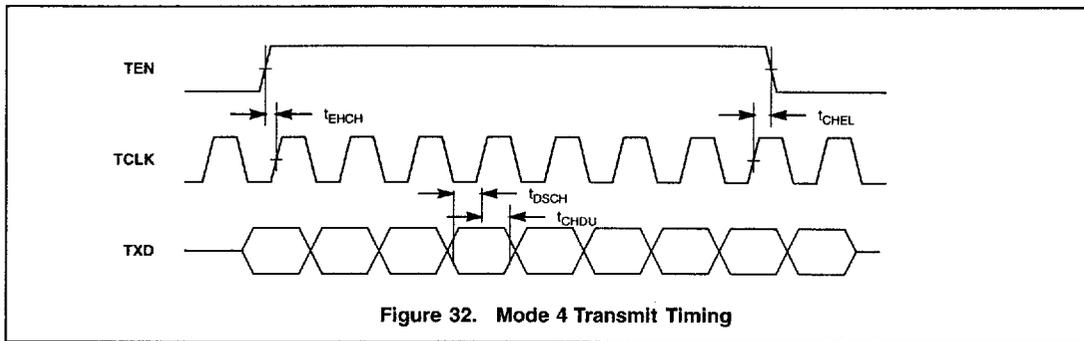


Figure 32. Mode 4 Transmit Timing

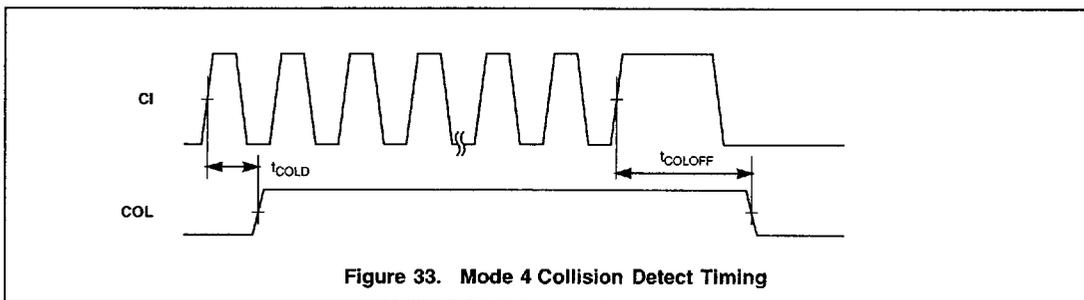


Figure 33. Mode 4 Collision Detect Timing

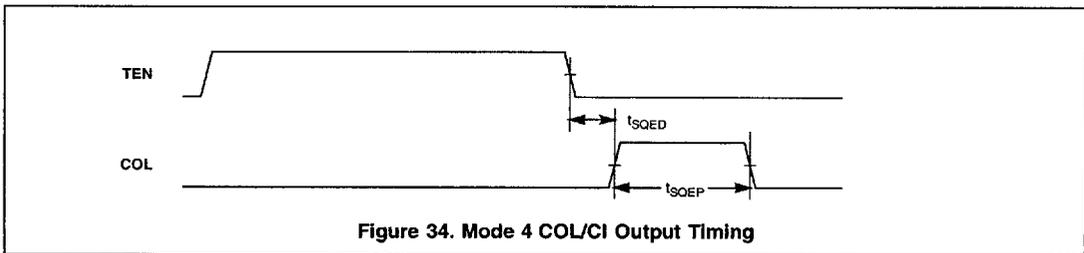


Figure 34. Mode 4 COL/CI Output Timing

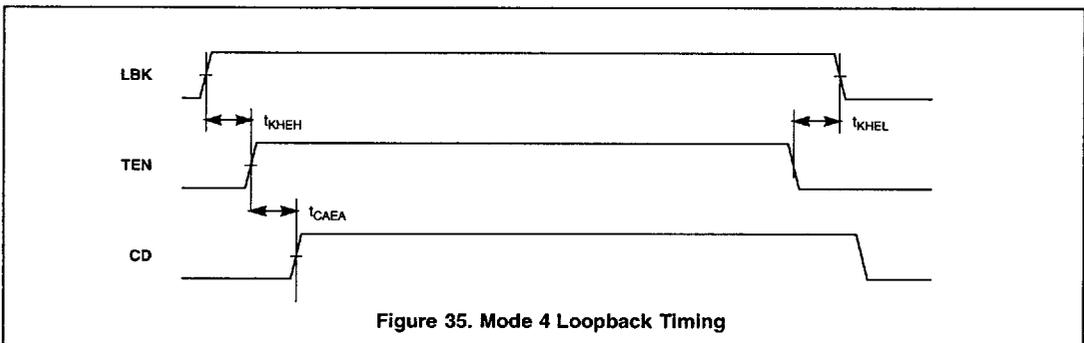
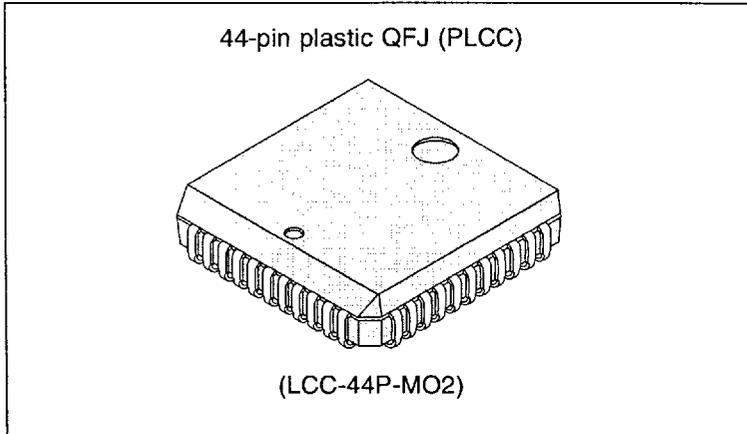
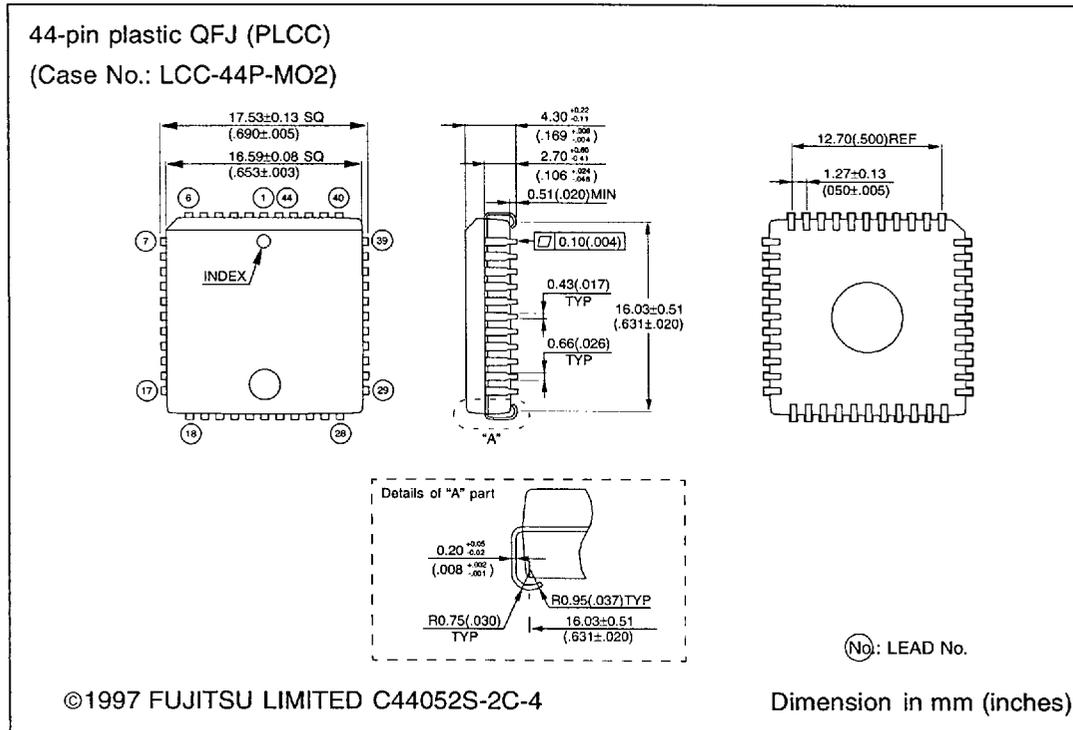
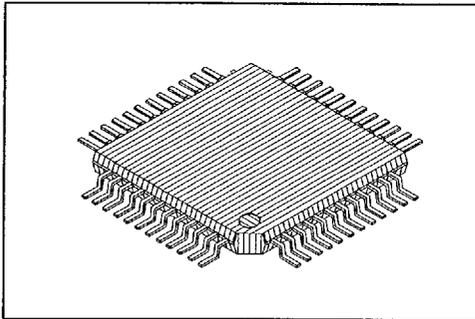


Figure 35. Mode 4 Loopback Timing



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