

### POWER MANAGEMENT

#### Description

The SC1453 is a low dropout linear regulator that operates from a +2.25V to +6.5V input range and delivers up to 150mA. A PMOS pass transistor allows the low 75 $\mu$ A supply current to remain independent of load, making these devices ideal for battery operated portable equipment such as cellular phones, cordless phones and personal digital assistants.

The SC1453 has a bandgap reference bypass pin for very low noise operation - a 10nF (typ.) capacitor may be connected between this pin and ground. Other features include low powered shutdown, short circuit protection, thermal shutdown protection and reverse battery protection. The SC1453 comes in the tiny 5 lead SOT-23 package and the ultra-low profile 5 lead TSOT-23.

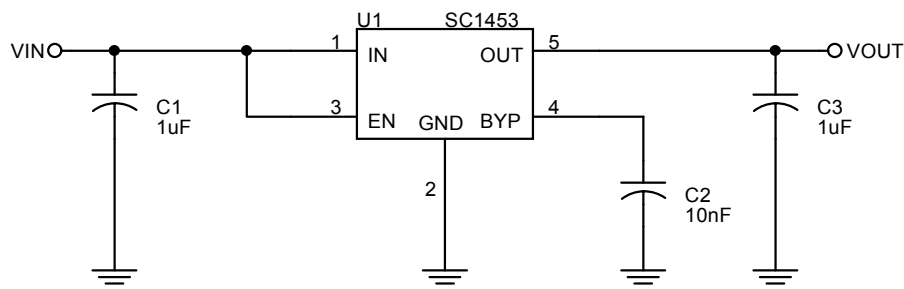
#### Features

- ◆ “2982/5205” compatible pinout
- ◆ Guaranteed 150 mA output current
- ◆ 2% output accuracy guaranteed over line, load and temperature
- ◆ Very small external components - designed to work with ceramic capacitors
- ◆ Low 26 $\mu$ V<sub>RMS</sub> output noise (1.5V option, C<sub>IN</sub> = C<sub>OUT</sub> = 1 $\mu$ F, C<sub>BYP</sub> = 10nF)
- ◆ Very low supply current
- ◆ Thermal overload protection
- ◆ Reverse battery protection
- ◆ Low power shutdown
- ◆ Full industrial temperature range
- ◆ Very low profile packaging available (1mm max. height)
- ◆ Surface mount packaging (5 pin SOT-23 and TSOT-23)
- ◆ Available in Lead-free packages, fully WEEE and RoHS compliant

#### Applications

- ◆ Battery Powered Systems
- ◆ Cellular Telephones
- ◆ Cordless Telephones
- ◆ Personal Digital Assistants
- ◆ Portable Instrumentation
- ◆ Modems
- ◆ PCMCIA cards

#### Typical Application Circuit



**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	$V_{IN}$	-0.6 to +7	V
Thermal Resistance Junction to Ambient	$\theta_{JA}$	256	°C/W
Thermal Resistance Junction to Case	$\theta_{JC}$	81	°C/W
Operating Ambient Temperature Range	$T_A$	-40 to +85	°C
Operating Junction Temperature Range	$T_J$	-40 to +125	°C
Storage Temperature Range	$T_{STG}$	-65 to 150	°C
Lead Temperature (Soldering) 10 Sec.	$T_{LEAD}$	300	°C
ESD Rating	ESD	2	kV

**Electrical Characteristics**

Unless specified:  $V_{IN} = V_{OUT} + 1V$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 100\mu A$ ,  $C_{IN} = C_{OUT} = 1\mu F$ ,  $T_A = 25^\circ C$ . Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>IN</b>						
Supply Voltage Range	$V_{IN}$		<b>2.25</b>		<b>6.50</b>	V
Supply Current	$I_Q$	$I_{OUT} = 0mA \text{ to } 150mA$		75	130	$\mu A$
		$V_{IN} = 6.5V, V_{EN} = 0V$		0.1	1.0	$\mu A$
<b>OUT</b>						
Output Voltage <sup>(1)</sup>	$V_{OUT}$	$I_{OUT} = 1mA$	-1.5%	$V_{OUT}$	+1.5%	V
		$0mA \leq I_{OUT} \leq 150mA, V_{OUT} + 1V \leq V_{IN} \leq 5.5V$	<b>-2.0%</b>		<b>+2.0%</b>	
Line Regulation <sup>(1)(2)</sup>	$REG_{(LINE)}$	$(V_{OUT(NOM)} + 0.1V) \leq V_{IN} \leq 5.5V, I_{OUT} = 1mA$		2.5	10	mV
					<b>12</b>	
Load Regulation <sup>(1)</sup>	$REG_{(LOAD)}$	$I_{OUT} = 0.1mA \text{ to } 150mA$		-3	-10	mV
					<b>-20</b>	

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

Unless specified:  $V_{IN} = V_{OUT} + 1V$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 100\mu A$ ,  $C_{IN} = C_{OUT} = 1\mu F$ ,  $T_A = 25^\circ C$ . Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>OUT (Cont.)</b>						
Current Limit	$I_{LIM}$		<b>400</b>			mA
Dropout Voltage <sup>(1)(3)</sup>	$V_D$	$I_{OUT} = 1mA$		1		mV
		$I_{OUT} = 50mA$		50	65	mV
					<b>75</b>	
		$I_{OUT} = 100mA$		100	125	mV
			<b>155</b>			
		$I_{OUT} = 150mA$		150	190	mV
					<b>230</b>	
Output Voltage Noise, $C_{OUT} = 1\mu F$	$e_n$	10Hz to 100kHz, $I_{OUT} = 1mA$ $C_{BYP} = 10nF$ , $V_{OUT} = 1.5V$		26		$\mu V_{RMS}$
		10Hz to 100kHz, $I_{OUT} = 1mA$ $C_{BYP} = 10nF$ , $V_{OUT} = 3.3V$		54		
Output Voltage Noise, $C_{OUT} = 100\mu F$	$e_n$	10Hz to 100kHz, $I_{OUT} = 1mA$ $C_{BYP} = 10nF$ , $V_{OUT} = 1.5V$		13		$\mu V_{RMS}$
		10Hz to 100kHz, $I_{OUT} = 1mA$ $C_{BYP} = 10nF$ , $V_{OUT} = 3.3V$		29		
Power Supply Rejection Ratio	PSRR	$f = 120Hz$ , $C_{BYP} = 10nF$		61		dB
<b>BYP</b>						
Start-up Rise Time	$t_r$	$C_{BYP} = 10nF$		1.3		ms
<b>EN</b>						
Enable Input Threshold	$V_{IH}$	$2.25V \leq V_{IN} \leq 6.5V$	<b>1.6</b>			V
	$V_{IL}$	$2.25V \leq V_{IN} \leq 6.5V$			<b>0.4</b>	
Enable Input Bias Current <sup>(4)</sup>	$I_{EN}$	$0V \leq V_{EN} \leq V_{IN}$	<b>-0.5</b>	0	<b>+0.5</b>	$\mu A$
<b>Over Temperature Protection</b>						
High Trip Level	$T_{HI}$			150		$^\circ C$
Hysteresis	$T_{HYST}$			20		$^\circ C$

**Notes:**

(1) Low duty cycle pulse testing with Kelvin connections required.

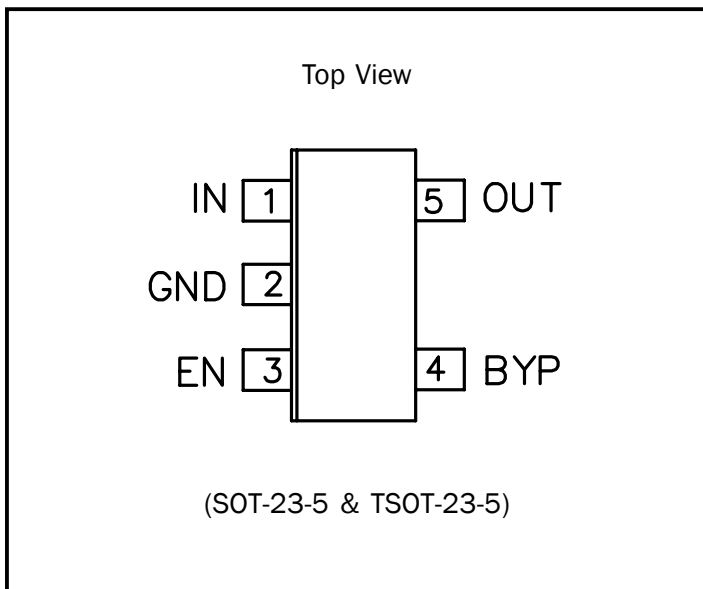
(2)  $V_{IN(MIN)} = 2.25V$ .

(3) Defined as the input to output differential at which the output voltage drops 100mV below the value measured at a differential of 1V. Not measurable on 1.5V and 1.8V parts due to minimum  $V_{IN}$  constraints.

(4) Guaranteed by design.

## POWER MANAGEMENT

### Pin Configuration



### Ordering Information

Part Number	Package
SC1453ISK-XXXTR <sup>(1)(2)</sup>	SOT-23-5
SC1453ISK-XXXTRT <sup>(1)(2)(3)</sup>	
SC1453ISK285TRT <sup>(2)(4)</sup>	TSOT-23-5
SC1453ITSK-XXXTR <sup>(1)(2)</sup>	
SC1453ITSK-XXXTRT <sup>(1)(2)(3)</sup>	
SC1453TSK285TRT <sup>(2)(4)</sup>	N/A
SC1453EVB <sup>(5)</sup>	

#### Notes:

(1) Where XXX denotes voltage options. Available voltages are: 1.5V (1.5), 1.8V (1.8), 2.5V (2.5), 2.7V (2.7), 2.8V (2.8), 2.9V (2.9), 3.0V (3.0), 3.1V (3.1), 3.2V (3.2) and 3.3V (3.3).

(2) Only available in tape and reel packaging. A reel contains 3000 devices.

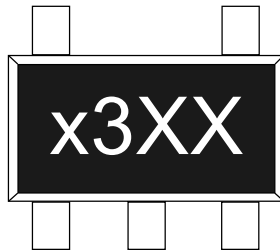
(3) Lead free packaging (ordered with suffix extension "TRT") is optional. Consult factory for availability. This product is fully WEEE and RoHS compliant.

(4) Use when ordering SC1453, 2.85V option, available in Lead-free packages only. This product is fully WEEE and RoHS compliant.

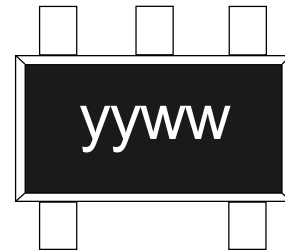
(5) Evaluation board for SC1453. Specify output voltage option when ordering.

### Pin Descriptions

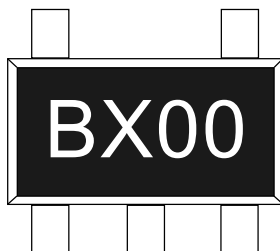
Pin #	Pin Name	Pin Function
1	IN	Input pin.
2	GND	Ground pin. Can be used for heatsinking if needed.
3	EN	Active high enable pin. Connect to IN if not being used.
4	BYP	Reference bypass. Connect a 10nF capacitor (typical) between this pin and GND to reduce output noise.
5	OUT	Regulator output, sourcing up to 150mA.

**POWER MANAGEMENT**
**Marking Information**
**Top Mark**


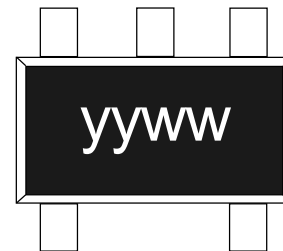
x = package (5 for SOT-23-5, T for TSOT-23-5)  
 3 = SC1453  
 XX = voltage option  
 (examples: 5331 for 3.1V option in SOT-23-5)

**Bottom Mark**


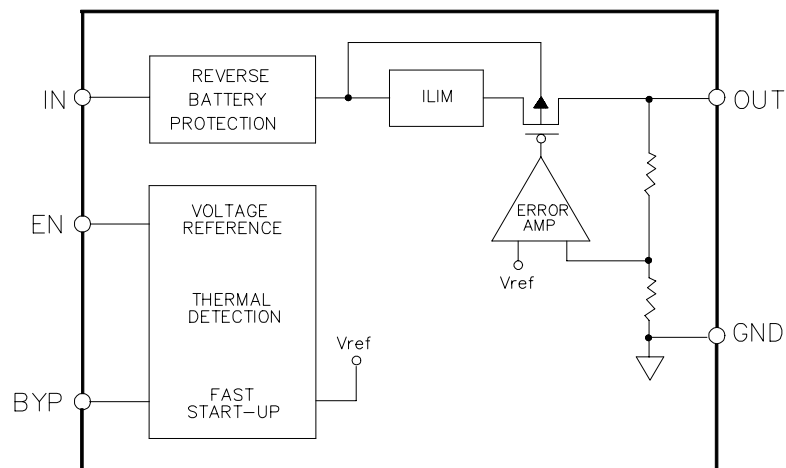
yyww = Date code  
 (example: 0008 for week 8 of 2000)

**Top Mark**


For SC1453, 2.85V option:  
 X = L for SOT-23-5 and N for TSOT-23-5

**Bottom Mark**


yyww = Date code  
 (example: 0008 for week 8 of 2000)

**Block Diagram**


**POWER MANAGEMENT**
**Applications Information**
**Theory Of Operation**

The SC1453 is intended for applications where very low dropout voltage, low supply current and low output noise are critical. It provides a very simple, low cost solution that uses very little pcb real estate. Only three external capacitors are required for operation (two if a low noise output is not required).

The SC1453 contains a bandgap reference trimmed for optimal temperature coefficient which is fed into the inverting input of an error amplifier. The output voltage of the regulator is divided down internally using a resistor divider and compared to the bandgap voltage. The error amplifier drives the gate of a low  $R_{DS(ON)}$  P-channel MOSFET pass device.

An active high enable pin (EN) allows the regulator to be shut down. Pulling this pin low causes the device to enter a very low power shutdown mode, where it will draw typically 0.1 $\mu$ A from the input supply.

A bypass pin (BYP) is provided to decouple the bandgap reference to reduce output noise and also to improve power supply rejection. This pin can be left open if low noise operation is not required.

The regulator has its own current limit circuitry to ensure that the output current will not damage the device during output short, overload or start-up. The current limit is guaranteed to be greater than 400mA to allow fast charging of the output capacitor and high initial currents for DSP initialization.

The SC1453 has a fast start-up circuit to speed up the initial charging time of the bypass capacitor to enable the output voltage to come up quicker (typically 1.3ms with  $C_{BYP} = 10nF$ ).

The SC1453 includes thermal shutdown circuitry to turn off the device if  $T_j$  exceeds 150°C (typical), with the device remaining off until  $T_j$  drops by 20°C (typical). Reverse battery protection circuitry ensures that the device cannot be damaged if the input supply is accidentally reversed, limiting the reverse current to less than 1.5mA.

**Component Selection - General**

Output capacitor - Semtech recommends a minimum capacitance of 1 $\mu$ F at the output with an equivalent series resistance (ESR) of < 1 $\Omega$  over temperature. While the SC1453 has been designed to be used with ceramic capacitors, it does not have to be used with ceramic capacitors, allowing the designer a choice. Increasing the bulk capacitance will further reduce output noise and improve the overall transient response.

Input capacitor - Semtech recommends the use of a 1 $\mu$ F ceramic capacitor at the input. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving overall load transient response.

Bypass capacitor - Semtech recommends the use of a 10nF ceramic capacitor to bypass the bandgap reference. Increasing this capacitor to 100nF will further improve power supply rejection and overall output noise.  $C_{BYP}$  may be omitted if low noise operation is not required.

**Thermal Considerations**

The worst-case power dissipation for this part is given by:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \cdot I_{OUT(MAX)} + V_{IN(MAX)} \cdot I_{Q(MAX)} \quad (1)$$

For all practical purposes, equation (1) can be reduced to the following expression:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \cdot I_{OUT(MAX)} \quad (2)$$

Looking at a typical application, 3.3V to 2.8V at 150mA:

$$V_{IN(MAX)} = 3.3 + 5\% = 3.465V$$

$$V_{OUT(MIN)} = 2.8V - 2\% = 2.744V$$

$$I_{OUT} = 150mA$$

$$T_A = 85^\circ C$$

**POWER MANAGEMENT****Applications Information (Cont.)**

Inserting these values into equation (2) gives us:

$$P_{D(\text{MAX})} = (3.465 - 2.744) \cdot 0.150 = 108\text{mW}$$

Using this figure, we can calculate the maximum thermal impedance allowable to maintain  $T_j \leq 125^\circ\text{C}$ :

$$\theta_{JA(\text{MAX})} = \frac{(T_{J(\text{MAX})} - T_{A(\text{MAX})})}{P_{D(\text{MAX})}} = \frac{(125 - 85)}{0.108} = 370^\circ\text{C/W}$$

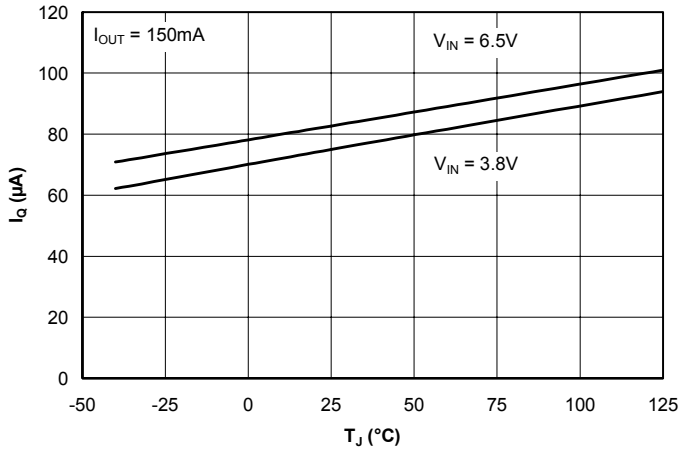
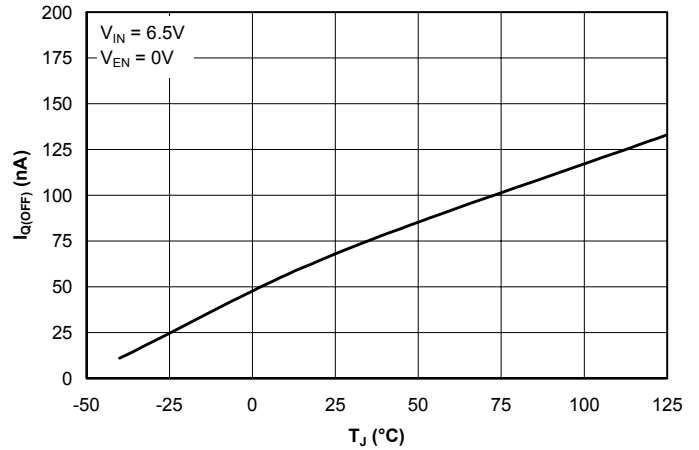
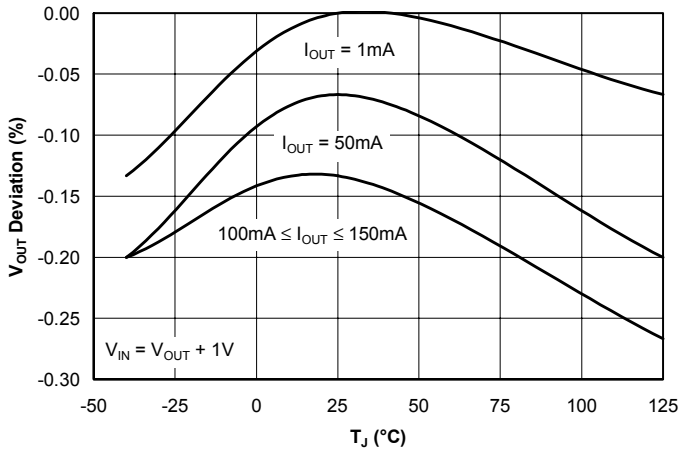
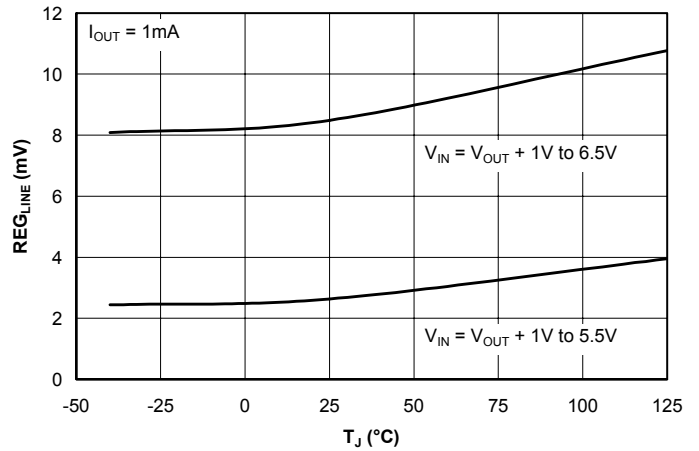
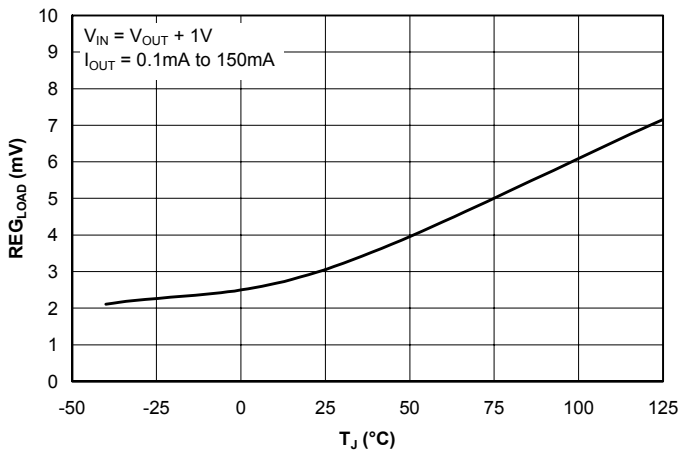
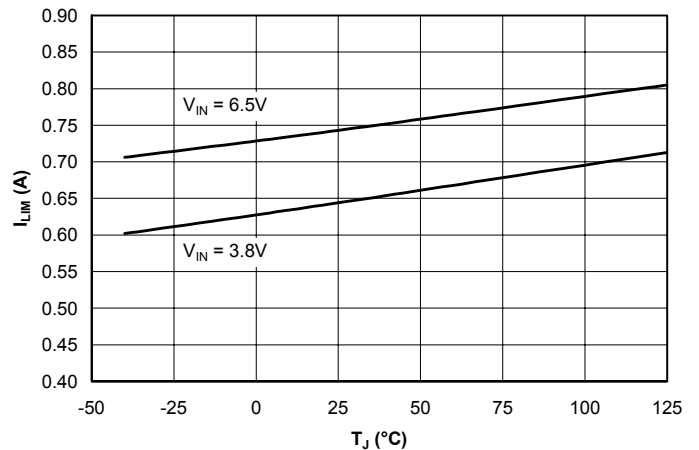
With the standard SOT-23-5/TSOT-23-5 Land Pattern shown at the end of this datasheet, and minimum trace widths, the thermal impedance junction to ambient for SC1453ISK is  $256^\circ\text{C/W}$ . Thus no additional heatsinking is required for this example.

The junction temperature can be reduced further (or higher power dissipation can be allowed) by the use of larger trace widths and connecting PCB copper to the GND pin (pin 2), which connects directly to the device substrate. Adding approximately one square inch of PCB copper to pin 2 will reduce  $\theta_{JA}$  to approximately  $130^\circ\text{C/W}$  and  $T_{J(\text{MAX})}$  for the example above to approximately  $100^\circ\text{C}$  for the SOT-23-5 package. The use of multi layer boards with internal ground/power planes will lower the junction temperature and improve overall output voltage accuracy.

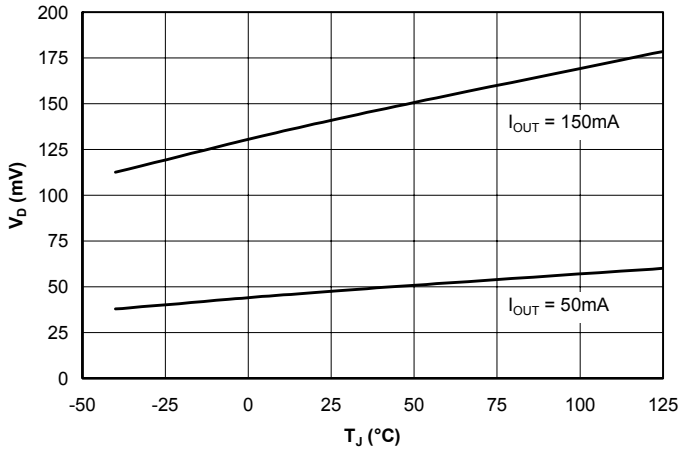
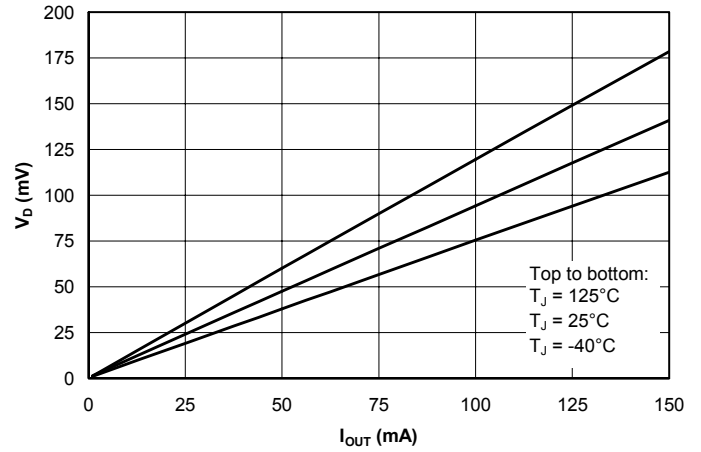
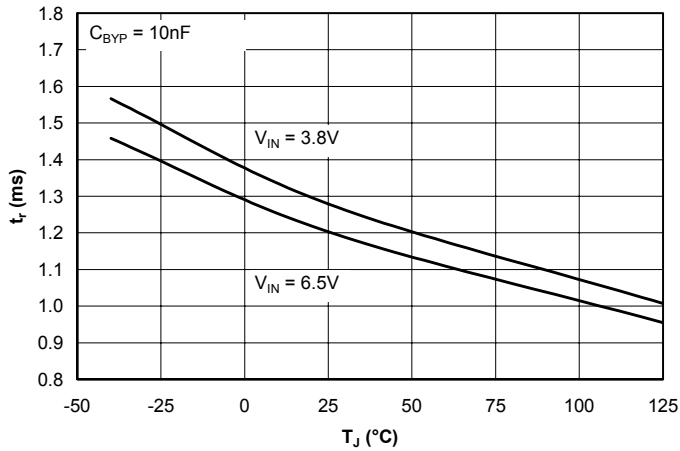
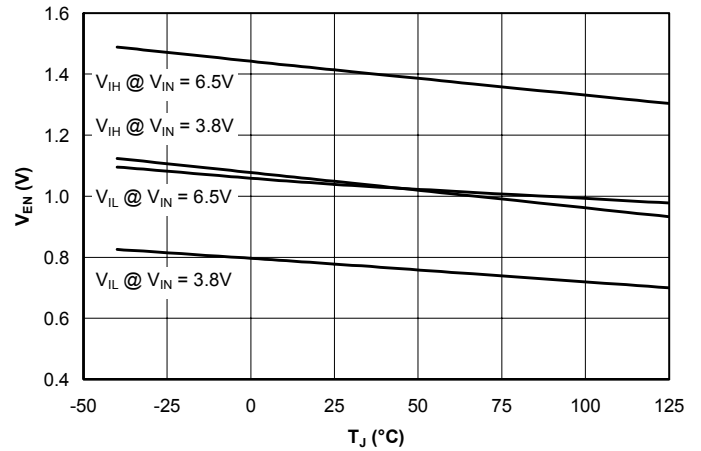
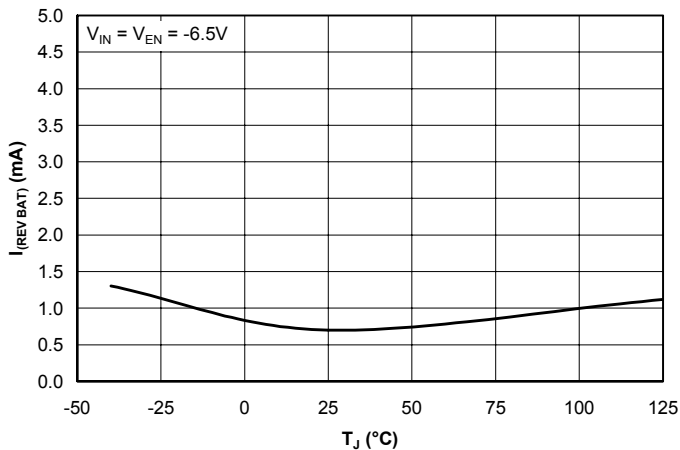
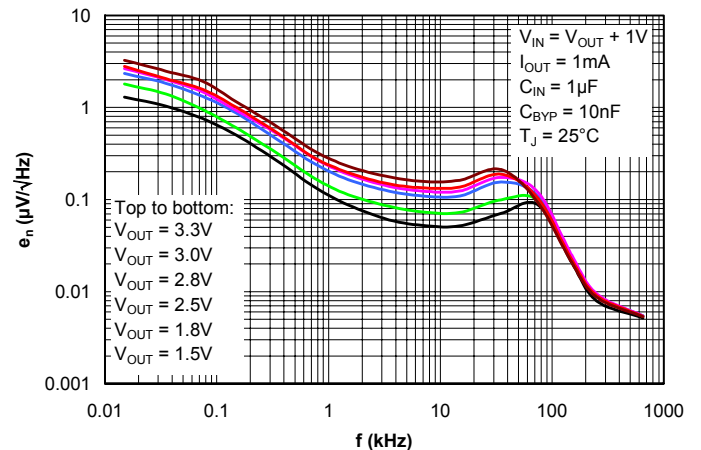
**Layout Considerations**

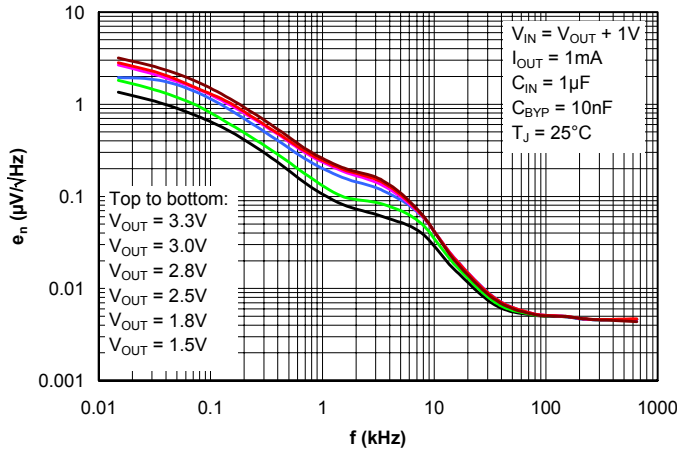
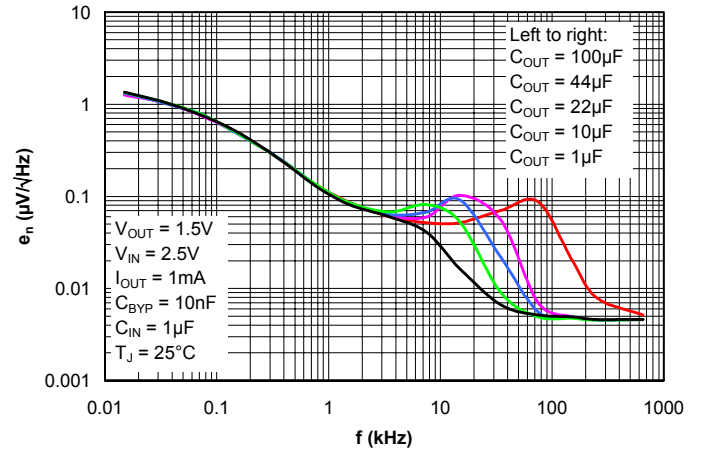
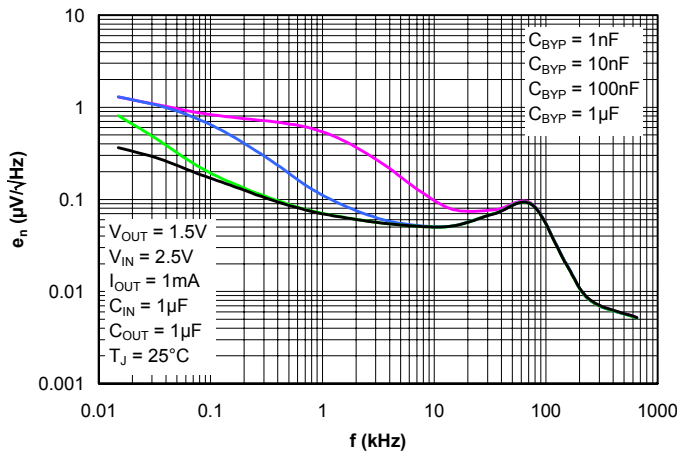
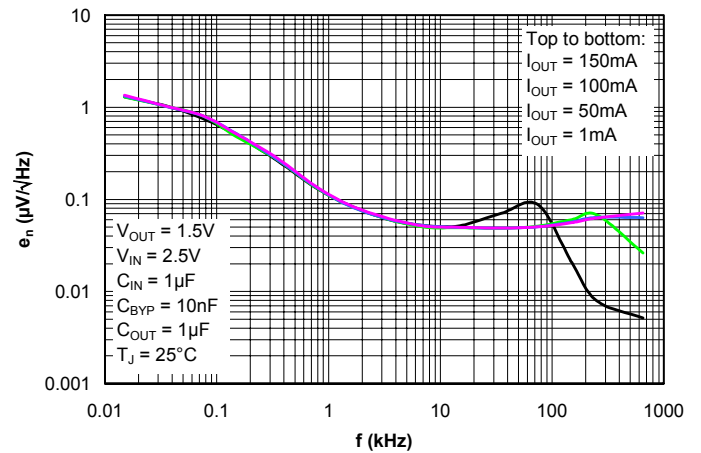
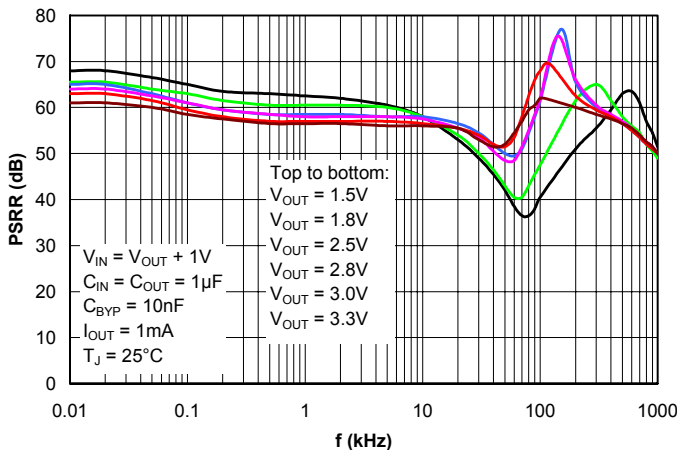
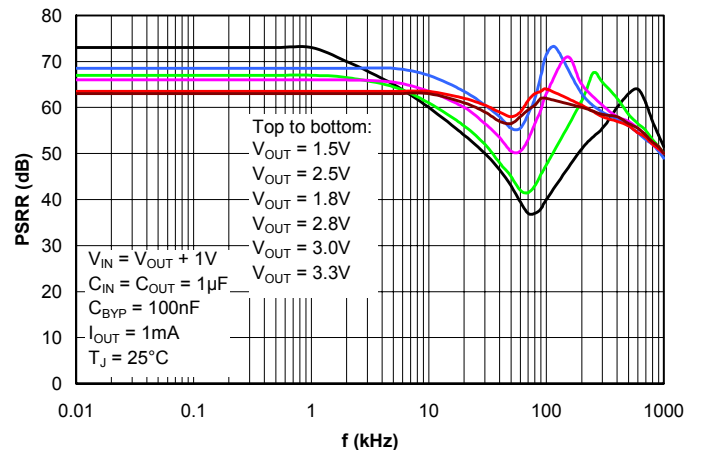
While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation.

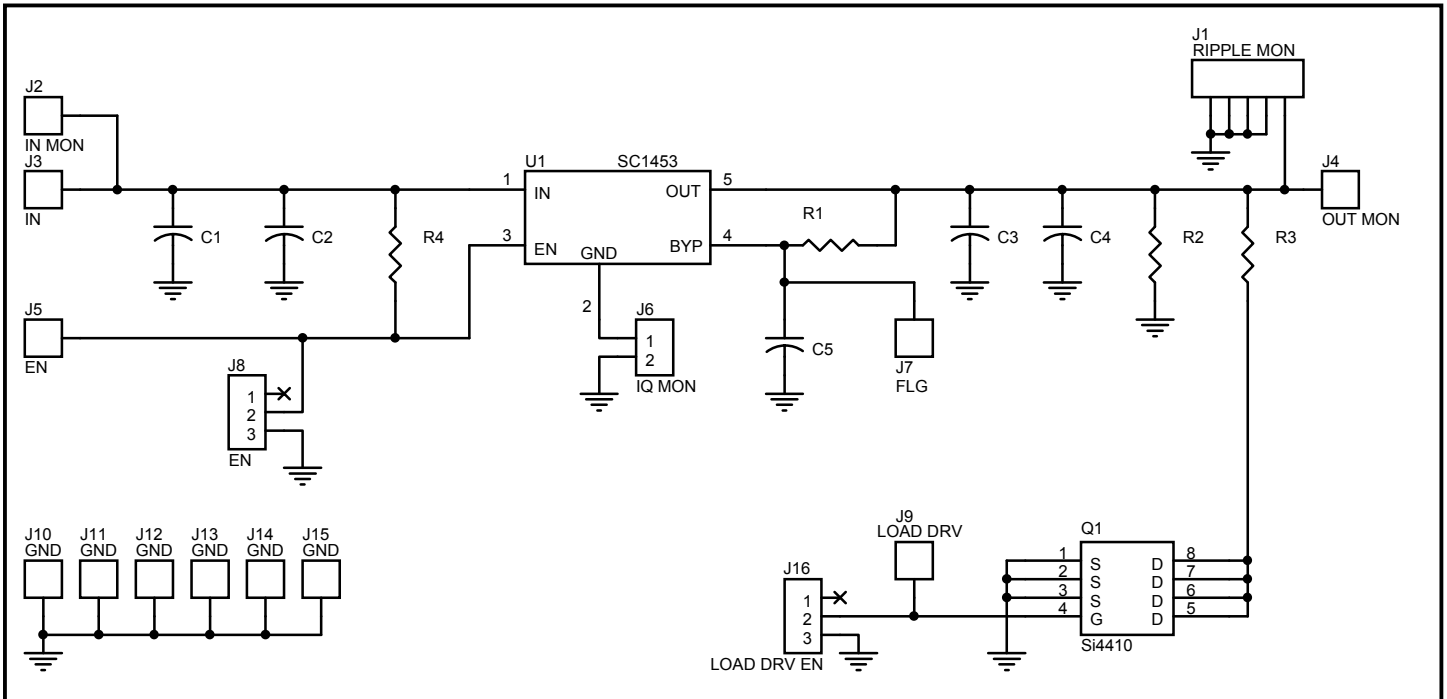
- 1) Attaching the part to a larger copper footprint will enable better heat transfer from the device, especially on PCBs where there are internal ground and power planes.
- 2) Place the input, output and bypass capacitors close to the device for optimal transient response and device behaviour.
- 3) Connect all ground connections directly to the ground plane. If there is no ground plane, connect to a common local ground point before connecting to board ground.

**POWER MANAGEMENT**
**Typical Characteristics**
**Quiescent Current vs. Junction Temperature  
vs. Input Voltage**

**Off-State Quiescent Current  
vs. Junction Temperature**

**Output Voltage vs. Junction Temperature  
vs. Output Current**

**Line Regulation vs. Junction Temperature  
vs. Input Voltage Change**

**Load Regulation vs.  
Junction Temperature**

**Current Limit vs. Junction Temperature  
vs. Input Voltage**


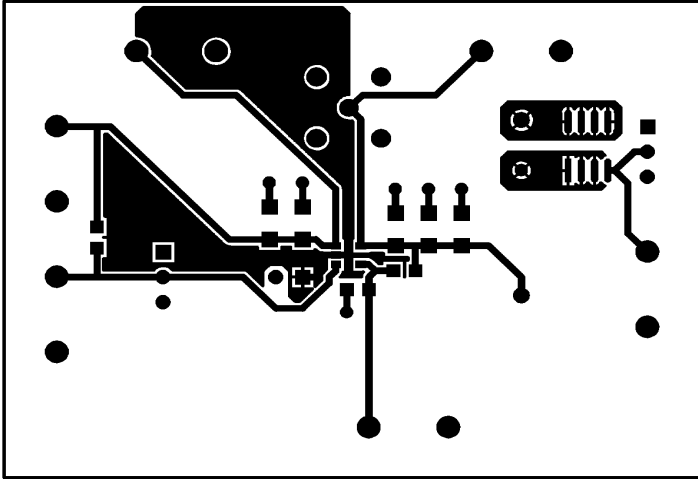
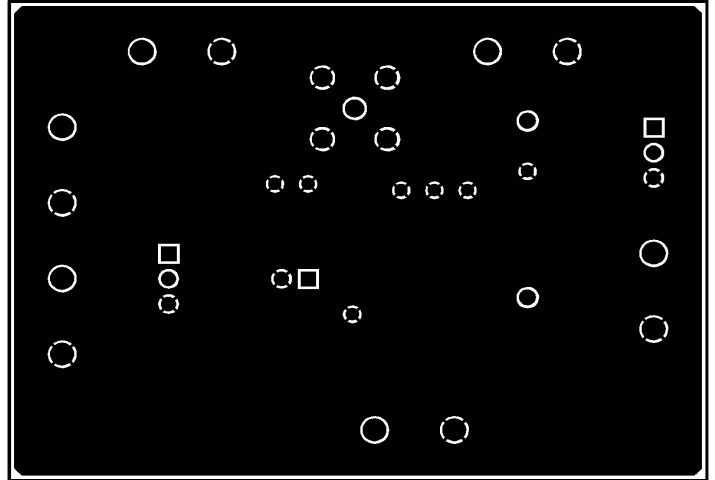
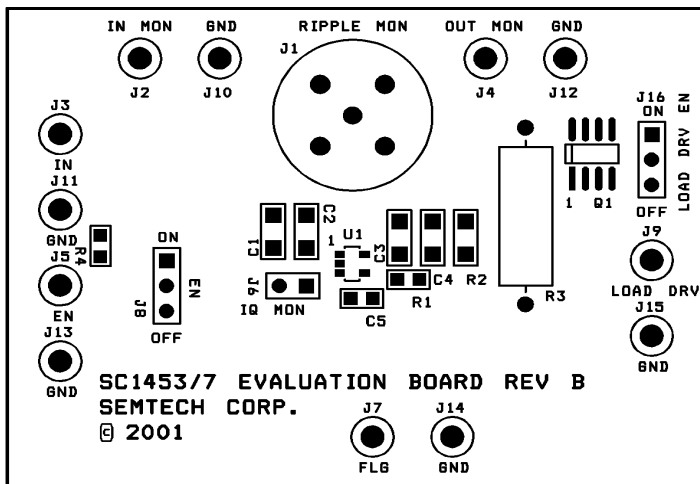


**POWER MANAGEMENT**
**Typical Characteristics (Cont.)**
**Dropout Voltage vs. Junction Temperature vs. Output Current**

**Dropout Voltage vs. Output Current vs. Junction Temperature**

**Bypass Start-up Rise Time vs. Junction Temperature vs. Input Voltage**

**Enable Input Threshold Voltage vs. Junction Temperature vs. Input Voltage**

**Reverse Battery Protection vs. Junction Temperature**

**Output Spectral Noise Density vs. Frequency vs. Output Voltage, C\_OUT = 1µF**


**POWER MANAGEMENT**
**Typical Characteristics (Cont.)**
**Output Spectral Noise Density vs. Frequency  
vs. Output Voltage,  $C_{OUT} = 100\mu F$** 

**Output Spectral Noise Density vs. Frequency  
vs. Output Capacitance**

**Output Spectral Noise Density vs. Frequency  
vs. Bypass Capacitance**

**Output Spectral Noise Density vs. Frequency  
vs. Output Current**

**Power Supply Rejection Ratio vs. Frequency  
vs. Output Voltage,  $C_{BYP} = 10nF$** 

**Power Supply Rejection Ratio vs. Frequency  
vs. Output Voltage,  $C_{BYP} = 100nF$** 


**POWER MANAGEMENT**
**Evaluation Board Schematic**

**Evaluation Board Bill of Materials**

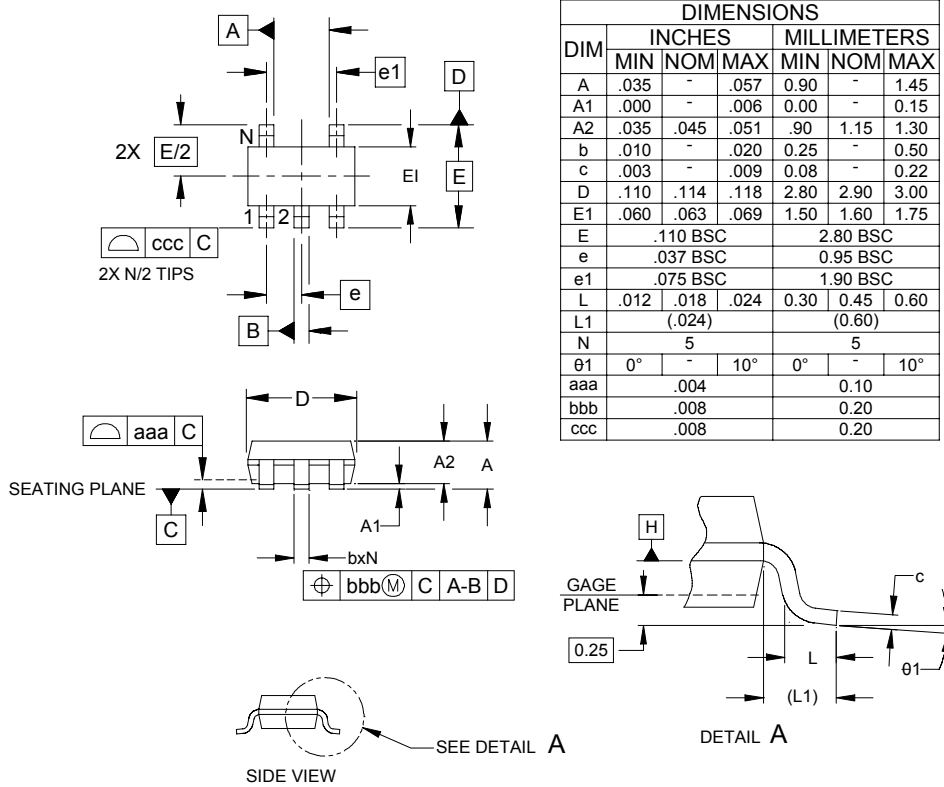
Quantity	Reference	Part/Description	Vendor	Notes
2	C1, C4	Not placed		
2	C2, C3	1 $\mu$ F ceramic	Murata	GRM42-6X7R105K10
1	C5	10nF ceramic	Various	
1	J1	BNC socket	Various	V <sub>OUT</sub> ripple monitor
3	J2 - J4	Test pin	Various	Red
1	J5	Test pin	Various	White
1	J6	Header, 2 pin	Various	
1	J7	Not placed		
2	J8, J16	Header, 3 pin	Various	
1	J9	Test pin	Various	Orange
6	J10 - J15	Test pin	Various	Black (J14 not placed)
1	Q1	Si4410	Vishay	
2	R1, R2	Not placed		
1	R3	See next page	Various	
1	R4	10k $\Omega$ , 1/10W	Various	
1	U1	<b>SC1453ISK-X.X</b> or <b>SC1453ITSK-XX</b>	Semtech	

**POWER MANAGEMENT**
**Evaluation Board Gerber Plots**

**Top Copper**

**Bottom Copper**

**Top Silk Screen**

Output Voltage Option (V)	R3 Value/Size
1.5	10Ω/0.5W
1.8	12Ω/0.5W
2.5	16Ω/0.5W
2.6	16Ω/0.5W
2.7	18Ω/0.5W
2.8	18Ω/0.5W
2.85	18Ω/0.5W
2.9	18Ω/0.5W
3.0	20Ω/0.5W
3.1	20Ω/0.5W
3.2	22Ω/0.5W
3.3	22Ω/0.5W

POWER MANAGEMENT

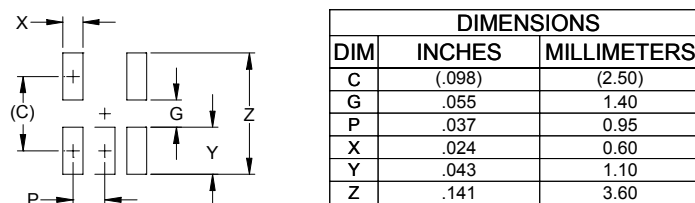
Outline Drawing - SOT-23-5



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SOT-23-5

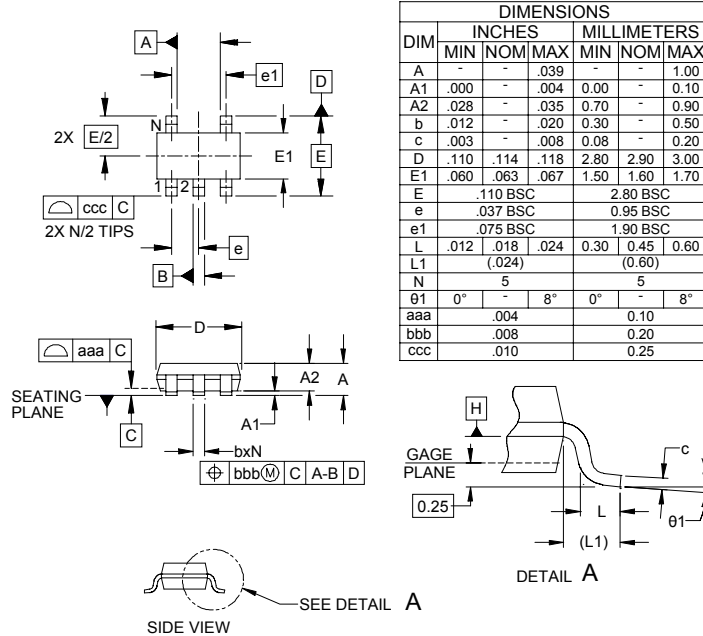


NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

**POWER MANAGEMENT**

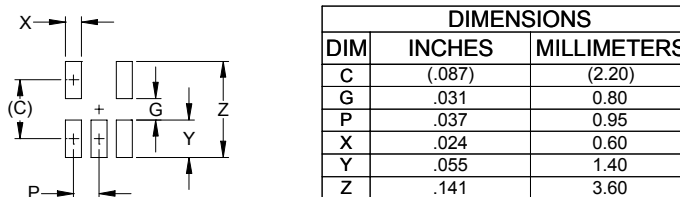
**Outline Drawing - TSOT-23-5**



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.039	-	-	1.00
A1	.000	-	.004	0.00	-	0.10
A2	.028	-	.035	0.70	-	0.90
b	.012	-	.020	0.30	-	0.50
c	.003	-	.008	0.08	-	0.20
D	.110	.114	.118	2.80	2.90	3.00
E1	.060	.063	.067	1.50	1.60	1.70
E	.110 BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075 BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(0.024)			(0.60)		
N	5			5		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.010			0.25		

- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MO-193, VARIATION AB.

**Land Pattern - TSOT-23-5**



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.087)	(2.20)
G	.031	0.80
P	.037	0.95
X	.024	0.60
Y	.055	1.40
Z	.141	3.60

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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