MC74ACT640

Octal 3-State Inverting Transciever1

The MC74ACT640 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus $\overline{A}$ to bus B when T/$\overline{R}$ = HIGH, or from bus $\overline{B}$ to bus A when T/$\overline{R}$ = LOW. The enable input can be used to disable the device so the buses are effectively isolated.

- Bidirectional Data Path
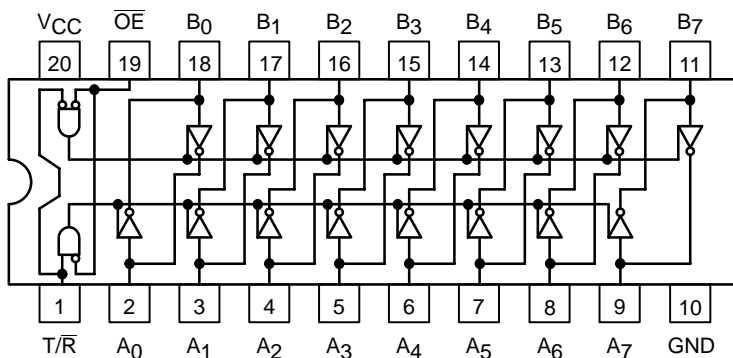- A and B Outputs Sink 24 mA/Source –24 mA
- TTL Compatible Inputs

Figure 1. Pinout: 20–Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
A_0–A_7	Side A Inputs or 3-State Outputs
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
B_0–B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

$\overline{OE}$	T/$\overline{R}$	Applied Inputs	Valid Direction I/P→O/P	Output
H	X	X	X	X
L	H	H	$\overline{A}$ to B	L
L	H	L	$\overline{A}$ to B	H
L	L	H	$\overline{B}$ to A	L
L	L	L	$\overline{B}$ to A	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
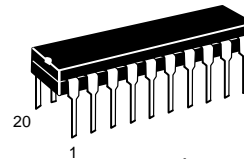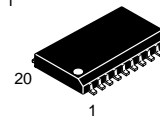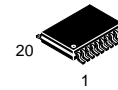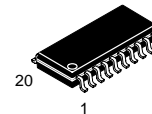
ORDERING INFORMATION

Device	Package	Shipping
MC74ACT640N	PDIP–20	18 Units/Rail
MC74ACT640DW	SOIC–20	38 Units/Rail
MC74AC640DWR2	SOIC–20	1000 Tape & Reel
MC74AC640DT	TSSOP–20	75 Units/Rail
MC74ACT640DTR2	TSSOP–20	2500 Tape & Reel
MC74ACT640M	EIAJ–20	40 Units/Rail
MC74AC640MEL	EIAJ–20	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 5 of this data sheet.

MC74ACT640

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to $+7.0$	V
V_I	DC Input Voltage		$-0.5 \leq V_I \leq V_{CC} + 0.5$	V
V_O	DC Output Voltage	(Note 2)	$-0.5 \leq V_O \leq V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current		± 20	mA
I_{OK}	DC Output Diode Current		± 50	mA
I_O	DC Output Sink/Source Current		± 50	mA
I_{CC}	DC Supply Current per Output Pin		± 50	mA
I_{GND}	DC Ground Current per Output Pin		± 50	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	$^\circ$C
T_L	Lead temperature, 1 mm from Case for 10 Seconds		260	$^\circ$C
T_J	Junction temperature under Bias		$+150$	$^\circ$C
θ_{JA}	Thermal resistance	PDIP SOIC TSSOP	67 96 128	$^\circ$C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V–0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 200 > 1000	V
$I_{Latch-Up}$	Latch–Up Performance	Above V_{CC} and Below GND at 85°C (Note 6)	± 100	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22–A114–A.
4. Tested to EIA/JESD22–A115–A.
5. Tested to JESD22–C101–A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	DC Input Voltage (Referenced to GND)		4.5		5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0		V_{CC}	V
T_A	Operating Temperature, All Package Types		−40	25	+85	$^\circ$C
t_r, t_f	Input Rise and Fall Time (Note 8)	V_{CC} = 4.5 V V_{CC} = 5.5 V	0 0	10 8.0	10 8.0	ns/V
T_J	Junction Temperature (PDIP)				140	$^\circ$C
I_{OH}	Output Current – High				−24	mA
I_{OL}	Output Current – Low				24	mA

7. Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
8. V_{in} from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = +25°C$ Guaranteed Limits	$T_A = -40°C$ to $+85°C$	Unit	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V V	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V V	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V V	$I_{OUT} = -50$ µA
		4.5 5.5		3.86 4.86	3.76 4.76	V V	*$V_{IN} = V_{IL}$ or V_{IH} $\quad$ −24 mA I_{OH} $\quad$ −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V V	$I_{OUT} = 50$ µA
		4.5 5.5		0.36 0.36	0.44 0.44	V V	*$V_{IN} = V_{IL}$ or V_{IH} $\quad$ −24 mA I_{OH} $\quad$ −24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	µA	$V_I = V_{CC}$, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1$ V
I_{OZ}	Maximum 3–State Current	5.5		±0.5	±5.0	µA	V_I (OE) $= V_{IL}$, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD} I_{OHD}	†Minimum Dynamic Output Current	5.5 5.5			75 −75	mA mA	$V_{OLD} = 1.65$ V Max
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	µA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS $t_r = t_f = 3.0$ ns (For Figures and Waveforms, See Figures 2 and 3.)

Symbol	Parameter		V_{CC}* (V)	$T_A = +25°C$ $C_L = 50$ pF Min	$T_A = +25°C$ $C_L = 50$ pF Max	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Max	Unit
t_{PLH}	Propagation Delay	An to Bn or Bn to An	5.0	1.5	8.0	1.0	8.5	ns
t_{PHL}	Propagation Delay	An to Bn or Bn to An	5.0	1.5	8.0	1.0	9.0	ns
t_{PZH}	Output Enable Time	$\overline{OE}$ to An or Bn	5.0	1.5	10.0	1.0	11.0	ns
t_{PZL}	Output Enable Time	$\overline{OE}$ to An or Bn	5.0	1.5	10.0	1.0	11.0	ns
t_{PHZ}	Output Disable Time	T/$\overline{R}$ or $\overline{OE}$ to An or Bn	5.0	1.5	10.0	1.0	11.0	ns
t_{PLZ}	Output Disable Time	T/$\overline{R}$ or $\overline{OE}$ to An or Bn	5.0	1.5	10.0	1.0	11.0	ns

*Voltage Range 5.0 V is 5.0 V ±0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0$ V
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CC} = 5.0$ V
C_{PD}	Power Dissipation Capacitance	45	pF	$V_{CC} = 5.0$ V

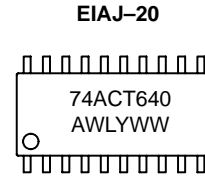# MC74ACT640

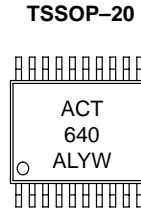## SWITCHING WAVEFORMS
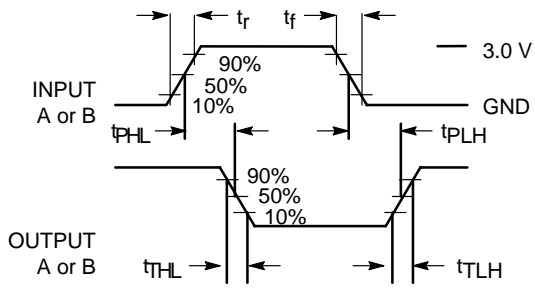
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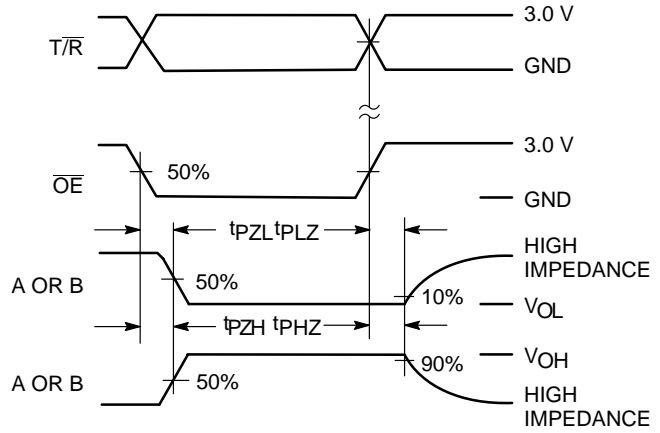
Figure 3.
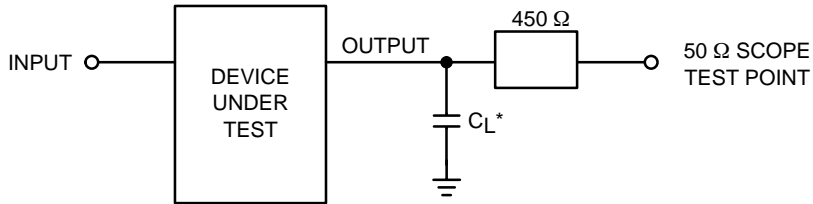
*Includes all probe and jig capacitance
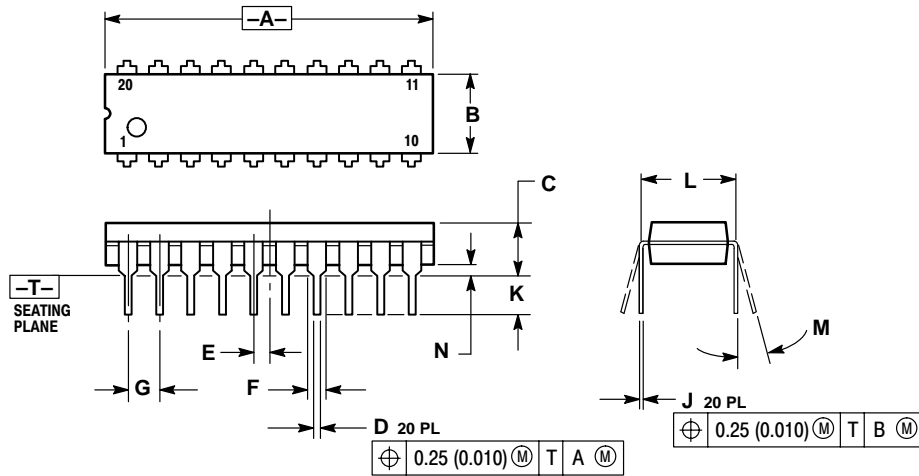
Figure 4. Test Circuit

MC74ACT640

MARKING DIAGRAMS23

PDIP–20	SO–20	TSSOP–20	EIAJ–20

MC74ACT640N
O   AWLYYWW

ACT640
AWLYYWW

ACT
640
ALYW

74ACT640
AWLYWW
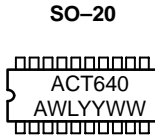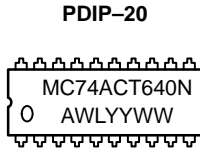
A   = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

PDIP–20
N SUFFIX
20 PIN PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

0.25 (0.010) Ⓜ T A Ⓜ

0.25 (0.010) Ⓜ T B Ⓜ

MC74ACT640

PACKAGE DIMENSIONS

SO–20
DW SUFFIX
20 PIN PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F
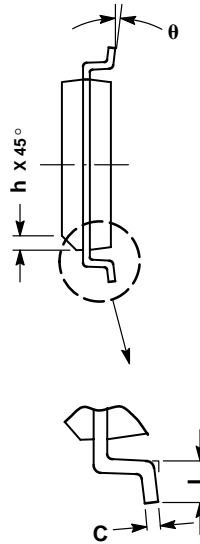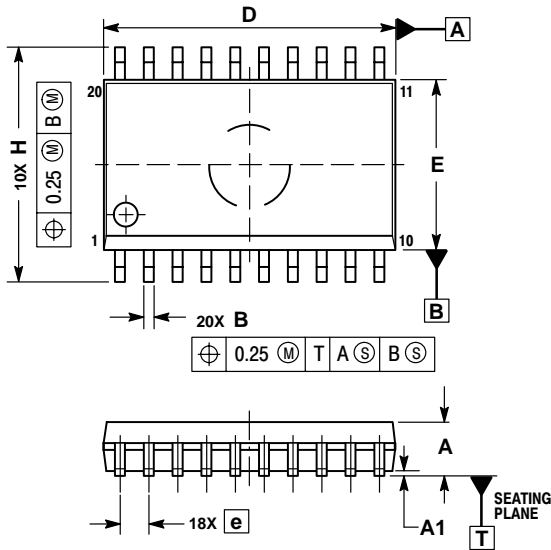
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

TSSOP–20
DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A
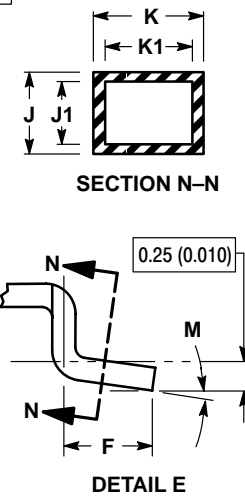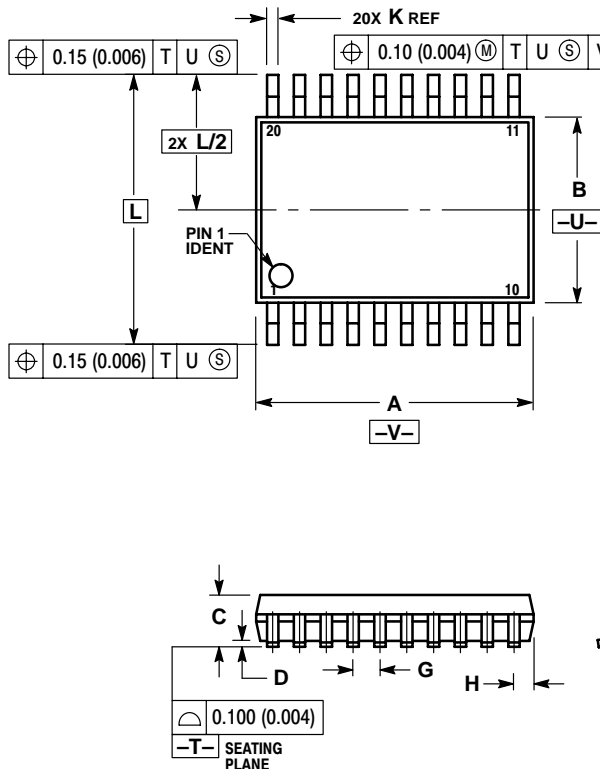
SECTION N–N

DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

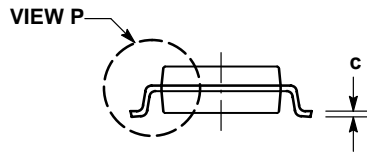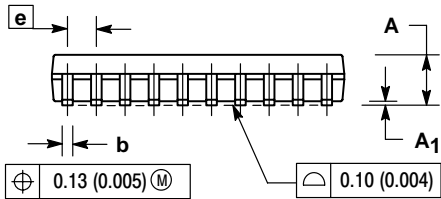| DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74ACT640

PACKAGE DIMENSIONS

EIAJ–20
M SUFFIX
20 PIN PLASTIC EIAJ PACKAGE
CASE 967–01
ISSUE O
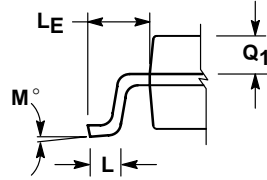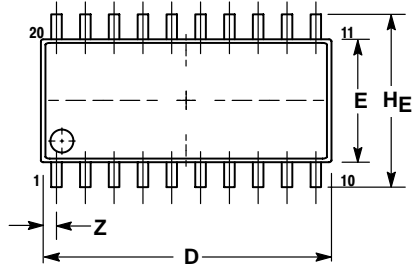
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

MC74ACT640

PUBLICATION ORDERING INFORMATION