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CMOS GATE ARRAYS HD61 SERIES DESIGNER'S MANUAL AND PRODUCT SPECIFICATION

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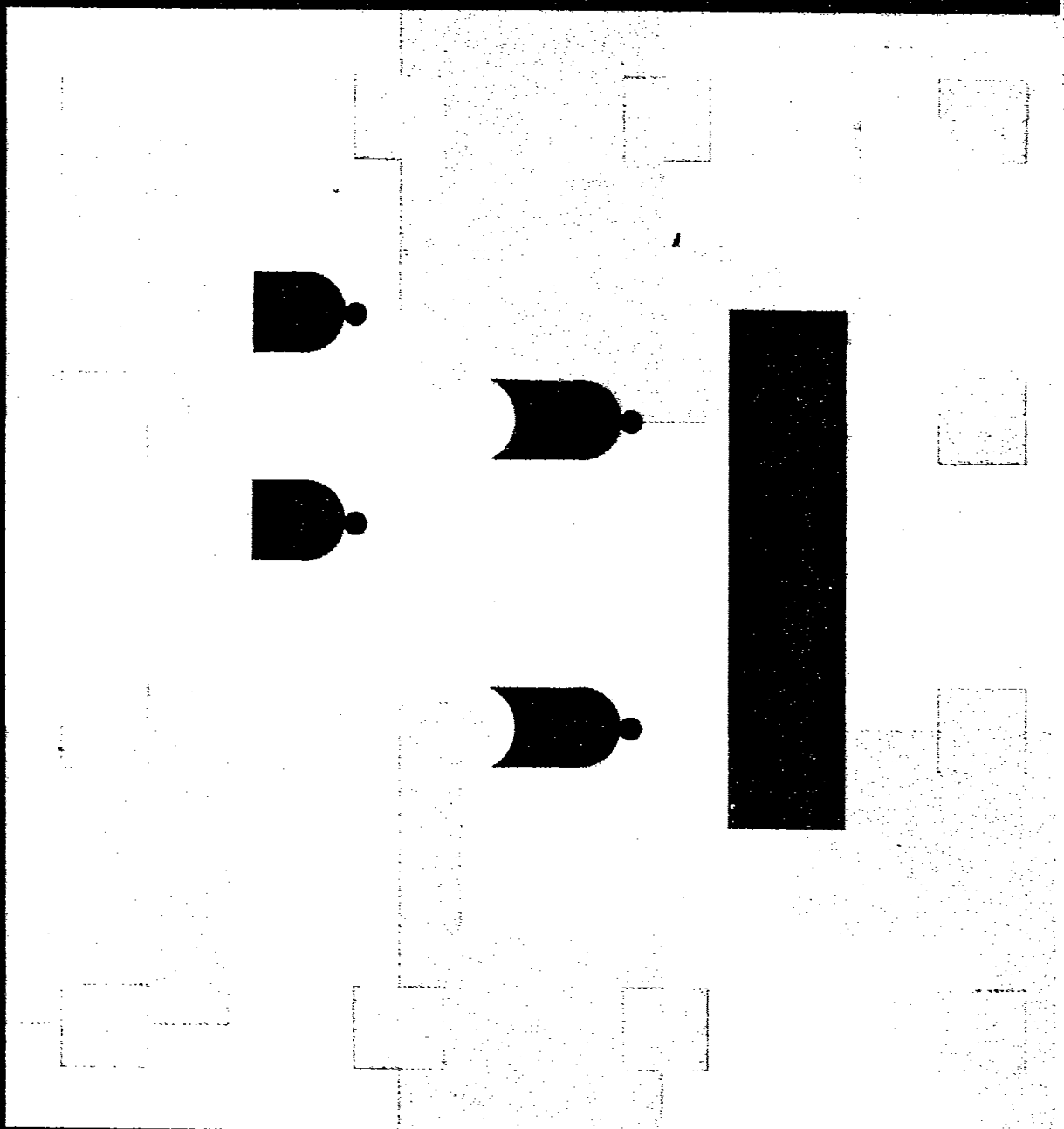

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CMOS GATE ARRAYS
HD61 SERIES
DESIGNER'S MANUAL
AND
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   (B) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, could reasonably be expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

This document is provided as guidance to design a system using a HITACHI CMOS GATE ARRAY. The reader is advised to use both sections of this document in order to gain a full understanding of the techniques and procedures involved.

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SECTION I: HD61 Series Designer's Manual

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1. LOGIC DESIGN

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1.1 GATE UTILIZATION FACTOR

The usual arrangement for laying out gates in a GA is to organize the gates in rows of cells, with gaps between the rows of comparable thickness to the cells so that sufficient space is allowed for connections to be made between cells.
Since layout is performed by a CAD system automatically, as the design becomes more complex and the total gate count of the logic design approaches the total number of gates available, routing of the interconnect becomes immensely difficult, requiring a long engineering period.
To guard against this situation, HITACHI recommends that the gate count utilization is limited to no greater than 90% for 61J, K, L and MM series (without RAM) and 80% for 61MM series with RAM.

Master	Gates	Max. Usage
HD61J	504	450
HD61K	1080	970
HD61L	1584	1420
HD61MM without RAM	2496	2150
HD61MM with RAM	2496	2000

EX.1 Calculation of equivalent gates

Macrocell	Equiv. gates (G)	Number used (N)	Gate Count (G × N)
FD	6	4	24
NA1	0.5	4	2
NA2	1	9	9
NA3	1.5	10	15
NA4	2	1	2
NA6	4.5	5	22.5
EOR	2.5	4	10
Total			84.5

Because input and output buffers are fixed at the peripherals of the gate array, they are ignored in the calculation of total gate count.

EX.2 TTL logic based diagram

When gate count is calculated with an equivalent TTL circuit, refer to the conversion table in section 6.8.

However, care should be taken when interpreting this table since in some situations the gate count assumes that the whole of the TTL function is utilized, whereas in reality only 70-80% might be used.

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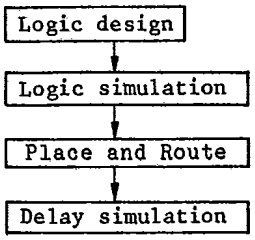
At the time of logic design approximate calculations should be made of the delays that are likely to occur through various logic paths in the GA.

Logic paths which exhibit delays likely to cause problems to the customer's design should then be identified to HITACHI as 'Critical Paths'.

Following simulation, auto routing will yield actual delay times that will occur in the GA which can then be checked by the customer to determine that the design is correct.

The procedure for Delay specification is as follows:



... Rough estimation

... Actual load capacitance will be determined at DA stage

(1) Rough estimation During logic design, estimate the total delay times along the critical path. $td = to + K \times C_L$ $C_L = 0.4 \times EFO$ $EFO = \sum_{F.O.} NLF$	When calculating, refer to the Macrocell library for delay parameters. Those figures are typical, i.e. they represent typical loading conditions for average routing length and fan out. Once the logic is autorouted, more precise delay times for the user defined paths are available from the DA for further analysis.
(2) Designation of critical paths A critical path should be designated when the logic diagram is released to Hitachi.	Delay check report is derived from the actual routing information.
(3) Evaluation of prototype devices Hitachi debugs the prototypes using the test vectors supplied by the user.	The user then evaluates these in the actual system in order to check that timing margins are within the design specification.

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13 FAN-OUT LIMITATIONS

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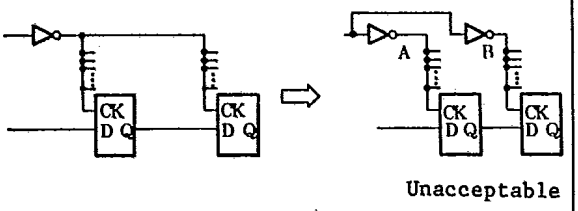
If delay times meet the requirements of the design, then no limitations are placed on fan out. However, in the case of a clock driver for F/F, when the fan out increases tr/tf will degrade until eventually a malfunction occurs.

Maximum fan out for clock drivers

Power inverter 20
Others 10

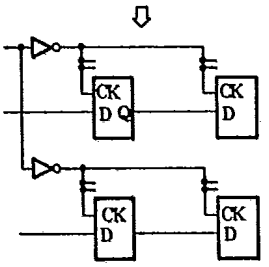
<Example>

Clock skew

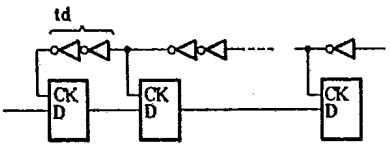


Unacceptable

When a large fan out is required, it is necessary to separate the loads by providing separate drivers. However, in the example shown, the driver may cause a malfunction due to the clock skew between A and B.



Group F/Fs which share the Data in serial.



Delay the clock supplied to the front-end F/F rather than the one which follows.
td ≧5 ns

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14 SIMULTANEOUS TRANSITION OF OUTPUT SIGNALS

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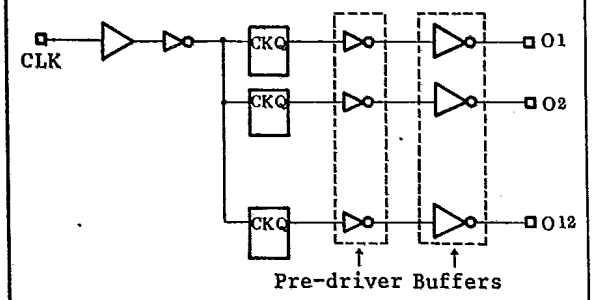
When many outputs change simultaneously, high transition currents are drawn through the ground line. This causes the ground level to swing due to the inductance existing in the chip. Consequently this leads to a reduction in the V_{IH} margin. As a general rule, for the purposes of reducing ground rise, Vcc and ground lines in PCB should be kept wide and short. And simultaneous transitions on output signals should be restricted according to the values shown in the table.

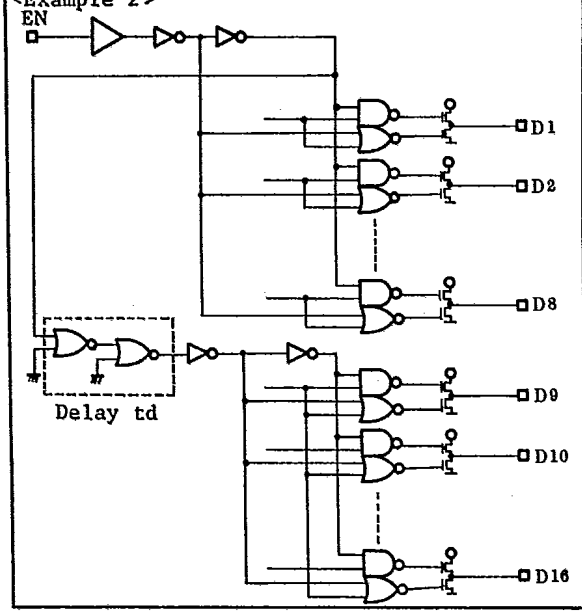
Pre-driver	Max. simultaneous transition
Inverter/NAND	12
2 input NOR	16
3 input NOR	18

<Example 1>



In example 1, inverter pre-drivers are used. In this case, the output should be limited to a maximum of 12.

<Example 2>



This example contains 2 sets of 8-bit bus drivers. Dummy gates are inserted to delay one set of bus drivers from the other.

In this case, data should be consistent during the time the buffer is enabled.

Note: Test vectors should also be stable during this period.

td $\geqq$ 10 ns. Typ.

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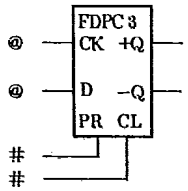
The input pins of unconnected macrocells are automatically modified by the DA and connected to either Vcc or OV. These levels are determined by DA program according to the rules described in the cell library. (Refer to Macrocell Library). Inputs which are not described in the Macrocell library will be connected to "1" (Vcc level) and "0" (GND level) respectively for AND/NAND and OR/NOR Macro. Inputs to other macros must be defined by the user to either "1" or a "0". Under no circumstances must these be left floating.

@ = "1" level

= "0" level

<Example 1>

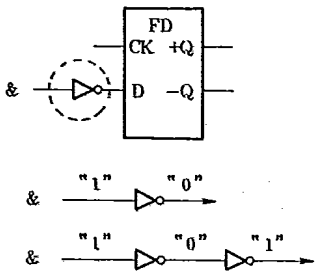


All unconnected pins will be modified as follows:

CK, D .... "1" level

PR, CL ... "0" level

<Example 2>



The DA automatically connects the D input of macrocell FD to "1" level. When an "0" level is required, an inverter should be added i.e. as shown in example 2.

fixed to "0"

fixed to "1"

<Example 3>

Example of macrocells which are not described in macrocell library.

AND/NAND ... "1"

OR/NOR ... "0"

EOR/ENOR ... "0"

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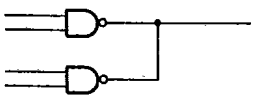
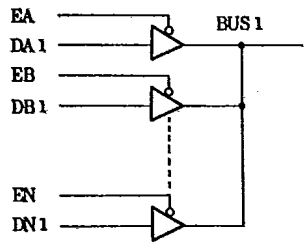
In general it is prohibited to connect multiple outputs together. However, a three-state gate in the core arrays can be used to make the interconnect, provided that multiple output buffers are not enabled simultaneously.



Unacceptable

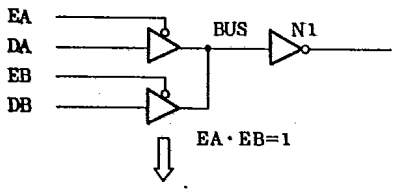
Example 1.



When several ANZs are wired-OR, buffers should not be enabled simultaneously.

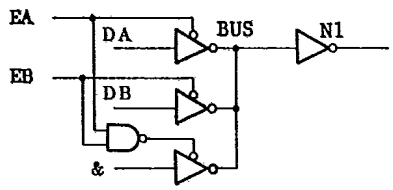
<Example 2>

Floating bus line



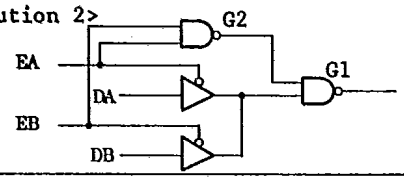
When a bus line is floating, the logic level of N1 becomes undefined, and a current surge is likely to occur.

<Solution 1>



1. Add another three-state buffer which is enabled when all others become off.

<Solution 2>



2. Disable G1 by adding G2.

<Example 3>

Enabled when E=1 and $\bar{E}$=0 Enabled when $\bar{E}$=0

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1.7 PROHIBITION ON LINKED INPUT CONNECTIONS

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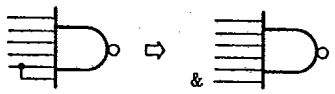
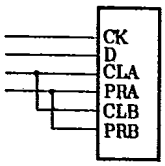
Linked input connections to a macrocell are prohibited. This principle is applied to the equivalent input terminals which will produce the same logic function when they are exchanged.



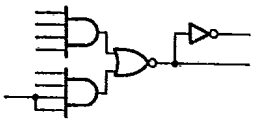
Unacceptable Acceptable

<Example 1> ZSRPC3



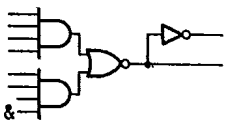
CLA and CLB of ZSRPC3 cell can share the single source because their input terminals are not logically interchangeable.

<Example 2> NR2A4N



Prohibited

Correct



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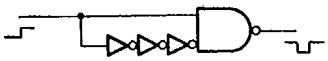
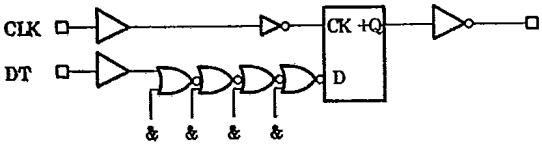
Since layout is automatic, delay times cannot be predetermined. As a consequence, a detection circuit for a rising or falling edge is not implementable.



Prohibited

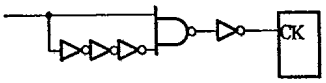
<Example 1> Testable example



In order to ensure that the set-up time is met for F/F types, dummy gates are suggested to introduce a delay.

In such situations, these delay paths should be designated as 'Critical Paths'. (Section 1.2)

<Example 2>



Unacceptable

This circuit is prohibited since the clock pulse width cannot be defined and therefore the circuit is untestable.

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1.9 LATCH BUILT WITH DISCRETE LOGIC GATES

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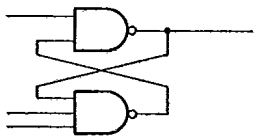
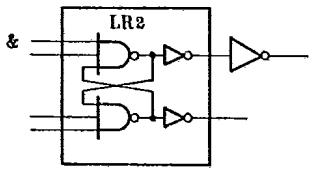
Latch circuit or gate circuit with feed back loop should not be constructed with NAND or NOR logic gates. Instead, flip-flops or latch macrocells should be used.

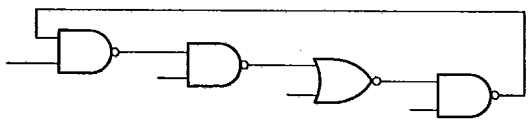
<Example 1> Latch



Should be replaced by



<Example 2> Looped circuit with primitive logic gates



Unacceptable

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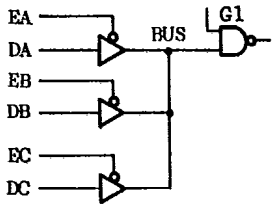
When internal bus could take three-state, a surge current may flow in the gate which is driven by this bus line because of the intermediate input level. In order to prevent these unacceptable conditions the following is suggested:

(1) Do not float the bus line
(2) Gate the successive gates by synchronizing with an enable signal of the bus line

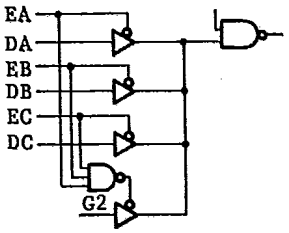
<Example 1>



Enabled when E=0

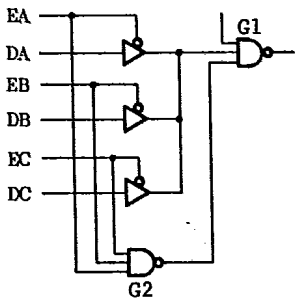
When the condition $E_A=E_B=E_C$ occurs a transitional surge current is likely to occur in successive G1.

Alternative 1



Addition of a dummy NAND gate, G2, forces the extra three-state buffer to "0" level, when E_A, E_B and E_C disable the bus line.

Alternative 2



The additional gate will disable G1 when the bus enters the high-impedance state.

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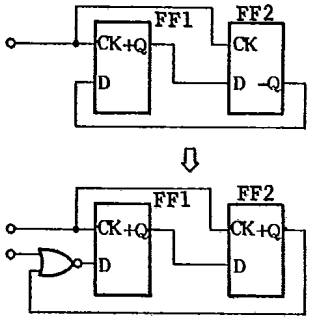
Just after power is applied, the logic states of latches and F/Fs are undefined. Logic should then be initialized with the appropriate test vectors, otherwise the design is not testable. During logic simulation, logic states are also undefined at t=0. As a consequence, the gates in the core have to be initiated step by step, starting with the gates nearest to the GA inputs until finally all gates are in a known state.

<Example 1>

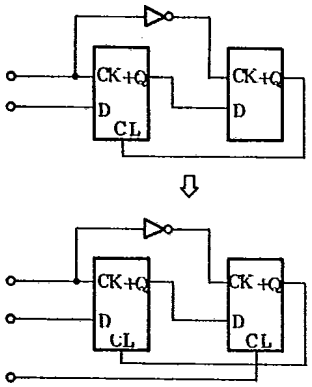
Example of a circuit which cannot be initialized



When an output of FF2 is fed back to the front FF1, it is not possible for these FFs to be initialized.

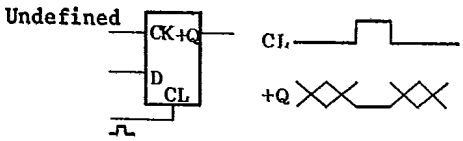
By providing an external control to the data input of FF1, FF1 can be initialized on the first clock and FF2 on the second clock.

<Example 2>

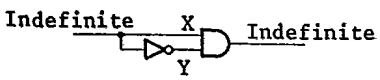


In the actual device, this circuit will be initialized when the data input is "0" and a clock occurs. However, for the simulation a problem will occur because the state of F/F is undefined when either CK, CL or PR are undefined.

<Example 3>



CK, CL & PR should be defined states during initialization.



Even though the relation between X and Y is evident, both X and Y need to be a "1" or an "0".

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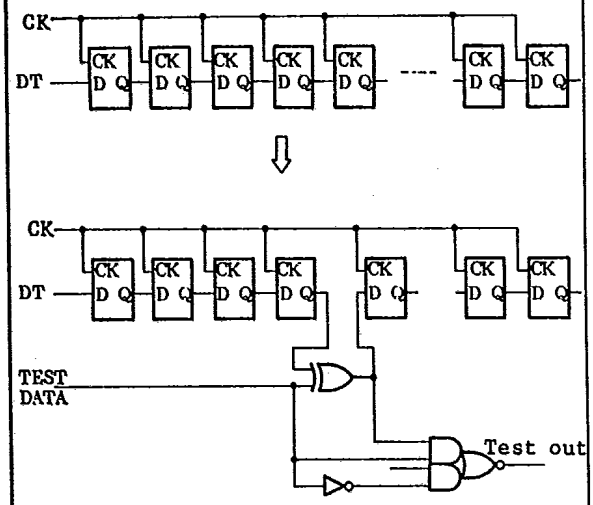
Because the hardware of the tester restricts the number of test vector steps, it is suggested that in the case of many serially cascaded counters, these counters should be split into groups and controlled from an external test pin.

<Example 1> Shift register



In this modification, timing of test DATA such as set-up time and hold time should be restricted so that testing speed is not affected.

Adding an output test pin is recommended to improve the testability from the viewpoint of reducing the number of test vectors.

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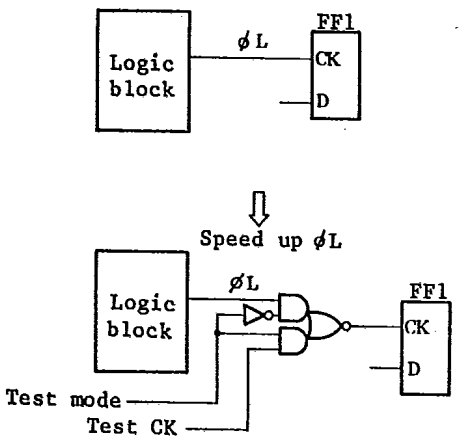
In order to minimize test vectors, (a situation that occurs when the logic configuration of a particular logic block results in long periods, relative to the maximum clock rate, between logic state changes), an effective method that can be used is to include in the logic of the GA a test circuit, controlled (enabled) from an external pin.

<Example 1>



In the example, the repetition rate of ϕL is much slower compared to maximum clock rate. To overcome this problem, a multiplexer can be placed between the logic block and FF1.

If the multiplexer switches when ϕL and TEST CK are both set to a logic "1", a glitch is likely to occur at the CK input to FF1.

Consequently, it is necessary to switch the multiplexer when ϕL and TEST clock are both set to '0' levels.

Note: Function of the multiplexer should not degrade the margin for set-up and hold times of FF1.

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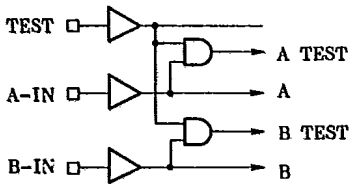
In the event that insufficient pins are available for including test pins, it is suggested that normal function input and output pins would be shared with those used for test functions.

<Example 1>

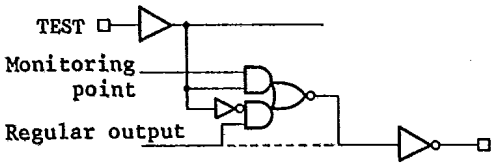
Combining test inputs with normal inputs:



''A TEST'' and ''B TEST'' are enabled when ''TEST'' goes to '1'. In this example regular functional pins A-IN and B-IN are used as test pins in conjunction with ''TEST'' pin.

<Example 2>

Sharing test outputs:



When "TEST" swings to "1" level certain core gates can be monitored. This can be very helpful in shortening the test vectors required, especially when the technique of monitoring the innermost core logic directly at the output pin via a multiplexer is applied.

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1.15 TEST CIRCUIT

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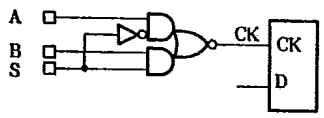
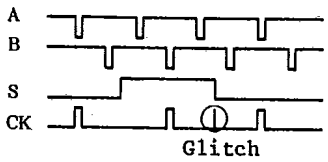
A test circuit is often implemented in order to improve the testability of the logic. The implementation necessarily requires that the timing of the design is such that glitches which can occur at the switching of modes are prevented, and that the margin of set-up and hold times for the F/F is met.

<Example 1>



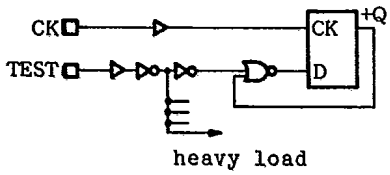


Switching the mode "S" during A = B = "1" causes a glitch due to the delay at inverter. Consequently, switching at A=B=0 is required.

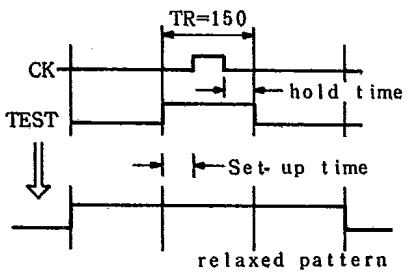
Note: Glitches should be prevented from occuring in the simulation even though they are unlikely to occur in the actual device.

<Example 2>

Margin for set-up time.



F/F may malfunction due to the shortage of set-up time.



Insertion of dummy step may provide a solution.

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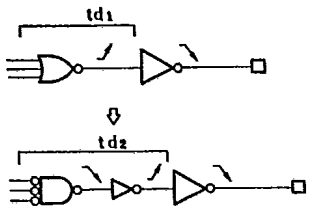
1.16 DRIVABILITY OF PRE-BUFFERS

T-42-11-09

Since the gate capacitance of an output buffer is relatively large, the drivability of pre-buffer should be considered when designed in. If the timing specification is tight, a NAND gate or an Inverter is recommended as a pre-buffer.

Example 1>



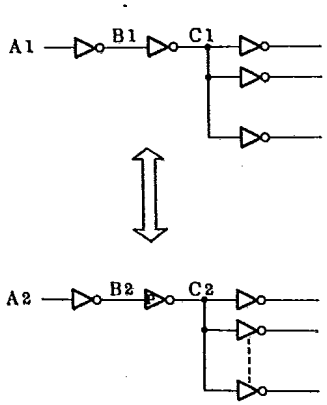
td1 = 16.5 ns

td2 = 9.5 ns

This calculation shows that a NAND gate is faster than a NOR gate.

(Realization of this modification is necessary to invert the related inputs).

Example 2>



Power gates are effective for minimizing the delay time if employed in a heavy loaded path. If, however a path is lightly loaded, delay times can be longer than expected as the load factor of power gates is larger than that of an inverter.

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1.17 CONSTRUCTION OF THREE-STATE BUFFER

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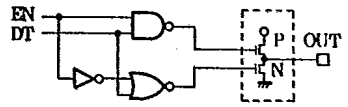
A three-state buffer cell does not provide the control gate but only a pair of C-MOS transistors. Control gates should be prepared from core gates.

An I/O common buffer needs to be designed in the same way since control gates are not included either.

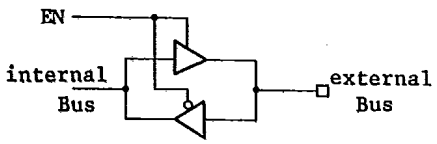
<Example 1>

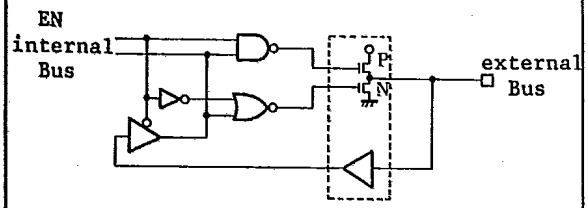


Output buffer cell

In the example the output buffer is enabled when EN = "1" and the output data has the same phase as an internal DT signal.

<Example 2>

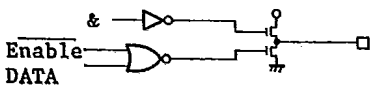




External bus line should not be floating since the input buffer in an I/O common buffer cell is always enabled.

When preparing the test vectors, I/O mode switching timing should be given careful consideration. (Refer to 5.2 page 49)

<Example 3>



Prohibited

Use of a three-state buffer as an open drain buffer with a built in pull up resistor is prohibited.

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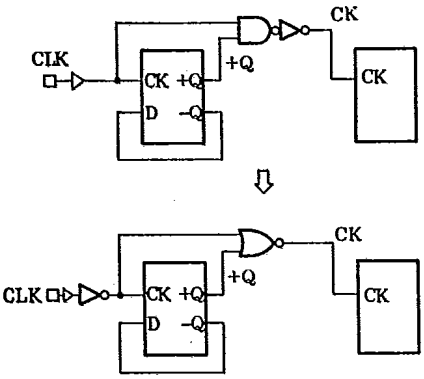
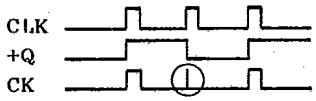
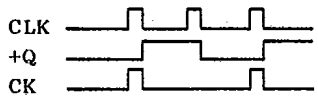
Timings relating to F/F logic should be carefully designed so that pulse width, set-up time and hold time are kept within adequate margins. (The test vectors for F/F types should be given careful consideration too).

<Example 1>

Glitch on clock:

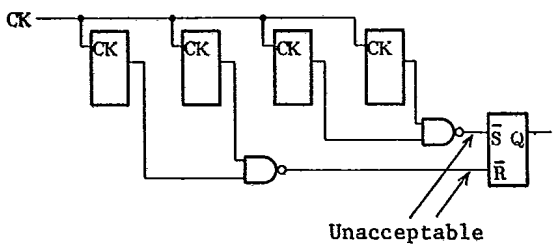






<Example 2>

Synchronous counter:



As outputs from synchronous counters are not exactly synchronized due to the routing path variations and differences in the processing parameters during wafer fabrication, logic should be designed so that such variations have no effect.

If a simultaneous transition occurs on multiple inputs, glitches are easily predictable. However, these are not always observable in the logic simulation.

In the logic design cycle, these logic dependent glitches and critical timing should be studied thoroughly.

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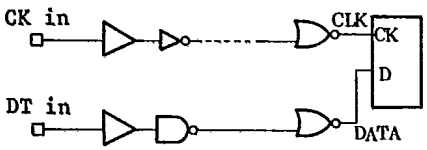
All F/F and latch types require that the following list of parameters be satisfied. The figures listed are the data referenced at the macrocells excluding the delay times along the path.

(Refer to 1.20 regarding synchronous data transmission).

Parameters	Symbol	Times (ns)
Clock pulse width	twck	50 min.
Data set up	tsu	40 min.
Hold time	th	20 min.
CLR, PR to clock	tr	50 min.
Pulse width CL, R	twCL	50 min.
PR, S	twPR	50 min.
R to S	tRS	50 min.
S to R	tSR	50 min.

<Example 1>

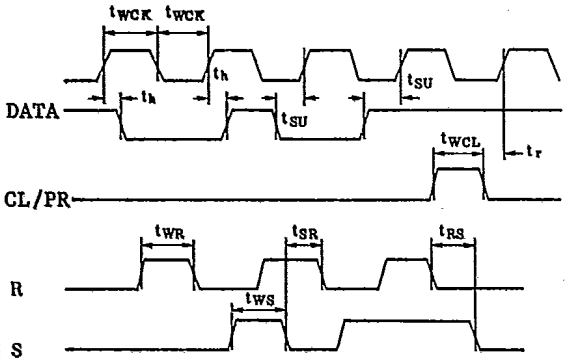


Delay times from CK in to CLK and DT in to DATA should be included when the timings of "CLK" and "DATA" are analyzed.

<Example 2>

It can be seen from the list of timing restrictions that F/F and latch types are allowed to operate up to approx. 10 MHz. However, it may be feasible to handle up to 15 MHz depending on the structure of the logic and the specification.

Timing chart:



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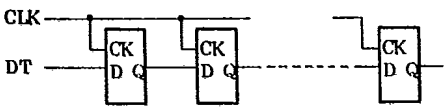
An exceptional application of a F/F type is when used as a shift register or synchronous counter supplied with a single clock and used in serial synchronous data transmission mode.

<Example 1>

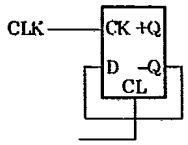
Shift register:



The clock can be shared for multiple F/Fs if serially cascaded. However, splitting the clock drivers may cause a malfunction of F/F types because of clock skew.

<Example 2>

Counter:



This design is acceptable despite a short hold time which is less than the specification.

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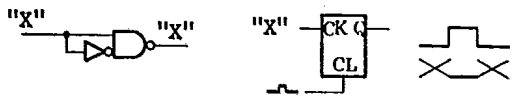
Reasons for discrepancies between the simulation and actual silicon are as follows:

(1) Because of limitations in the simulator model some gates cannot be initialized. (Ref. 1.10)

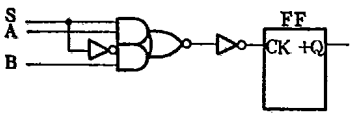
(2) Glitches and spikes while possible in a simulation, do not necessarily occur in the actual device.

(3) Glitches can occur in the silicon due to layout or process variation.

<Example 1>



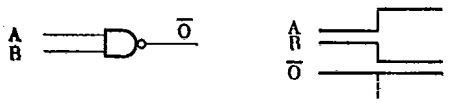
<Example 2>



In the simulation a glitch is observed at the switching during A=B=1, and it will enable F/F.

In the silicon, F/F may not respond to a narrow glitch.
Consequently, it is prohibited to prepare test vectors that are conditional on the glitch to enabling successive gates.

<Example 3>



Even though the glitch is not observed in simulation, since there is no process variation and the timing is exact, in the actual device these variations may occur and so too the resultant glitches.

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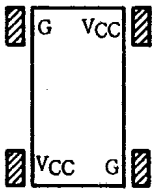
All I/O pins can be assigned by the user except power supply pins.

It is recommended that any noise sensitive functions such as clock for F/F and latch and asynchronous clear inputs should be assigned close to the ground pin. On the contrary, pins which are a source of noise, such as 8-bit bus drivers which switch simultaneously, should be tracked close to the other ground pin.



<Example 1>

It is recommended that pins that are not connected (NC) should not be utilized, but should be connected to power supply pins or be left open.

In Gate Arrays, since all processing of manufacturing is standardized, NC pins are also bonded inside the mould. Consequently, excessive voltage at the package terminals may cause malfunction or damage the chips.

RESTRICTION ON PIN ASSIGNMENT

Assignment of power supply pins is fixed. Modification from this standard should be consulted of its feasibility for each package respectively.

		DP-28	DP-40	DP-42	DP-64	FP-54	FP-80	FP-100	DC-28	DC-40	PGA-72
HD61J	GND	1,15	1,21	1,22		1,28			1,15	1,21	
	VCC	14,28	20,40	21,42		27,54			14,28	20,40	
HD61K	GND	1,15	1,21	1,22	1,33		33,74		1,15	1,21	
	VCC	14,28	20,40	21,42	32,64		31,72		14,28	20,40	
	NC						1,3,22,24,41,43,62,64				
HD61L	GND	1,15	1,21	1,22	1,33		34,74		1,15	1,21	44,72
	VCC	14,28	20,40	21,42	32,64		32,72		14,28	20,40	60,65
	NC						2,3,22,23,42,43,62,63				
HD61MM	GND		1,21		1,33			29,41,79,91	1,15	1,21	
	VCC		20,40		32,64			2,39,52,89	14,28	20,40	

Vcc: 5V ± 5%
GND: 0.V

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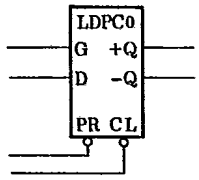
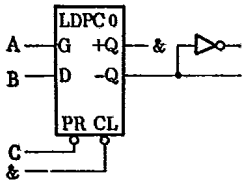
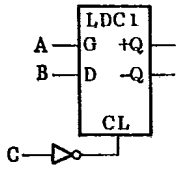
Note 1. LDPC0

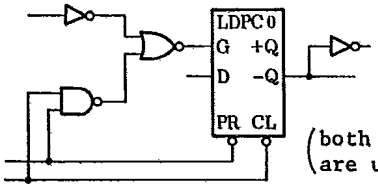




(CL is fixed)



(PR is fixed)

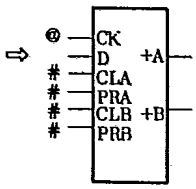


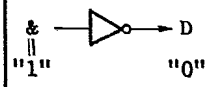
(both PR and CL are used)

1. While clear is enabled, if D = 1 and G goes high both +Q and -Q become "0".

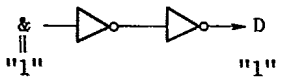
2. While preset is enabled, if D = "0" and G goes high both +Q and -Q become "0".

Note 2. ZSRCP3





D is requested to be fixed "0".



D is requested to be fixed "1".

1. D input of macorcell ZSRCP3 is not automodified when non-connected.

2. The preset function is enabled synchronously to clock, while clear function is enabled asynchronously.

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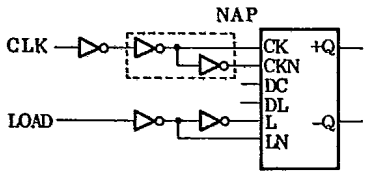
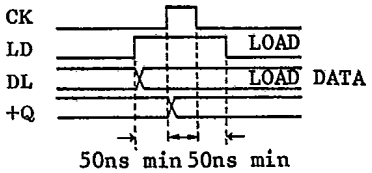
Note 3. FDL



1. CK and CKN need to be driven by a power inverter cell, NAP.

2. Timing of loading data.



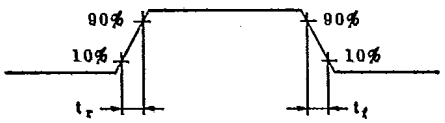
FDL operates the same way as ordinary F/F under the condition of L = 0 and LN = 1.

Note 4. Simultaneous enabling of clear, preset, set or reset

Cell	PR(S)	CL(R)	+Q	-Q
LRS0	0	0	0	0
LRS3	1	1	1	1
LR2S20	0	0	0	0
LR2S23	1	1	1	1
LDPC0	0	0	0	0
FDPC3	1	1	1	1
FJC1	0	0	0	0
ZSRCP3	1	1	0	-

Disabling these signals simultaneously is prohibited because the logic state will be undefined after the signals are released.

Note 5. tr, tf

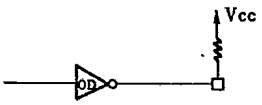


The following waveform is recommended:

$tr \leqq 100$ ns

$tf \leqq 100$ ns

Note 6.



An external pull-up resistor applied to an open-drain buffer should be biased within the same range of Vcc or GND as is supplied to the gate array chip.

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2. DELAY TIMES

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Precise delay times for all logic paths in the GA will ultimately become known once the DA has auto-routed the interconnect. However, before this stage is reached the designer should check, by hand calculation, that the delay times are realizable.

(Refer to the macrocell library for the values "to" & "K".)

Formula

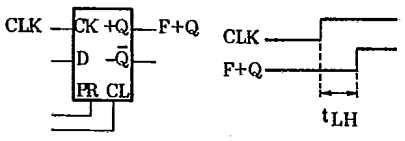
$$t_{pLH} = t_{oLH} + K_{LH} \cdot C_L$$
$$t_{pHL} = t_{oHL} + K_{HL} \cdot C_L$$

LH: Low to High
HL: High to Low

<Example 1> FDPC3

How to calculate delay

Symbol	Symbol No.	Input Name	Output Name	t_{pLH} (ns) t_{oLH}	t_{pLH} (ns) K_{LH}	t_{pHL} (ns) t_{oHL}	t_{pHL} (ns) K_{HL}
FD	C	CK	+Q	4.6	2.4	3.9	1.6
			-Q	5.2	2.2	5.5	1.4
FDL	B4	CK/CKN	+Q	2.5	2.5	3.1	2.1
		L/LN		7.7		9.0	
		CK/CKN	-Q	4.3	2.2	3.6	1.4
		L/LN		10.7		8.5	
FDPC3	C	CK	+Q	5.4	4.4	4.2	1.7
		CL		2.5		1.2	1.7
		PR		5.5		—	—
		CK	-Q	6.8	4.4	6.8	1.5
		CL		5.8		—	—
		PR		4.0		1.5	1.5



tLH: Low to high at(F + Q)
when calculating from a rising CK edge.

1. Select the related inputs (CK, +Q)
2. Pick out the figures
   (t_{oLH} = 5.4, K_{LH} = 4.4)
3. Calculate according to the formula
   $t_{pLH} = 5.4 + 4.4 \times C_L$ (ns)

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Loading capacitance is obtained from the summation of input capacitance and stray capacitance which exists in the inter-connection metal layer.
The DA supplies the ultimate precise value of capacitance, however, during the logic design phase capacitance is estimated as 0.4 pF/inverter gate.

Effective fan-out

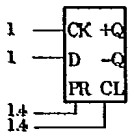
$$EFO = \sum_{F.O.} NLF$$

Total capacitance

$$C_L = 0.4 \times EFO \ (pF)$$

NLF: Refer to cell library

<Example 1> NLF

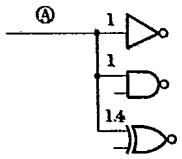


CK : 0.4pF
D : 0.4pF
PR : 0.56pF
CL : 0.56pF

The value 0.4 pF, which is equivalent to the inverter's input capacitance, is the basic unit load that represents a typical loading including typical routing stray capacitance.
NLF is the normalized load factor.

Load capacitance = 0.4 × NLF (pF)

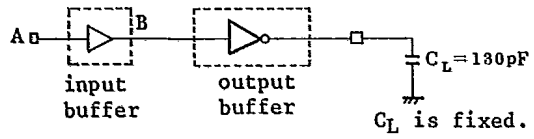
<Example 2> EFO



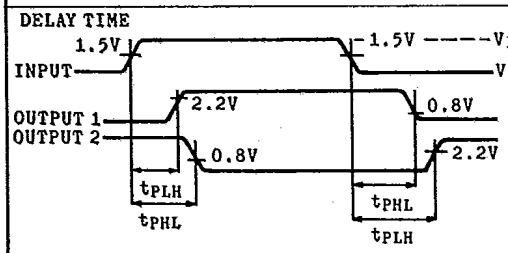
EFO=3.4
CL=0.4×3.4
=1.36(pF)

EFO is the summation of all NLF which are attached to the output node.

<Example 3>



130 pF should be used for output buffers, as this is the value that appears at the tester. This means that the delay times are guaranteed at capacitance level of 130 pF.



Input buffer delay is defined from the input reference level (V_{IH}, V_{IL}) to output reference level (V_{OH}, V_{OL}).

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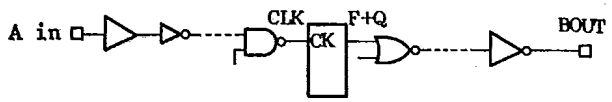
Typical delay times are obtained by the formula shown in 2.1. These values vary depending on the operational conditions such as environmental temperature, power supply tolerance, variation of wafer processing and as a result of errors existing within the calculation.

Variational range:

Min. = 0.3 × typ.
Max. = 2.2 × typ.

<Example 1> Critical Path:



Delay checking list

No	Critical path	Requirement(ns)
	A in ∫∿ B out ⌉	180

Indicate the points of origin and termination when the path is unique.

Designate the interadjacent nodes when the signal has multiple routes between the original and the termination.

ex: AIN∫∿CLK∫∿ (F + Q)⌉∿Bout⌉

<Example 2>

Delay times after auto-layout

Delay times of critical paths which are calculated using actual loading capacitance, are supplied after auto-layout (place & route).

Variation after layout:

Min. = 0.4 × typ
Max. = 2.0 × typ

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The procedure for delay calculation for the logic diagram in section 6.6 is shown below.

Example 1> Path 1:

Clock↗ ∿ FFA + Q↘ ∿ CAA↗ ∿ A 306↘ ∿ RCA↘

No.	input ∿ output	Cell	Ⓐto	ⒷK	ⒸEFO	ⒹCL	td
1	Clock -ClockI↗	ANI	7.7	2.0	4	1.6	10.9
2	ClockI↗-FFA+Q↘	FD	3.9	1.6	2.4	0.96	5.4
3	FFA+Q↘-CAA↗	EOR	4.2	4.5	9.0	3.6	20.4
4	CAA↗-A306↘	NA6	6.0	2.0	1	0.4	6.8
5	A306↘-A332↗	NA2	1.3	3.6	4.7	1.88	8.1
6	A332↗-RCA↘	NAOT	4.0	0.34	-	130	48.2
7	total						99.8

Maximum delay time = 99.8 x 2.2
= 220 (ns)

EFO = ΣNLF
fan out

$C_L = 0.4 \times EFO$

$td = to + KC_L$

<Example 2> Path 2:

Clock I↗ ∿ FFA+Q ↗ ∿ CAA↗ ∿ A317↘ ∿ FFD+2↗

No.	input ∿ output	Cell	Ⓐto	ⒷK	ⒸEFO	ⒹCL	td
1	ClockI↗∿FFA+Q↗	FD	4.6	2.4	2.4	0.96	6.9
2	FFA+Q↗∿CAA↗	EOR	4.2	4.5	9	3.6	20.4
3	CAA↗∿A317↘	NA6	6.0	2.0	1	0.4	6.8
4	A317↘∿FFD+2↗	NA3	2.0	3.9	1	0.4	3.6
5	total						37.7

Maximum delay time = 37.7 × 2.2
= 83 (ns)

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3. TEST VECTORS

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A test vector is the expression of translated functions which should be implemented in the GA. Test vectors are utilized not only for the functional verification of the logic but also for final testing during the mass-production phase.

<Example 1> Contents of test vectors: 1. DC parameter test 2. Function test 3. High speed operational test. Fundamentally, functional test vectors are the only ones which are usually required from the customer. However, a high speed operational test vector may be required if the functional test vectors are not adequate.	* DC parameter test: Output level (V_{OH}, V_{OL}), input leakage, (I_{LI}), output leakage of three-state buffer and/or open drain buffer (I_{LO}) are tested. Since these items are automatically compiled from the function test vector, it should contain all logic states within 2000 steps. * Functional test: For the functional test the logic function fault coverage should be greater than 95%. It is suggested that input/output timing is similar to that required for the actual application. * High speed operational test: If requested, high speed tests will be applied and may be abbreviated if the required speed is slow. If the functional test vectors are not applicable to this test, another set of test vectors will be requested: (1) When there are major differences in delay times from multiple outputs. (2) When strobe timing is critical because of high test rate and also because of large delays due to the 130 pF loading capacitance.
<Example 2> Timing test: 1. Timing tolerance (set up, hold time) 2. Cycle time 3. Absolute delay times 4. Time difference between output pins	← input timing ← test rate ← strobe timing ← not applicable

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The following faults are injected (single stuck at "1" or stuck at "0".

1. Input of all logic gates - "0" "1"

2. Output buffer - "0" "1"
   excluding: internal gates of macrocell
   : indistinguishable equivalent faults (collapsing)

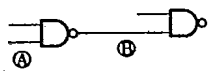
Definition:

"0" injection = fault stuck at "0"
"1" injection = fault stuck at "1"

Injections

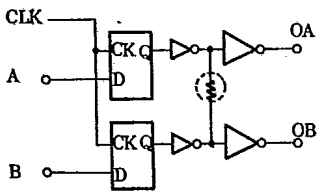
AND/NAND	"1"
OR/NOR	"0"
EOR	"0" "1"
D input (F/F)	"0" "1"
Output pin	"0" "1"

<Example 1> Equivalent fault:



The stuck at "0" fault at node Ⓐ is equivalent to a stuck at "1" fault at node Ⓑ In this case stuck at "0" fault at Ⓐ is not injected.

<Example 2> 0/1 fault injection:



A fault is detected by comparing the fault injected simulation with a normal (fault free) simulation.

However, faults may go undetected if incorrect test vectors are applied to the input of a particular logic function.

In the left figure, a fault shown will not be detected by the test pattern (A,B) = (0,0), (1,1) even though this gives a coverage of 100%. To detect this fault requires the pattern (A,B) = (1,0), (0,1) to be applied.

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Faults are ultimately detected at the output terminals of the GA, after the error in the logic function during the simulation is propagated to the terminals.

Since fault coverage has the dominant influence on the quality of the products, the acceptable coverage level is at least 95%.

$$\text{Fault coverage} = \frac{\text{detected faults}}{\text{total injected faults}} \times 100\%$$

Acceptable coverage $\geqq$ 95%

<Example 1>

A 0/1 stuck fault is detectable when the node provides both 0/1 logic levels and the condition can be observed at the related output pin. This concept should be considered when designing test vectors.

<Example 2>

Transition characteristics:

Transition times (Tr/Tf) are not involved in fault simulation but DC 0/1 levels are considered. Delay times should be tested by a separate functional speed test.

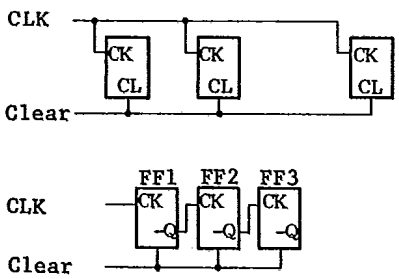
<Example 3>

Detection of level-fixed node:

Macrocell pins which are clamped to Vcc or OV are excluded from the fault simulation.

<Example 4>

Detection of clear signal of counter:



Detection of signal at the clear pin of an F/F is achieved by the following procedure:

1. Set the F/F at "1", first.
2. Enable the clear pins.
3. Supply the clock so that the state of all F/Fs is transferred to the related output pin.

This example highlights the case which requires a relatively longer test pattern. Also, enabling the clear input after setting all F/Fs to a "1" level is invalid. This is because when the clear input is enabled -Q of FF1 goes high. Consequently, it is not possible to distinguish if the F/F2 was activated by CK or the clear signal.

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Just after the power is supplied to the GA, the logic states of all the gates are initially unknown. Therefore a requirement of the test vectors is that an initialization sequence should be included as part of the test set.

This is an important consideration, since even though the hardware may allow for external synchronization, the testing method is standardized and cannot be modified.

<Example 1> Number of vector steps: The synchronous clear function is often employed for counters and for minimization of the gate count. Consequently, F/F types or counters need a well organized test circuit so that the whole circuitry can be cleared by single pulse or within a few steps.	Since the number of test vector steps is limited, efficient initialization is absolutely essential.
<Example 2> Splitting of test vectors into separate sets: It may be convenient to separate the whole logic into a number of blocks and prepare the test vectors accordingly. However, even in this case, it is recommended that the whole logic is initialized in the first group of vectors that are submitted.	If some portions of the logic remain uninitialized, problems may result when designing the test vectors for another portion. Initialization of the whole logic can help to minimize the steps since the portions which are not being tested may operate anyway.

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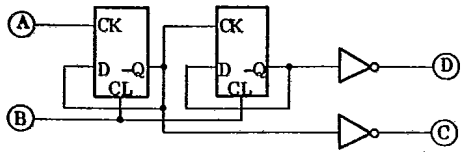
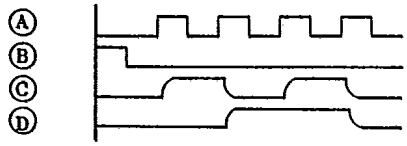
Test vectors should be binary coded using the formated test vector sheet.

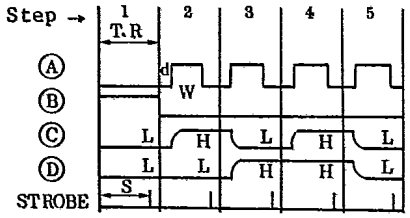


Timing chart



Procedure for converting a timing chart into binary coding.

1. Designate the cycle time of the fastest input. ⇨ test rate
2. Specify the clock wave form of (1). ⇨ PP/NP, delay, pulse width
3. Define the timings of other signals referring to the clock. ⇨ PP/NP, delay, pulse width for the clocks & delay time for DT
4. Check the timing of all outputs assuming zero delay for all gates.
5. Calculate the delay times.
6. Designate the output which has the largest delay time (or the smallest delay time). ⇨ strobe timing
7. Decide the strobe timing according to (6).



Step	1	2	3	4	5
A	0	1	1	1	1
B	1	0	0	0	0
C	L	H	L	H	L
D	L	L	H	H	L

Binary coding

or

Step	1	2	3	4	5
A	0	1			
B	1	0			
C	L	H	L	H	L
D	L		H		L

abbreviated expression

In order to decide the timing definition, operation of an F/F type should be considered with regard to the followings:

1. Set-up time, hold time
2. Timing tolerance between the rising edge of the CK and disabling edge of CL or PR inputs on the F/F.

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4. GATE ARRAY FORMATTED LOGIC DRAWING

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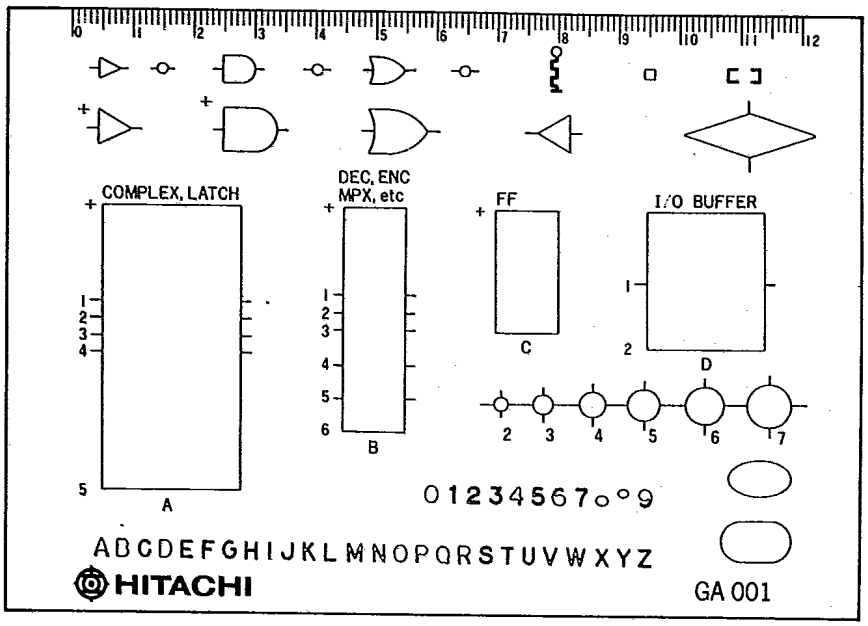
The drawing sheet and templates will be supplied by Hitachi to the customer. Size of sheet is A3.

(1) Refer to the drawing sheet in section 6.4

(2) Use the template shown below



(Actual size)

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It is required that logic diagrams be drawn with HITACHI templates.

* Refer to the Macrocell library for symbols. Draw the schematic using the same function names, terminal names and the sizes as given in the library.

* Complex gates enclosed with dotted lines can be described in an abbreviated form with only the function name. The input location will be the same as in the non-abbreviated case.

<Example 1>

Complex gate use

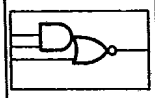
Ordinary gate use

For complex gates enclosed with a dotted line. (Refer to Macrocell Library.)

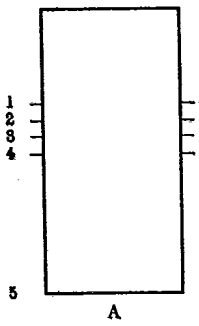
Function name and terminal name are not needed for AND/OR symbols.

<Example 2>

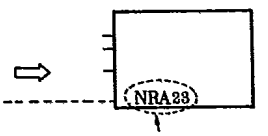
NRA23

Function name	Symbol	Symbol No.
NRA23		A1

COMPLEX, LATCH



Abbreviated case



Function name should be designated

The symbol no. in the macrocell library indicates which shape should be adopted while drawing.

An '&' mark should be attached to the level fixed input pins of a macro. They will be then clamped to the appropriate level automatically.
(@ : "H" # : "L")

The location of I/O pins of a macro should be approximately identical to that shown in macrocell library.

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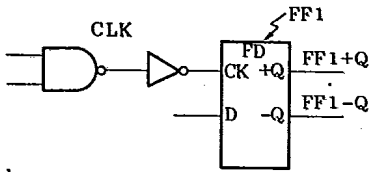
Each gate should be named using alphabet and signs of +,-. All names should be begun with alphabetical characters. Each line has its own name if the line is independent of another. (i.e. if it is not connected).

Limitation on naming:

* Terminals of package ... 2-5 letters
* Macrocell 2-5
* Memory macrocell ..... up to 2
* Three-state gate ..... up to 4

<Example 1>



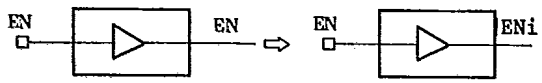
Each macrocell should be named first. Then,

(1) Output signal would be named with macrocell name itself if macro provides only one output terminal.

(2) In case of the macros which provide multiple outputs, output signals would be named with the combination of macrocell name and the output-suffix such as +Q, -Q, +Y, -Y and so on.

(3) It is allowed to omit naming the line which is terminated on a sheet of diagram.

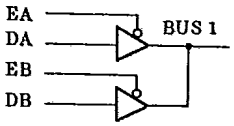
<Example 2>



Unacceptable Acceptable

Separate node should provide unique name.

<Example 3>



Wire-ored lines should not be named respectively but be sharing the name as shown in example.

Definition

* Macro function name ...function of macro (ex: NA, NR, FD)
* Macro terminal name ...pin function of macro (ex: CK, D, +Q, -Q)
* Macro name ...unique name given to each macrocell
* Terminal name ...name given to each node

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This macro is used when it is necessary to duplicate complex blocks of gates, thus saving time when drawing the schematic.

Name Allocation:

* All nodes inside macro ... within 4 letters beginning with @+/@-
* Input nodes of macro ... names are constrained to 2 letters of alphabet.
* Function name ... these are constrained to 5 letters with the first letter of alphabet.
* Output nodes out of macro ... exclude "@".
* Symbol size ...
  Width: A size of template
  Hight: (N+1)×2 divisions of the drawing sheet, where, N is the number of either inputs or outputs whichever is greater.

<Example 1>

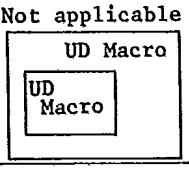
It is prohibited to define a UD macro for a F/F type or a latch.

In this case:

* It is impossible to guarantee the functional operation and the delay time.

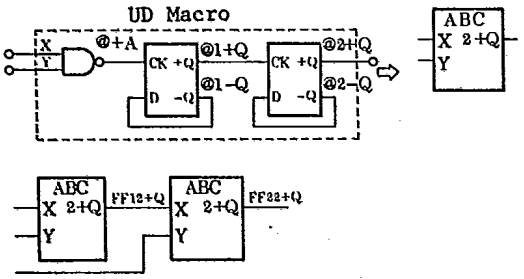
<Example 2>

Not applicable



* Nested UD macros are not supported.
* I/O buffer cells cannot be included in UD macro.

<Example 3>



* Employ unique names for the nodes in a UD macro. For fixed output names of macrocell, such as +Q/-Q of F/F types, the names should be attached like the example shown.
* Outputs of UD macros should be named with a maximum of 4 letters.

<Example 4>

The maximum number of I/O connections of either input or output is 40.

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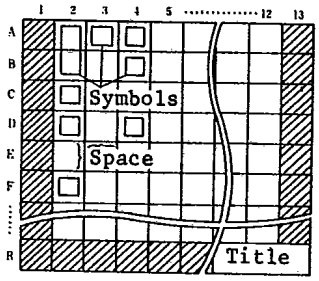
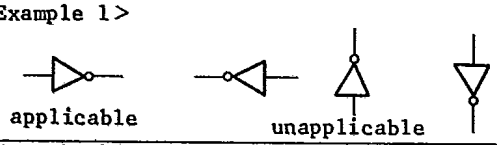
Symbols need to be positioned in point to the right so that signals flow from left to right. Placement in the shaded area is prohibited as in the overlapping of symbols.

In order to ensure sufficient space for routing at least one row in five should be kept blank. Spacing on columns should be for every other column.

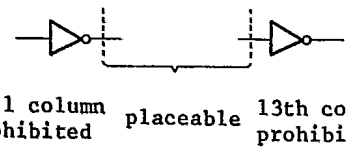


<Example 1>



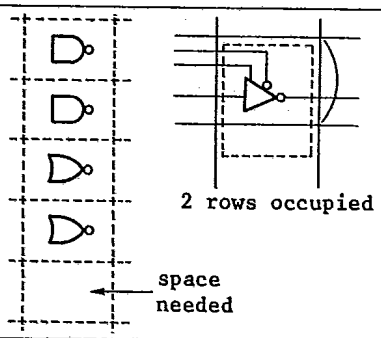
Rotation of symbols is not supported.

<Example 2>

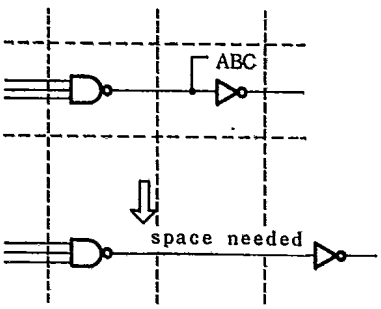


Cell cannot be placed on first and 13th columns.

<Example 3>



<Example 4>



Macrocells should be placed every other column.

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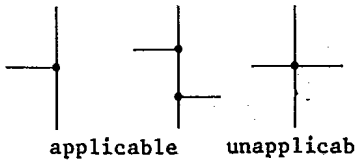
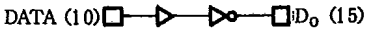
Drawing of lines:

Spacing of the lines is a minimum of 1 mesh. No more than 3 lines can be connected together to a junction point, (see example right), and a junction point should be designated clearly with solid circle.

The use of templates is recommended at all times.

Input and output signals should be described as shown in the example with signal names, pin numbers and pad. (□)



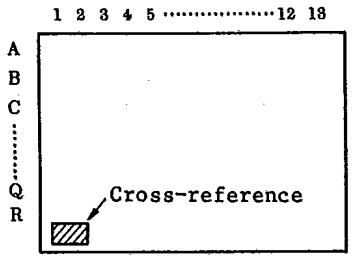


Cross reference:

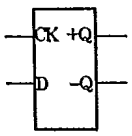
On the machine drawings, if the line is interconnected over a number of sheets, the following information should be listed.

K ··· 15, B10

- K ··· 15, B10
  - Location that the line is connected to sheet No.
  - Specification of destination
    - K : sink
    - S : source
    - Z : three-state output
    - N : three-state control



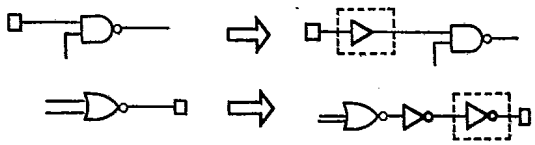
Meaning of +/-:



* In the case when a macro cell provides multiple outputs, the outputs are prefixed with the signs such as +/-.

+ : True, - : False

I/O Buffers



Not applicable Applicable

All inputs and outputs need to be buffered.

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■ 4.7 Example of Logic Description

Schematic description

```
*1
HD61J001          TRANS
HD61J             TYPE      DILP28
```

Device type, master type package

```
NB1       01Q8   BLOCK     V, W, X, Y, Z
@+1       01Q10  NA        @+Q, W, X
@+2       01Q11  NA        @+1, Y, Z
@         01Q12  FD        V, @+2
                 BEND      @+Q, @−Q
```

UD-macro definition

```
UP          02  INPUT
CLOCK       03  INPUT
DATAA       04  INPUT
DATAB       05  INPUT
DATAC       06  INPUT
DATAD       07  INPUT
ENAPN       08  INPUT
LOADN       09  INPUT
ENATN       10  INPUT
OD          11  OUTPUT   OD1
OC          12  OUTPUT   OC1
OB          13  OUTPUT   OB1
OA          16  OUTPUT   OA1
RCA         17  OUTPUT   RCA1
```

Description of I/O terminal including pin assignment.

LOADN → LOAND is an input pin located at pin 9 of the package.

```
CLOCK1    01B2   ANI    CLOCK
UDP       01D2   ANI    UD
E021      01E2   ANI    LOADN
J1        01F2   ANI    ENAPN
J2        01G2   ANI    ENATN
J3        01H2   ANI    DATAA
J4        01K2   ANI    DATAB
J5        01M2   ANI    DATAC
J6        01P2   ANI    DATAD
OA1       01B12  NAOT   FFA-Q
OB1       01D12  NAOT   FFB-Q
OC1       01F12  NAOT   FFC-Q
OD1       01H12  NAOT   FFD-Q
RCA1      01L12  NAOT   P0701
UDN       01D3   NA     UDP
LOADI     01E3   NA     E0201
ENATI     01G3   NA     J2
B0701     01B7   NA     ENLDN
DAALO     01H3   NA     J3, LOADI
DABLO     01K3   NA     J4, LOADI
DACLO     01M3   NA     J5, LOADI
DADLO     01P3   NA     J6, LOADI
G0501     01G5   NA     UDP, CAD
E0701     01E7   NA     ENLDN, CAA
L0701     01L7   NA     ENLDN, CAA
P0701     01P7   NA     P0601, Q0601
C0801     01C8   NA     ENLDN, FFA-Q
H0701     01H7   NA     ENLDN, CAA, CAB
P0601     01P6   NA     CAD, CAA, UDP, ENATI
ENLDN     01F4   NR     LOADI, J1, J2
J0501     01J5   NA     CAD, CAC, CAB, CAA, UDN
Q0601     01Q6   NA     CAD, CAC, CAB, CAA, UDN, ENATI
F0801     01F8   NA     CAA, ENLDN, G0501, J0501, FFB-Q
J0801     01J8   NA     ENLDN, J0501, CAB, CAA, FFC-Q
M0801     01M8   NA     ENLDN, CAC, CAB, CAA, FFD-Q
CAA       01C5   EOR    FEA+Q, UDN
CAB       01F5   EOR    FFB+Q, UDN
CAC       01L5   EOR    FFC+Q, UDN
CAD       01M5   EDR    UDN, FFD+Q
FFA       01B10  NB1    CLOCKI, B0701, E0201, C0801, DAALO
FFB       01E10  NB1    CLOCKI, E0201, E0701, F0801, DABLO
FFC       01H10  NB1    CLOCKI, E0201, H0701, J0801, DACLO
FFD       01L10  NB1    CLOCKI, E0201, L0701, M0801, DADLO
                 END
```

Detail description of logic

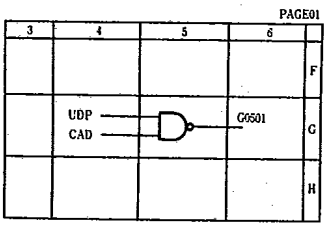
G0501 → G0501 | 01G5 | NA | UPD, CAD

INPUT SIGNALS

NAND GATE

LOCATION OF SYMBOL (G5 IN PAGE 01)

OUTPUT SIGNAL



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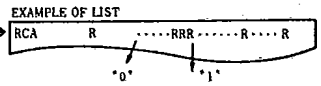
Output definition

```
*2
HD61J001        RTSL
CLOCK           OUTDEF  C
UD              OUTDEF  U
LOADN           OUTDEF  L
ENAPN           OUTDEF  P
ENATN           OUTDEF  T
DATAA           OUTDEF  A
DATAB           OUTDEF  B
DATAC           OUTDEF  C
DATAD           OUTDEF  D
RCA             OUTDEF  R
OA              OUTDEF  1
OB              OUTDEF  2
OC              OUTDEF  4
OD              OUTDEF  8
CAA             OUTDEF  A
CAB             OUTDEF  B
CAC             OUTDEF  C
CAD             OUTDEF  D
                INTV    400,250
                EDTIM   1000
                ETIME   0, 0, 400, 250
                END
```

Description of signals which you want to appear in the simulation lists.
(Internal signals can be monitored as well.)
Example of list:

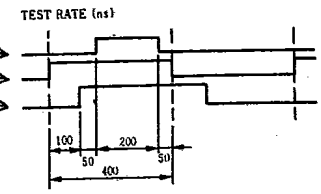


→ Sampling period (ns)
→ Start time of sampling (ns)
→ Maximum simulation step
→ Sampling period and start time for fault simulation.

Timing

```
*3
                STL     400, 0
CLOCK           CLK     0/150, 1/200, 0/50
UD              SIG
LOADN           SIG     100
ENAPN           SIG
ENATN           SIG
DATAA           SIG
DATAB           SIG
DATAC           SIG
DATAD           SIG
                END
```

→ Test period (ns) per cycle



Test vectors

```
*4
INPUT SIGNAL    1 - 30      ( 1 STEP - 60 STEP)
1           01
01      0
101
10      1 0
10      1 0
01  0
01  0
01  0
0
                LOOP 2
INPUT SIGNAL    1 - 5       ( 61 STEP - 83 STEP)
01010
01
0
0
101
01  0
01  0
01  0
0
                LOOP 1-2/10-
                END
```

→ Defines column 1 to column 30 as valid.

→ The test vectors from column 1 to column 30 are repeated twice.

→ Sequential step number (This is just a comment)

→ This expression means that the first two steps are repeated 10 times.

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5. GENERATING TEST VECTORS

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5.1 TEST VECTOR SHEET

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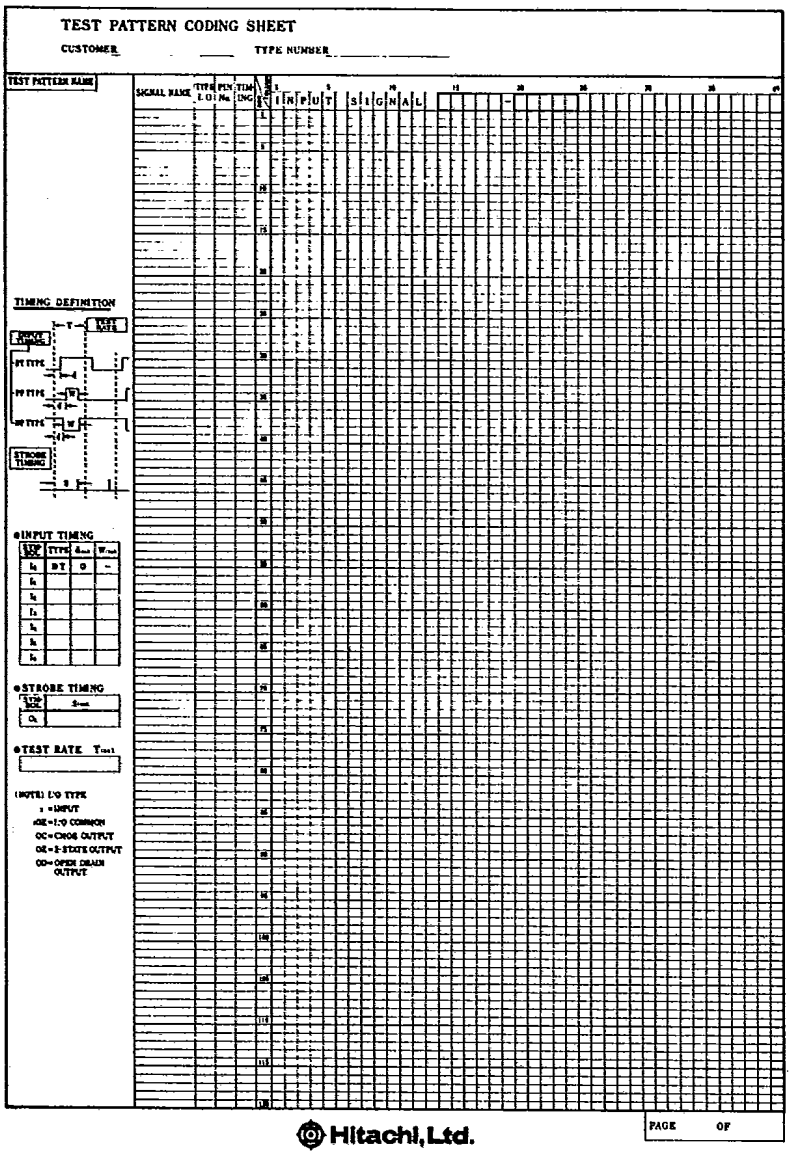
It is recommended that test vectors are described on Hitachi format coding sheets.

Coding sheet:



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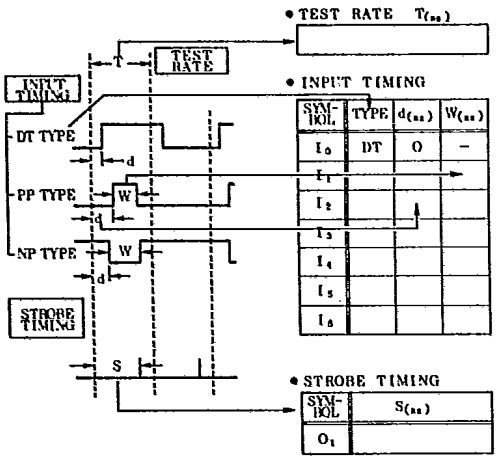
At first a user should define the timing required for testing. The test equipment provides 7 timing generators, I_0 through to I_6. I_0 is fixed as DT type signal with d= 0. Further, only one strobe timing is available for each set of test vector.

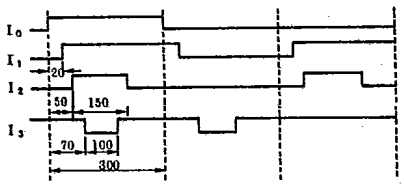
timing restrictions

$T \geqq 150$ $T-(d+w) \geqq 20$
$d \geqq 20$ $T-S \geqq 30$
$W \geqq 50$
$S \geqq 20$

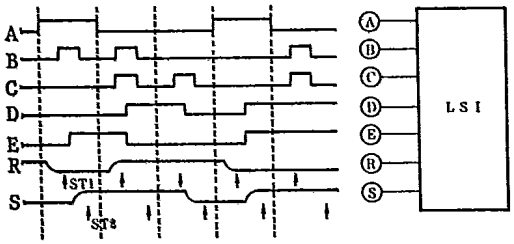
Definition:



TEST RATE		300ns		
	SYMBOL	TYPE	d(ns)	w(ns)
INPUT	I_0	DT	-	-
	I_1	DT	20	-
	I_2	PP	50	150
	I_3	NP	70	100
	I_4			
	I_5			
	I_6			
OUTPUT	O_1	250ns		



<Example 1>



* In the example, B has the same timing as C while D as E. Consequently 3 types of timing are required.
The timing for output R is different from S and requires different strobe timing.

For this situation, test vectors need to be run twice with S1/S2 strobe timing respectively. S1 should be positioned so that there is a good margin before output S changes.

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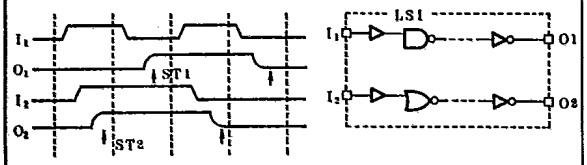
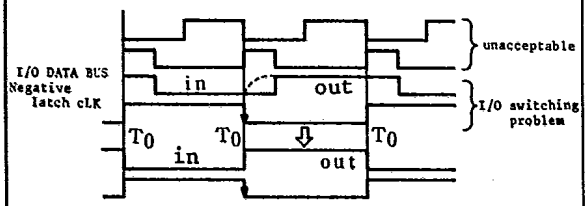
<Example 2>



* In the actual system, the timing for I_1 is different from I_2 and consequently the timing of O_1 differs from that of O_2. However, during testing they may not necessarily need to follow the actual operation. Such considerations would reduce the complexity of test vectors.

<Example 3>



* Clocks which have no delay are not acceptable, nor is the situation of $d + w \geq T$.

* In the actual testing, I/O switching occurs at To. So, latch clock should be shifted back-wards in order to improve the hold time.

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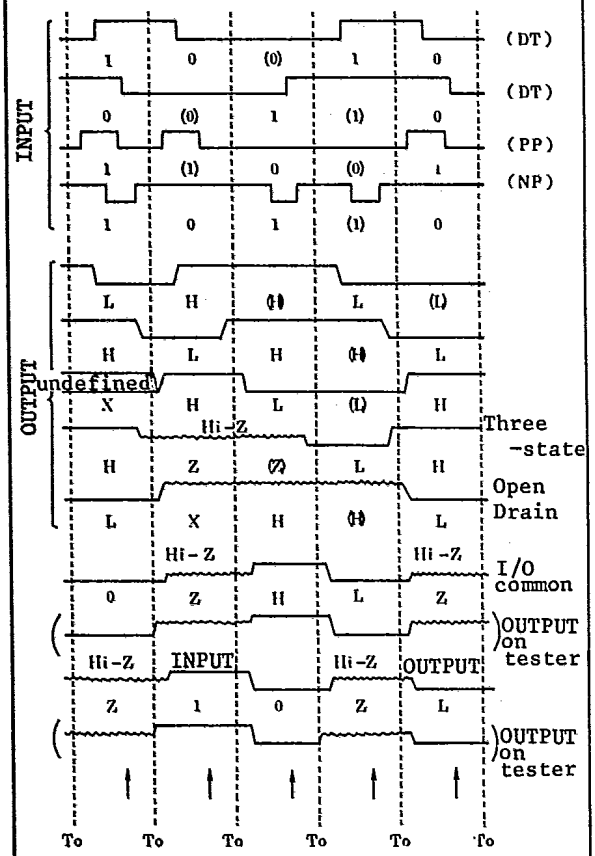
Describe the inputs ... 0, 1
outputs ... H, L, Z, X

Input	DT	0, 1
	PP	0, 1
	NP	0, 1
OUTPUT		H, L, Z, X

Note:

1. PP/NP: Pulse is given when "1"
2. Z; Hi-Z, X; undefined or masked
3. Blank: continue the previous state



* Input pattern; describe the state after a change occurs

DT 0-1 ... 1
1-0 ... 0
no change ... blank

PP/NP Pulse given ... 1
no pulse ... 0
no change ... blank
(repetitive)

* Output pattern; describe the state at the instant the strobe occurs.

Strobe timing should be set with sufficient margin.

Strobe after the signal transition should be determined after consideration of the maximum delay, on the other hand minimum delays should be considered with reference to the period before the transition.

Open drain; when disabled the state should be described "H" (transition from an "L" to an "H"), requiring a period of time before stability is achieved depending on the time constant determined by external components. In this situation the state right after the transition should be masked by an "X".

* I/O common

input mode ... 0, 1
output mode ... X, H, L, Z

* I/O switching occurs at To in the testing hardware. Thus, if the test vectors are designed with some delay time, both input/output shall be enabled simultaneously.

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	To avoid this problem as the cycle switches it is necessary to insert a "Z" cycle. A "Z" cycle requires a well organized input circuit in order to prevent the "Z" state affecting the logic function.

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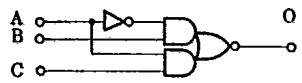
As mentioned in the previous sections, test vectors are utilized not only for logic verification but also for final testing in mass production. Therefore high fault coverage is required. In order to prepare the sophisticated test vectors, consideration of cell-level fault coverage is not as straight forward as describing vectors to represent the operation of the system.

<Example 1>



Vector A

Signal \ Cycle	1	2
A	1	0
B	0	0
C	1	1
O	L	H

Vector B

Signal \ Cycle	1	2	3	4
A	1	1	0	0
B	0	1	1	0
C	1	0	0	1
O	L	H	L	H

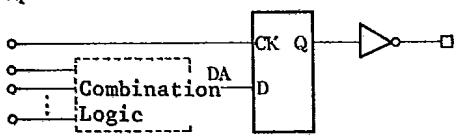
Vector C

Signal \ Cycle	1	2	3	4	5	6	7	8
A	1	1	1	1	0	0	0	0
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
O	H	L	H	L	H	H	L	L

* If vector group A is just for verifying the function and group C provides all the combinations of inputs; from the standpoint of fault coverage cycle 3 is omittable since it is equivalent to cycle 1.

Thus, vector group B would be the most efficient vector set.

<Example 2>



Output of combination logic, DA, needs to be clocked out to an output of the GA.

As mentioned in 3.2 injected fault is ultimately detected at an output of the GA. If many stages of F/F type are involved before the signal appears at the terminal, a very sophisticated set of vectors may be needed.

<Example 3>

Expected outputs should be described together with the associated inputs.

Expected outputs can be compared and checked with the simulation results done by DA program. Expected outputs should be included in test vectors supplied by the customer.

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Repetitive patterns can be compressed into a short number of loop cycles where the maximum length of a loop cycle is 4096. During loop cycles, if it is difficult to describe the expected outputs, they can be masked (X).

Expression

Column	17	24
Loop of block	LOOP	10
Loop of limited columns	LOOP	2-4/15

Nesting is not supported.

- Loop of signal block

  Vectors

  Loop n

- Loop of limited columns

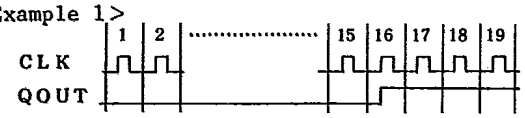
  Vectors

  Loop S1-e1/n1, S2-e2/n2 .....

  n; loop times, Sn; start column,

  en; end column

<Example 1>



• Straight expression

	1	2	.....	15	16	17	18	19
CLK	1							
QOUT	L				H			

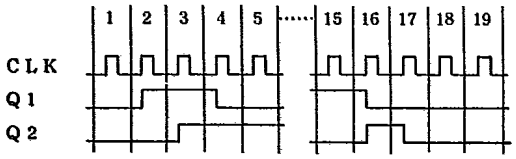
• Looped expression

	1	2	3	4
CLK	1			
QOUT	L	H	.	

LOOP 1-1/15

In this example, 1 through 15 steps both inputs/outputs are repeated. If a looped expression is employed all the cycles described in 15 columns are compressed into 1 column.

<Example 2>



While Q1 is checked, Q2 should be masked.

	1	2	3	4	5	6	7
CLK	1						
Q1	L	H		L			
Q2	X				L		

LOOP 1-4/4

An output which changes regularly is checkable while the loop is cycled. Outputs that change in an irregular manner should be masked (X).
In this case, fault coverage may be degraded.

<Example 3>

Loop S1-e1/n1, S2-e2/n2,

Loop Sm-em/nm

When loop commands cannot be described in one line, they can extend to multiple lines with 'Loop' commands at the head of each line respectively.

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Test vectors should be designed to be as short as possible in order to achieve a fast throughput on the simulation. Also as test vectors are utilized for production testing, memory capacity imposes a limitation on the number of cycles. In the logic design phase, this limitation should be considered when designing the test circuit.

* Maximum vector set is 10 and every set requires initialization.
* The maximum number of cycles for each set including expanded loop cycles is 4000.
* The total number of cycles before expansion is 4000.
* Maximum test time is 100 ms.

<1>

The DC parametric test is generated by the DA, which supports up to 2000 cycles. Consequently, all logical states should be covered within 2000 cycles.

<2>

While a vector is in progress, changes in input timing definition are not supported. If an input should change, it is necessary to separate vector.

<3>

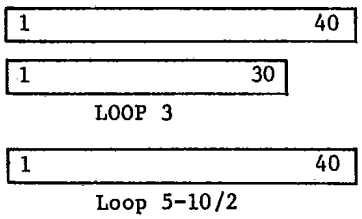
Each individual set of vectors should provide initialization cycles at the beginning.

Timing definition is also required respectively.

DC parametric test: V_{OH}, V_{OL}, input/output leakage current

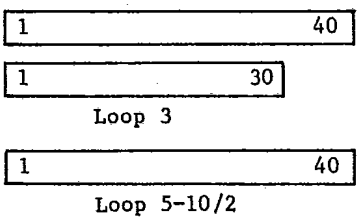
Calculation of cycles required for a vector:

Ex. 1



Cycles: 40+30×3+4+6×2+30=176

Ex. 2 Total cycles



Total cycles.

40 + 30 + 40 = 110

(Before expanding loop cycles)

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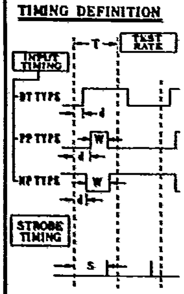
TEST PATTERN CODING SHEET

CUSTOMER ______________ TYPE NUMBER HD61J10C

TEST PATTERN NAME

TIMING DEFINITION



SIGNAL NAME	TYPE I/O	PIN No.	TIMING	ROW	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
					I	N	P	U	T		S	I	G	N	A	L			1				-			4	0																	
CLOCK	I	03	12	1	1										0	1																												
U D	I	02	10		0	1							0																															
LOADN	I	09	11		1	0	1																																					
ENAPN	I	08	10		1	0						1		0																														
ENATN	I	10	10	5	1	0						1																																
DATA A	I	04	10		0	1			0																																			
DATA B	I	05	10		0	1			0																																			
DATA C	I	06	10		0	1			0																																			
DATA D	I	07	10		0				1																																			
				10																																								
RCAX	O	17			H			L	H							L	H									L	H									L	H							
OAX	O	16			X	H	L	H	L	H	L			H		L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
OBX	O	13			X	H	L				H			L					H		L		H		L				H		L		H		L				H		L		H	
OCX	O	12			X	H	L												H				L						H				L						H				L	
ODX	O	11		15	X	L	H		L								H		L								H		L								H		L					
																						L	O	O	P				2															
				20																																								
				25	I	N	P	U	T		S	I	G	N	A	L			1				-			3	3																	
CLOCK	I	03	12		1										0	1	0	1	0	1							1					1	1	1	1	1	1							
U D	I	02	10		0										0	1																0	1	1	1	0	0							
LOADN	I	09	11		1										0					1	0	1	0	1			0	1	0		1	0			1	0	1							
ENAPN	I	08	10		0															1				0							1	0			1	0	1							
ENATN	I	10	10	30	0										1	0	1															0				0	0							
DATA A	I	04	10		0										0	1			0	1				0	1		0	1				0		1	0	0								
DATA B	I	05	10		0										0	1			0	1				0	1		0	1				0				0								
DATA C	I	06	10		0										0	1			0	1				0	1		0	1		0		0				0								
DATA D	I	07	10		0															1					0							0				0								
				35																																								
RCAX	O	17			H	L	H																																					
OAX	O	16			H										L	H																												
OBX	O	13			L										H																													
OCX	O	12			L										L	H																												
ODX	O	11		40	L																																							
																						L	O	O	P				1	-	1	0	/	2	,	1	1	-	12	/	1	0		
				45																																								
				50																																								
				55																																								
				60																																								
				65																																								

● INPUT TIMING

SYMBOL	TYPE	$t_{d(ns)}$	$W_{(ns)}$
I_0	DT	0	-
I_1	DT	100	-
I_2	PP	150	200
I_3			
I_4			
I_5			
I_6			

● STROBE TIMING

SYMBOL	$S_{(ns)}$
O_1	250

● TEST RATE $T_{(ns)}$

400

(NOTE) I/O TYPE
- I = INPUT
- IOZ = I/O COMMON
- OC = CMOS OUTPUT
- OZ = 3-STATE OUTPUT
- OD = OPEN DRAIN OUTPUT

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6. HITACHI DOCUMENTATION

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Macrocell			Equ. count (G)	Sheet No. n pcs	Sheet No. Gate count G × n	Sheet No. n pcs	Sheet No. Gate count G × n	Sheet No. n pcs	Sheet No. Gate count G × n	Sheet No. n pcs	Sheet No. Gate count G × n
Power gate	NAP NRP	1	1								
		2	2								
		3	3								
		4	4								
Gate	NA NR	1	0.5								
		2	1								
		3	1.5								
		4	2								
		6	9.5								
		8	5 5								
		9	6.5								
		12	8								
		16	10.5								
	EOR/ENOR		2.5								
Flip-flop	LD		3.5								
	LDC1		4								
	LDPC0		6								
	FD		6								
	FDPC3		8								
	FDL		6								
	FJ		9								
	FJPC1		12								
Latch	LRS0/LRS3		3								
	LR2S20/LR2S23		4								
S/R	ZSR		10								
	ZSRCP3		12								
Complex gate	NRA23/NAR23		1.5								
	NR2A2/NA2R2		2								
	NR4A2N		4.5								
	NR8A2N		9.5								
	NR2A3N		3.5								
	NR2A4N		4.5								
Multi-plexer	M2T1N		3								
	M4T1N		8.5								
	M1T2N		3.5								
Decoder	D2T4N		8								
	D3T8		12								
Three-state gate	ANZ		3.5								
	NAZ		1.5								
Others	ZEQC4		12								
Total											

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6.2 PATH DELAY CHECK SHEET

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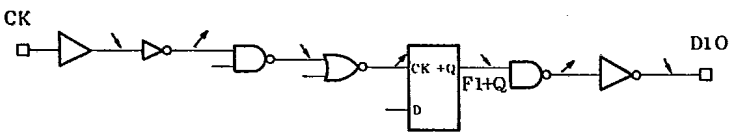
No.	CRITICAL PATH/ DELAY CHECK PATH	REQUEST	(typical) ESTIMATE	AFTER ROUTING
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
19				
20				
Example	CK ⌐~ D1O⌊		210	
Note	 Loading capacitance of output pin : 130pF			

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6.3 I/O TRANSITION TIMING CHECK SHEET

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Type No.:_____ Pattern:_____ TR=_____(ns) SB=_____(ns)

PIN No.	PIN Name	I/O Type	TIMING	PIN No.	PIN Name	I/O Type	TIMING
1				41			
2				42			
3				43			
4				44			
5				45			
6				46			
7				47			
8				48			
9				49			
10				50			
11				51			
12				52			
13				53			
14				54			
15				55			
16				56			
17				57			
18				58			
19				59			
20				60			
21				61			
22				62			
23				63			
24				64			
25				65			
26				66			
27				67			
28				68			
29				69			
30				70			
31				71			
32				72			
33				73			
34				74			
35				75			
36				76			
37				77			
38				78			
39				79			
40				80			

	I0	I1	I2	I3	I4	I5	I6
Type	DT						
D (ns)	d=0						
W (ns)	–						

①Non-inverting input buffer = i ②Inverting output = OC ③Three-state output = OZ ④I/O common = iOZ
⑤Open drain = OD (nMOS) Note;Loading capacitance is 130pF

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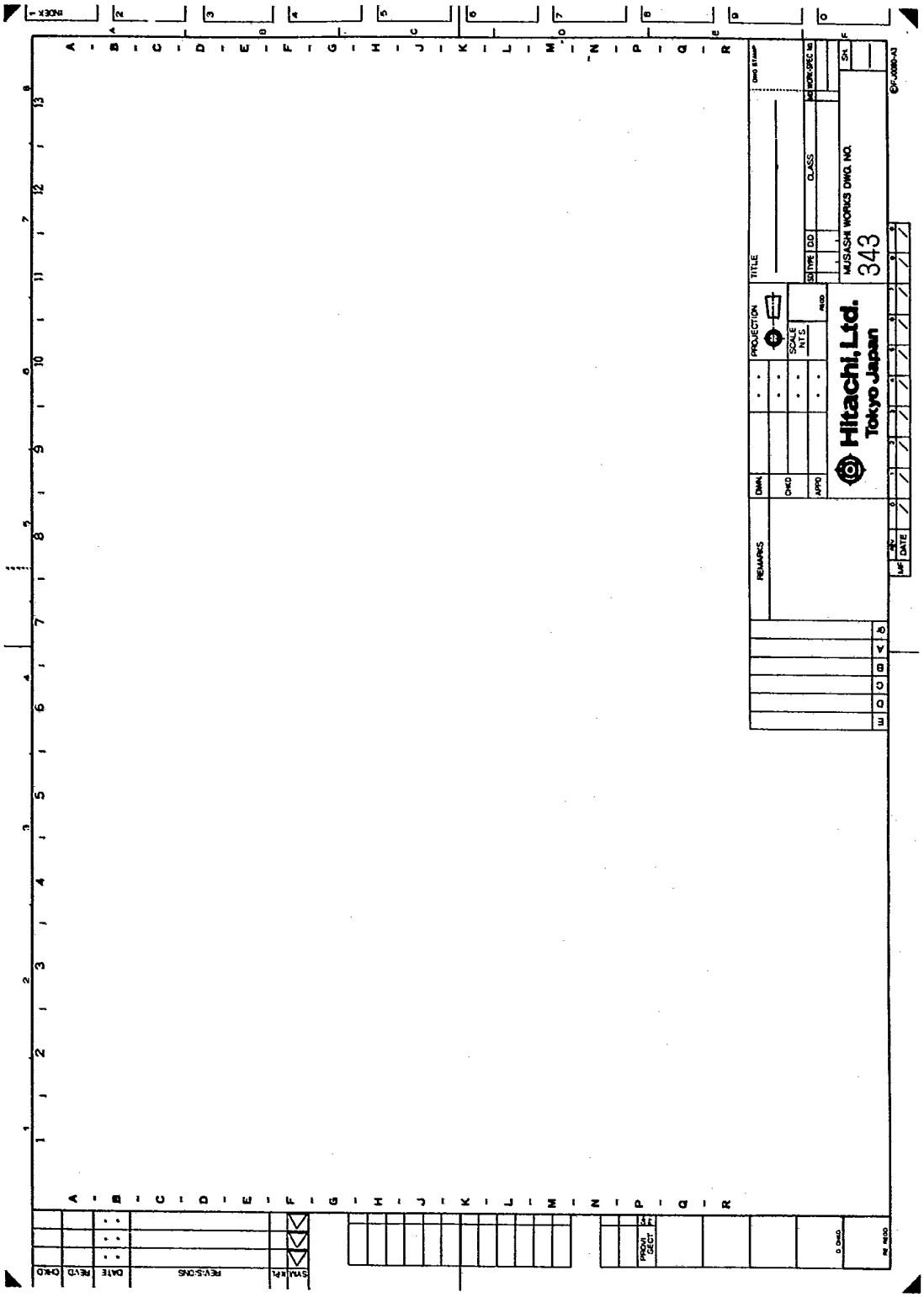

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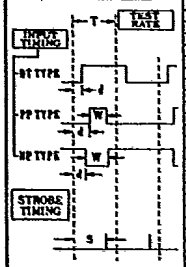
TEST PATTERN CODING SHEET

CUSTOMER _____ TYPE NUMBER _____

TEST PATTERN NAME

SIGNAL NAME | TYPE I/O | PIN No. | TIMING | SEQUENCE NO. | INPUT SIGNAL

TIMING DEFINITION



●INPUT TIMING

SYMBOL	TYPE	d_{min}	W_{min}
I_0	DT	0	-
I_1			
I_2			
I_3			
I_4			
I_5			
I_6			

●STROBE TIMING

SYMBOL	S_{min}
O_1	

●TEST RATE T_{min}

(NOTE) I/O TYPE
- I =INPUT
- IOZ=I/O COMMON
- OC=CMOS OUTPUT
- OZ=3-STATE OUTPUT
- OD=OPEN DRAIN OUTPUT

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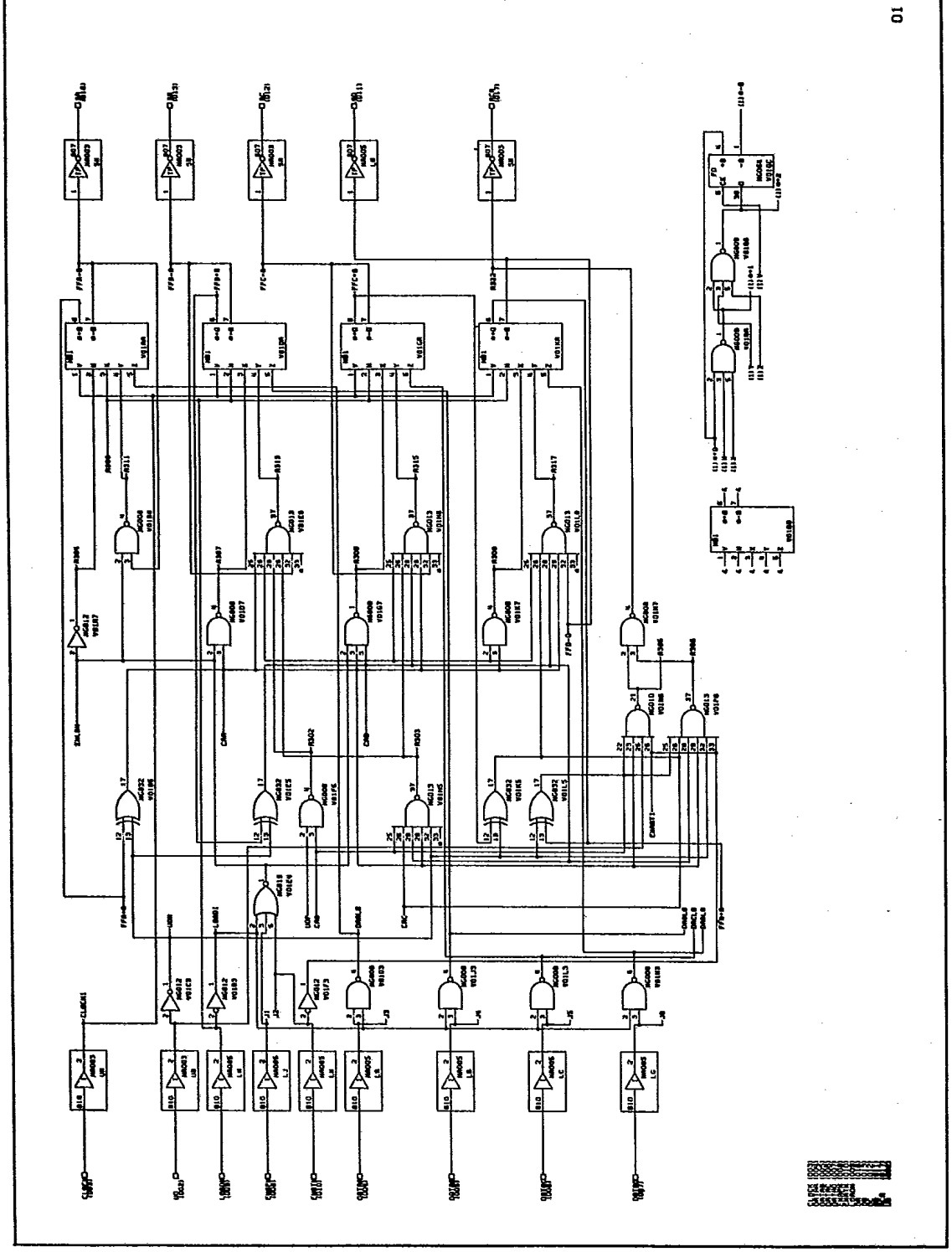

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Pin Assignment

Product version: (J,K,L) Series

Package type: (DP,DC) 28pin

Type No. _____ Customer: _____

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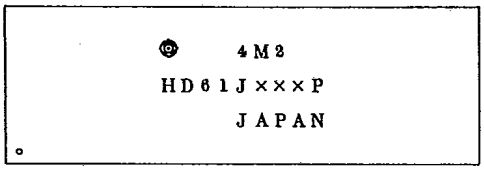
PIN No.	PIN NAME	I/O type
1	GND	–
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14	V_{CC}	–

PIN No.	PIN NAME	I/O type
15	GND	–
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28	V_{CC}	–

Note : Power supply pins are fixed.

I/O types

i : Non inverting input buffer
iOZ : I/O common
OC : CMOS inverting output buffer
OZ : Three-state output buffer
OD : Open drain output buffer



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Pin Assignment | Product version: HD61K | Package type FP80 pin

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Type No. | Customer

PIN No.	PIN NAME	I/O type
1	NC	–
2		
3	NC	–
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17		
18		
19		
20		
21		
22	NC	–
23		
24	NC	–
25		
26		
27		
28		
29		
30		
31	V_{CC}	–
32		
33	GND	–
34		
35		
36		
37		
38		
39		
40		

PIN No.	PIN NAME	I/O type
41	NC	–
42		
43	NC	–
44		
45		
46		
47		
48		
49		
50		
51		
52		
53		
54		
55		
56		
57		
58		
59		
60		
61		
62	NC	–
63		
64	NC	–
65		
66		
67		
68		
69		
70		
71		
72	V_{CC}	–
73		
74	GND	–
75		
76		
77		
78		
79		
80		

Notes : Power supply pins are fixed.

I/O types
- i : Non inverting input buffer
- iOZ : I/O common
- OC : CMOS inverting output buffer
- OZ : Three-state output buffer
- OD : Open drain output buffer

NC Pins should not be utilized.

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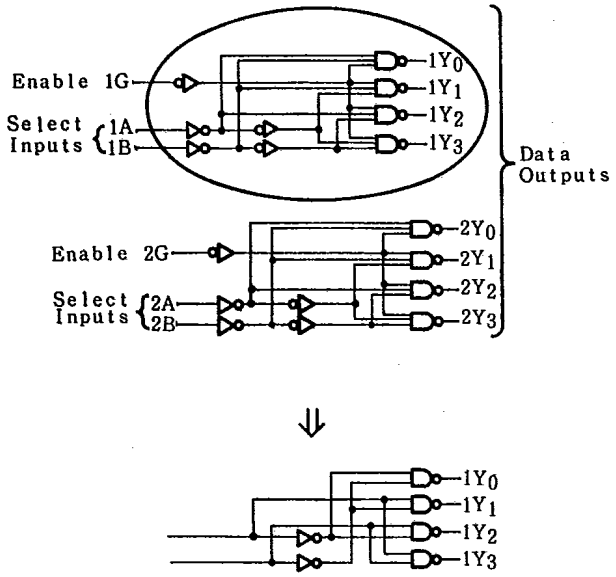
Notification on conversion

The following conversion table indicates the equivalent gate count when one of the built-in functions is utilized.

For instance HD74LS139 integrates dual 2-line to 4-line decoders, then equivalent gate count 8.5 represents one of the two decoders.



Equivalent gate=5

Fig. 1

This example shows that we have the possibility to reduce the gate count in reality if we do not utilize all pin functions.

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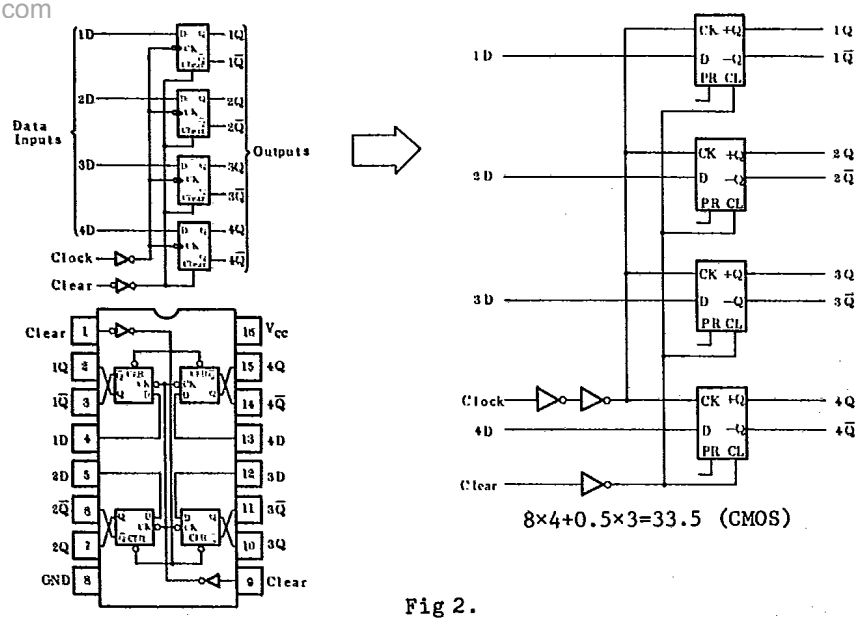

Fig 2.

□ HD74LS393 (Dual 4-bit Binary Counters)

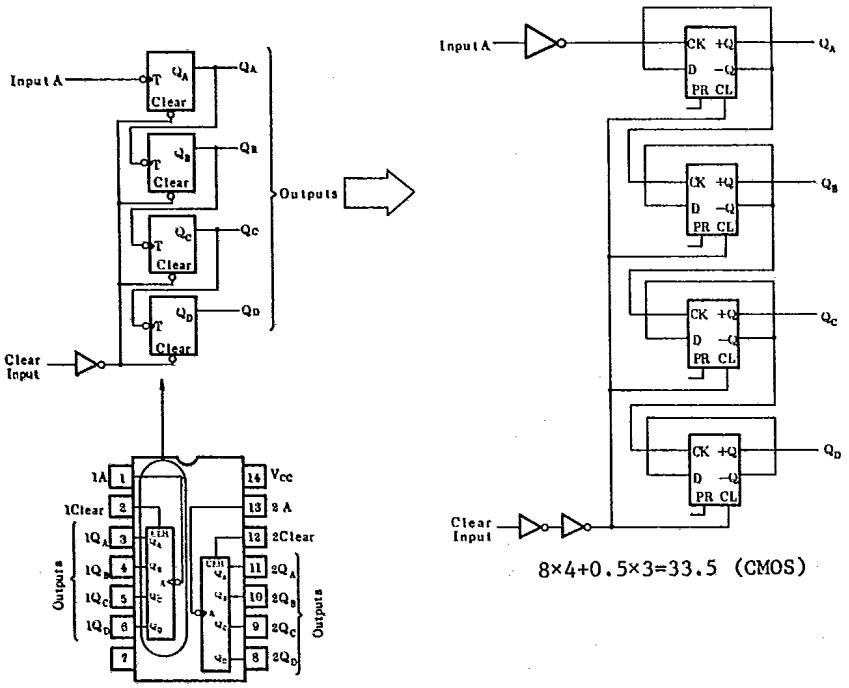

Fig. 3

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SECTION II: HD61 Series Product Specification

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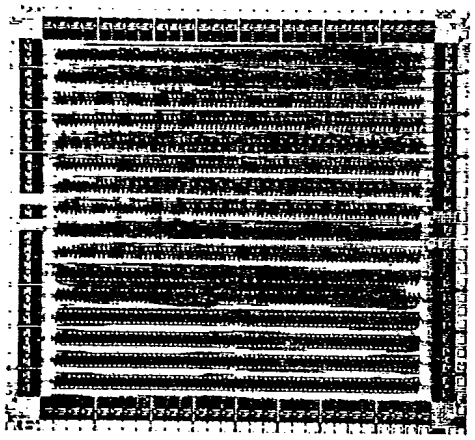
The HD61 series is a master slice CMOS gate array using 2-layer metal interconnect technology. This series has four master chips with gate counts ranging from 504 to 2496, and I/O terminal counts ranging from 50 to 104. These chips can replace not only CMOS logic but also TTL logic due to their high speed of 3.5 ns typ and the compatibility of input and output buffers at TTL level.
LSI design is fully automated by DA (Design Automation) system and a custom LSI is developed based on logic diagram, timing and electrical specifications and test patterns from customer.



FEATURES

- **Technology**
  Silicon-gate 3-micron CMOS technology
  Dual-layer metal interconnection
- **Fast operation**
  Internal gate (2-input NAND, FO = 3, AL = 3mm)
  .....3.5 ns typ
  Input buffer (FO = 3, AL = 3mm).....9ns typ
  Output buffer (C_L = 50pF) .....24ns typ
  Memory access time (HD61MM) .....60ns typ
- **Low power dissipation**
  At 10MH$_z$ operation (Internal gate).....130μW/gate typ
- **Abundant input and output configuration**
  Allocation of all pins except power supply pins to input/output/input-output
  Output can be CMOS/open drain/3-state
- **Memory on-chip (HD61MM)**
  Flexibility of memory capacity and word organization
  Selection of single port / dual port memory
- **Wide operating temperature range**
  −20 to + 75°C
- **Wide package selection**
  Featuring plastic packages with high pin counts
- **Powerful design support**
  User-Defined-Macro
  Worldwide network of design and engineering support centers
  - **Logic simulation**
  - **Fault grading**
  - **Timing verification (delay simulation)**

■ LINE UP

			HD61J	HD61K	HD61L	HD61MM
Gate count			504	1080	1584	2496
I/O pin count			50	68	68	104
RAM on chip			—	—	—	16 bits x 32 words max.
Package	Plastic	DP28	o	o	o	—
		DP40	o	o	o	—
		DP42	o	o	o	—
		DP64	—	o	o	o
		FP54	o	—	—	—
		FP80	—	o	o	—
		FP100	—	—	—	**
	Ceramic	DC28	o	o	o	**
		DC40	o	o	o	**
		PGA72	—	—	o	—
		PGA120	—	—	—	o

**Under Development

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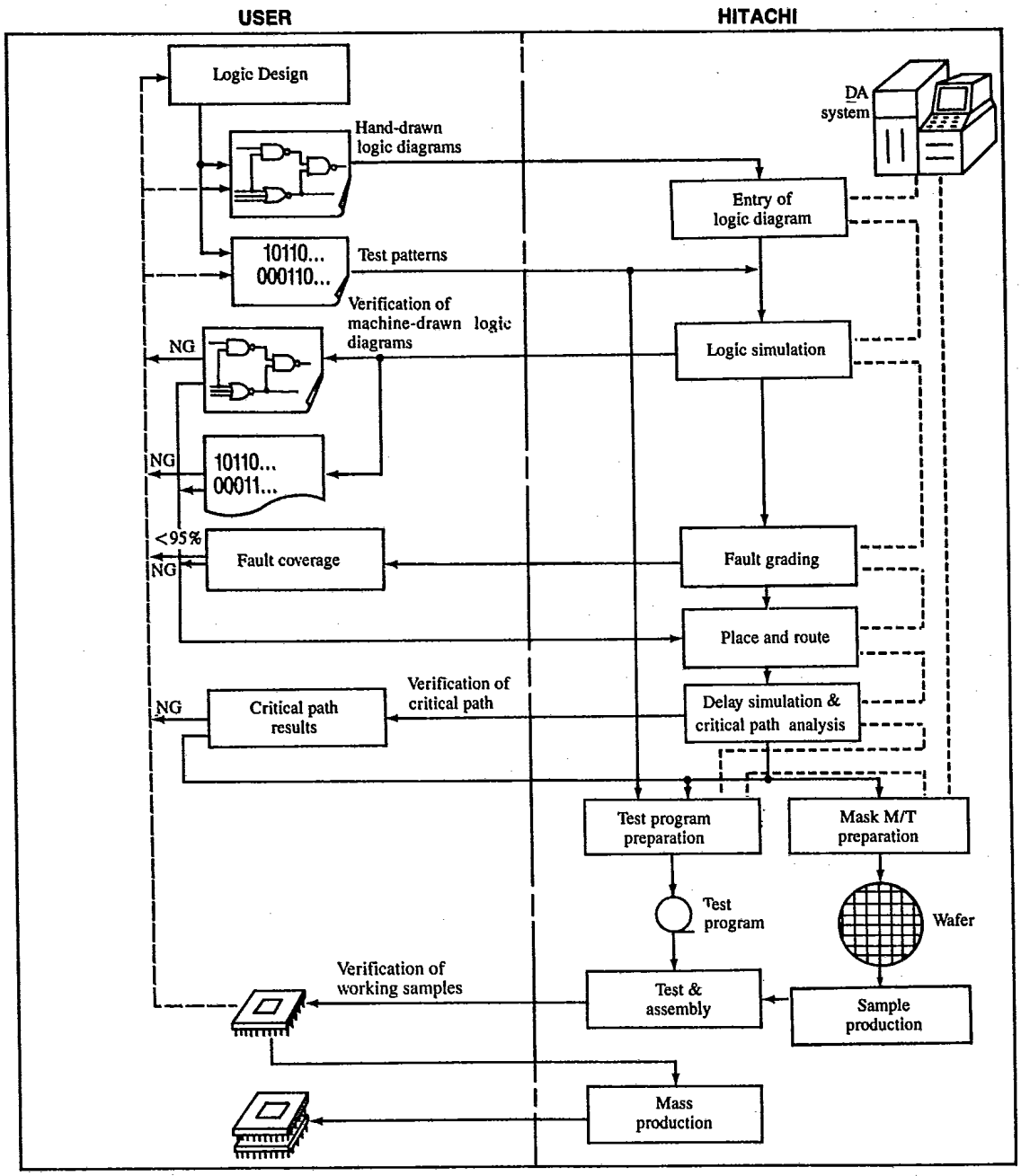
■ DEVELOPMENT FLOW

The gate array design flow is shown below.
The interface between the user and Hitachi is based on hand-drawn logic diagrams and test patterns provided by the user. Hitachi will input these into our computer for logic simulation, fault grading, placement and routing, delay simulation and test program preparation. After verification of above by user, samples will be produced, checked by user and mass production will begin.



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■ ABSOLUTE MAXIMUM RATINGS

Item		Symbol	Rating	Unit
Supply Voltage*		V_{CC}	-0.3 to + 6.7	V
Terminal Voltage*		V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature		T_{opr}	-20 to + 75	°C
Storage Temperature	With Bias	T_{bias}	-20 to + 85	°C
	Without Bias	T_{stg}	-55 to +125	°C
Output Current	Per Output Pin	IOH	-8 to 8	MA
	Total		-40 to 40	

*With respect to GND

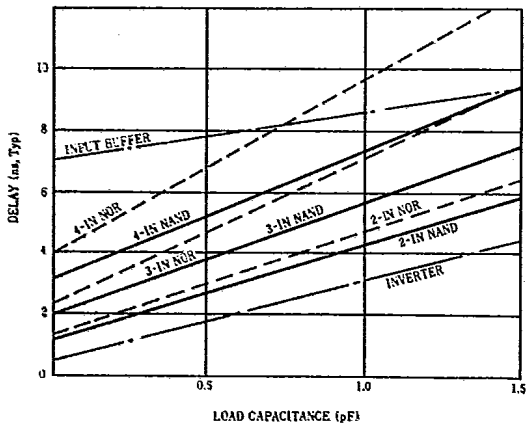
Note) Permanent damage may occur if maximum ratings are exceeded.
Normal operation should be under recommended operating condition, that is GND ≤ (Vin and/or Vout) ≤ V_{CC}.
If these conditions are exceeded, reliability of LSI could be affected.

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5V ± 5%, Ta=-20 to +75°C)

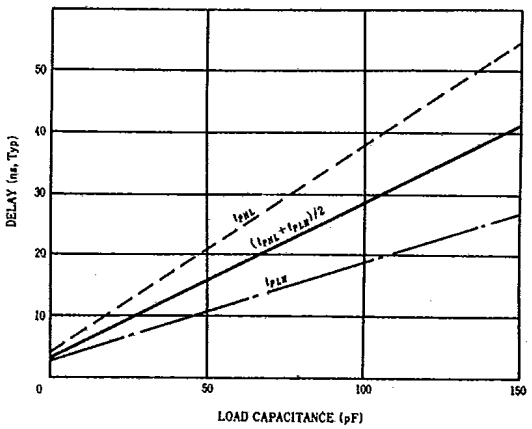
Item		Symbol	Test Conditions	min	typ	max	Unit
Input Voltage		V_{IH}		2.2	—	Vcc+0.3	V
		V_{IL}		-0.3	—	0.8	V
Output Voltage		V_{OH}	I_{OH} = — 2mA	2.4	—	—	V
		V_{OL}	I_{OL} = 2mA	—	—	0.4	V
Input Leakage Current		I_{LI}	VIN = GND or VCC	—	—	1	μA
Output Leakage Current		I_{LO}	at high impedance	—	—	1	μA
Gate Delay	Internal	t_{pd}	2 input NAND, FO = 3, Metal = 3mm	—	3.5	—	ns
	Input Buffer		FO = 3,Metal = 3mm	—	9	—	ns
	Output Buffer		C_L = 5OPF	—	24	—	ns
Power Dissipation		I_{CC}	Internal 2 input NAND, 10MHz	—	130	—	μW/Gate
Terminal Capacitance*		CT	Ta = 25°C, f = 1MHz V_{IN}=0V	—	—	12.5	pF

*This parameter is sampled, not 100% tested.

■ INTERNAL GATE DELAY vs LOAD (REFERENCE)



■ OUTPUT BUFFER DELAY vs LOAD (REFERENCE)



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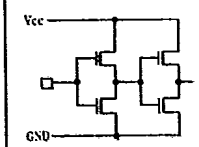
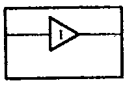
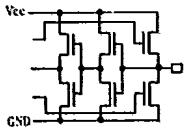
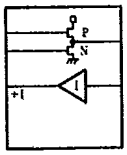
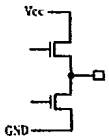
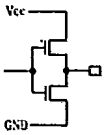
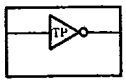
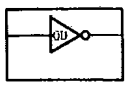
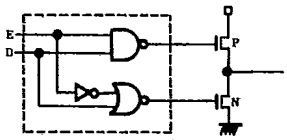
■ MACROCELL LIBRARY

1. I/O BUFFERS

Macrocell: Function / Macro Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) k_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) k_{HL}
Input Buffer ANI		–				D1	7.7	2.0	6.7	1.0
I/O Buffer ANIO		–	2.2 3.2			D2	Input See "Input Buffer" Output See "3-state Buffer"			
3-state Buffer NAOZ		–	2.2 3.2			D1	8.0	0.12	22.0	0.19
Output NAOT		–	4.7			D1	8.5	0.12	23.5	0.19
Open Drain Output NAOD		–	3.2			D1	–	–	22.0	0.19

Note) Application of Tri-state buffer

Equivalent circuit



This control circuit has to be built by internal gate

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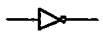
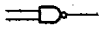
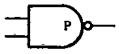
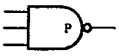
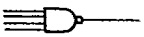
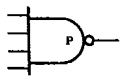
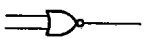
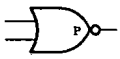
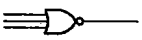
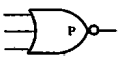
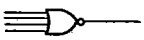
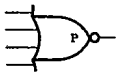
2. POWER GATES

Macrocell: Function / Macro Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Delay: Symbol No.	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) k_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) k_{HL}
Power inverter NAP		1	1.4	@		–	1.2	1.2	0.9	1.5
Power-2 input NAND NAP		2	1.4			–	1.3	1.9	1.2	1.3
Power-3 input NAND NAP		3	1.4			–	2.1	2.0	1.9	1.7
Power-4 input NAND NAP		4	1.4			–	2.7	2.2	2.9	2.1
Power-2 input NOR NRP		2	1.4			–	1.9	2.5	0.9	1.5
Power-3 input NOR NRP		3	1.4			–	3.7	3.3	1.5	1.5
Power-4 input NOR NRP		4	1.4			–	6.1	4.3	1.8	1.5

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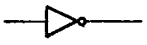
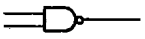
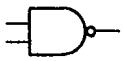
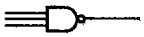
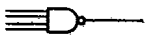
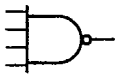
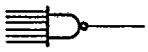
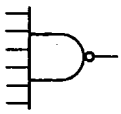
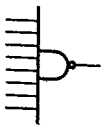
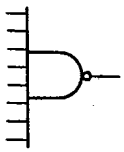
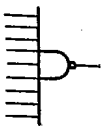
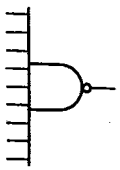
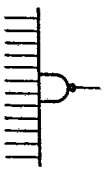
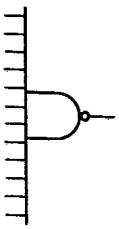
3. GATES

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Delay				
Function	Equivalent Circuit					Symbol No.	t_{PLH} (ns)		t_{PHL} (ns)	
Macro Function Name							t_{OLH}	k_{LH}	t_{OHL}	k_{HL}
Inverter NA		0.5	1	@		–	0.6	3.0	0.4	2.2
2-Input NAND NA		1	1			–	1.3	3.6	1.0	2.7
3-Input NAND NA		1.5	1			–	2.0	3.9	1.9	3.4
4-Input NAND NA		2	1			–	2.9	4.3	3.2	4.1
6-Input NAND NA		4.5	1			–	4.1	2.7	6.0	2.0
8-Input NAND NA		5.5	1			–	4.7	2.9	7.7	2.0
9-Input NAND NA		6.5	1			–	4.6	2.9	8.2	2.2
12-Input NAND NA		8	1			–	5.0	3.0	9.9	2.2

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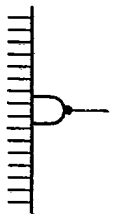
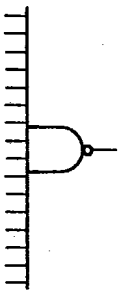
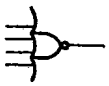
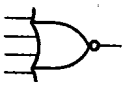
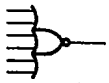
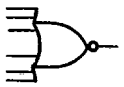
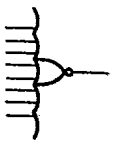
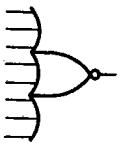
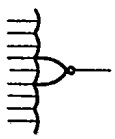
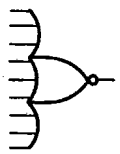
Macrocell: Function / Macro Function Name	Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Delay: Symbol No.	t_{PLH} (ns): t_{OLH}	k_{LH}	t_{PHL} (ns): t_{OHL}	k_{HL}
16-Input NAND NA		10.5	1			–	5.3	3.0	12.5	2.5
2-Input NOR NR		1	1			–	1.8	4.7	1.0	2.7
3-Input NOR NR		1.5	1			–	3.7	6.8	1.4	2.7
4-Input NOR NR		2	1			–	6.5	8.5	1.5	3.1
6-Input NOR NR		4.5	1			–	7.6	2.6	3.6	2.1
8-Input NOR NR		5.5	1			–	10.5	2.8	3.7	2.0
9-Input NOR NR		6.5	1			–	8.6	2.8	4.2	2.1

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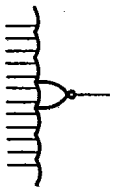
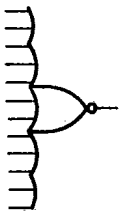
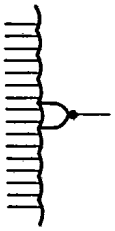
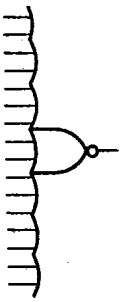
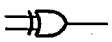
Macrocell: Function / Macro Function Name	Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Delay: Symbol No.	Delay: t_{PLH} (ns): t_{OLH}	Delay: t_{PLH} (ns): k_{LH}	Delay: t_{PHL} (ns): t_{OHL}	Delay: t_{PHL} (ns): k_{HL}
12-Input NOR NR		8	1			–	12.1	2.8	4.5	2.0
16-Input NOR NR		10.5	1			–	13.2	3.0	4.9	2.1
2-Input EOR EOR		2.5	1.4			–	4.2	4.5	3.9	2.0
2-Input ENOR ENR		2.5	1.4			–	3.2	2.5	3.2	3.0

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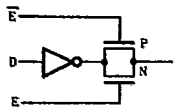
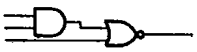
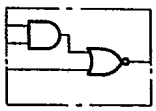
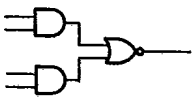
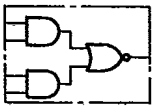
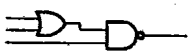
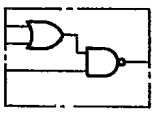
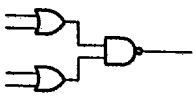
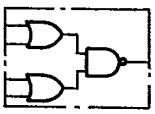
4. 3-STATE GATES

Macrocell: Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) K_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) K_{HL}
3-State Inverter (Internal) NAZ		1.5	1	# @ @		–	D		2.4	2.6	1.8	1.9
							E/$\overline{E}$		1.0		0.4	
3-State Buffer (Internal) ANZ		3.5	1.4 1	# @		–	D		2.4	2.3	3.0	1.7
							$\overline{E}$		3.9		2.9	

5. AND-NOR, OR-NAND GATES

Macrocell: Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) K_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) K_{HL}
2-AND-NOR NRA23		1.5	1			A1	AND Input		2.6	5.5	1.4	2.9
							NOR Input		2.0	–	1.4	–
2 Wide-2 Input AND-NOR NR2A2		2	1			A1			3.0	4.1	2.2	2.8
2-OR-NAND NAR23		1.5	1			A1	OR Input		2.5	5.0	1.9	3.8
							NAND Input		1.9	–	1.2	–
2 Wide-2 Input OR-NAND NA2R2		2	1			A1			3.8	5.0	1.8	2.7

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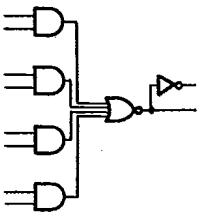
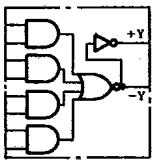
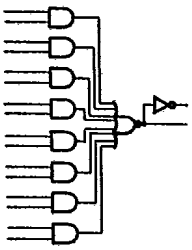
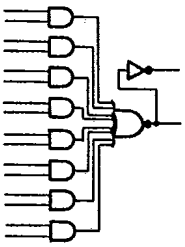
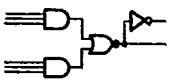
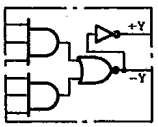
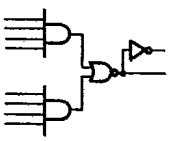
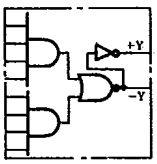
Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) K_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) K_{HL}
4 Wide-2 Input AND-NOR NR4A2N		4.5	1	###		A4		−Y	8.5	5.1	3.8	2.6
								+Y	5.6	3.5	9.0	3.5
8 Wide-2 Input AND-NOR NR8A2N		9.5	1	###		A5		−Y	6.3	2.5	10.5	3.2
								+Y	11.8	3.4	6.8	2.4
2 Wide-3 Input AND-NOR NR2A3N		3.5	1			A2		−Y	4.4	2.9	4.5	3.1
								+Y	6.2	4.0	5.0	2.8
2 Wide-4 Input AND-NOR NR2A4N		4.5	1			A4		−Y	4.5	2.6	7.2	3.8
								+Y	9.4	4.9	5.1	2.9

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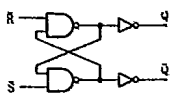
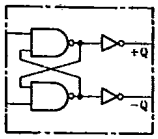
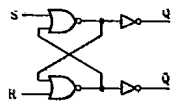
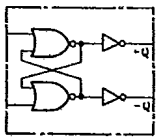
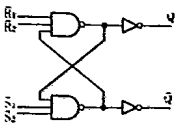
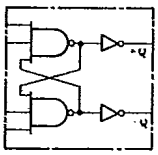
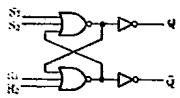
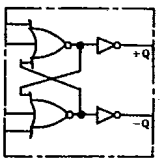
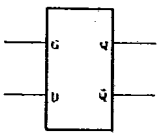
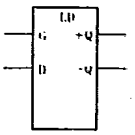
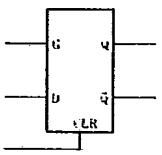
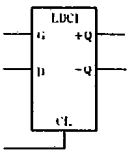
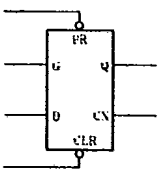
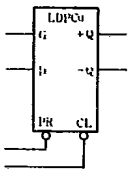
6. LATCHES

Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) K_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) K_{HL}
$\overline{RS}$-Latch LRS0		3	1			A3	$\overline{S}$	+Q	5.1	2.5	–	1.5
							$\overline{R}$		3.0		3.3	
							$\overline{S}$	–Q	3.4	2.3	2.9	1.5
							$\overline{R}$		5.6		–	
RS-Latch LRS3		3	1			A3	S	+Q	2.9	2.3	4.0	1.8
							R		–		5.5	
							S	–Q	–	2.3	5.8	1.8
							R		3.0		4.2	
$\overline{R}2\overline{S}2$- Latch LR2S20		4	1			A4	$\overline{S}$	+Q	7.2	2.6	–	1.6
							$\overline{R}$		4.5		3.4	
							$\overline{S}$	–Q	4.4	2.6	3.7	1.7
							$\overline{R}$		6.9		–	
R2S2- LATCH LR2S23		4	1			A4	S	+Q	3.3	2.3	6.4	2.2
							R		–		7.5	
							S	–Q	–	2.3	7.5	2.2
							R		3.3		6.6	
D-Latch LD		3.5	1.4	@		C	G	+Q	2.7	2.2	3.1	1.7
			1	@			D		3.4		3.9	1.7
							G	–Q	4.4	2.2	3.6	1.3
							D		5.0		4.4	
D-Latch with CLR LDC1		4	1.4	@		C	G	+Q	3.5	4.3	3.2	1.8
			1	@			CL		2.8		1.2	
							D		4.2		3.9	
			1	#			G	–Q	4.6	2.3	4.7	1.6
							CL		3.3		3.6	
							D		5.2		5.4	
D-Latch with PRE/CLR LDPC0		6	1.4	#		C	G	+Q	8.6	2.7	5.3	1.9
			1	@			$\overline{PR}$		6.6		–	
							$\overline{CL}$		4.5		3.4	
			1	@			D		9.1		6.8	
			1	@			G	–Q	9.1	2.7	5.3	1.8
							$\overline{PR}$		4.5		3.1	
							$\overline{CL}$		7.3		–	
							D		10.5		5.6	

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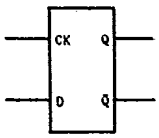
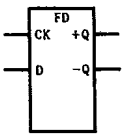
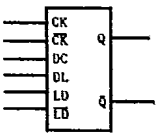
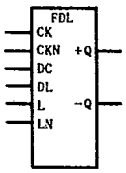
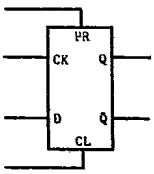
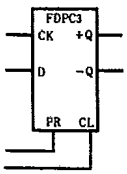
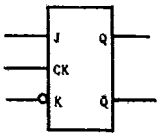
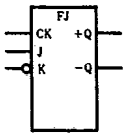
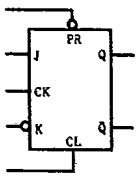
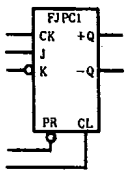
7. FLIP-FLOPS

Macrocell: Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) K_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) K_{HL}
DFF FD		6	1 1	@ @		C	CK	+Q	4.6	2.4	3.9	1.6
								−Q	5.2	2.2	5.5	1.4
DFF with Load FDL		6	1.4 1.4 1 1 1 1	@ # @ @ # @		B4	CK	+Q	2.5	2.5	3.1	2.1
							DL		7.7		9.0	
							CK	−Q	4.3	2.2	3.6	1.4
							DL		10.7		8.5	
DFF with PRE/CLR FDPC3		8	1 1 1.4 1.4	@ @ # #		C	CK	+Q	5.4	4.4	4.2	1.7
							CL		2.5		1.2	1.7
							PR		5.5		–	–
							CK	−Q	6.8	4.4	6.8	1.5
							CL		5.8		–	–
							PR		4.0		1.5	1.5
JKFF FJ		9	1.4 1 1	@ @ #		C	CK	+Q	3.8	2.3	6.8	2.8
								−Q	5.0	2.5	5.4	2.3
JKFF with PRE/CLR FJPC1		12	1.4 1 1 1.4 1	@ @ # @ #		C	CK	+Q	7.2	2.3	7.5	5.8
							PR		3.0		3.0	
							CL		–		7.2	
							CK	−Q	4.7	2.3	10.1	5.8
							PR		–		5.7	
							CL		4.4		4.5	

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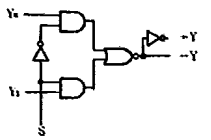
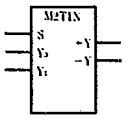
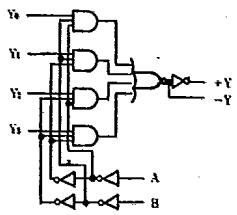
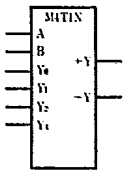
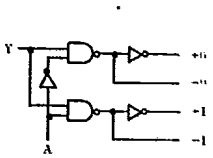
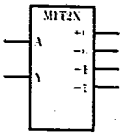
8. MULTIPLEXERS

Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	Delay: t_{PLH} (ns) t_{OLH}	Delay: t_{PLH} (ns) K_{LH}	Delay: t_{PHL} (ns) t_{OHL}	Delay: t_{PHL} (ns) K_{HL}
2 to 1 Multiplexer M2T1N		3	1.4 1 1	# # #		B2	Y_0	+Y	3.3	3.2	5.0	2.8
							Y_1		4.4		3.8	
							S		3.8		4.7	
							Y_0	−Y	4.4	4.2	2.0	2.6
							Y_1		3.3		3.1	
							S		3.8		2.4	
4 to 1 Multiplexer M4T1N		8.5	1	# # # # # #		B4	Y_0	+Y	9.5	4.8	9.3	3.7
							Y_1		8.6		9.6	
							Y_2		6.2		6.8	
							Y_3		4.8		5.8	
							A		11.3		15.5	
							B		10.5		13.0	
							Y_0	−Y	8.5	6.7	7.5	3.5
							Y_1		8.8		6.3	
							Y_2		6.0		4.6	
							Y_3		5.0		3.3	
							A		15.1		8.5	
							B		12.0		7.2	
1 to 2 Demultiplexer M1T2N		3.5	1.4	# @		B3	Y	+0	3.4	3.4	2.6	2.2
							A		4.2		3.5	
							Y	+1	2.7	3.5	2.3	2.3
							A		2.9		3.1	
							Y	−0	2.0	2.3	2.0	2.7
							A		2.8		3.1	
							Y	−1	1.6	2.3	1.6	2.3
							A		2.5		1.8	

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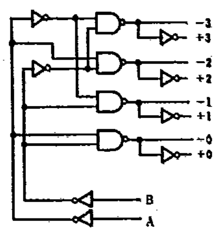
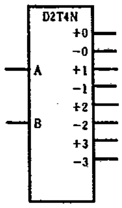
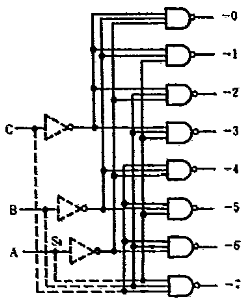
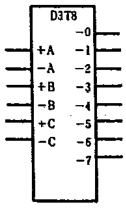
9. DECODERS/ENCODERS

Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	t_{PLH} (ns): t_{OLH}	t_{PLH} (ns): K_{LH}	t_{PHL} (ns): t_{OHL}	t_{PHL} (ns): K_{HL}
2-bit Decoder D2T4N		8	1	# # 		B5	A	−0	3.3	2.3	4.0	2.3
							B		3.4		3.9	
							A	−1	4.9	2.3	4.7	2.3
							B		3.7		3.8	
							A	−2	3.7	2.4	4.1	2.3
							B		4.9		4.7	
							A	−3	5.1	2.2	4.7	2.3
							B		5.1		4.8	
							A	+0	4.9	3.6	4.0	2.1
							B		4.6		4.0	
							A	+1	5.8	3.6	5.5	2.2
							B		4.6		4.3	
							A	+2	5.0	3.7	4.4	2.5
							B		5.6		5.2	
							A	+3	5.6	3.3	5.6	2.4
							B		5.8		5.4	
3-bit Decoder D3T8		12	2.2	@@@@@@		B5	A B C	−0 ~ −7	2.0	3.9	1.9	3.4

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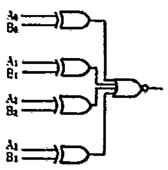
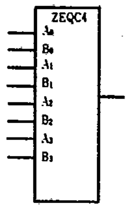
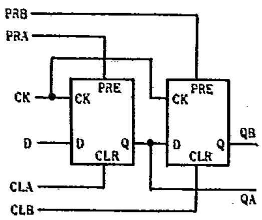
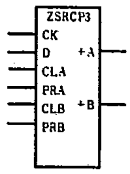
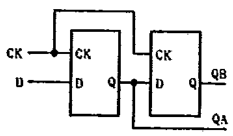
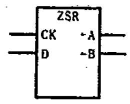
10. OTHERS

Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay: Input Name	Delay: Output Name	t_{PLH} (ns): t_{OLH}	t_{PLH} (ns): K_{LH}	t_{PHL} (ns): t_{OHL}	t_{PHL} (ns): K_{HL}
4-bit Equal Comparator ZEQC4		12	1.4	# # # # # # # #		B5	A_0 A_1 A_2 A_3 B_0 B_1 B_2 B_3		11.1	9.0	6.9	1.9
2-bit SR with CLR/PRE ZSRCP3		12	1 1 1.4 1 1.4 1	@ # # # #		B4	CK	+A	8.8	4.4	8.2	1.9
							CLA	+A	13.2	4.4	2.0	1.9
							PRA	+A	13.8	4.4	–	1.9
							CK	+B	8.8	4.4	8.2	1.9
							CLB	+B	13.2	4.4	2.0	1.9
							PRB	+B	13.8	4.4	–	1.9
2-bit SR ZSR		10	1	@ @		B1	CK	+A	4.6	2.4	3.9	1.6
							CK	+B	5.2	2.2	5.5	1.4

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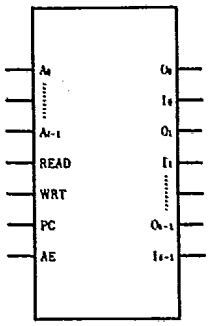
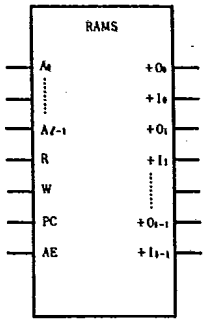
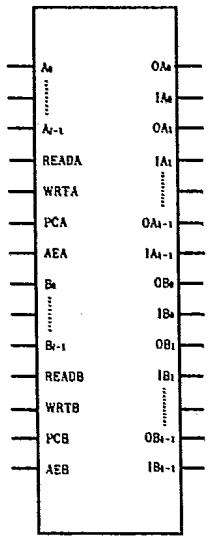
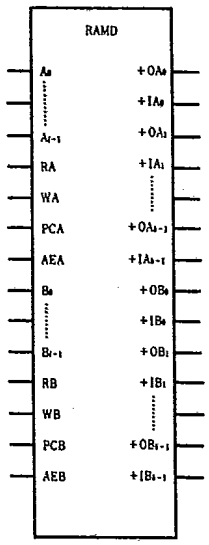
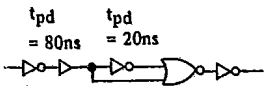
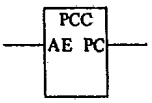
11. RAM (Only for HD61MM)

Macrocell: Function / Function Name	Macrocell: Equivalent Circuit	Equivalent Gate Count	Normalized Load Factor	Symbol	Symbol No.	Delay
Single Port RAM b bits/word w=2^{ℓ} word b=2, 4, ..., 16 w=1, 2, ..., 32 RAMS		1.5·b·w + 3b + 6w + 70		 when b−1≧10, the expressions are like follows. b-1 | --8 | 9 | 10 | 11 | 12 | -- Expressions | --8 | 9 | A | B | C | --	A	60 ns
Dual Port RAM b bits/words w=2^{ℓ} words b=2, 4, ..., 16 w=1, 2, ..., 32 RAMD		2·b·w + 7.5b + 8w + 70			A	60 ns
RAM Pre-charge PCC		28	1		B1	

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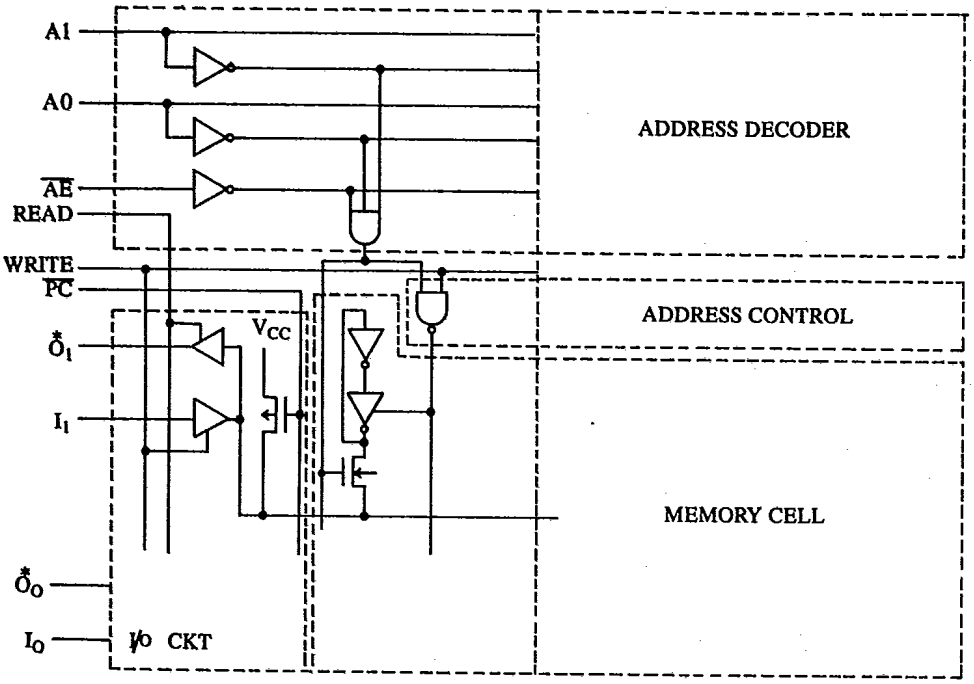
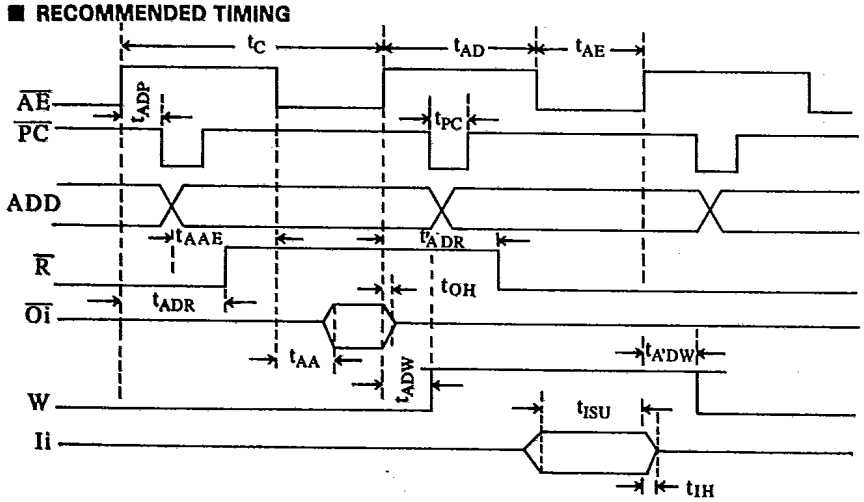
■ EQUIVALENT CIRCUIT OF RAM (SINGLE PORT RAM)

The following figure is not exactly the same as the actual circuit.



■ RECOMMENDED TIMING



	MIN	TYP	MAX
t_C	400	—	—
t_{AD}	250	—	—
t_{AE}	150	—	—
t_{ADP}	30	80	160
t_{PC}	10	30	60
t_{AAE}	30	—	—
t_{ADR}	0	—	t_{AD}
t'_{ADR}	0	—	t_{AD}
t_{AA}	20	60	130
t_{OH}	4	10	20
t_{ADW}	0	—	t_{AD}
t'_{ADW}	0	—	t_{AD}
t_{ISU}	30	—	—
t_{IH}	30	—	—

■ FUNCTIONAL TEST FOR ON-CHIP RAM

In order to easily test on-chip RAM, the logic design should be done so as to access the RAM directly outside the chip, for instance in RAM-TEST MODE.

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■ TTL TO CMOS GATE ARRAY CONVERSION

(1) Equivalent Gate Count

No.	TTL	Gate Count	No.	TTL	Gate Count
1	74LS00	1	41	74LS90	42
2	74LS01	1	42	74LS91	66
3	74LS02	1	43	74LS92	50.5
4	74LS03	1	44	74LS93	50.5
5	74LS04	0.5	45	74LS95	53
	74LS05		46	74LS107	13
6	74LS08	1.5	47	74LS109	13
7	74LS09	1.5	48	74LS112	13.5
8	74LS10	1.5	49	74LS113	13
9	74LS11	2	50	74LS114	13.5
10	74LS12	1.5	51	74LS125	2
11	74LS15	2	52	74LS126	2
12	74LS20	2	53	74LS136	2.5
13	74LS21	2.5	54	74LS137	31
14	74LS22	2	55	74LS138	19.5
15	74LS26	1	56	74LS139	7.5
16	74LS27	1.5	57	74LS145	22
17	74LS28	1	58	74LS147	36
18	74LS30	5.5	59	74LS148	38
19	74LS32	1.5	60	74LS151	45.5
20	74LS33	1	61	74LS152	25
21	74LS37	1	62	74LS153	23
22	74LS38	1	63	74LS154	77
23	74LS40	2	64	74LS155	16.5
24	74LS42	24	65	74LS156	16.5
25	74LS47	40	66	74LS157	12.5
26	74LS48	42	67	74LS158	10.5
27	74LS49	35	68	74LS160	64.5
28	74LS51	3.5	69	74LS161	64.5
29	74LS54	6.5	70	74LS162	58
30	74LS55	4.5	71	74LS163	64
31	74LS63	1	72	74LS164	82
32	74LS73	13	73	74LS166	102
33	74LS74	9	74	74LS170	114
34	74LS75	7	75	74LS174	49.5
35	74LS76	13.5	76	74LS175	33.5
36	74LS77	7	77	74LS181	93
37	74LS78	13.5	78	74LS183	12
38	74LS83	52.5	79	74LS190	84.5
39	74LS85	63	80	74LS191	78.5
40	74LS86	2.5	81	74LS192	63

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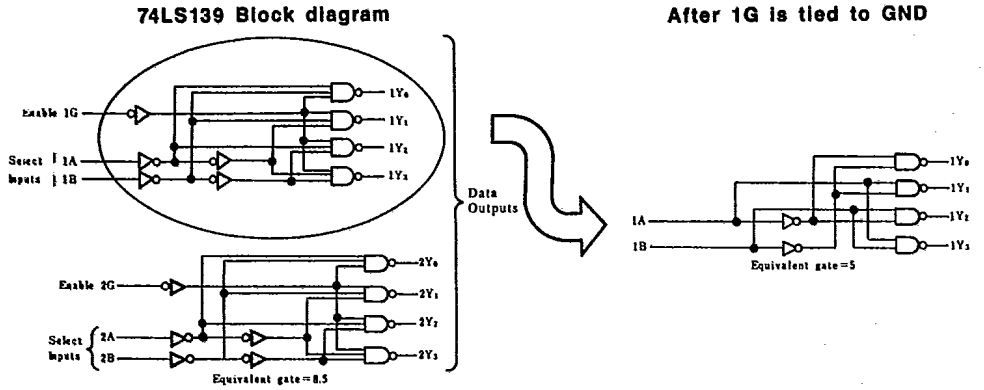
No.	TTL	Gate Count	No.	TTL	Gate Count
82	74LS193	63	97	74LS283	51.5
83	74LS194	77.5	98	74LS290	41.5
84	74LS195	56	99	74LS298	43.5
85	74LS246	48.5	100	74LS299	144
	74LS247		101	74LS365	25
86	74LS248	48.5	102	74LS366	25
87	74LS249	48.5	103	74LS367	12.5
88	74LS251	39	104	74LS368	12.5
89	74LS253	25.5	105	74LS375	7
90	74LS257	21.5	106	74LS386	2.5
91	74LS258	19	107	74LS390	37.5
92	74LS259	79	108	74LS393	33.5
93	74LS266	2.5	109	74LS490	40.5
94	74LS273	65.5	110	74LS668	82
95	74LS279	4	111	74LS669	71.5
96	74LS280	45.5	112	74LS670	115.5

(2) Figures indicated in the table are the guidelines when all pin functions are fully converted.



Note: Exact conversion is not necessarily achieved since certain pins are tied to GND level, such as Enable 1G pin of LS139 shown above. In this case, the equivalent gate count will be off by 2.5 gates.
Therefore, users might overestimate the gate count by 20 to 30% if the figures above are employed without due consideration.

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■ CMOS LOGIC TO CMOS GATE ARRAY

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(1) Equivalent Gate Count

No.	CMOS	Gate Count	No.	CMOS	Gate Count
1	HD14001B	1	41	HD14161B	68
2	HD14002B	2	42	HD14162B	67
3	HD14006B	144.5	43	HD14163B	68
4	HD14008B	44.5	44	HD14174B	48.5
5	HD14011B	1	45	HD14175B	32.5
6	HD14012B	2	46	HD14194B	65.5
7	HD14013B	8	47	HD14501UB	2, 1.5
8	HD14014B	69.5	48	HD14502B	18.5
9	HD14015B	32.5	49	HD14503B	13
10	HD14017B	N/A	50	HD14506B	11
11	HD14020B	116	51	HD14508B	17.5
12	HD14021B	50.5	52	HD14510B	78.5
13	HD14023B	1.5	53	HD14512B	20.5
14	HD14024B	57	54	HD14514B	55
15	HD14025B	1.5	55	HD14515B	63
16	HD14027B	12	56	HD14516B	78.5
17	HD14028B	26	57	HD14517B	563.5
18	HD14032B	68.5	58	HD14518B	39
19	HD14035B	57.5	59	HD14519B	26
20	HD14038B	80	60	HD14520B	38
21	HD14040B	N/A	61	HD14529B	21
22	HD14042B	16.5	62	HD14531B	30
23	HD14043B	20.5	63	HD14532B	41.5
24	HD14044B	20.5	64	HD14538B	N/A
25	HD14049UB	0.5	65	HD14539B	24
26	HD14050B	1	66	HD14541B	N/A
27	HD14068B	5.5	67	HD14555B	7.5
28	HD14069UB	0.5	68	HD14556B	8.5
29	HD14070B	2.5	69	HD14558B	53
30	HD14071B	1.5	70	HD14560B	68
31	HD14072B	2.5	71	HD14562B	768.5
32	HD14073B	2	72	HD14572UB	1, 0.5
33	HD14075B	2	73	HD14583B	12
34	HD14076B	53	74	HD14584B	N/A
35	HD14077B	2.5	75	HD14585B	37.5
36	HD14078B	5.5			
37	HD14081B	1.5			
38	HD14082B	2.5			
39	HD14093B	N/A			
40	HD14160B	67			

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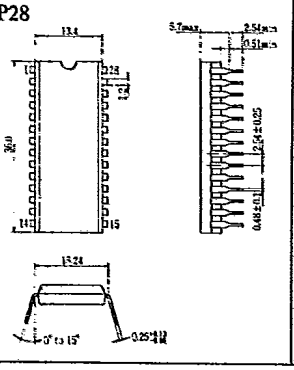
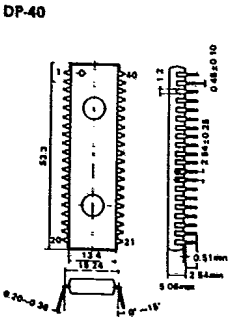
■ PACKAGE OUTLINE

Unit: mm

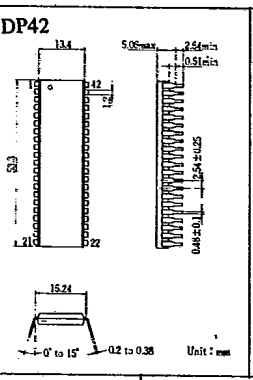
DP28



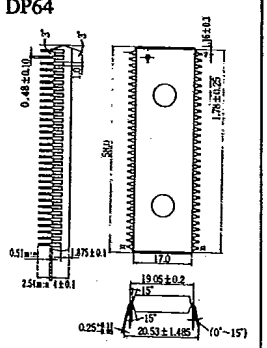
DP-40



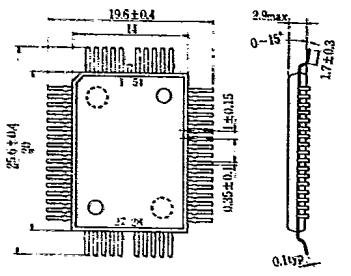
DP42



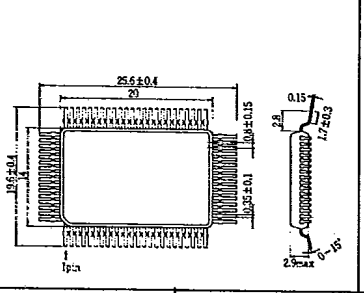
DP64



FPP54



FPP80



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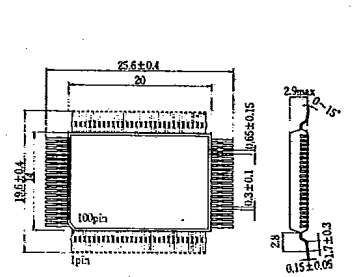
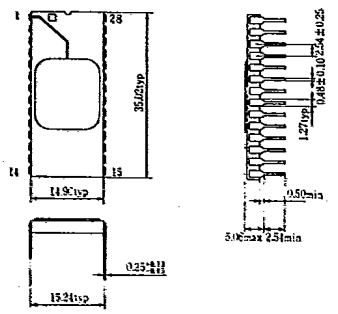
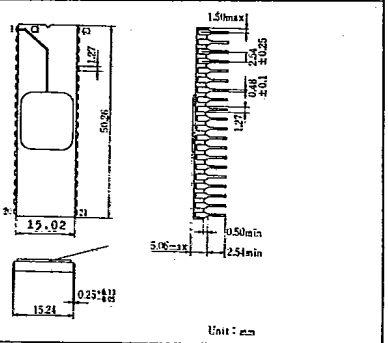


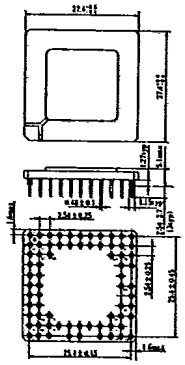
DC28



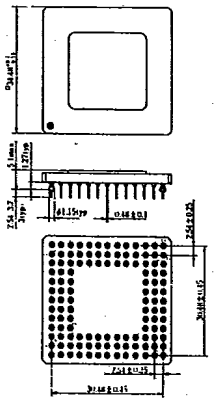
DC40



PGA72



PGA120



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