



# STD4NC50 STD4NC50-1

## N-CHANNEL 500V - 1.3Ω - 3.7A DPAK/IPAK PowerMesh™II MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD4NC50	500V	<1.5Ω	3.7A
STD4NC50-1	500V	<1.5Ω	3.7A

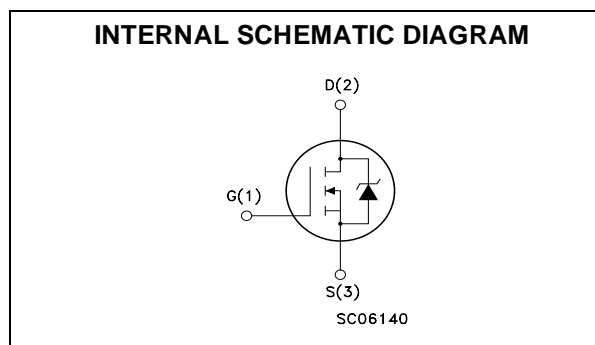
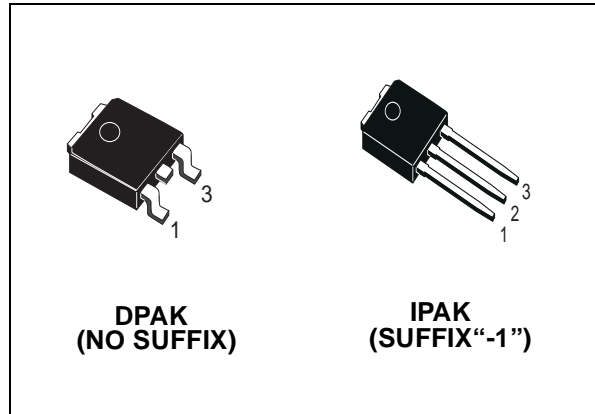
- TYPICAL R<sub>DS(on)</sub> = 1.3Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

### DESCRIPTION

The PowerMESH™II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron\*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

### APPLICATIONS

- SWITCH MODE LOW POWER SUPPLIES (SMPS)
- HIGH CURRENT, HIGH SPEED SWITCHING
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVES



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	500	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	500	V
V <sub>GS</sub>	Gate- source Voltage	±30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	3.7	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	2.3	A
I <sub>DM</sub> (*)	Drain Current (pulsed)	14.8	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	50	W
	Derating Factor	0.4	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(\*)Pulse width limited by safe operating area

(1)I<sub>SD</sub> ≤ 3.7A, di/dt ≤ 100A/μs, V<sub>DD</sub> ≤ V(BR)DSS, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

## STD4NC50/-1

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	2.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	100	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	275	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	3.7	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	220	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1.9 A		1.3	1.5	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 1.9A		3		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		700		pF
C <sub>OSS</sub>	Output Capacitance			85		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			9		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V, I_D = 1.9 A$ $R_G = 4.7\Omega, V_{GS} = 10V$		11.5		ns
$t_r$	Rise Time	(see test circuit, Figure 3)		9		ns
$Q_g$	Total Gate Charge	$V_{DD} = 400V, I_D = 3.7 A,$ $V_{GS} = 10V$		18	25	nC
$Q_{gs}$	Gate-Source Charge			6		nC
$Q_{gd}$	Gate-Drain Charge			8		nC

**SWITCHING OFF**

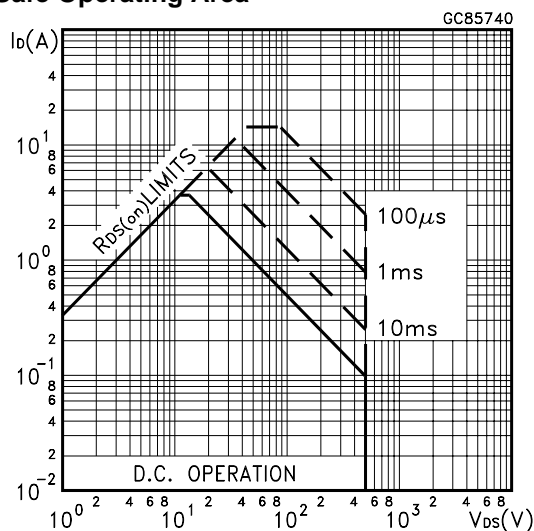
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400V, I_D = 3.7 A,$ $R_G = 4.7\Omega, V_{GS} = 10V$		7		ns
$t_f$	Fall Time	(see test circuit, Figure 5)		6		ns
$t_c$	Cross-over Time			13		ns

**SOURCE DRAIN DIODE**

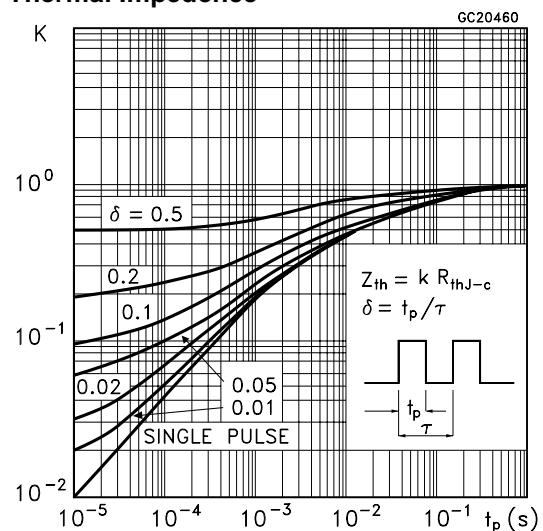
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				3.7	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				14.8	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 3.7A, V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 3.7A, di/dt = 100A/\mu s,$ $V_{DD} = 100V, T_j = 150^\circ C$		380		ns
$Q_{rr}$	Reverse Recovery Charge	(see test circuit, Figure 5)		2.3		$\mu C$
$I_{RRM}$	Reverse Recovery Current			12		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

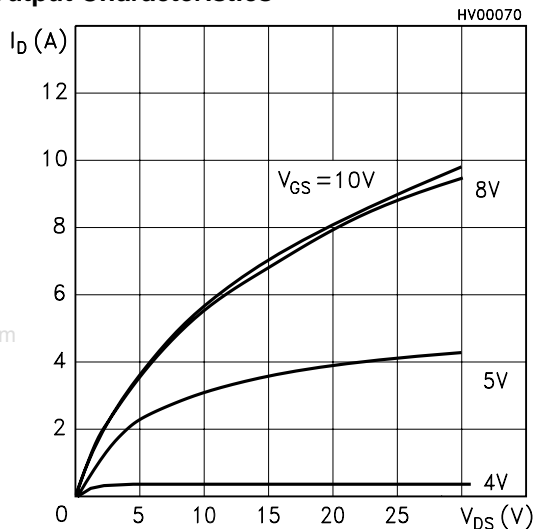
**Safe Operating Area**



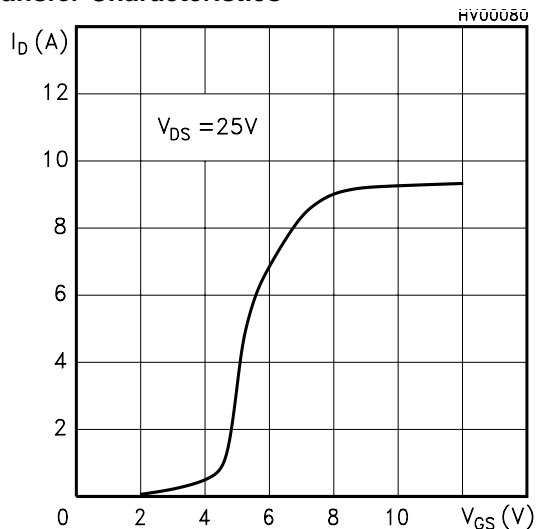
**Thermal Impedance**



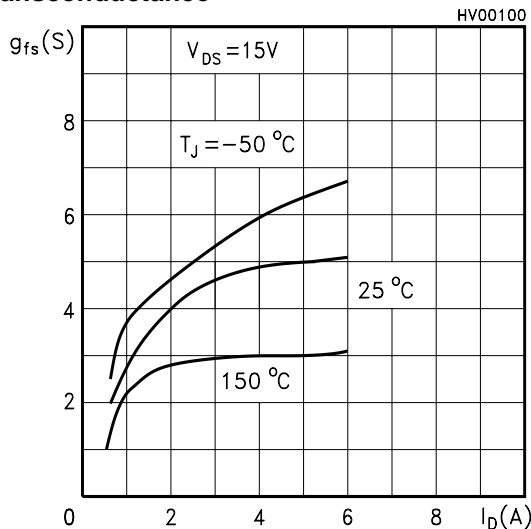
Output Characteristics



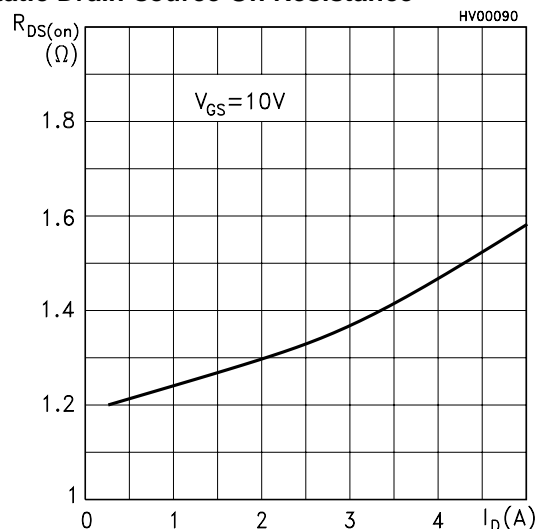
Transfer Characteristics



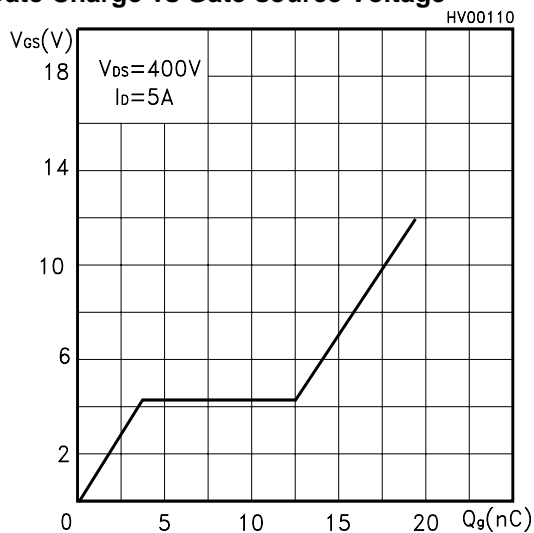
Transconductance



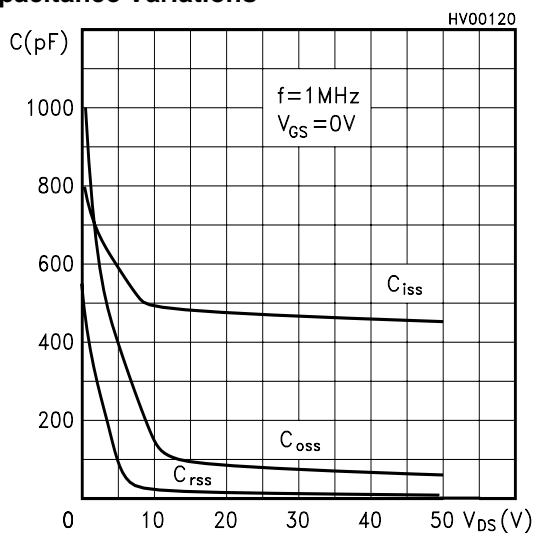
Static Drain-source On Resistance



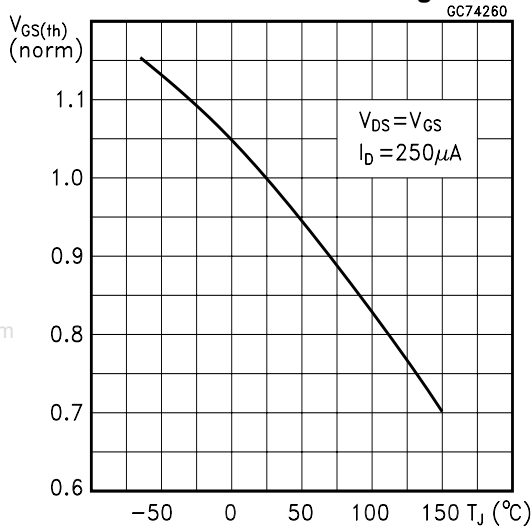
Gate Charge vs Gate-source Voltage



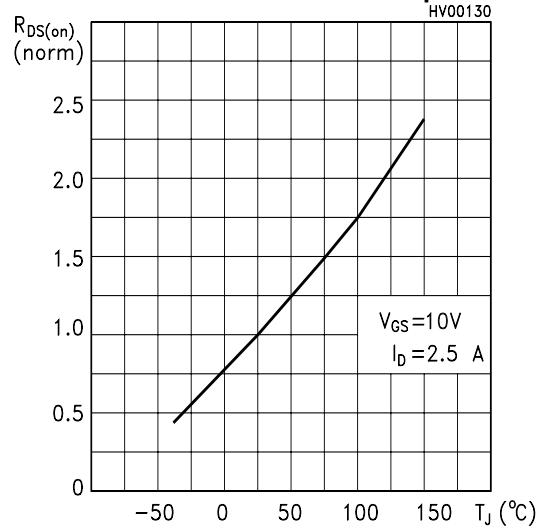
Capacitance Variations



Normalized Gate Thershold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

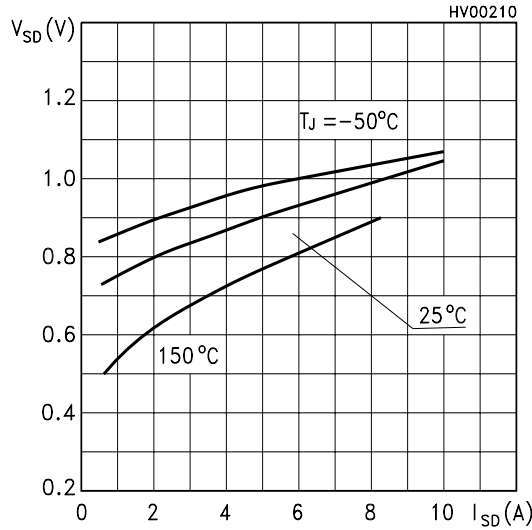


Fig. 1: Unclamped Inductive Load Test Circuit

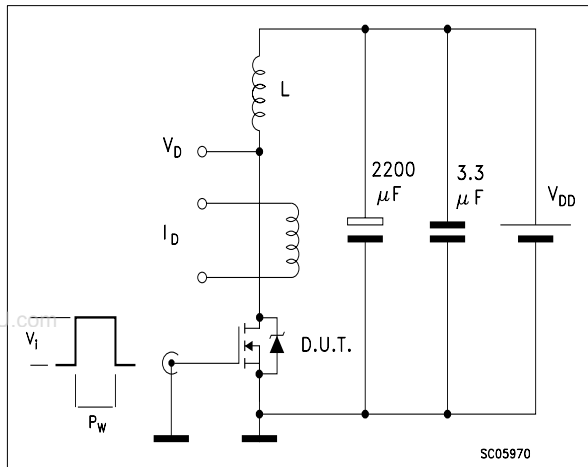


Fig. 2: Unclamped Inductive Waveform

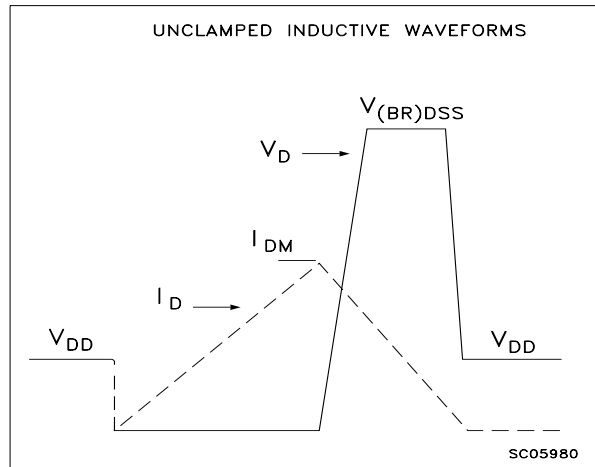


Fig. 3: Switching Times Test Circuit For Resistive Load

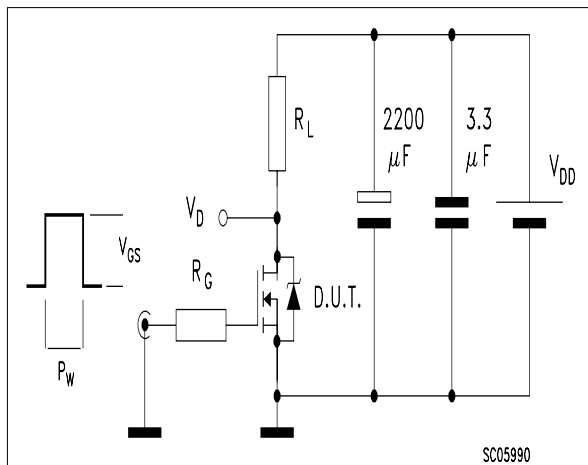


Fig. 4: Gate Charge test Circuit

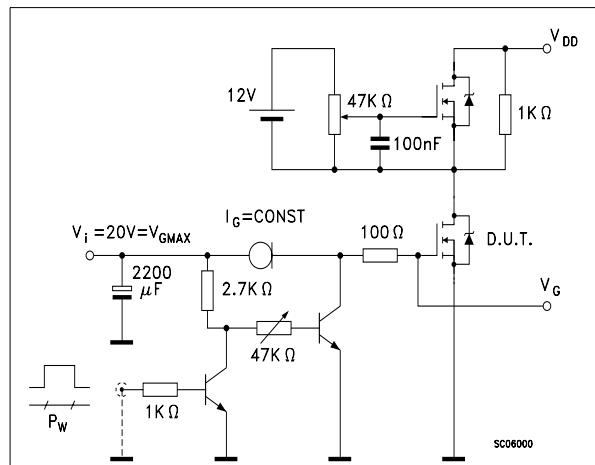
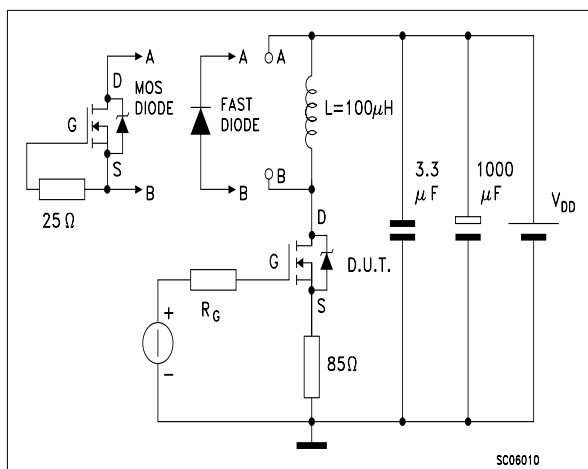
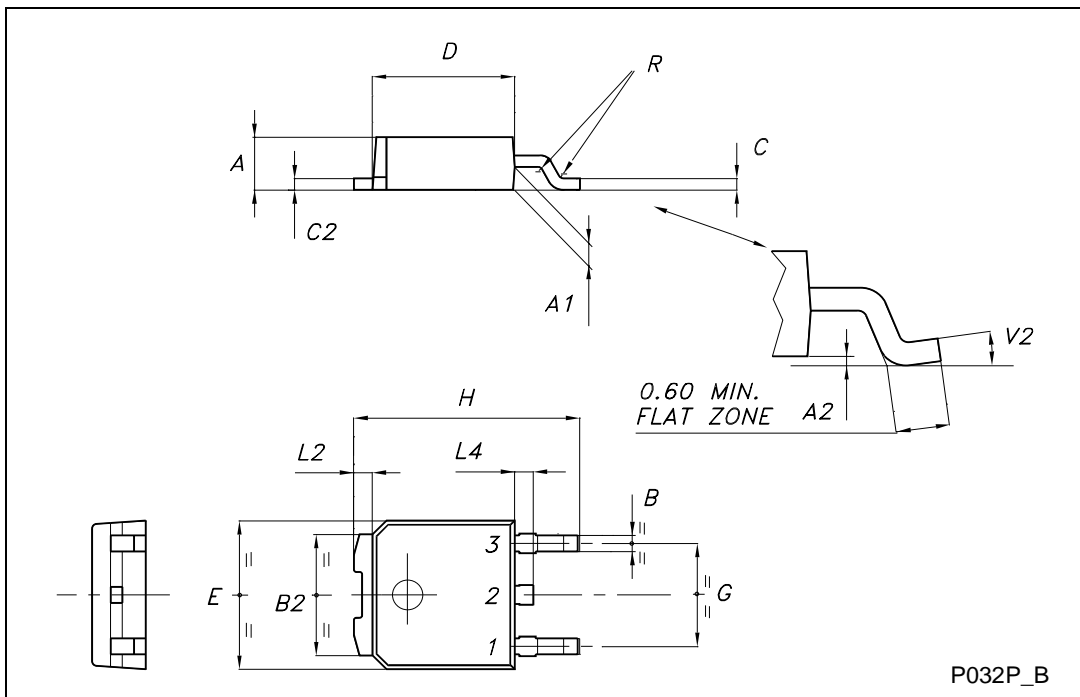


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

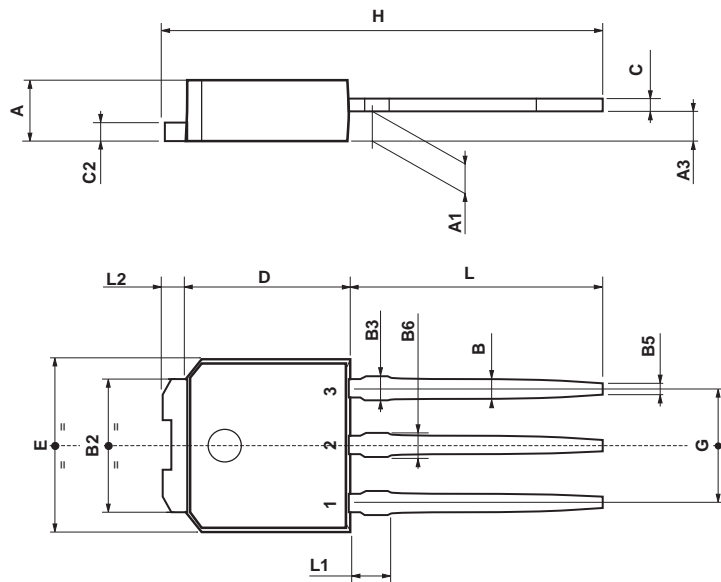
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



P032P\_B

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



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