PM7820 PALADIN 20

Digital Multicarrier Device

Preliminary
Product Brief

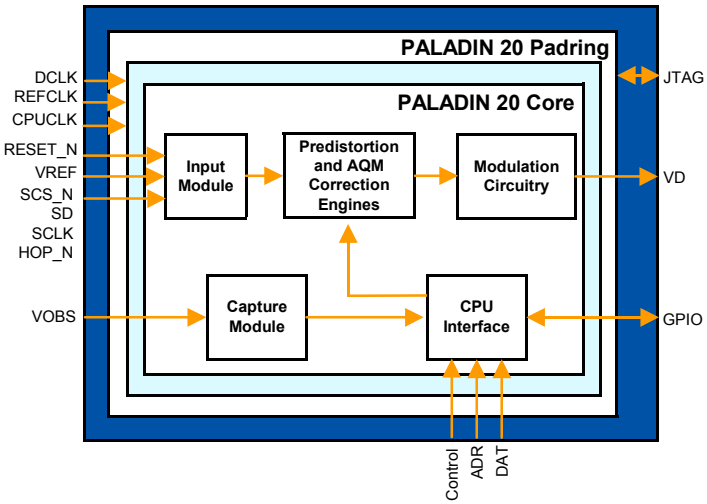
PRODUCT OVERVIEW

The PALADIN family of digital multicarrier chip technologies enables the development of spectrally efficient and power efficient 3G and WiMAX base stations that use fewer and less expensive components than traditional feedforward designs. The PALADIN products, which include the PM7800 PALADIN 10, PM7815 PALADIN 15, PM7820 PALADIN 20, and the PM7819 PALADIN WAVESHAPER, make extensive use of proprietary advanced high-speed DSP-based architectures and techniques.

The PM7820 PALADIN 20 device inhibits distortion in the power amplifier and transmitter chain of cellular base stations using digital adaptive predistortion techniques. The PALADIN 20 device supports the new Doherty power amplifier (PA) architectures in BTS designs, which achieve power efficiencies of more than 40 per cent, doubling the efficiency of currently deployed Class A/B LDMOS PAs. The device also enables integration into space-constrained next generation Remote Radio Head (RRH) architectures, through its 23 mm x 23 mm footprint. As well, the device provides 20 MHz of bandwidth for WCDMA, CDMA2000, and WiMAX applications.

The PALADIN 20 system comprises a Digital Correction Signal Processor (DCSP) chip and an Adaptive Control Processor Compensation Engine (ACPCE). The DCSP applies corrective parameters to each sample in real time, while the ACPCE automatically adapts the corrective parameters to maintain optimum performance as the distortions change over time.

BLOCK DIAGRAM



BENEFITS

- The PALADIN 20 device is the only complete, off-the-shelf, production-released, standard product for DPD.
- The PALADIN family is deployed in Carrier Networks today.
- The PALADIN family has proven performance and reliability.
- The PALADIN family includes production-ready firmware that implements a comprehensive, industry-leading, predistortion algorithm.

PRODUCT HIGHLIGHTS

- Input signal bandwidth up to 20 MHz
- Output sample rate up to 93 MHz
- Digital AQM compensation
- Automatic Gain Control to +/-0.1 dB
- Constant-gain mode to facilitate operation at higher efficiency
- Variable input sample rate
- 32-bit complex baseband reference signal input
- 32-bit complex baseband or 16-bit IF output
- 16- or 32-bit observation signal input
- Digital correction of Analog Quadrature
- Modulation distortion for practical zero-IF upconversion.
- Automatic adjustment of corrective parameters in response to changing RMS signal levels
- Algorithm structure takes into account the challenging magnitude and phase variations in the Doherty power amplifier
- Algorithm's fast adaptation time assists in mitigating the non-linear effects in the PA
- Pre-distortion kernel for linearization of power amplifiers in wireless base-stations
- Built-in interpolation-by-*n* of baseband input sample rate to the required DCSP sample rate where the integer *n* can be set to a value between 1 and 10 inclusive
- Generic 16-bit microprocessor bus interface for configuration, control, and monitoring
- 48 general-purpose I/O pins, eight of which are edge-triggered interrupt sources
- Standard five-signal IEEE 1149.1 JTAG test port for boundary scan board test purposes

PMC-2061427, Issue 2

PMC-SIERRA

MULTIPLE AIR INTERFACES

- Supports macro BTS, micro BTS, and RRH architectures
- Supports up to 4-carrier WCDMA systems
- Supports up to 16-carrier CDMA2000 systems
- Meets the FCC 04-258 WiMAX specification

DIGITAL CORRECTION SIGNAL PROCESSOR (DCSP)

- Includes the following interfaces:
  - Digital Baseband interface to the base station modem (Vref)
  - Digital IF or Digital Baseband interface to DAC(s) and RF Upconverter (VD)
  - Digital IF interface from ADC(s) and RF Downconverter (Vobs)
  - GPIO interface for auxliary monitor and control
  - CPU interface to ACPCE processor (external DSP)

ALARMS/DEBUGGING CAPABILITY

- Real time tracking of PA state
- Alarms that alert users to issues in the field such as potential ACPR violation and PA aging
- Various PA statistic monitoring (magnitude and phase behavior)
- Logging to detect issues in transmit chain and observation path

FIRMWARE

- State-of-the-art firmware provided
- Firmware upgradeable to accommodate new features

POWER, TEMPERATURE & PACKAGING

- Maximum 1 W power output
- Industrial temperature range (-40 °C to +85 °C)
- Low-power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs
- 324-pin PBGA with a body size of 23 mm x 23 mm optimized for RRH architectures

APPLICATIONS

- Multi-carrier WCDMA, CDMA2000 1xRTT, CDMA2000 EV-DO, WiMAX, and WiBRO base station transmitters

FURTHER RESOURCES

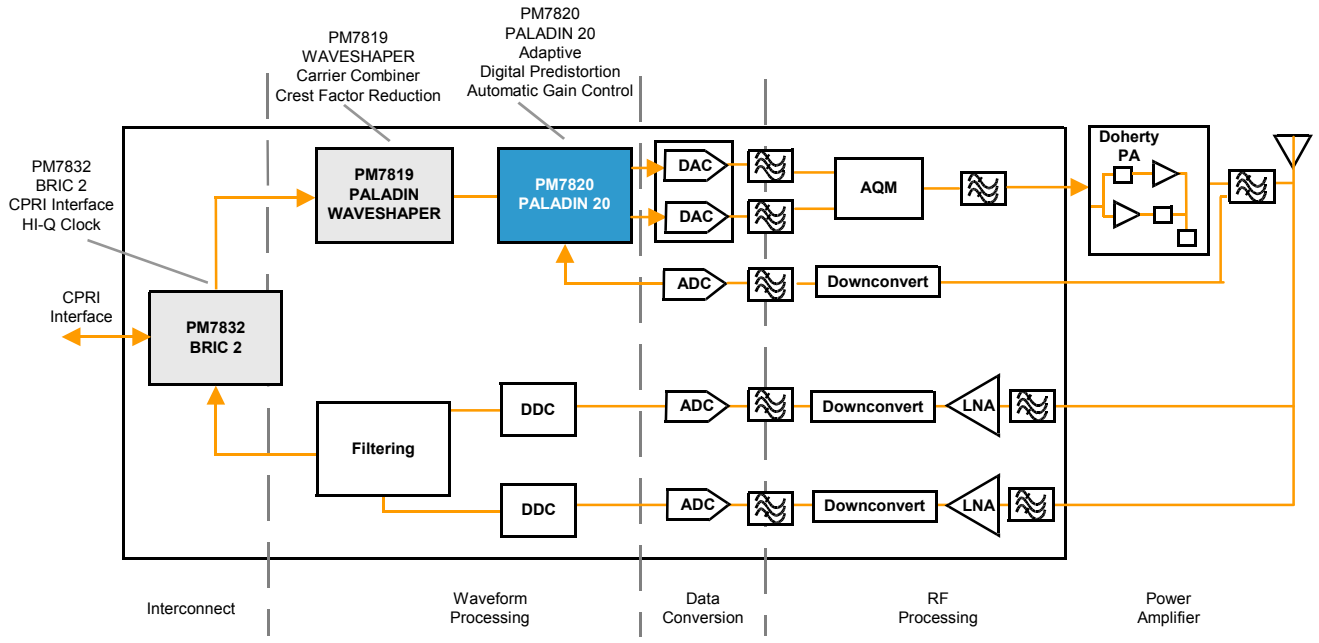
WIRELESS BSC/BTS PRODUCTS

www.pmc-sierra.com/wireless/

TECHNICAL DOCUMENTATION

www.pmc-sierra.com/documentation/

REMOTE RADIO HEAD RF SYSTEM



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