Independent Clock Quad HOTLink II™ Reclocking Deserializer

Features

- **Second-generation HOTLink® technology**
- **Compliant to SMPTE 292M and SMPTE 259M video standards**
- **Quad channel video reclocking deserializer**
  - **195- to 1500-Mbps serial data signaling rate**
  - **Simultaneous operation at different signaling rates**
- **Supports reception of either 1.485 or 1.485/1.001 Gbps data rate with the same training clock**
- **Supports half-rate and full-rate clocking**
- **Internal phase-locked loops (PLLs) with no external PLL components**
- **Selectable differential PECL-compatible serial inputs**
  - **Internal DC-restoration**
- **Synchronous LVTTL parallel interface**
- **JTAG boundary scan**
- **Built-In Self-Test (BIST) for at-speed link testing**
- **Link Quality Indicator**
  - **Analog signal detect**
  - **Digital signal detect**
- **Low-power 3W @ 3.3V typical**
- **Single 3.3V supply**
- **Thermally enhanced BGA**
- **Pb-Free package option available**
- **0.25μ BiCMOS technology**

Functional Description

The CYV15G0404RB Independent Clock Quad HOTLink II™ Deserializing Reclocker is a point-to-point or point-to-multi-point communications building block enabling transfer of data over a variety of high-speed serial links including SMPTE 292 and SMPTE 259 video applications. It supports signaling rates in the range of 195 to 1500 Mbps per serial link. The four channels are independent and can simultaneously operate at different rates. Each receive channel accepts serial data and converts it to 10-bit parallel characters and presents these characters to an Output Register. The received serial data can also be reclocked and retransmitted through the reclocker serial outputs. *Figure 1* illustrates typical connections between independent video co-processors and corresponding CYV15G0404RB Reclocking Deserializer and CYV15G0403TB Serializer chips.

The CYV15G0404RB satisfies the SMPTE-259M and SMPTE-292M compliance as per SMPTE EG34-1999 Patho-logical Test Requirements.

As a second-generation HOTLink device, the CYV15G0404RB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data and BIST) with other HOTLink devices.

Each channel of the CYV15G0404RB Quad HOTLink II device accepts a serial bit-stream from one of two selectable PECL-compatible differential line receivers, and using a completely integrated Clock and Data Recovery PLL, recovers the timing information necessary for data reconstruction. The recovered bit-stream is reclocked and retransmitted through the reclocker serial outputs. Also, the recovered serial data is deserialized and presented to the destination host system.

Each channel contains an independent BIST pattern checker. This BIST hardware allows at-speed testing of the high-speed serial data paths in each receive section of this device, each transmit section of a connected HOTLink II device, and across the interconnecting links.

The CYV15G0404RB is ideal for SMPTE applications where different data rates and serial interface standards are necessary for each channel. Some applications include multi-format routers, switchers, format converters, SDI monitors, and camera control units.

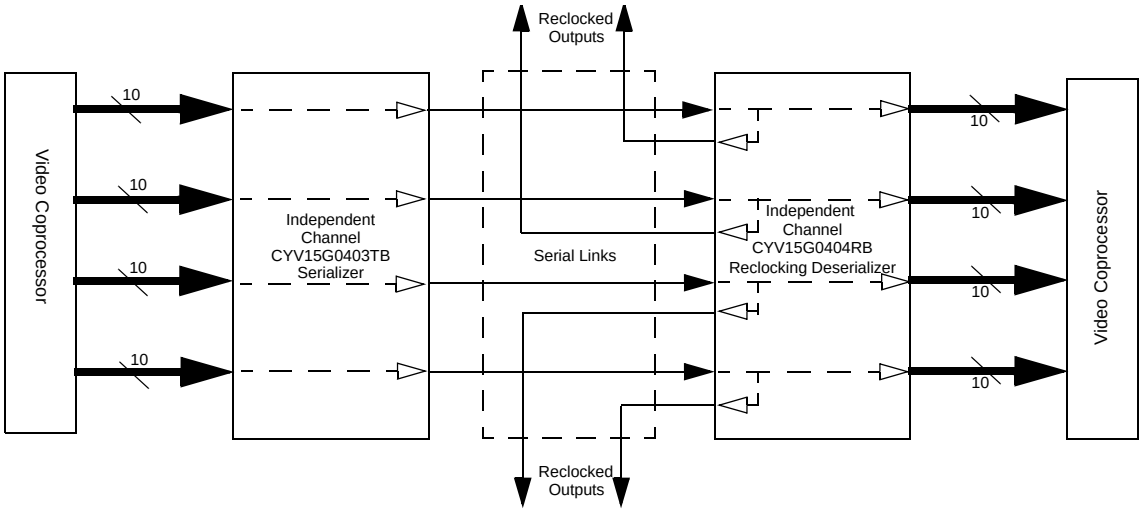
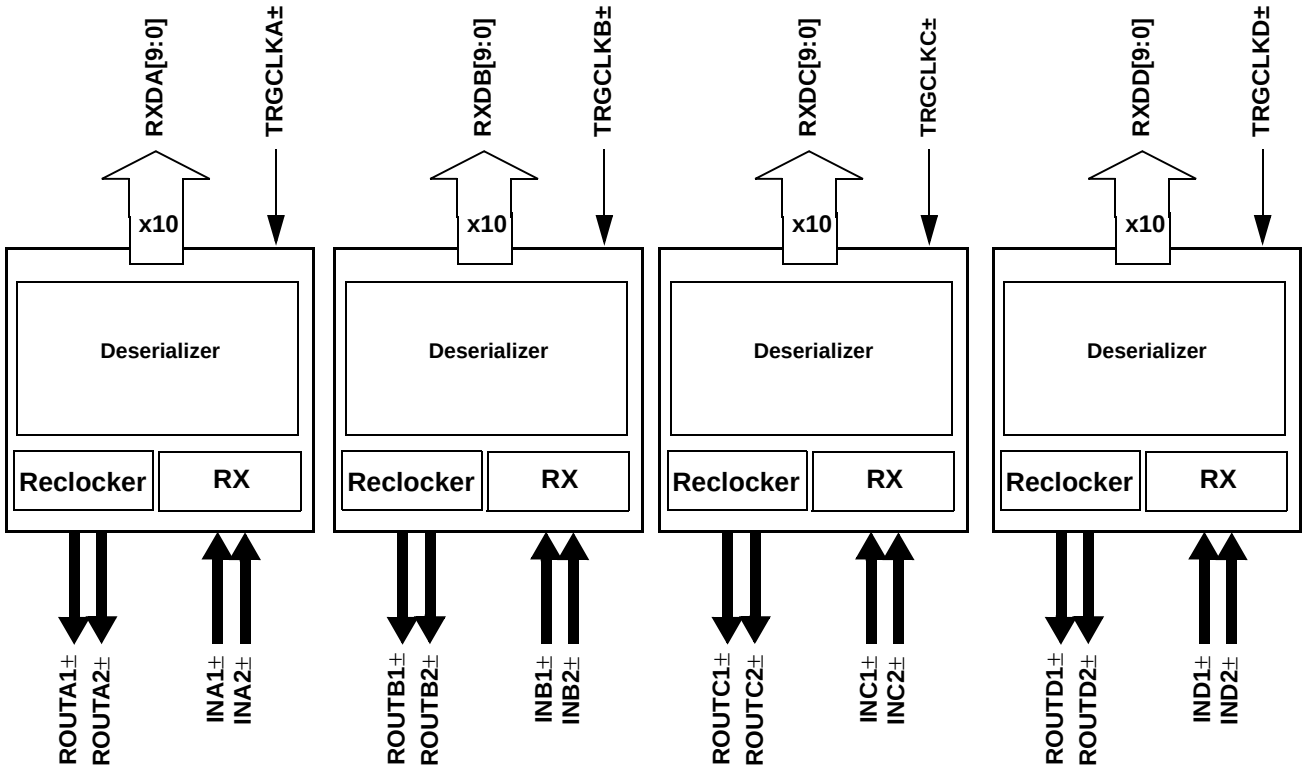
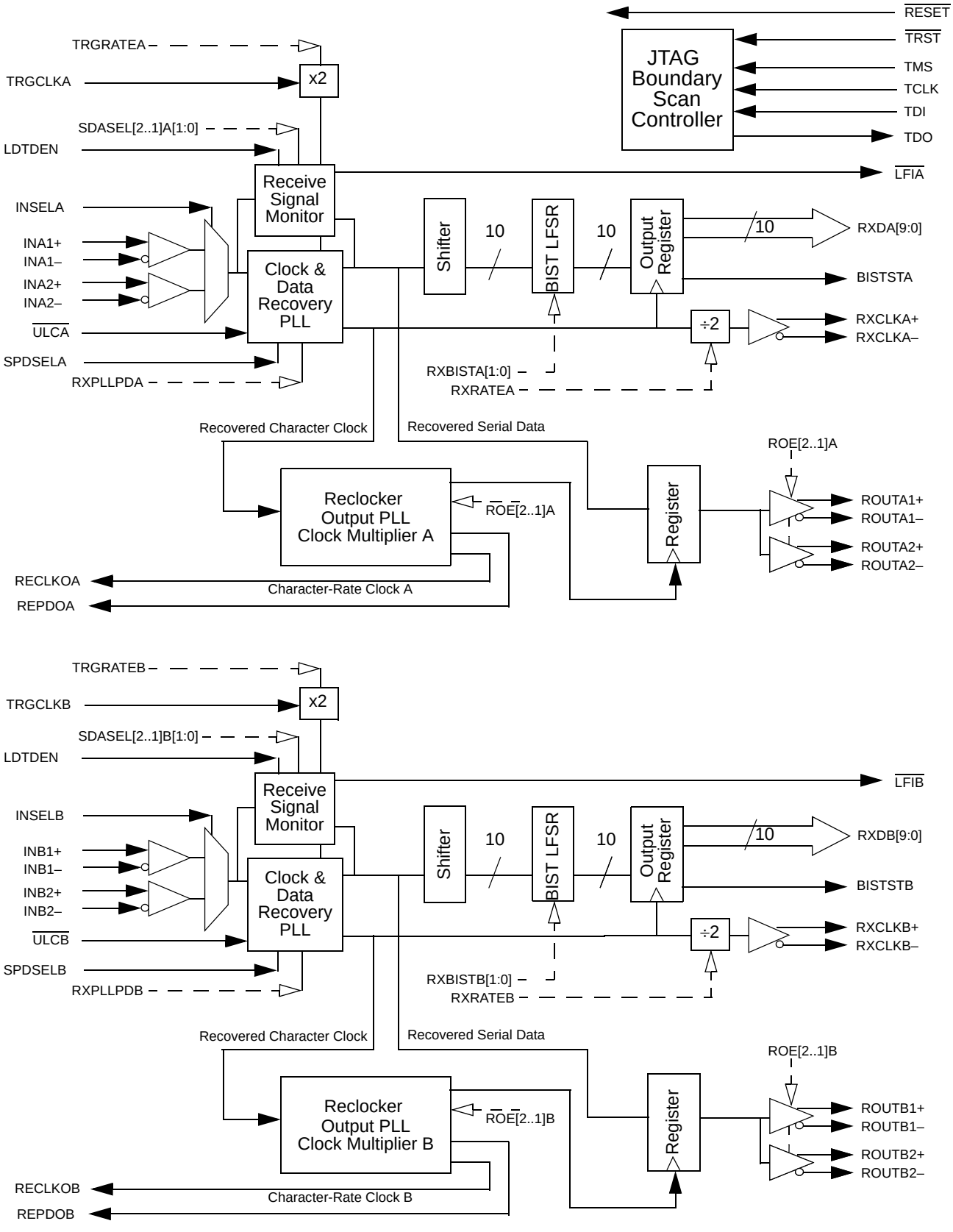


Figure 1. HOTLink II™ System Connections

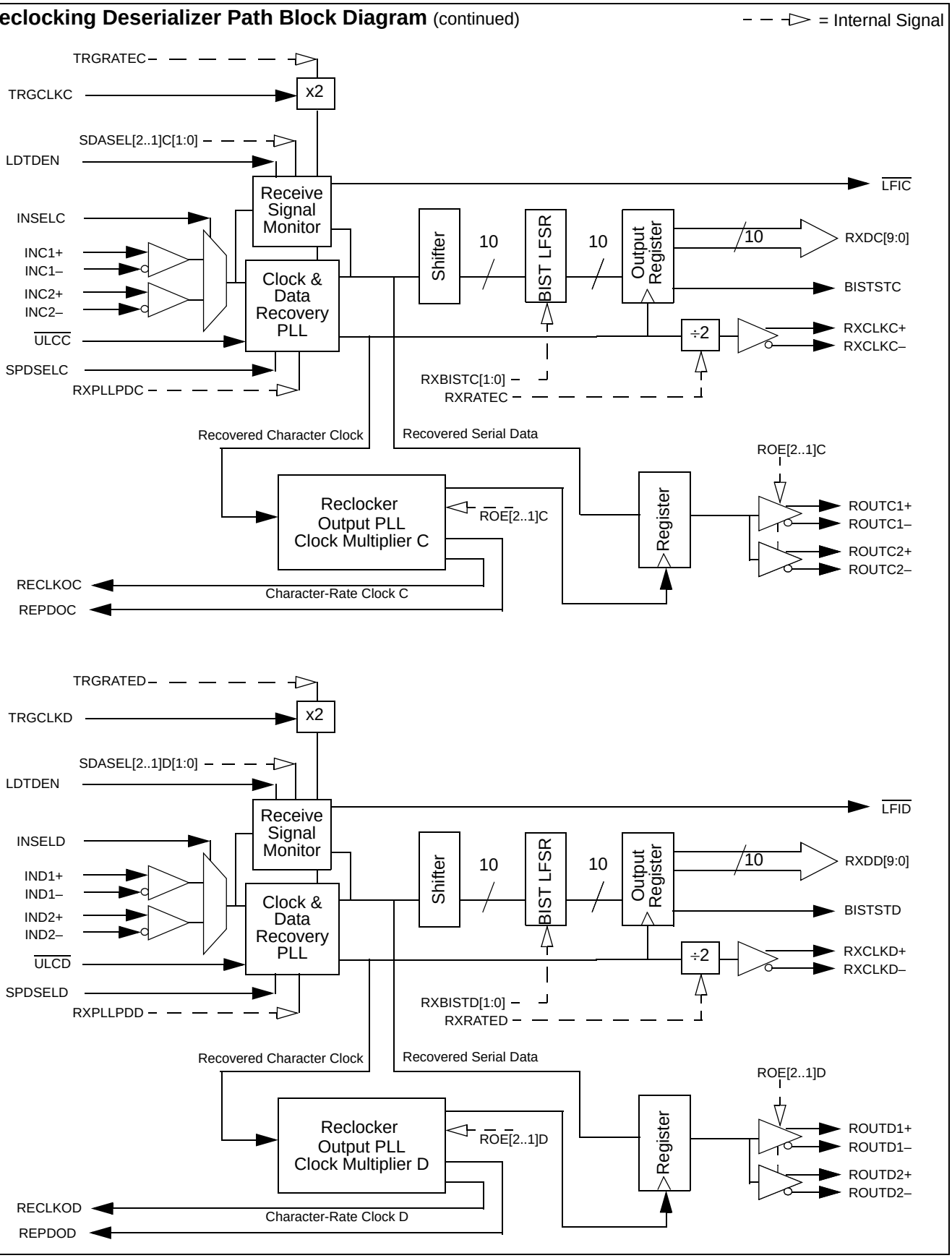
CYV15G0404RB Deserializing Reclocker Logic Block Diagram



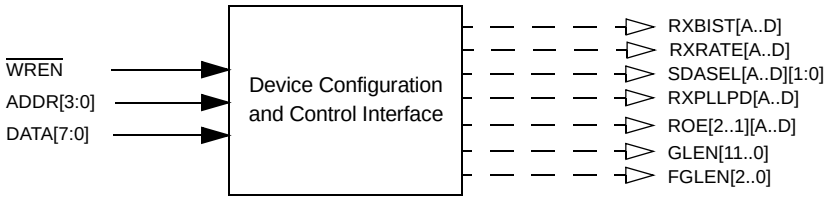
Reclocking Deserializer Path Block Diagram



Reclocking Deserializer Path Block Diagram (continued)



Device Configuration and Control Block Diagram



Pin Configuration (Top View)[1]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	IN C1–	ROUT C1–	IN C2–	ROUT C2–	V_{CC}	IN D1–	ROUT D1–	GND	IN D2–	ROUT D2–	IN A1–	ROUT A1–	GND	IN A2–	ROUT A2–	V_{CC}	IN B1–	ROUT B1–	IN B2–	ROUT B2–
B	IN C1+	ROUT C1+	IN C2+	ROUT C2+	V_{CC}	IN D1+	ROUT D1+	GND	IN D2+	ROUT D2+	IN A1+	ROUT A1+	GND	IN A2+	ROUT A2+	V_{CC}	IN B1+	ROUT B1+	IN B2+	ROUT B2+
C	TDI	TMS	INSELC	INSELB	V_{CC}	$\overline{\text{ULCD}}$	$\overline{\text{ULCC}}$	GND	DATA [7]	DATA [5]	DATA [3]	DATA [1]	GND	V_{CC}	SPD SELD	V_{CC}	LDTD EN	$\overline{\text{TRST}}$	GND	TDO
D	TCLK	$\overline{\text{RESET}}$	INSELD	INSELA	V_{CC}	$\overline{\text{ULCA}}$	SPD SELC	GND	DATA [6]	DATA [4]	DATA [2]	DATA [0]	GND	GND	$\overline{\text{ULCB}}$	V_{CC}	NC	V_{CC}	SCAN EN2	TMEN3
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	RX DC[8]	RX DC[9]	V_{CC}	V_{CC}													V_{CC}	RX DB[0]	RE CLKOB	RX DB[1]
G	GND	$\overline{\text{WREN}}$	GND	GND													SPD SELB	NC	SPD SELA	RX DB[3]
H	GND	GND	GND	GND													GND	GND	GND	GND
J	GND	GND	GND	GND													BIST STB	RX DB[2]	RX DB[7]	RX DB[4]
K	RX DC[4]	TRG CLKC–	GND	GND													RX DB[5]	RX DB[6]	RX DB[9]	$\overline{\text{LFIB}}$
L	RX DC[5]	TRG CLKC+	$\overline{\text{LFIC}}$	GND													RX DB[8]	RX CLKB+	RX CLKB–	GND
M	RX DC[6]	RX DC[7]	V_{CC}	RE PDOC													TRG CLKB+	TRG CLKB–	RE PDOB	GND
N	GND	GND	GND	GND													GND	GND	GND	GND
P	RX DC[3]	RX DC[2]	RX DC[1]	RX DC[0]													GND	GND	GND	GND
R	BIST STC	RE CLKOC	RX CLKC+	RX CLKC–													V_{CC}	V_{CC}	V_{CC}	V_{CC}
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	RX DD[4]	RX DD[3]	GND	GND	ADDR [0]	TRG CLKD–	GND	GND	GND	V_{CC}	V_{CC}	RX DA[4]	V_{CC}	BIST STA	RX DA[0]
V	V_{CC}	V_{CC}	V_{CC}	RX DD[8]	V_{CC}	RX DD[5]	RX DD[1]	GND	BIST STD	ADDR [2]	TRG CLKD+	RE CLKOA	GND	GND	V_{CC}	V_{CC}	RX DA[9]	RX DA[5]	RX DA[2]	RX DA[1]
W	V_{CC}	V_{CC}	$\overline{\text{LFID}}$	RX CLKD–	V_{CC}	RX DD[6]	RX DD[0]	GND	ADDR [3]	ADDR [1]	RX CLKA+	RE PDOA	GND	GND	V_{CC}	V_{CC}	$\overline{\text{LFIA}}$	TRG CLKA+	RX DA[6]	RX DA[3]
Y	V_{CC}	V_{CC}	RX DD[9]	RX CLKD+	V_{CC}	RX DD[7]	RX DD[2]	GND	RE CLKOD	NC	GND	RX CLKA–	GND	GND	V_{CC}	V_{CC}	RE PDOD	TRG CLKA–	RX DA[8]	RX DA[7]

Note:
1. NC = Do not connect.

Pin Configuration (Bottom View)[1]

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	ROUT B2–	IN B2–	ROUT B1–	IN B1–	V_{CC}	ROUT A2–	IN A2–	GND	ROUT A1–	IN A1–	ROUT D2–	IN D2–	GND	ROUT D1–	IN D1–	V_{CC}	ROUT C2–	IN C2–	ROUT C1–	IN C1–
B	ROUT B2+	IN B2+	ROUT B1+	IN B1+	V_{CC}	ROUT A2+	IN A2+	GND	ROUT A1+	IN A1+	ROUT D2+	IN D2+	GND	ROUT D1+	IN D1+	V_{CC}	ROUT C2+	IN C2+	ROUT C1+	IN C1+
C	TDO	GND	$\overline{TRST}$	LDTD EN	V_{CC}	SPD SELD	V_{CC}	GND	DATA [1]	DATA [3]	DATA [5]	DATA [7]	GND	$\overline{ULCC}$	$\overline{ULCD}$	V_{CC}	INSELB	INSELC	TMS	TDI
D	TMEN3	SCAN EN2	V_{CC}	NC	V_{CC}	$\overline{ULCB}$	GND	GND	DATA [0]	DATA [2]	DATA [4]	DATA [6]	GND	SPD SELC	$\overline{ULCA}$	V_{CC}	INSELA	INSELD	$\overline{RESET}$	TCLK
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	RX DB[1]	RE CLKOB	RX DB[0]	V_{CC}													V_{CC}	V_{CC}	RX DC[9]	RX DC[8]
G	RX DB[3]	SPD SELA	NC	SPD SELB													GND	GND	$\overline{WREN}$	GND
H	GND	GND	GND	GND													GND	GND	GND	GND
J	RX DB[4]	RX DB[7]	RX DB[2]	BIST STB													GND	GND	GND	GND
K	$\overline{LFIB}$	RX DB[9]	RX DB[6]	RX DB[5]													GND	GND	TRG CLKC–	RX DC[4]
L	GND	RX CLKB–	RX CLKB+	RX DB[8]													GND	$\overline{LFIC}$	TRG CLKC+	RX DC[5]
M	GND	RE PDOB	TRG CLKB–	TRG CLKB+													RE PDOC	V_{CC}	RX DC[7]	RX DC[6]
N	GND	GND	GND	GND													GND	GND	GND	GND
P	GND	GND	GND	GND													RX DC[0]	RX DC[1]	RX DC[2]	RX DC[3]
R	V_{CC}	V_{CC}	V_{CC}	V_{CC}													RX CLKC–	RX CLKC+	RE CLKOC	BIST STC
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	RX DA[0]	BIST STA	V_{CC}	RX DA[4]	V_{CC}	V_{CC}	GND	GND	GND	TRG CLKD–	ADDR [0]	GND	GND	RX DD[3]	RX DD[4]	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V	RX DA[1]	RX DA[2]	RX DA[5]	RX DA[9]	V_{CC}	V_{CC}	GND	GND	RE CLKOA	TRG CLKD+	ADDR [2]	BIST STD	GND	RX DD[1]	RX DD[5]	V_{CC}	RX DD[8]	V_{CC}	V_{CC}	V_{CC}
W	RX DA[3]	RX DA[6]	TRG CLKA+	$\overline{LFIA}$	V_{CC}	V_{CC}	GND	GND	RE PDOA	RX CLKA+	ADDR [1]	ADDR [3]	GND	RX DD[0]	RX DD[6]	V_{CC}	RX CLKD–	$\overline{LFID}$	V_{CC}	V_{CC}
Y	RX DA[7]	RX DA[8]	TRG CLKA–	RE PDOD	V_{CC}	V_{CC}	GND	GND	RX CLKA–	GND	NC	RE CLKOD	GND	RX DD[2]	RX DD[7]	V_{CC}	RX CLKD+	RX DD[9]	V_{CC}	V_{CC}

Pin Definitions
CYV15G0404RB Quad HOTLink II Deserializing Reclocker

Name	I/O Characteristics	Signal Description
Receive Path Data and Status Signals		
RXDA[9:0] RXDB[9:0] RXDC[9:0] RXDD[9:0]	LVTTL Output, synchronous to the RXCLK± output	**Parallel Data Output**. RXDx[9:0] parallel data outputs change relative to the receive interface clock. If RXCLKx± is a full-rate clock, the RXCLKx± clock outputs are complementary clocks operating at the character rate. The RXDx[9:0] outputs for the associated receive channels follow rising edge of RXCLKx+ or falling edge of RXCLKx–. If RXCLKx± is a half-rate clock, the RXCLKx± clock outputs are complementary clocks operating at half the character rate. The RXDx[9:0] outputs for the associated receive channels follow both the falling and rising edges of the associated RXCLKx± clock outputs. When BIST is enabled on the receive channel, the BIST status is presented on the RXDx[1:0] and BISTSTx outputs. See *Table 5* for each status reported by the BIST state machine. Also, while BIST is enabled, the RXDx[9:2] outputs should be ignored.
BISTSTA BISTSTB BISTSTC BISTSTD	LVTTL Output, synchronous to the RXCLKx ± output	**BIST Status Output.** When RXBISTx[1:0] = 10, BISTSTx (along with RXDx[1:0]) displays the status of the BIST reception. See *Table 5* for the BIST status reported for each combination of BISTSTx and RXDx[1:0]. When RXBISTx[1:0] ≠ 10, BISTSTx should be ignored.
REPDOA REPDOB REPDOC REPDOD	Asynchronous to reclocker output channel enable / disable	**Reclocker Powered Down Status Output.** REPDOx is asserted HIGH, when the associated channel's reclocker output logic is powered down. This occurs when ROE2x and ROE1x are both disabled by setting ROE2x = 0 and ROE1x = 0.
Receive Path Clock Signals		
TRGCLKA± TRGCLKB± TRGCLKC± TRGCLKD±	Differential LVPECL or single-ended LVTTL input clock	**CDR PLL Training Clock**. TRGCLKx± clock inputs are used as the reference source for the frequency detector (Range Controller) of the associated receive PLL to reduce PLL acquisition time. In the presence of valid serial data, the recovered clock output of the receive CDR PLL (RXCLKx±) has no frequency or phase relationship with TRGCLKx±. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement TRGCLKx input, and leave the alternate TRGCLKx input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs.
RXCLKA± RXCLKB± RXCLKC± RXCLKD±	LVTTL Output Clock	**Receive Clock Output**. RXCLKx± is the receive interface clock used to control timing of the RXDx[9:0] parallel outputs. These true and complement clocks are used to control timing of data output transfers. These clocks are output continuously at either the half-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATEx.
RECLKOA RECLKOB RECLKOC RECLKOD	LVTTL Output	**Reclocker Clock Output**. RECLKOx output clock is synthesized by the associated reclocker output PLL and operates synchronous to the internal recovered character clock. RECLKOx operates at either the same frequency as RXCLKx± (RXRATEx = 0), or at twice the frequency of RXCLKx± (RXRATEx = 1).The reclocker clock outputs have no fixed phase relationship to RXCLKx±.
Device Control Signals		
$\overline{\text{RESET}}$	LVTTL Input, asynchronous, internal pull-up	**Asynchronous Device Reset**. $\overline{\text{RESET}}$ initializes all state machines, counters, and configuration latches in the device to a known state. $\overline{\text{RESET}}$ must be asserted LOW for a minimum pulse width. When the reset is removed, all state machines, counters and configuration latches are at an initial state. See *Table 3* for the initialize values of the device configuration latches.

Pin Definitions (continued)
CYV15G0404RB Quad HOTLink II Deserializing Reclocker

Name	I/O Characteristics	Signal Description
LDTDEN	LVTTL Input, internal pull-up	**Level Detect Transition Density Enable**. When LDTDEN is HIGH, the Signal Level Detector, Range Controller, and Transition Density Detector are all enabled to determine if the RXPLL tracks TRGCLKx± or the selected input serial data stream. If the Signal Level Detector, Range Controller, or Transition Density Detector are out of their respective limits while LDTDEN is HIGH, the RXPLL locks to TRGCLKx± until such a time they become valid. The SDASEL[A..D][1:0] inputs are used to configure the trip level of the Signal Level Detector. The Transition Density Detector limit is one transition in every 60 consecutive bits. When LDTDEN is LOW, only the Range Controller is used to determine if the RXPLL tracks TRGCLKx± or the selected input serial data stream. It is recommended to set LDTDEN = HIGH.
ULCA ULCB ULCC ULCD	LVTTL Input, internal pull-up	**Use Local Clock**. When ULCx is LOW, the RXPLL is forced to lock to TRGCLKx± instead of the received serial data stream. While ULCx is LOW, the LFIx for the associated channel is LOW indicating a link fault. When ULCx is HIGH, the RXPLL performs Clock and Data Recovery functions on the input data streams. This function is used in applications in which a stable RXCLKx± is needed. In cases when there is an absence of valid data transitions for a long period of time, or the high-gain differential serial inputs (INx±) are left floating, there may be brief frequency excursions of the RXCLKx± outputs from TRGCLKx±.
SPDSELA SPDSELB SPDSELC SPDSELD	3-Level Select[2] static control input	**Serial Rate Select**. The SPDSELx inputs specify the operating signaling-rate range of each channel's receive PLL. LOW = 195 – 400 MBd MID = 400 – 800 MBd HIGH = 800 – 1500 MBd.
INSELA INSELB INSELC INSELD	LVTTL Input, asynchronous	**Receive Input Selector**. The INSELx input determines which external serial bit stream is passed to the receiver's Clock and Data Recovery circuit. When INSELx is HIGH, the Primary Differential Serial Data Input, INx1±, is selected for the associated receive channel. When INSELx is LOW, the Secondary Differential Serial Data Input, INx2±, is selected for the associated receive channel.
LFIA LFIB LFIC LFID	LVTTL Output, asynchronous	**Link Fault Indication Output**. LFIx is an output status indicator signal. LFIx is the logical OR of six internal conditions. LFIx is asserted LOW when any of the following conditions is true: • Received serial data rate outside expected range • Analog amplitude below expected levels • Transition density lower than expected • Receive channel disabled • ULCx is LOW • Absence of TRGCLKx±.
Device Configuration and Control Bus Signals		
WREN	LVTTL input, asynchronous, internal pull-up	**Control Write Enable**. The WREN input writes the values of the DATA[7:0] bus into the latch specified by the address location on the ADDR[3:0] bus.[3]
ADDR[3:0]	LVTTL input asynchronous, internal pull-up	**Control Addressing Bus**. The ADDR[3:0] bus is the input address bus used to configure the device. The WREN input writes the values of the DATA[7:0] bus into the latch specified by the address location on the ADDR[3:0] bus.[3] *Table 3* lists the configuration latches within the device, and the initialization value of the latches upon the assertion of RESET. *Table 4* shows how the latches are mapped in the device.

Notes:
2. 3-Level Select inputs are used for static configuration. These are ternary inputs that make use of logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). The MID level is usually implemented by not connecting the input (left floating), which allows it to self bias to the proper level.
3. See *Device Configuration and Control Interface* for detailed information on the operation of the Configuration Interface.

Pin Definitions (continued)
CYV15G0404RB Quad HOTLink II Deserializing Reclocker

Name	I/O Characteristics	Signal Description
DATA[7:0]	LVTTL input asynchronous, internal pull-up	**Control Data Bus**. The DATA[7:0] bus is the input data bus used to configure the device. The WREN input writes the values of the DATA[7:0] bus into the latch specified by address location on the ADDR[3:0] bus.[3] *Table 3* lists the configuration latches within the device, and the initialization value of the latches upon the assertion of RESET. *Table 4* shows how the latches are mapped in the device.
Internal Device Configuration Latches		
RXRATE[A..D]	Internal Latch[4]	**Receive Clock Rate Select**.
SDASEL[2..1][A..D][1:0]	Internal Latch[4]	**Signal Detect Amplitude Select**.
RXPLLPD[A..D]	Internal Latch[4]	**Receive Channel Power Control**.
RXBIST[A..D][1:0]	Internal Latch[4]	**Receive Bist Disabled**.
ROE2[A..D]	Internal Latch[4]	**Reclocker Differential Serial Output Driver 2 Enable**.
ROE1[A..D]	Internal Latch[4]	**Reclocker Differential Serial Output Driver 1 Enable**.
GLEN[11..0]	Internal Latch[4]	**Global Latch Enable**.
FGLEN[2..0]	Internal Latch[4]	**Force Global Latch Enable**.
Factory Test Modes		
SCANEN2	LVTTL input, internal pull-down	**Factory Test 2.** SCANEN2 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.
TMEN3	LVTTL input, internal pull-down	**Factory Test 3**. TMEN3 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.
Analog I/O		
ROUTA1± ROUTB1± ROUTC1± ROUTD1±	CML Differential Output	**Primary Differential Serial Data Output**. The ROUTx1± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
ROUTA2± ROUTB2± ROUTC2± ROUTD2±	CML Differential Output	**Secondary Differential Serial Data Output**. The ROUTx2± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
INA1± INB1± INC1± IND1±	Differential Input	**Primary Differential Serial Data Input**. The INx1± input accepts the serial data stream for deserialization. The INx1± serial stream is passed to the receive CDR circuit to extract the data content when INSELx = HIGH.
INA2± INB2± INC2± IND2±	Differential Input	**Secondary Differential Serial Data Input**. The INx2± input accepts the serial data stream for deserialization. The INx2± serial stream is passed to the receiver CDR circuit to extract the data content when INSELx = LOW.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**.
TDO	3-State LVTTL Output	**Test Data Out**. JTAG data output buffer. High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
$\overline{\text{TRST}}$	LVTTL Input, internal pull-up	**JTAG reset signal**. When asserted (LOW), this input asynchronously resets the JTAG test access port controller.

Note:
4. See *Device Configuration and Control Interface* for detailed information on the internal latches.

Pin Definitions (continued)

CYV15G0404RB Quad HOTLink II Deserializing Reclocker

Name	I/O Characteristics	Signal Description
Power		
V_{CC}		**+3.3V Power**.
GND		**Signal and Power Ground for all internal circuits**.

CYV15G0404RB HOTLink II Operation

The CYV15G0404RB is a highly configurable, independent clocking, quad-channel reclocking deserializer designed to support reliable transfer of large quantities of digital video data, using high-speed serial links from multiple sources to multiple destinations. This device supports four 10-bit channels.

CYV15G0404RB Receive Data Path

Serial Line Receivers

Two differential Line Receivers, INx1± and INx2±, are available on each channel for accepting serial data streams. The active Serial Line Receiver on a channel is selected using the associated INSELx input. The Serial Line Receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL family, not limited to 100K PECL) or AC-coupled to +5V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

Signal Detect/Link Fault

Each selected Line Receiver (i.e., that routed to the clock and data recovery PLL) is simultaneously monitored for

- analog amplitude above amplitude level selected by SDASELx
- transition density above the specified limit
- range controls report the received data stream inside normal frequency range (±1500 ppm[21])
- receive channel enabled
- Presence of reference clock
- ULCx is not asserted.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFIx (Link Fault Indicator) output associated with each receive channel, which changes synchronous to the receive interface clock.

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable to allow operation with highly attenuated signals, or in high-noise environments. The analog amplitude level detection is set by the SDASELx latch via device configuration interface. The SDASELx latch sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 1*. This control input affects the analog monitors for all receive channels. The Analog Signal Detect monitors are active for the Line Receiver as selected by the associated INSELx input.

Table 1. Analog Amplitude Detect Valid Signal Levels[5]

SDASEL	Typical Signal with Peak Amplitudes Above
00	Analog Signal Detector is disabled
01	140 mV p-p differential
10	280 mV p-p differential
11	420 mV p-p differential

Transition Density

The Transition Detection logic checks for the absence of transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received, the Detection logic for that channel asserts LFIx.

Range Controls

The CDR circuit includes logic to monitor the frequency of the PLL Voltage Controlled Oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been "missing."
- when the incoming data stream is outside the acceptable signaling rate range.

To perform this function, the frequency of the RXPLL VCO is periodically compared to the frequency of the TRGCLKx± input. If the VCO is running at a frequency beyond ±1500 ppm[21] as defined by the TRGCLKx± frequency, it is periodically forced to the correct frequency (as defined by TRGCLKx±, SPDSELx, and TRGRATEx) and then released in an attempt to lock to the input data stream.

The sampling and relock period of the Range Control is calculated as follows: RANGE_CONTROL_ SAMPLING_PERIOD = (RECOVERED BYTE CLOCK PERIOD) * (4096).

During the time that the Range Control forces the RXPLL VCO to track TRGCLKx±, the LFIx output is asserted LOW. After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which LFIx should be HIGH.

Note:

5. The peak amplitudes listed in this table are for typical waveforms that have generally 3–4 transitions for every ten bits. In a worse case environment the signals may have a sine-wave appearance (highest transition density with repeating 0101...). Signal peak amplitudes levels within this environment type could increase the values in the table above by approximately 100 mV.

The operating serial signaling-rate and allowable range of TRGCLK± frequencies are listed in *Table 2*.

Table 2. Operating Speed Settings

SPDSELx	TRGRATEx	TRGCLKx± Frequency (MHz)	Signaling Rate (Mbps)
LOW	1	reserved	195–400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

Receive Channel Enabled

The CYV15G0404RB contains four receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the RXPLLPDx input latch as controlled by the device configuration interface. When the RXPLLPDx latch = 0, the associated PLL and analog circuitry of the channel is disabled. Any disabled channel indicates a constant link fault condition on the LFIx output. When RXPLLPDx = 1, the associated PLL and receive channel is enabled to receive a serial stream.

Note. When a disabled receive channel is reenabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 2 ms.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate CDR block within each receive channel. The clock extraction function is performed by an integrated PLL that tracks the frequency of the transitions in the incoming bit stream and align the phase of the internal bit-rate clock to the transitions in the selected serial data stream.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) training clock from the associated TRGCLKx± input. This TRGCLKx± input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency (rather than a harmonic of the bit-rate)
- reduce PLL acquisition time
- limit unlocked frequency excursions of the CDR VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR attempts to recover a data stream from it. If the signalling rate of the recovered data stream is outside the limits set by the range control monitors, the CDR tracks TRGCLKx± instead of the data stream. Once the CDR output (RXCLK±) frequency returns back close to TRGCLKx± frequency, the CDR input is switched back to the input data stream. If no data is present at the selected line receiver, this switching behavior may result in brief RXCLK± frequency excursions from TRGCLKx±. However, the validity of the input data stream is indicated by the LFIx output. The frequency of TRGCLKx± is required to be within ±1500ppm[21] of the frequency of the clock that drives the reference clock input of the *remote* transmitter to ensure a lock to the incoming data stream. This large ppm tolerance allows the CDR PLL to reliably receive a 1.485 or 1.485/1.001 Gbps SMPTE HD-SDI data stream with a constant TRGCLK frequency.

For systems using multiple or redundant connections, the $\overline{\text{LFIx}}$ output can be used to select an alternate data stream. When an LFIx indication is detected, external logic can toggle selection of the associated INx1± and INx2± input through the associated INSELx input. When a port switch takes place, it is necessary for the receive PLL for that channel to reacquire the new serial stream.

Reclocker

Each receive channel performs a reclocker function on the incoming serial data. To do this, the Clock and Data Recovery PLL first recovers the clock from the data. The data is retimed by the recovered clock and then passed to an output register. Also, the recovered character clock from the receive PLL is passed to the reclocker output PLL which generates the bit clock that is used to clock the retimed data into the output register. This data stream is then transmitted through the differential serial outputs.

Reclocker Serial Output Drivers

The serial output interface drivers use differential Current Mode Logic (CML) drivers to provide source-matched drivers for 50Ω transmission lines. These drivers accept data from the reclocker output register in the reclocker channel. These drivers have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

Reclocker Output Channels Enabled

Each driver can be enabled or disabled separately via the device configuration interface.

When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both reclocker serial drivers for a channel are in this disabled state, the associated internal reclocker logic is also powered down. The deserialization logic and parallel outputs will remain enabled. A device reset ($\overline{\text{RESET}}$ sampled LOW) disables all output drivers.

Note. When the disabled reclocker function (i.e., both outputs disabled) is re-enabled, the data on the reclocker serial outputs may not meet all timing specifications for up to 250 µs.

Output Bus

Each receive channel presents a 10-bit data signal (and a BIST status signal when RXBISTx[1:0] = 10).

Receive BIST Operation

Each receiver channel contains an internal pattern checker that can be used to validate both device and link operation. These pattern checkers are enabled by the associated RXBISTx[1:0] latch via the device configuration interface. When enabled, a register in the associated receive channel becomes a signature pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received data stream, the associated Receiver checks each character from the

deserializer with each character generated by the LFSR and indicates compare errors and BIST status at the RXDx[1:0] and BISTSTx bits of the Output Register.

The BIST status bus {BISTSTx, RXDx[0], RXDx[1]} indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress.

The specific status reported by the BIST state machine is listed in *Table 5*. These same codes are reported on the receive status outputs.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to look for the start of the BIST sequence again.

A device reset ($\overline{\text{RESET}}$ sampled LOW) presets the BIST Enable Latches to disable BIST on all channels.

BIST Status State Machine

When a receive path is enabled to look for and compare the received data stream with the BIST pattern, the {BISTSTx, RXDx[0], RXDx[1]} bits identify the present state of the BIST compare operation.

The BIST state machine has multiple states, as shown in *Figure 2* and *Table 5*. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than 16, the state machine is forced to the WAIT_FOR_BIST state where it monitors the receive path for the first character of the next BIST sequence.

Power Control

The CYV15G0404RB supports user control of the powered up or down state of each transmit and receive channel. The receive channels are controlled by the RXPLLPDx latch via the device configuration interface. When RXPLLPDx = 0, the associated PLL and analog circuitry of the channel is disabled. The transmit channels are controlled by the OE1x and the OE2x latches via the device configuration interface. The reclocker function is controlled by the ROE1x and the ROE2x latches via the device configuration interface. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. When the reclocker serial drivers are disabled, the reclocker function will be disabled, but the deserialization logic and parallel outputs will remain enabled.

Device Reset State

When the CYV15G0404RB is reset by assertion of $\overline{\text{RESET}}$, all state machines, counters, and configuration latches in the device are initialized to a reset state. See *Table 3* for the initialize values of the configuration latches.

Following a device reset, it is necessary to enable the receive channels used for normal operation. This can be done by sequencing the appropriate values on the device configuration interface.[3]

Device Configuration and Control Interface

The CYV15G0404RB is highly configurable via the configuration interface. The configuration interface allows the device to be configured globally or allows each channel to be configured independently. *Table 3* lists the configuration latches within the device including the initialization value of the latches upon the assertion of $\overline{\text{RESET}}$. *Table 4* shows how the latches are mapped in the device. Each row in the *Table 4* maps to a 8-bit latch bank. There are 16 such write-only latch banks. When $\overline{\text{WREN}}$ = 0, the logic value in the DATA[7:0] is latched to the latch bank specified by the values in ADDR[3:0]. The second column of *Table 4* specifies the channels associated with the corresponding latch bank. For example, the first three latch banks (0,1 and 2) consist of configuration bits for channel A. The latch banks 12, 13 and 14 consist of Global configuration bits and the last latch bank (15) is the Mask latch bank that can be configured to perform bit-by-bit configuration.

Global Enable Function

The global enable function, controlled by the GLENx bits, is a feature that can be used to reduce the number of write operations needed to setup the latch banks. This function is beneficial in systems that use a common configuration in multiple channels. The GLENx bit is present in bit 0 of latch banks 0 through 11 only. Its default value (1) enables the global update of the latch bank's contents. Setting the GLENx bit to 0 disables this functionality.

Latch Banks 12, 13, and 14 are used to load values in the related latch banks in a global manner. A write operation to latch bank 12 could do a global write to latch banks 0, 3, 6, and 9 depending on the value of GLENx in these latch banks; latch bank 13 could do a global write to latch banks 1, 4, 7 and 10; and latch banks 14 could do a global write to latch banks 2, 5, 8 and 11. The GLENx bit cannot be modified by a global write operation.

Force Global Enable Function

FGLENx forces the global update of the target latch banks, but does not change the contents of the GLENx bits. If FGLENx = 1 for the associated global channel, FGLENx forces the global update of the target latch banks.

Mask Function

An additional latch bank (15) is used as a global mask vector to control the update of the configuration latch banks on a bit-by-bit basis. A logic 1 in a bit location allows for the update of that same location of the target latch bank(s), whereas a logic 0 disables it. The reset value of this latch bank is FFh, thereby making its use optional by default. The mask latch bank is not maskable. The FGLEN functionality is not affected by the bit 0 value of the mask latch bank.

Latch Types

There are two types of latch banks: static (S) and dynamic (D). Each channel is configured by 2 static and 1 dynamic latch banks. The S type contain those settings that normally do not change for a given application, whereas the D type controls the settings that could change during the application's lifetime. The first and second rows of each channel (address numbers 0, 1, 3, 4, 6, 7, 9, and 10) are the static control latches. The third row of latches for each channel (address numbers 2, 5,

8, and 11) are the dynamic control latches that are associated with enabling dynamic functions within the device.

Latch Bank 14 is also useful for those users that do not need the latch-based programmable feature of the device. This latch bank could be used in those applications that do not need to modify the default value of the static latch banks, and that can afford a global (i.e., not independent) control of the dynamic signals. In this case, this feature becomes available when ADDR[3:0] is left unchanged with a value of “1110” and WREN is left asserted. The signals present in DATA[7:0] effectively become global control pins, and for the latch banks 2, 5, 8 and 11.

Static Latch Values

There are some latches in the table that have a static value (ie. 1, 0, or X). The latches that have a ‘1’ or ‘0’ must be configured with their corresponding value each time that their associated latch bank is configured. The latches that have an ‘X’ are don’t cares and can be configured with any value

Table 3. Device Configuration and Control Latch Descriptions

Name	Signal Description
RXRATEA RXRATEB RXRATEC RXRATED	**Receive Clock Rate Select**. The initialization value of the RXRATEx latch = 1. RXRATEx is used to select the rate of the RXCLKx± clock output. When RXRATEx = 1, the RXCLKx± clock outputs are complementary clocks that follow the recovered clock operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–. When RXRATEx = 0, the RXCLKx± clock outputs are complementary clocks that follow the recovered clock operating at the character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–.
SDASEL1A[1:0] SDASEL1B[1:0] SDASEL1C[1:0] SDASEL1D[1:0]	**Primary Serial Data Input Signal Detector Amplitude Select**. The initialization value of the SDASEL1x[1:0] latch = 10. SDASEL1x[1:0] selects the trip point for the detection of a valid signal for the INx1± Primary Differential Serial Data Inputs. When SDASEL1x[1:0] = 00, the Analog Signal Detector is disabled. When SDASEL1x[1:0] = 01, the typical p-p differential voltage threshold level is 140 mV. When SDASEL1x[1:0] = 10, the typical p-p differential voltage threshold level is 280 mV. When SDASEL1x[1:0] = 11, the typical p-p differential voltage threshold level is 420 mV.
SDASEL2A[1:0] SDASEL2B[1:0] SDASEL2C[1:0] SDASEL2D[1:0]	**Secondary Serial Data Input Signal Detector Amplitude Select**. The initialization value of the SDASEL2x[1:0] latch = 10. SDASEL2x[1:0] selects the trip point for the detection of a valid signal for the INx2± Secondary Differential Serial Data Inputs. When SDASEL2x[1:0] = 00, the Analog Signal Detector is disabled When SDASEL2x[1:0] = 01, the typical p-p differential voltage threshold level is 140 mV. When SDASEL2x[1:0] = 10, the typical p-p differential voltage threshold level is 280 mV. When SDASEL2x[1:0] = 11, the typical p-p differential voltage threshold level is 420 mV.
TRGRATEA TRGRATEB TRGRATEC TRGRATED	**Training Clock Rate Select**. The initialization value of the TRGRATEx latch = 0. TRGRATEx is used to select the clock multiplier for the training clock input to the associated CDR PLL. When TRGRATEx = 0, the associated TRGCLKx± input is not multiplied before it is passed to the CDR PLL. When TRGRATEx = 1, the TRGCLKx± input is multiplied by 2 before it is passed to the CDR PLL. TRGRATEx = 1 and SPDSELx = LOW is an invalid state and this combination is reserved.
RXPLLPDA RXPLLPDB RXPLLPDC RXPLLPDD	**Receive Channel Enable**. The initialization value of the RXPLLPDx latch = 0. RXPLLPDx selects if the associated receive channel is enabled or powered-down. When RXPLLPDx = 0, the associated receive PLL and analog circuitry are powered-down. When RXPLLPDx = 1, the associated receive PLL and analog circuitry are enabled.
RXBISTA[1:0] RXBISTB[1:0] RXBISTC[1:0] RXBISTD[1:0]	**Receive Bist Disable / SMPTE Receive Enable**. The initialization value of the RXBISTx[1:0] latch = 11. For SMPTE data reception, RXBISTx[1:0] should not remain in this initialization state (11). RXBISTx[1:0] selects if receive BIST is disabled or enabled and sets the associated channel for SMPTE data reception. When RXBISTx[1:0] = 01, the receiver BIST function is disabled and the associated channel is set to receive SMPTE data. When RXBISTx[1:0] = 10, the receive BIST function is enabled and the associated channel is set to receive BIST data. RXBISTx[1:0] = 00 and RXBISTx[1:0] = 11 are invalid states.
ROE2A ROE2B ROE2C ROE2D	**Reclocker Secondary Differential Serial Data Output Driver Enable**. The initialization value of the ROE2x latch = 0. ROE2x selects if the ROUT2± secondary differential output drivers are enabled or disabled. When ROE2x = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When ROE2x = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.

Table 3. Device Configuration and Control Latch Descriptions (continued)

Name	Signal Description
ROE1A ROE1B ROE1C ROE1D	**Reclocker Primary Differential Serial Data Output Driver Enable**. The initialization value of the ROE1x latch = 0. ROE1x selects if the ROUT1± primary differential output drivers are enabled or disabled. When ROE1x = 1, the associated serial data output driver is enabled allowing data to be transmitted from the transmit shifter. When ROE1x = 0, the associated serial data output driver is disabled. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset (RESET sampled LOW) disables all output drivers.
GLEN[11..0]	**Global Enable**. The initialization value of the GLENx latch = 1. The GLENx is used to reconfigure several channels simultaneously in applications where several channels may have the same configuration. When GLENx = 1 for a given address, that address is allowed to participate in a global configuration. When GLENx = 0 for a given address, that address is disabled from participating in a global configuration.
FGLEN[2..0]	**Force Global Enable**. The initialization value of the FGLENx latch is NA. The FGLENx latch forces a GLobal ENable no matter what the setting is on the GLENx latch. If FGLENx = 1 for the associated Global channel, FGLEN forces the global update of the target latch banks.

Device Configuration Strategy

The following is a series of ordered events needed to load the configuration latches on a per channel basis:

1. Pulse $\overline{\text{RESET}}$ Low after device power-up. This operation resets all four channels.
2. Set the static latch banks for the target channel. May be performed using a global operation, if the application permits it. [Optional step if the default settings match the desired configuration.]
3. Set the dynamic bank of latches for the target channel. Enable the Receive PLLs and set each channel for SMPTE data reception (RXBISTx[1:0] = 01) or BIST data reception (RXBISTx[1:0] = 10). May be performed using a global operation, if the application permits it. [Required step.]

Table 4. Device Control Latch Configuration Table

ADDR	Channel	Type	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	Reset Value
0 (0000b)	A	S	1	0	X	X	0	0	RXRATEA	GLEN0	10111111
1 (0001b)	A	S	SDASEL2A[1]	SDASEL2A[0]	SDASEL1A[1]	SDASEL1A[0]	X	X	TRGRATEA	GLEN1	10101101
2 (0010b)	A	D	RXBISTA[1]	RXPLLPDA	RXBISTA[0]	X	ROE2A	ROE1A	X	GLEN2	10110011
3 (0011b)	B	S	1	0	X	X	0	0	RXRATEB	GLEN3	10111111
4 (0100b)	B	S	SDASEL2B[1]	SDASEL2B[0]	SDASEL1B[1]	SDASEL1B[0]	X	X	TRGRATEB	GLEN4	10101101
5 (0101b)	B	D	RXBISTB[1]	RXPLLPDB	RXBISTB[0]	X	ROE2B	ROE1B	X	GLEN5	10110011
6 (0110b)	C	S	1	0	X	X	0	0	RXRATEC	GLEN6	10111111
7 (0111b)	C	S	SDASEL2C[1]	SDASEL2C[0]	SDASEL1C[1]	SDASEL1C[0]	X	X	TRGRATEC	GLEN7	10101101
8 (1000b)	C	D	RXBISTC[1]	RXPLLPDC	RXBISTC[0]	X	ROE2C	ROE1C	X	GLEN8	10110011
9 (1001b)	D	S	1	0	X	X	0	0	RXRATED	GLEN9	10111111
10 (1010b)	D	S	SDASEL2D[1]	SDASEL2D[0]	SDASEL1D[1]	SDASEL1D[0]	X	X	TRGRATED	GLEN10	10101101
11 (1011b)	D	D	RXBISTD[1]	RXPLLPDD	RXBISTD[0]	X	ROE2D	ROE1D	X	GLEN11	10110011
12 (1100b)	GLOBAL	S	1	0	X	X	0	0	RXRATEGL	FGLEN0	N/A
13 (1101b)	GLOBAL	S	SDASEL2GL[1]	SDASEL2GL[0]	SDASEL1GL[1]	SDASEL1GL[0]	X	X	TRGRATEGL	FGLEN1	N/A
14 (1110b)	GLOBAL	D	RXBISTGL[1]	RXPLLPDGL	RXBISTGL[0]	X	ROE2GL	ROE1GL	X	FGLEN2	N/A
15 (1111b)	MASK	D	D7	D6	D5	D4	D3	D2	D1	D0	11111111

JTAG Support

The CYV15G0404RB contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, boundary scan, and bypass are supported. This capability is present only on the LVTTL inputs and outputs and the TRGCLKx± clock input. The high-speed serial inputs and outputs are not part of the JTAG test chain.

3-Level Select Inputs

Each 3-Level select inputs reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11 respectively

JTAG ID

The JTAG device ID for the CYV15G0404RB is ‘0C811069’x.

Table 5. Receive BIST Status Bits

{BISTSTx, RXDx[0], RXDx[1]}	Description
	Receive BIST Status (Receive BIST = Enabled)
000, 001	**BIST Data Compare**. Character compared correctly.
010	**BIST Last Good**. Last Character of BIST sequence detected and valid.
011	Reserved.
100	**BIST Last Bad**. Last Character of BIST sequence detected invalid.
101	**BIST Start**. Receive BIST is enabled on this channel, but character compares have not yet commenced. This also indicates a PLL Out of Lock condition.
110	**BIST Error**. While comparing characters, a mismatch was found in one or more of the character bits.
111	**BIST Wait**. The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

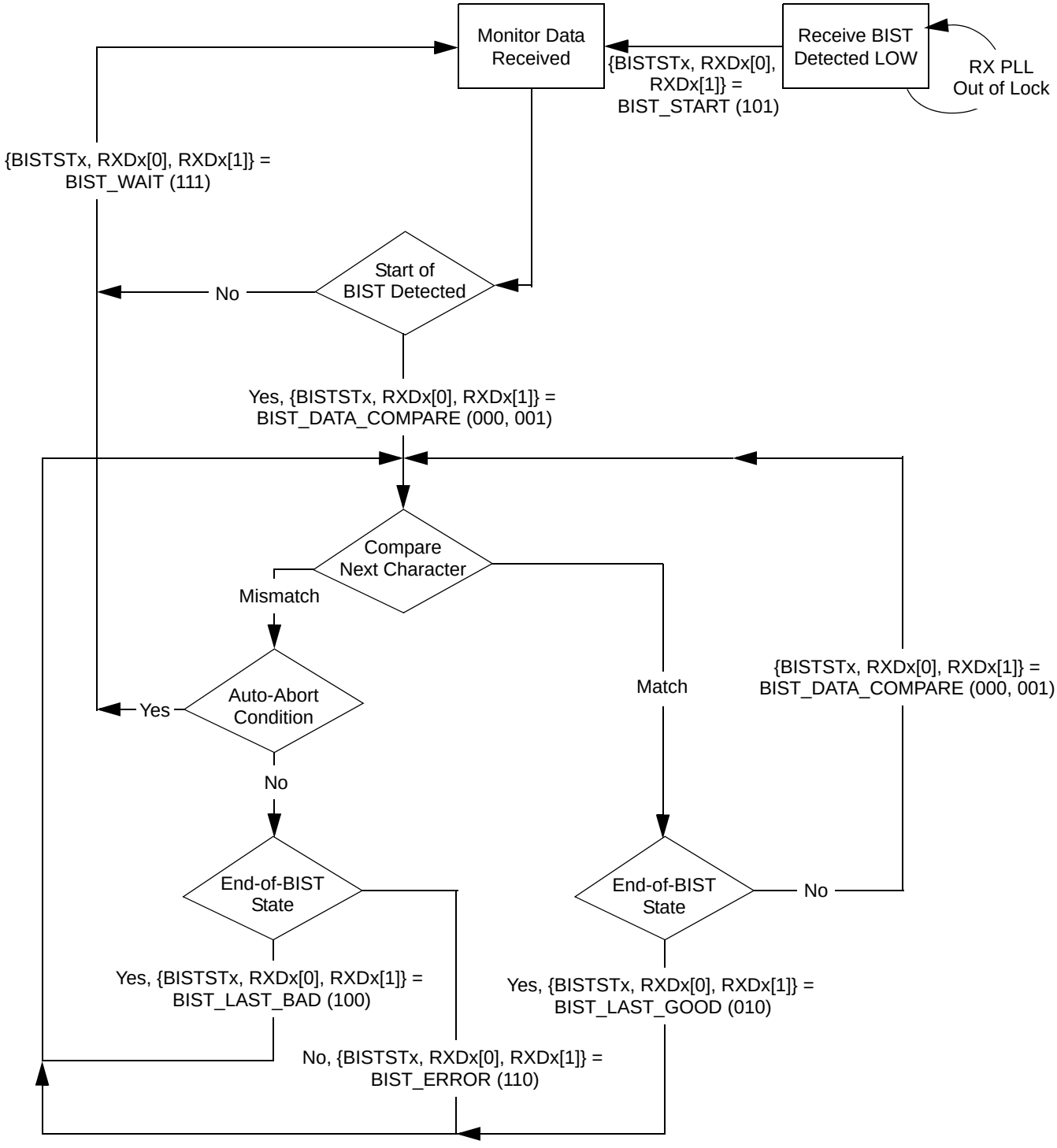


Figure 2. Receive BIST State Machine

Maximum Ratings

Above which the useful life may be impaired. User guidelines only, not tested

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.8V

DC Voltage Applied to LVTTL Outputs in High-Z State .....–0.5V to V_{CC} + 0.5V

Output Current into LVTTL Outputs (LOW).....60 mA

DC Input Voltage.....–0.5V to V_{CC} + 0.5V

Static Discharge Voltage.....> 2000 V (per MIL-STD-883, Method 3015)

Latch-up Current.....> 200 mA

Power-up Requirements

The CYV15G0404RB requires one power supply. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ±5%

CYV15G0404RB DC Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL-compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = – 4 mA, V_{CC} = Min.	2.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min.		0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[6], V_{CC} = 3.3V	–20	–100	mA
I_{OZL}	High-Z Output Leakage Current	V_{OUT} = 0V, V_{CC}	–20	20	µA
LVTTL-compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	TRGCLKx Input, V_{IN} = V_{CC}		1.5	mA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	TRGCLKx Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: TRGCLKx±					
V_{DIFF}[7]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW voltage		0.0	V_{CC}/2	V
V_{COMREF}[8]	Common Mode Range		1.0	V_{CC} – 1.2V	V
3-Level Inputs					
V_{IHH}	Three-Level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-Level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID current	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW current	V_{IN} = GND		–200	µA
Differential CML Serial Outputs: ROUTA1±, ROUTA2±, ROUTB1±, ROUTB2±, ROUTC1±, ROUTC2±, ROUTD1±, ROUTD2±					
V_{OHC}	Output HIGH Voltage (V_{CC} Referenced)	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
		150Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
V_{OLC}	Output LOW Voltage (V_{CC} Referenced)	100Ω differential load	V_{CC} – 1.4	V_{CC} – 0.7	V
		150Ω differential load	V_{CC} – 1.4	V_{CC} – 0.7	V

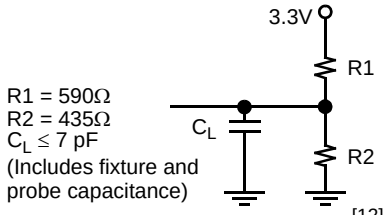
Notes:

6. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
7. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
8. The common mode range defines the allowable range of TRGCLKx+ and TRGCLKx– when TRGCLKx+ = TRGCLKx–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

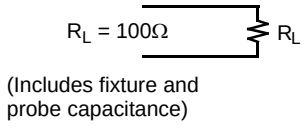
CYV15G0404RB DC Electrical Characteristics (continued)

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load		450	900	mV
		150Ω differential load		560	1000	mV
Differential Serial Line Receiver Inputs: INA1±, INA2±, INB1±, INB2±, INC1±, INC2±, IND1±, IND2±						
V_{DIFFs}[7]	Input Differential Voltage |(IN+) – (IN–)|			100	1200	mV
V_{IHE}	Highest Input HIGH Voltage				V_{CC}	V
V_{ILE}	Lowest Input LOW Voltage			V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHE}$ Max.			1350	µA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILE}$ Min.		–700		µA
VI_{COM}[9]	Common Mode input range	((V_{CC} – 2.0V)+0.5)min, (V_{CC} – 0.5V) max.		+1.25	+3.1	V
Power Supply				**Typ.**	**Max.**	
I_{CC}[10,11]	Max Power Supply Current	TRGCLKx= MAX	Commercial	910	1270	mA
			Industrial		1320	mA
I_{CC}[10,11]	Typical Power Supply Current	TRGCLKx= 125 MHz	Commercial	900	1270	mA
			Industrial		1320	mA

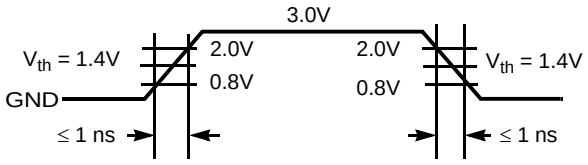
AC Test Loads and Waveforms



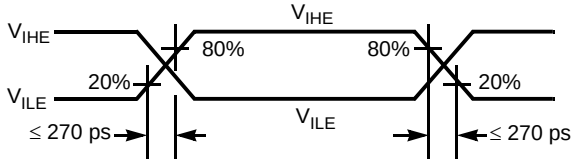
(a) LVTTL Output Test Load[12]



(b) CML Output Test Load[12]



(c) LVTTL Input Test Waveform[13]



(d) CML/LVPECL Input Test Waveform

CYV15G0404RB AC Electrical Characteristics

Parameter	Description	Min.	Max	Unit
CYV15G0404RB Receiver LVTTL Switching Characteristics Over the Operating Range				
f_{RS}	RXCLKx± Clock Output Frequency	9.75	150	MHz
t_{RXCLKP}	RXCLKx± Period = $1/f_{RS}$	6.66	102.56	ns
t_{RXCLKD}	RXCLKx± Duty Cycle Centered at 50% (Full Rate and Half Rate)	–1.0	+1.0	ns
t_{RXCLKR}[14]	RXCLKx± Rise Time	0.3	1.2	ns
t_{RXCLKF}[14]	RXCLKx± Fall Time	0.3	1.2	ns

Notes:

9. The common mode range defines the allowable range of INPUT+ and INPUT– when INPUT+ = INPUT–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.
10. Maximum I_{CC} is measured with V_{CC} = MAX, T_A = 25°C, with all channels and Serial Line Drivers enabled, sending a continuous alternating 01 pattern, and outputs unloaded.
11. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3V, T_A = 25°C, with all channels enabled and one Serial Line Driver per transmit channel sending a continuous alternating 01 pattern. The redundant outputs on each channel are powered down and the parallel outputs are unloaded.
12. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
13. The LVTTL switching threshold is 1.4V. All timing references are made relative to where the signal edges cross the threshold voltage.
14. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.

CYV15G0404RB AC Electrical Characteristics (continued)

Parameter	Description	Min.	Max	Unit
t_{RXDv-}[18]	Status and Data Valid Time to RXCLKx± (RXRATEx = 0) (Full Rate)	5UI–2.0[19]		ns
	Status and Data Valid Time to RXCLKx± (RXRATEx = 1) (Half Rate)	5UI–1.3[19]		ns
t_{RXDv+}[18]	Status and Data Valid Time to RXCLKx± (RXRATEx = 0)	5UI–1.8[19]		ns
	Status and Data Valid Time to RXCLKx± (RXRATEx = 1)	5UI–2.6[19]		ns
f_{ROS}	RECLKOx Clock Frequency	19.5	150	MHz
t_{RECLKO}	RECLKOx Period=1/f_{ROS}	6.66	51.28	ns
$t_{RECLKOD}$	RECLKOx Duty Cycle centered at 60% HIGH time	–1.9	0	ns
CYV15G0404RB TRGCLKx Switching Characteristics Over the Operating Range				
f_{TRG}	TRGCLKx Clock Frequency	19.5	150	MHz
TRGCLK	TRGCLKx Period = 1/f_{REF}	6.6	51.28	ns
t_{TRGH}	TRGCLKx HIGH Time (TRGRATEx = 1)(Half Rate)	5.9		ns
	TRGCLKx HIGH Time (TRGRATEx = 0)(Full Rate)	2.9[14]		ns
t_{TRGL}	TRGCLKx LOW Time (TRGRATEx = 1)(Half Rate)	5.9		ns
	TRGCLKx LOW Time (TRGRATEx = 0)(Full Rate)	2.9[14]		ns
t_{TRGD}[20]	TRGCLKx Duty Cycle	30	70	%
t_{TRGR}[14, 15, 16, 17]	TRGCLKx Rise Time (20%–80%)		2	ns
t_{TRGF}[14, 15, 16, 17]	TRGCLKx Fall Time (20%–80%)		2	ns
t_{TRGRX}[21]	TRGCLKx Frequency Referenced to Received Clock Frequency	–0.15	+0.15	%
CYV15G0404RB Bus Configuration Write Timing Characteristics Over the Operating Range				
t_{DATAH}	Bus Configuration Data Hold	0		ns
t_{DATAS}	Bus Configuration Data Setup	10		ns
t_{WRENP}	Bus Configuration WREN Pulse Width	10		ns
CYV15G0404RB JTAG Test Clock Characteristics Over the Operating Range				
f_{TCLK}	JTAG Test Clock Frequency		20	MHz
t_{TCLK}	JTAG Test Clock Period	50		ns
CYV15G0404RB Device RESET Characteristics Over the Operating Range				
t_{RST}	Device RESET Pulse Width	30		ns

CYV15G0404RB Reclocker Serial Output Characteristics Over the Operating Range

Parameter	Description	Condition	Min.	Max.	Unit
t_B	Bit Time		5128	660	ps
t_{RISE}[14]	CML Output Rise Time 20–80% (CML Test Load)	SPDSELx = HIGH	50	270	ps
		SPDSELx = MID	100	500	ps
		SPDSELx =LOW	180	1000	ps
t_{FALL}[14]	CML Output Fall Time 80–20% (CML Test Load)	SPDSELx = HIGH	50	270	ps
		SPDSELx = MID	100	500	ps
		SPDSELx =LOW	180	1000	ps

Notes:
15. The ratio of rise time to falling time must not vary by greater than 2:1.
16. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
17. All transmit AC timing parameters measured with 1ns typical rise time and fall time.
18. Parallel data output specifications are only valid if all outputs are loaded with similar DC and AC loads.
19. Receiver UI (Unit Interval) is calculated as 1/(f_{TRG} * 20) (when TRGRATEx = 1) or 1/(f_{TRG} * 10) (when TRGRATEx = 0). In an operating link this is equivalent to t_B.
20. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the TRGCLKx± duty cycle cannot be as large as 30%–70%.
21. TRGCLKx± has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. TRGCLKx± must be within ±1500 PPM (±0.15%) of the transmitter PLL reference (REFCLKx±) frequency. Although transmitting to a HOTLink II receiver channel necessitates the frequency difference between the transmitter and receiver reference clocks to be within ±1500-PPM, the stability of the crystal needs to be within the limits specified by the appropriate standard when transmitting to a remote receiver that is compliant to that standard.

PLL Characteristics

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
CYV15G0404RB Reclocker Output PLL Characteristics						
$t_{JRGENSD}$[14, 22]	Reclocker Jitter Generation - SD Data Rate	TRGCLKx = 27 MHz		133		ps
$t_{JRGENHD}$[14, 22]	Reclocker Jitter Generation - HD Data Rate	TRGCLKx = 148.5 MHz		107		ps
CYV15G0404RB Receive PLL Characteristics Over the Operating Range						
t_{RXLOCK}	Receive PLL lock to input data stream (cold start)				376k	UI
	Receive PLL lock to input data stream				376k	UI
$t_{RXUNLOCK}$	Receive PLL Unlock Rate				46	UI

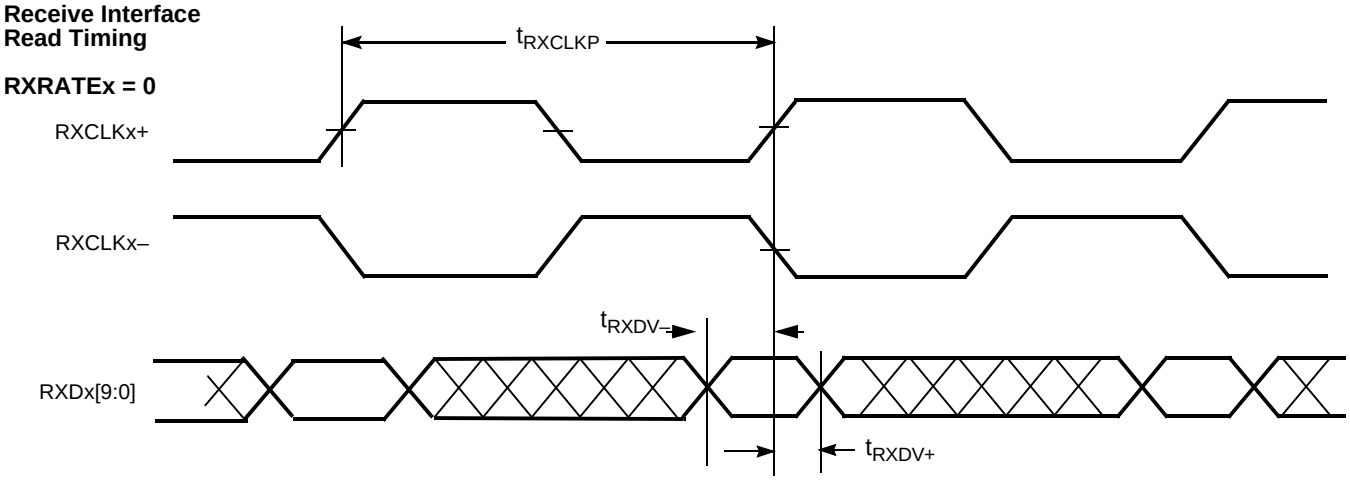
Capacitance[14]

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	7	pF
C_{INPECL}	PECL input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	4	pF

Switching Waveforms for the CYV15G0404RB HOTLink II Receiver

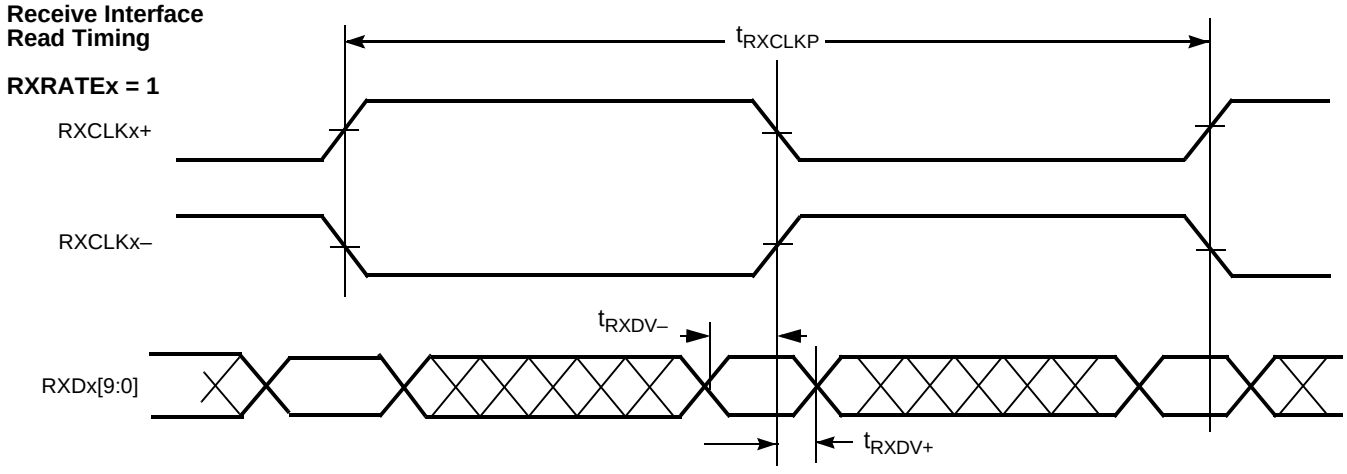
Receive Interface Read Timing

RXRATEx = 0



Receive Interface Read Timing

RXRATEx = 1



Notes:

22. Receiver input stream is BIST data from the transmit channel. This data is reclocked and output to a wide-bandwidth digital sampling oscilloscope. The measurement was recorded after 10,000 histogram hits, time referenced to REFCLKx± of the transmit channel.

CYV15G0404RB HOTLink II Bus Configuration Switching Waveforms

Bus Configuration Write Timing

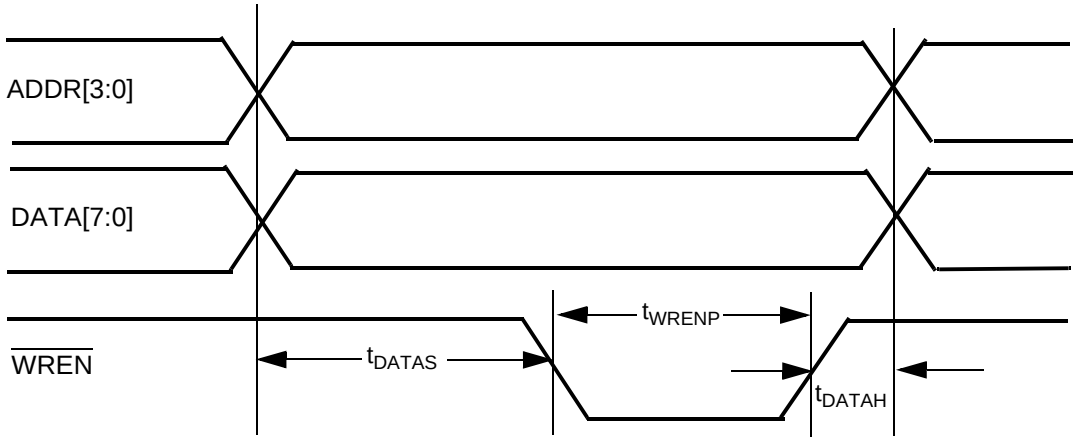


Table 6. Package Coordinate Signal Allocation

Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type
A01	INC1–	CML IN	C07	ULCC	LVTTL IN PU	F17	VCC	POWER
A02	ROUTC1–	CML OUT	C08	GND	GROUND	F18	RXDB[0]	LVTTL OUT
A03	INC2–	CML IN	C09	DATA[7]	LVTTL IN PU	F19	RECLKOB	LVTTL OUT
A04	ROUTC2–	CML OUT	C10	DATA[5]	LVTTL IN PU	F20	RXDB[1]	LVTTL OUT
A05	VCC	POWER	C11	DATA[3]	LVTTL IN PU	G01	GND	GROUND
A06	IND1–	CML IN	C12	DATA[1]	LVTTL IN PU	G02	WREN	LVTTL IN PU
A07	ROUTD1–	CML OUT	C13	GND	GROUND	G03	GND	GROUND
A08	GND	GROUND	C14	VCC	POWER	G04	GND	GROUND
A09	IND2–	CML IN	C15	SPDSELD	3-LEVEL SEL	G17	SPDSELB	3-LEVEL SEL
A10	ROUTD2–	CML OUT	C16	VCC	POWER	G18	NC	NO CONNECT
A11	INA1–	CML IN	C17	LDTDEN	LVTTL IN PU	G19	SPDSELA	3-LEVEL SEL
A12	ROUTA1–	CML OUT	C18	TRST	LVTTL IN PU	G20	RXDB[3]	LVTTL OUT
A13	GND	GROUND	C19	GND	GROUND	H01	GND	GROUND
A14	INA2–	CML IN	C20	TDO	LVTTL 3-S OUT	H02	GND	GROUND
A15	ROUTA2–	CML OUT	D01	TCLK	LVTTL IN PD	H03	GND	GROUND
A16	VCC	POWER	D02	RESET	LVTTL IN PU	H04	GND	GROUND
A17	INB1–	CML IN	D03	INSELD	LVTTL IN	H17	GND	GROUND
A18	ROUTB1–	CML OUT	D04	INSELA	LVTTL IN	H18	GND	GROUND
A19	INB2–	CML IN	D05	VCC	POWER	H19	GND	GROUND
A20	ROUTB2–	CML OUT	D06	ULCA	LVTTL IN PU	H20	GND	GROUND
B01	INC1+	CML IN	D07	SPDSELC	3-LEVEL SEL	J01	GND	GROUND
B02	ROUTC1+	CML OUT	D08	GND	GROUND	J02	GND	GROUND
B03	INC2+	CML IN	D09	DATA[6]	LVTTL IN PU	J03	GND	GROUND
B04	ROUTC2+	CML OUT	D10	DATA[4]	LVTTL IN PU	J04	GND	GROUND
B05	VCC	POWER	D11	DATA[2]	LVTTL IN PU	J17	BISTSTB	LVTTL OUT
B06	IND1+	CML IN	D12	DATA[0]	LVTTL IN PU	J18	RXDB[2]	LVTTL OUT
B07	ROUTD1+	CML OUT	D13	GND	GROUND	J19	RXDB[7]	LVTTL OUT
B08	GND	GROUND	D14	GND	GROUND	J20	RXDB[4]	LVTTL OUT
B09	IND2+	CML IN	D15	ULCB	LVTTL IN PU	K01	RXDC[4]	LVTTL OUT
B10	ROUTD2+	CML OUT	D16	VCC	POWER	K02	TRGCLKC–	PECL IN
B11	INA1+	CML IN	D17	NC	NO CONNECT	K03	GND	GROUND
B12	ROUTA1+	CML OUT	D18	VCC	POWER	K04	GND	GROUND
B13	GND	GROUND	D19	SCANEN2	LVTTL IN PD	K17	RXDB[5]	LVTTL OUT
B14	INA2+	CML IN	D20	TMEN3	LVTTL IN PD	K18	RXDB[6]	LVTTL OUT
B15	ROUTA2+	CML OUT	E01	VCC	POWER	K19	RXDB[9]	LVTTL OUT
B16	VCC	POWER	E02	VCC	POWER	K20	LFIB	LVTTL OUT
B17	INB1+	CML IN	E03	VCC	POWER	L01	RXDC[5]	LVTTL OUT
B18	ROUTB1+	CML OUT	E04	VCC	POWER	L02	TRGCLKC+	PECL IN
B19	INB2+	CML IN	E17	VCC	POWER	L03	LFIC	LVTTL OUT
B20	ROUTB2+	CML OUT	E18	VCC	POWER	L04	GND	GROUND
C01	TDI	LVTTL IN PU	E19	VCC	POWER	L17	RXDB[8]	LVTTL OUT
C02	TMS	LVTTL IN PU	E20	VCC	POWER	L18	RXCLKB+	LVTTL OUT
C03	INSELC	LVTTL IN	F01	RXDC[8]	LVTTL OUT	L19	RXCLKB–	LVTTL OUT

Table 6. Package Coordinate Signal Allocation (continued)

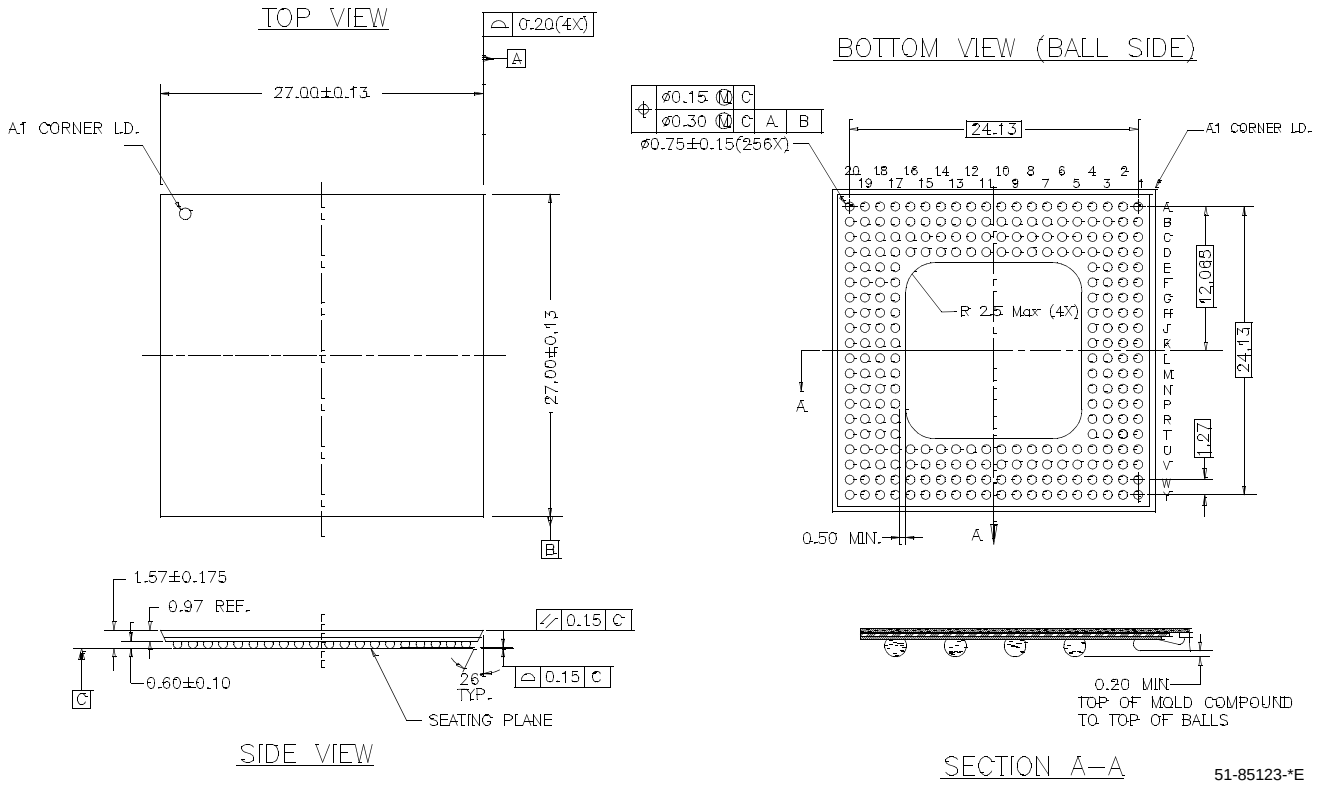
Ball ID	Signal Name	Signal Type
C04	INSELB	LVTTL IN
C05	VCC	POWER
C06	$\overline{\text{ULCD}}$	LVTTL IN PU
M03	VCC	POWER
M04	REPDOC	LVTTL OUT
M17	TRGCLKB+	PECL IN
M18	TRGCLKB–	PECL IN
M19	REPDOB	LVTTL OUT
M20	GND	GROUND
N01	GND	GROUND
N02	GND	GROUND
N03	GND	GROUND
N04	GND	GROUND
N17	GND	GROUND
N18	GND	GROUND
N19	GND	GROUND
N20	GND	GROUND
P01	RXDC[3]	LVTTL OUT
P02	RXDC[2]	LVTTL OUT
P03	RXDC[1]	LVTTL OUT
P04	RXDC[0]	LVTTL OUT
P17	GND	GROUND
P18	GND	GROUND
P19	GND	GROUND
P20	GND	GROUND
R01	BISTSTC	LVTTL OUT
R02	RECLKOC	LVTTL OUT
R03	RXCLKC+	LVTTL OUT
R04	RXCLKC–	LVTTL OUT
R17	VCC	POWER
R18	VCC	POWER
R19	VCC	POWER
R20	VCC	POWER
T01	VCC	POWER
T02	VCC	POWER
T03	VCC	POWER
T04	VCC	POWER
T17	VCC	POWER
T18	VCC	POWER
T19	VCC	POWER
T20	VCC	POWER
U01	VCC	POWER
U02	VCC	POWER
F02	RXDC[9]	LVTTL OUT
F03	VCC	POWER
F04	VCC	POWER
U03	VCC	POWER
U04	VCC	POWER
U05	VCC	POWER
U06	RXDD[4]	LVTTL OUT
U07	RXDD[3]	LVTTL OUT
U08	GND	GROUND
U09	GND	GROUND
U10	ADDR [0]	LVTTL IN PU
U11	TRGCLKD–	PECL IN
U12	GND	GROUND
U13	GND	GROUND
U14	GND	GROUND
U15	VCC	POWER
U16	VCC	POWER
U17	RXDA[4]	LVTTL OUT
U18	VCC	POWER
U19	BISTSTA	LVTTL OUT
U20	RXDA[0]	LVTTL OUT
V01	VCC	POWER
V02	VCC	POWER
V03	VCC	POWER
V04	RXDD[8]	LVTTL OUT
V05	VCC	POWER
V06	RXDD[5]	LVTTL OUT
V07	RXDD[1]	LVTTL OUT
V08	GND	GROUND
V09	BISTSTD	LVTTL OUT
V10	ADDR [2]	LVTTL IN PU
V11	TRGCLKD+	PECL IN
V12	RECLKOA	LVTTL OUT
V13	GND	GROUND
V14	GND	GROUND
V15	VCC	POWER
V16	VCC	POWER
V17	RXDA[9]	LVTTL OUT
V18	RXDA[5]	LVTTL OUT
V19	RXDA[2]	LVTTL OUT
V20	RXDA[1]	LVTTL OUT
W01	VCC	POWER
W02	VCC	POWER
L20	GND	GROUND
M01	RXDC[6]	LVTTL OUT
M02	RXDC[7]	LVTTL OUT
W03	$\overline{\text{LFID}}$	LVTTL OUT
W04	RXCLKD–	LVTTL OUT
W05	VCC	POWER
W06	RXDD[6]	LVTTL OUT
W07	RXDD[0]	LVTTL OUT
W08	GND	GROUND
W09	ADDR [3]	LVTTL IN PU
W10	ADDR [1]	LVTTL IN PU
W11	RXCLKA+	LVTTL OUT
W12	REPDOA	LVTTL OUT
W13	GND	GROUND
W14	GND	GROUND
W15	VCC	POWER
W16	VCC	POWER
W17	$\overline{\text{LFIA}}$	LVTTL OUT
W18	TRGCLKA+	PECL IN
W19	RXDA[6]	LVTTL OUT
W20	RXDA[3]	LVTTL OUT
Y01	VCC	POWER
Y02	VCC	POWER
Y03	RXDD[9]	LVTTL OUT
Y04	RXCLKD+	LVTTL OUT
Y05	VCC	POWER
Y06	RXDD[7]	LVTTL OUT
Y07	RXDD[2]	LVTTL OUT
Y08	GND	GROUND
Y09	RECLKOD	LVTTL OUT
Y10	NC	NO CONNECT
Y11	GND	GROUND
Y12	RXCLKA–	LVTTL OUT
Y13	GND	GROUND
Y14	GND	GROUND
Y15	VCC	POWER
Y16	VCC	POWER
Y17	REPDOD	LVTTL OUT
Y18	TRGCLKA–	PECL IN
Y19	RXDA[8]	LVTTL OUT
Y20	RXDA[7]	LVTTL OUT

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYV15G0404RB-BGC	BL256	256-Ball Thermally Enhanced Ball Grid Array	Commercial
Standard	CYV15G0404RB-BGXC	BL256	Pb-Free 256-Ball Thermally Enhanced Ball Grid Array	Commercial

Package Diagram

256-Lead L2 Ball Grid Array (27 x 27 x 1.57 mm) BL256



Document History Page

Document Title: CYV15G0404RB Independent Clock Quad HOTLink II™ Deserializing Reclocker Document Number: 38-02102				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	246850	See ECN	FRE	New Data Sheet
*A	338721	See ECN	SUA	Added Pb-Free package option availability
*B	384307	See ECN	AGT	Revised setup and hold times (t_{RXDv-}, t_{RXDv+})