FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12561-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89202 Series

MB89202/F202/V201

■ DESCRIPTION

The MB89202 series is a line of single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such, timers, a serial interface, an A/D converter and an external interrupt.

■ FEATURES

- F²MC-8L family CPU core
- Maximum memory space : 64 Kbytes
- Minimum execution time : 0.32 µs/12.5 MHz
- Interrupt processing time : 2.88 µs/12.5 MHz
- I/O ports : Max 26 channels
- 21-bit time-base timer
- 8-bit PWM timer
- 8/16-bit capture timer/counter
- 10-bit A/D converter : 8 channels
- UART
- 8-bit serial I/O
- External interrupt 1 : 3 channels
- External interrupt 2 : 8 channels
- Wild Register : 2 bytes

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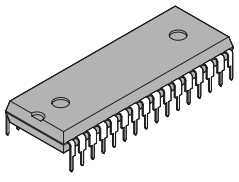
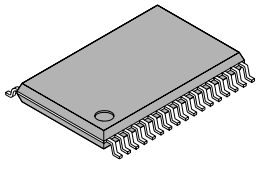
■ PACKAGES

32-pin plastic SH-DIP



(DIP-32P-M06)

34-pin plastic SSOP



(FPT-34P-M03)

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- MB89F202 : Flash (at least 10,000 program / erase cycles) with read protection
- Low-power consumption modes (sleep mode, and stop mode)
- SH-DIP-32, SSOP-34 package
- CMOS Technology

■ PRODUCT LINEUP

Parameter \ Part number	MB89202	MB89F202	MB89V201
Classification	Mask ROM product	Flash memory product (read protection)	Evaluation product (for development)
ROM size	16 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal flash)	32K x 8 bits (external EPROM)
RAM size	512 × 8 bits		
CPU functions	Number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.32 µs to 5.1 µs (12.5 MHz) Interrupt processing time : 2.88 µs to 46.1 µs (12.5 MHz)		
Ports	General-purpose I/O ports (CMOS) : 26 (also serve as peripherals) (4 ports are also an N-ch open-drain type.)		
21-bit time-base timer	21-bit Interrupt cycle : 0.66 ms, 2.64 ms, 21 ms, or 335.5 ms with 12.5 MHz main clock		
Watchdog timer	Reset generation cycle : 335.5 ms minimum with 12.5 MHz main clock		
8-bit PWM timer	8-bit interval timer operation (square output capable, operating clock cycle : 0.32 µs , 2.56 µs, 5.1 µs, 20.5 µs) 8-bit resolution PWM operation (conversion cycle : 81.9 µs to 21.47 s : in the selection of internal shift clock of 8/16-bit capture timer) Count clock selectable between 8-bit and 16-bit timer/counter outputs		
8/16-bit capture, timer/counter	8-bit capture timer/counter × 1 channel + 8-bit timer or 16-bit capture timer/counter × 1 channel Capable of event count operation and square wave output using external clock input with 8-bit timer 0 or 16-bit counter		
UART	Transfer data length : 6/7/8 bits		
8-bit Serial I/O	8 bits LSB first/MSB first selectable One clock selectable from four operation clocks (one external shift clock, three internal shift clocks : 0.8 µs, 6.4 µs, 25.6 µs)		
12-bit PPG timer	Output frequency : Pulse width and cycle selectable		
External interrupt 1 (wake-up function)	3 channels (Interrupt vector, request flag, request output enabled) Edge selectable (Rising edge, falling edge, or both edges) Also available for resetting stop/sleep mode (Edge detectable even in stop mode)		
External interrupt 2 (wake-up function)	1 channel with 8 inputs (Independent L-level interrupt and input enable) Also available for resetting stop/sleep mode (Level detectable even in stop mode)		

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Parameter \ Part number	MB89202	MB89F202	MB89V201
10-bit A/D converter	10-bit precision × 8 channels A/D conversion function (Conversion time : 12.16 µs/12.5 MHz) Continuous activation by 8/16-bit timer/counter output or time-base timer counter		
Wild Register	8-bit × 2		
Standby mode	Sleep mode, and Stop mode		
Overhead time from reset to the first instruction execution	Power-on reset : Oscillation stabillization wait*1 External reset : a few µs Software reset : a few µs	Power-on reset : Voltage regulator and oscillation stabillization wait (31.5 ms/12.5 MHz) External reset : Oscillation stabillization wait (21.0 ms/12.5 MHz) Software reset : a few µs	Power-on reset : Oscillation stabillization wait (21.0 ms / 12.5 MHz) External reset : Oscillation stabillization wait (21.0 ms / 12.5 MHz) Software reset : a few µs
Power supply voltage*2	2.2 V to 5.5 V	3.5 V to 5.5 V	2.7 V to 5.5 V

*1 : Check section “■ MASK OPTIONS”

*2 : The minimum operating voltage varies with the operating frequency, the function, and the connected ICE. (The operating voltage of the A/D converter is assured separately. Check section “■ ELECTRICAL CHARACTERISTICS.”)

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89202	MB89F202	MB89V201
DIP-32P-M06	○	○	×
FPT-34P-M03	○	○	×
FPT-64P-M03	×	×	○

○ : Available × : Not available

■ DIFFERENCES AMONG PRODUCTS

• Memory Size

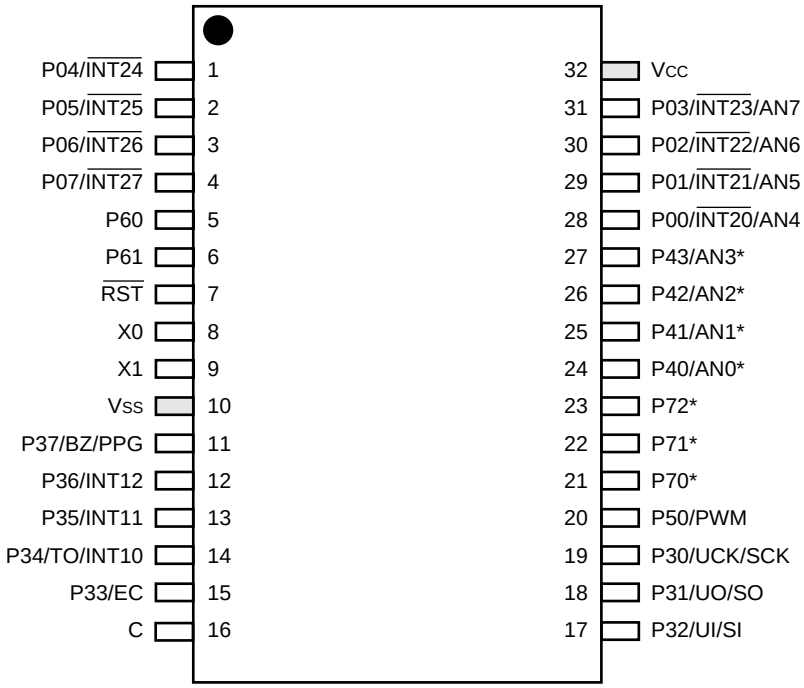
Before evaluating using the evaluation product, verify its differences from the product that will actually be used.

• Mask Options

Functions that can be selected as options and how to designate these options vary by the product. Before using options check section “■ MASK OPTIONS”.

■ PIN ASSIGNMENTS

(TOP VIEW)



* : Large-current drive type

(DIP-32P-M06)

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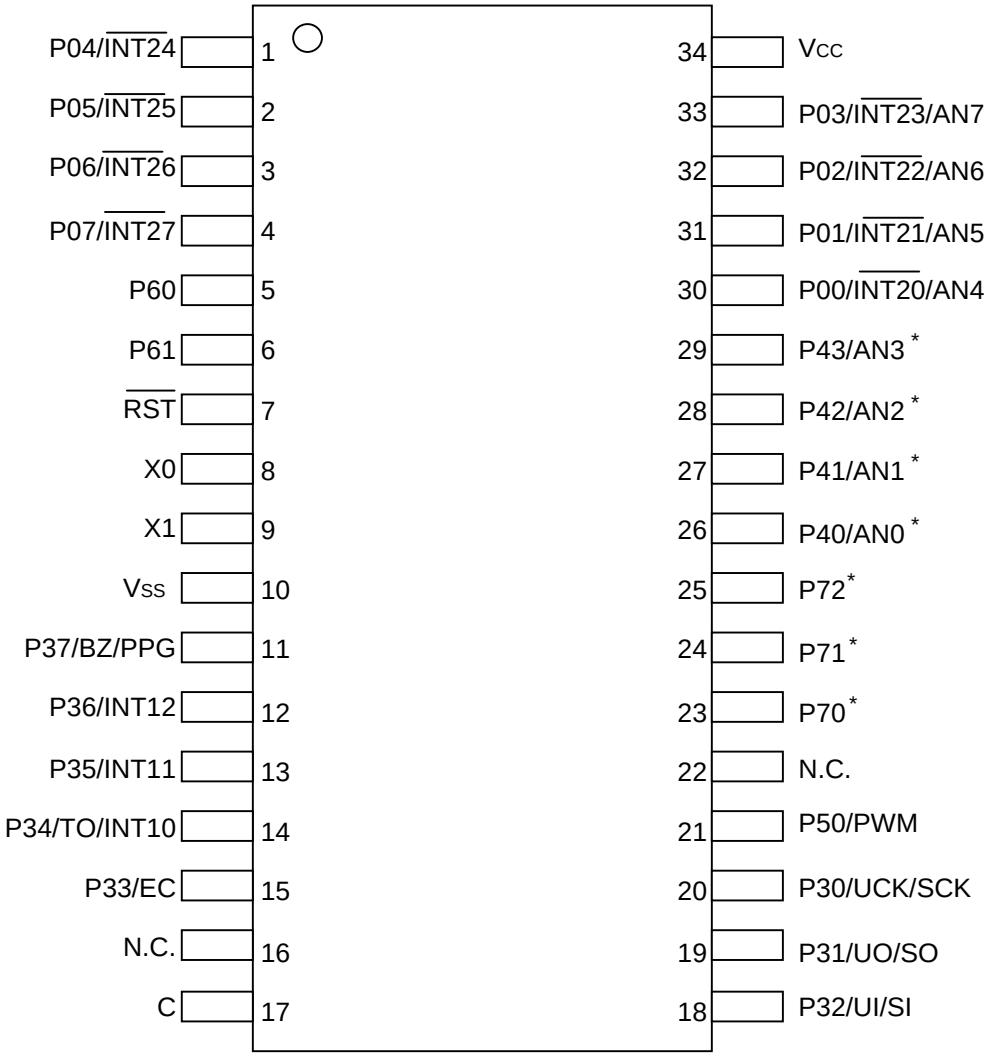
(TOP VIEW)



* : Large-current drive type
N.C. : Internally connected. Do not use.

(FPT-34P-M03)

■ PIN DESCRIPTION

Pin No.		Pin name	Circuit type	Function
SH-DIP32*1	SSOP34*2			
8	8	X0	A	Pins for connecting the crystal for the main clock. To use an external clock, input the signal to X0 and leave X1 open.
9	9	X1		
5, 6	5, 6	P60, P61	H / E	General-purpose CMOS input port for MB89F202. General-puspose CMOS I/O port for MB89202/MB89V201.
7	7	$\overline{\text{RST}}$	C	Reset I/O pin. This pin serves as an N-channel open-drain reset output with pull-up resistor (not available for MB89F202) and a reset input as well. The reset is a hysteresis input. It outputs the “L” signal in response to an internal reset request. Also, it initializes the internal circuit upon input of the “L” signal.
28 to 31	30 to 33	P00/$\overline{\text{INT20}}$/AN4 to P03/$\overline{\text{INT23}}$/AN7	G	General-purpose CMOS I/O ports. These pins also serve as an input (wake-up input) of external interrupt 2 or as an 10-bit A/D converter analog input. The input of external interrupt 2 is a hysteresis input.
1 to 4	1 to 4	P04/$\overline{\text{INT24}}$ to P07/$\overline{\text{INT27}}$	D	General-purpose CMOS I/O ports. These pins also serve as an input (wake-up input) of external interrupt 2. The input of external interrupt 2 is a hysteresis input.
19	20	P30/UCK/SCK	B	General-purpose CMOS I/O ports. This pin also serves as the clock I/O pin for the UART or 8-bit serial I/O. The resource is a hysteresis input.
18	19	P31/UO/SO	E	General-purpose CMOS I/O ports. This pin also serves as the data output pin for the UART or 8-bit serial I/O.
17	18	P32/UI/SI	B	General-purpose CMOS I/O ports. This pin also serves as the data input pin for the UART or 8-bit serial I/O. The resource is a hysteresis input.
15	15	P33/EC	B	General-purpose CMOS I/O ports. This pin also serves as the external clock input pin for the 8/16-bit capture timer/counter. The resource is a hysteresis input.
14	14	P34/TO/INT10	B	General-purpose CMOS I/O ports. This pin also serves as the output pin for the 8/16-bit capture timer/counter or as the input pin for external interrupt 1. The resource is a hysteresis input.
13, 12	13, 12	P35/INT11, P36/INT12	B	General-purpose CMOS I/O ports. These pins also serve as the input pin for external interrupt 1. The resource is a hysteresis input.
11	11	P37/BZ/PPG	E	General-purpose CMOS I/O ports. This pin also serves as the buzzer output pin or the 12-bit PPG output.
20	21	P50/PWM	E	General-purpose CMOS I/O ports. This pin also serves as the 8-bit PWM timer output pin.

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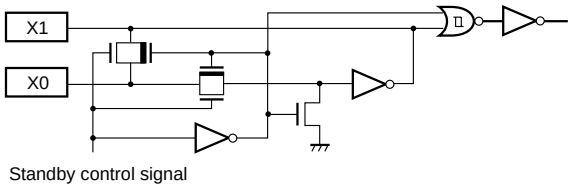
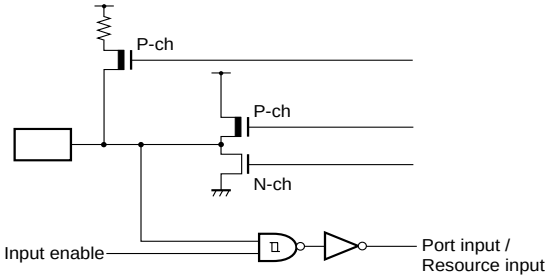
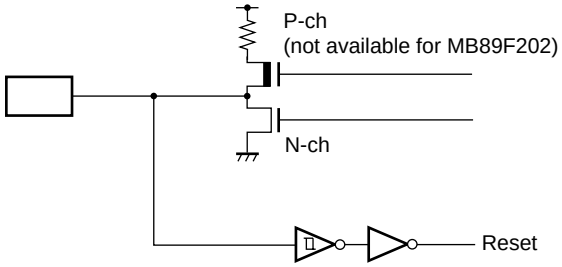
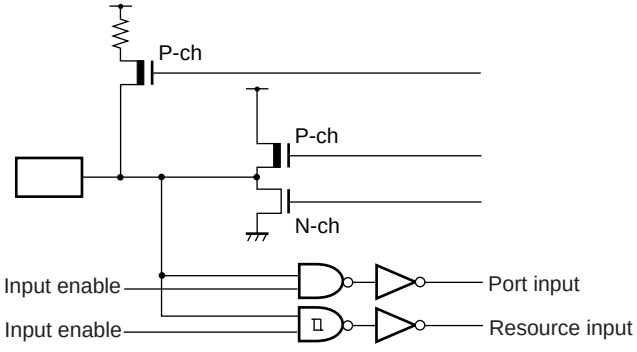
Pin No.		Pin name	Circuit type	Function
SH-DIP32*1	SSOP34*2			
24 to 27	26 to 29	P40/AN0 to P43/ AN3	F	General-purpose CMOS I/O ports. These pins can also be used as N-channel open-drain ports. These pins also serve as 10-bit A/D converter analog input pins.
21 to 23	23 to 25	P70 to P72	E	General-purpose CMOS I/O ports.
32	34	V_{CC}	—	Power supply pin
10	10	V_{SS}	—	Power (GND) pin
16	17	C	—	MB89F202: Capacitance pin for regulating the power supply. Connect an external ceramic capacitor of about 0.1µF. MB89202: This pin is not internally connected. It is unnecessary to connect a capacitor.
—	16, 22	N.C.	—	Internally connected pins Be sure to leave it open.

*1 : DIP-32P-M06

*2 : FPT-34P-M03

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• At an oscillation feedback resistance of approximately 500 kΩ
B		• CMOS output • Hysteresis input • Pull-up resistor optional
C		• At an output pull-up resister (P-ch) of approximately 50 kΩ/5.0 V (not available for MB89F202) • N-ch open-drain reset output • Hysteresis input
D		• CMOS output • CMOS input • Hysteresis input (Resource input) • Pull-up resistor optional

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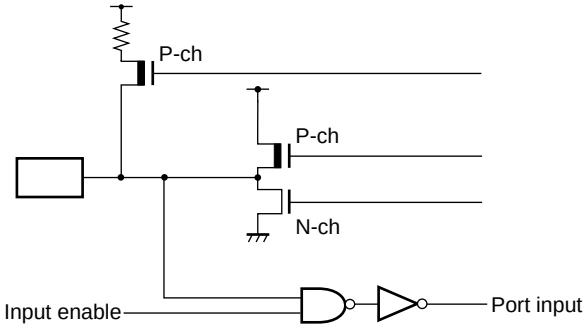
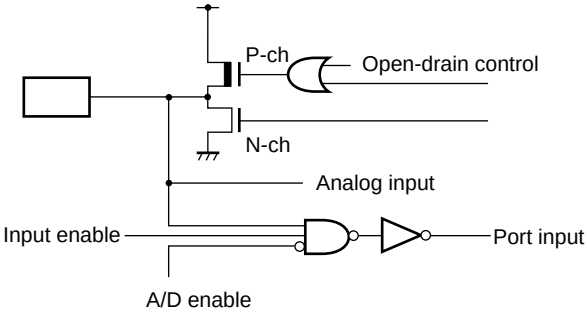
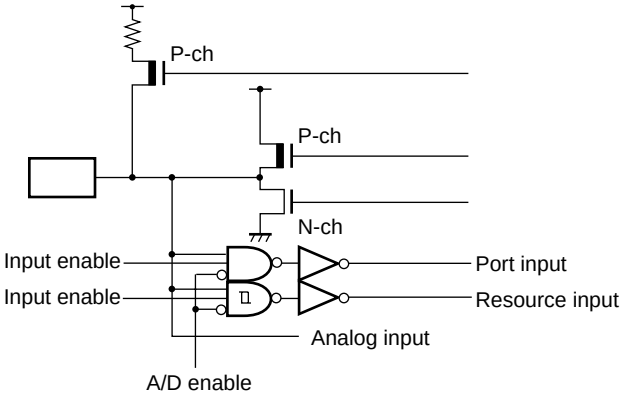
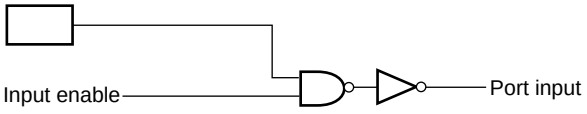
Type	Circuit	Remarks
E		• CMOS output • CMOS input • Pull-up resistor optional • P70-P72 are large-current drive type
F		• CMOS output • CMOS input • Analog input • N-ch open-drain output available • P40-P43 are large-current drive type
G		• CMOS output • CMOS input • Hysteresis input (Resource input) • Analog input
H		• CMOS input

■ HANDLING DEVICES

• Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ ELECTRICAL CHARACTERISTICS” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

• Treatment of Unused Input Pins

Leaving unused input terminals open may lead to permanent damage due to malfunction and latchup; pull up or pull down the terminals through the resistors of 2 kΩ or more.

Make the unused I/O terminal in a state of output and leave it open or if it is in an input state, handle it with the same procedure as the input terminals.

• Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

• Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

• Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

• About the Wild Register Function

No wild register can be debugged on the MB89V201. For the operation check, test the MB89F202 installed on a target system.

• Program Execution in RAM

When the MB89V201 is used, no program can be executed in RAM.

• Note to Noise in the External Reset Pin ($\overline{RST}$)

If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$).

• External pullup for the External Reset Pin ($\overline{RST}$) of MB89F202

Internal pullup control for $\overline{RST}$ pin is not available for MB89F202. To ensure proper external reset control in MB89F202, an external pullup (recommend 100 kΩ) for $\overline{RST}$ pin must be required.

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- **Notes on selecting mask option**

  Please select “With reset output” by the mask option when power-on reset is generated at the power supply ON, and the device is used without inputting external reset.

■ PROGRAMMING AND ERASE FLASH MEMORY ON THE MB89F202

1. Flash Memory

The flash memory is located between $C000_H$ and $FFFF_H$ in the CPU memory map and incorporates a flash memory interface circuit that allows read access and program access from the CPU to be performed in the same way as mask ROM. Programming and erasing flash memory is also performed via the flash memory interface circuit by executing instructions in the CPU. This enables the flash memory to be updated in place under the control of the CPU, providing an efficient method of updating program and data.

2. Flash Memory Features

- 16 K byte × 8-bit configuration
- Automatic programming algorithm (Embedded Algorithm*)
- Data polling and toggle bit for detection of program/erase completion
- Detection of program/erase completion via CPU interrupt
- Compatible with JEDEC-standard commands
- No. of program / erase cycles : Minimum 10,000

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

3. Procedure for Programming and Erasing Flash Memory

Programming and reading flash memory cannot be performed at the same time. Accordingly, to program or erase flash memory, the program must first be copied from flash memory to RAM so that programming can be performed without program access from flash memory.

4. Flash Memory Control Status Register (FMCS)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
0079_H	INTE	RDYINT	WE	RDY	—	—	—	—	$000X----_B$
	R/W	R/W	R/W	R	—	—	—	—	

5. Memory Space

The memory space for the CPU access and for the flash programmer access is listed below.

Memory size	CPU address	Programmer address
16 K bytes	$FFFF_H$ to $C000_H$	$FFFF_H$ to $C000_H$

6. Flash Programmer Adapter and Recommended Flash Programmers

• Parallel programmer

Part number	Package	Adapter Part number	Programmer Part number *
MB89F202P-SH	DIP-32P-M06	TEF200-89F202-PSH	AF9708, AF9709/B, AF9723 + AF9834
MB89F202PFV	FPT-34P-M03	TEF200-89F202-PFV	

* : For the programmer and the version of the programmer,contact the Flash Support Group, Inc.
Inquiry : Flash Support Group, Inc. : FAX : 81-(53)-428-8377
: E-mail : support@j-fsg.co.jp

• Serial programmer (PC programmer)

Part number	Package	Adapter Part number
MB89F202P-SH	DIP-32P-M06	ROM3-DIP32PM06-8L
MB89F202PFV	FPT-34P-M03	ROM3-FPT34PM03-8L

Inquiries :
Adapter : Sunhayato Corp. : FAX : 81-(3)-3971-0535
E-mail : adapter@sunhayato.co.jp
PC programmer software : FUJITSU LIMITED

7. Flash Content Protection

Flash content can be read using parallel / serial programmer if the flash content protection mechanism is not activated.

One predefined area of the flash ($FFFC_H$) is assigned to be used for preventing the read access of flash content. If the protection code "01_H" is written in this address ($FFFC_H$), the flash content cannot be read by any parallel/ serial programmer.

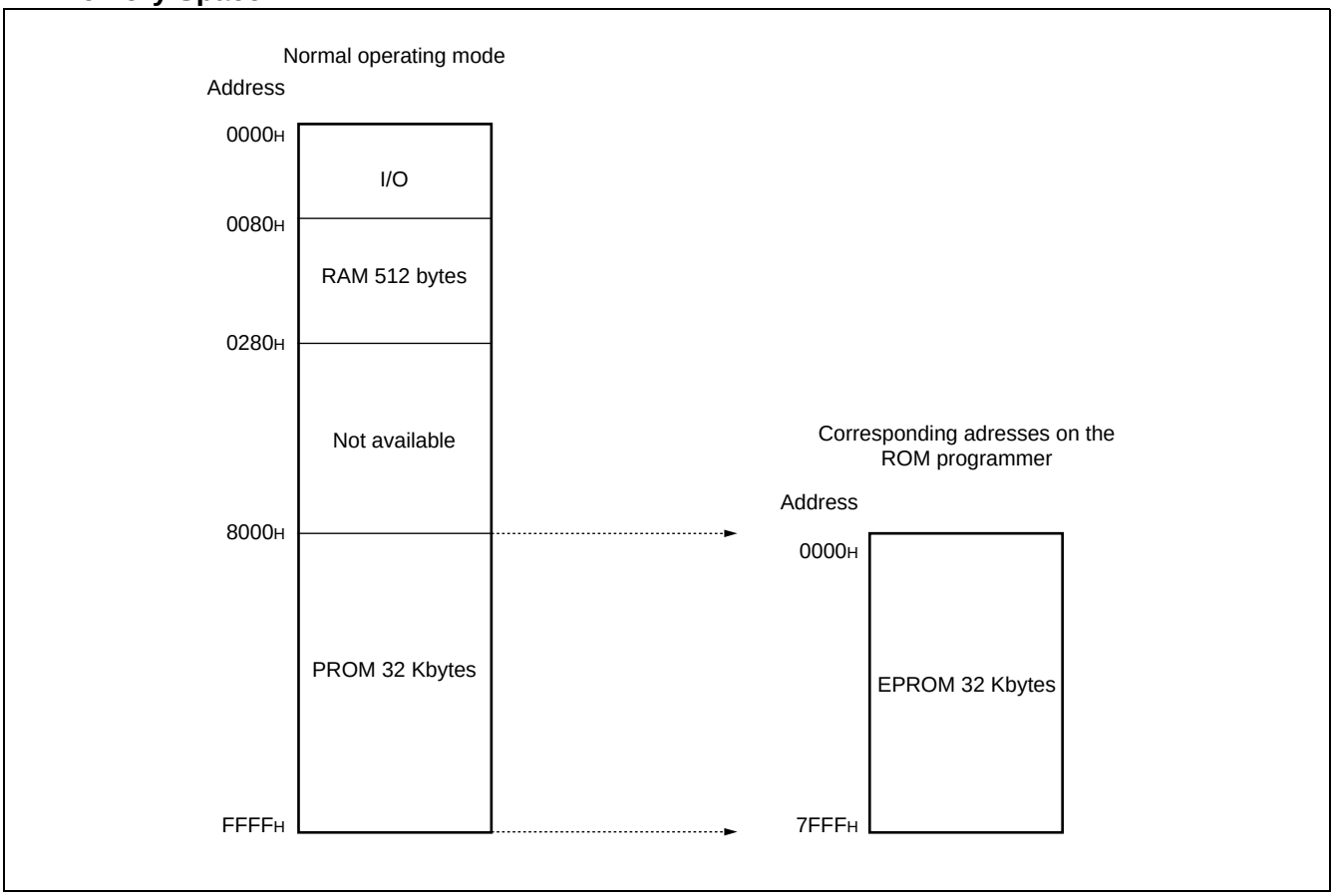
Note : The program written into the flash cannot be verified once the flash protection code is written ("01_H" in $FFFC_H$). It is advised to write the flash protection code at last.

■ PROGRAMMING TO THE EPROM WITH EVALUATION PRODUCT DEVICE

1. EPROM for Use

MBM27C256A (DIP-28)

2. Memory Space.



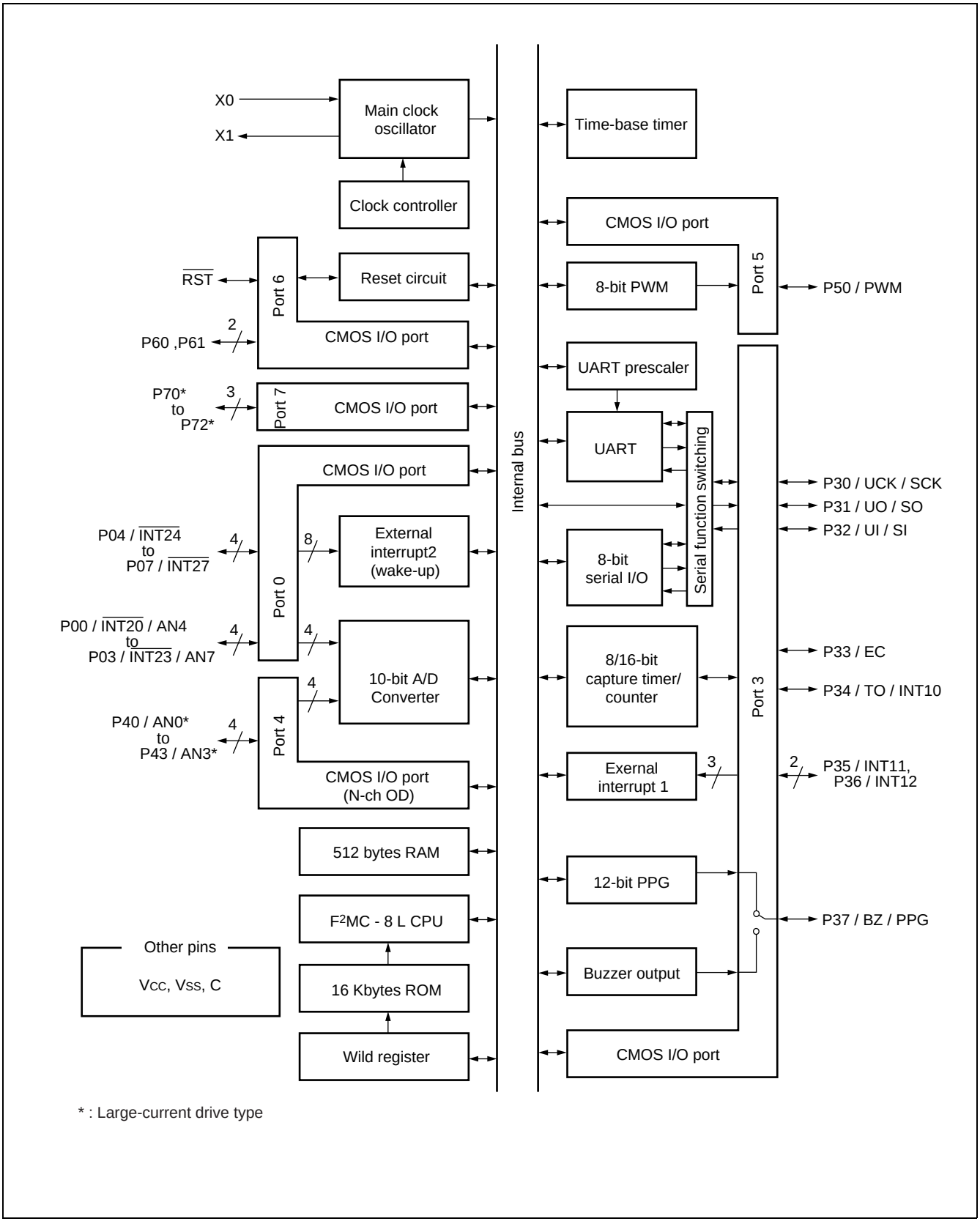
3. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM



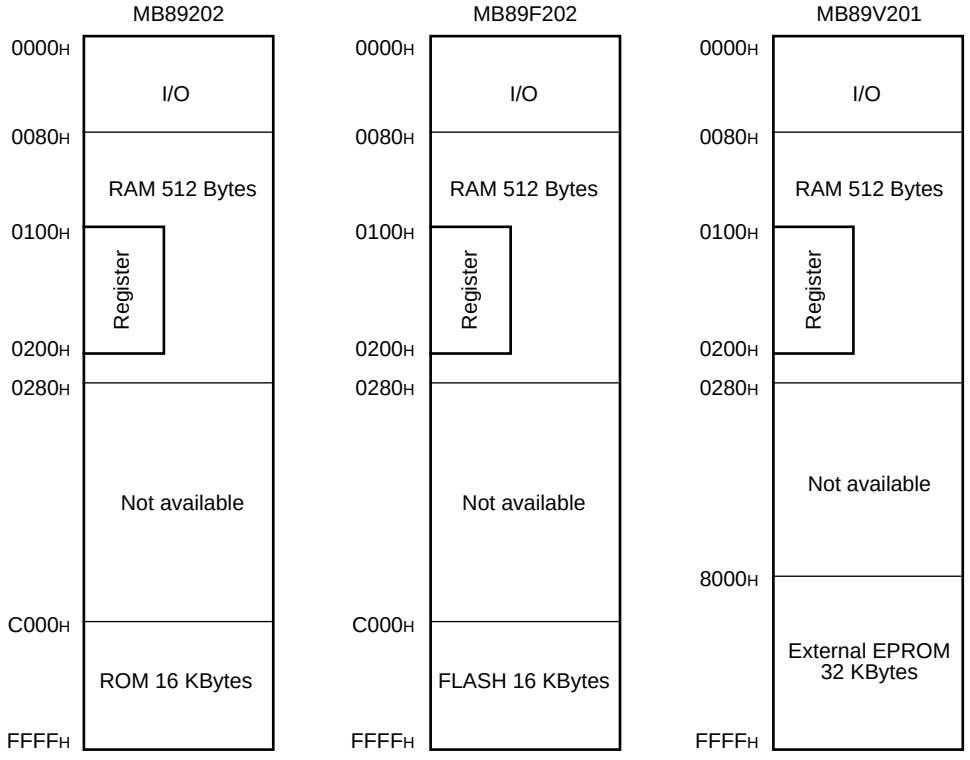
* : Large-current drive type

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89202 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89202 series is structured as illustrated below.

- **Memory Space**



2. Registers

The MB89202 series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided :

Program counter (PC) : A 16-bit register for indicating instruction storage positions

Accumulator (A) : A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.

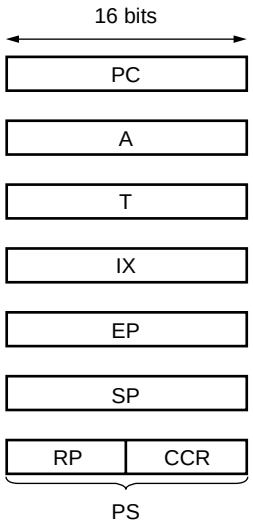
Temporary accumulator (T) : A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX) : A 16-bit register for index modification

Extra pointer (EP) : A 16-bit pointer for indicating a memory address

Stack pointer (SP) : A 16-bit register for indicating a stack area

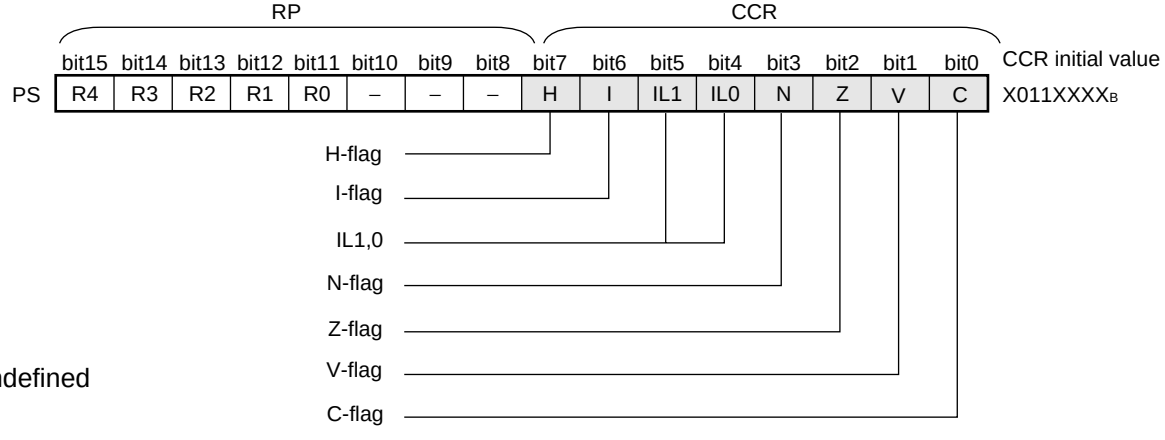
Program status (PS) : A 16-bit register for storing a register pointer, a condition code



	Initial value
: Program counter	$FFFD_H$
: Accumulator	Undefined
: Temporary accumulator	Undefined
: Index register	Undefined
: Extra pointer	Undefined
: Stack pointer	Undefined
: Program status	I-flag = 0, IL1, 0 = 11 The other bit values are undefined.

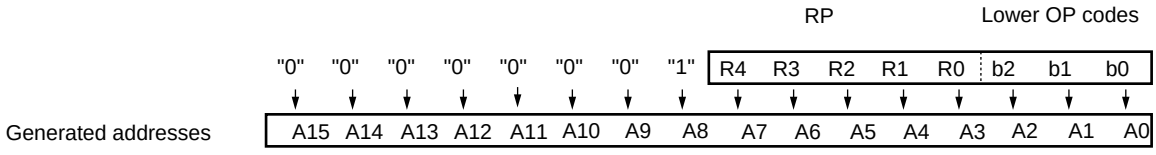
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) . (See the diagram below.)

- **Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag : Set to “1” when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is enabled when this flag is set to “1”. Interrupt is disabled when the flag is cleared to “0”. Cleared to “0” at the reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag : Set to “1” if the MSB becomes to “1” as the result of an arithmetic operation. Cleared to “0” when the bit is cleared to “0”.

Z-flag : Set to “1” when an arithmetic operation results in 0. Cleared to “0” otherwise.

V-flag : Set to “1” if the complement on 2 overflows as a result of an arithmetic operation. Cleared to “0” if the overflow does not occur.

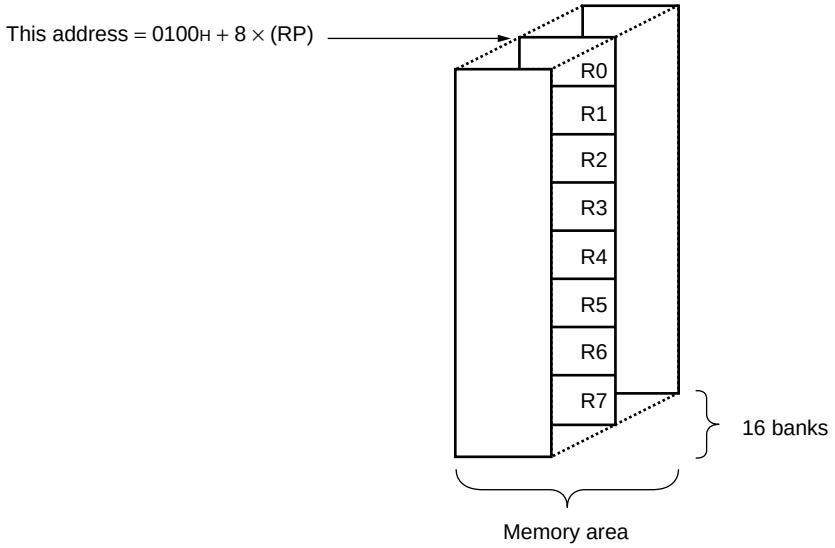
C-flag : Set to “1” when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided :

General-purpose registers : An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89202 series. The bank currently in use is indicated by the register bank pointer (RP) .

- **Register Bank Configuration**



■ I/O MAP

Address	Register name	Register description	Read/write	Initial value
0000H	PDR0	Port 0 data register	R/W	X X X X X X X X
0001H	DDR0	Port 0 data direction register	W	0 0 0 0 0 0 0 0
0002H to 00006H	Reserved			
0007H	SYCC	System clock control register	R/W	1 - - MM1 0 0
0008H	STBC	Standby control register	R/W	0 0 0 1 0 - - -
0009H	WDTC	Watchdog timer control register	R/W	0 - - - X X X X
000AH	TBTC	Time-base timer control register	R/W	0 0 - - - 0 0 0
000BH	Reserved			
000CH	PDR3	Port 3 data register	R/W	X X X X X X X X
000DH	DDR3	Port 3 data direction register	W	0 0 0 0 0 0 0 0
000EH	RSFR	Reset flag register	R	X X X X - - - -
000FH	PDR4	Port 4 data register	R/W	- - - - X X X X
0010H	DDR4	Port 4 data direction register	R/W	- - - - 0 0 0 0
0011H	OUT4	Port 4 output format register	R/W	- - - - 0 0 0 0
0012H	PDR5	Port 5 data register	R/W	- - - - - - - X
0013H	DDR5	Port 5 data direction register	R/W	- - - - - - - 0
0014H	RCR21	12-bit PPG control register 1	R/W	0 0 0 0 0 0 0 0
0015H	RCR22	12-bit PPG control register 2	R/W	- - 0 0 0 0 0 0
0016H	RCR23	12-bit PPG control register 3	R/W	0 - 0 0 0 0 0 0
0017H	RCR24	12-bit PPG control register 4	R/W	- - 0 0 0 0 0 0
0018H	BZCR	Buzzer register	R/W	- - - - - 0 0 0
0019H	TCCR	Capture control register	R/W	0 0 0 0 0 0 0 0
001AH	TCR1	Timer 1 control register	R/W	0 0 0 - 0 0 0 0
001BH	TCR0	Timer 0 control register	R/W	0 0 0 0 0 0 0 0
001CH	TDR1	Timer 1 data register	R/W	X X X X X X X X
001DH	TDR0	Timer 0 data register	R/W	X X X X X X X X
001EH	TCPH	Capture data register H	R	X X X X X X X X
001FH	TCPL	Capture data register L	R	X X X X X X X X
0020H	TCR2	Timer output control register	R/W	- - - - - - 0 0
0021H	Reserved			
0022H	CNTR	PWM control register	R/W	0 - 0 0 0 0 0 0
0023H	COMR	PWM compare register	W	X X X X X X X X
0024H	EIC1	External interrupt 1 Control register 1	R/W	0 0 0 0 0 0 0 0

(Continued)

Address	Register name	Register description	Read/write	Initial value
0025H	EIC2	External interrupt 1 Control register 2	R/W	- - - - 0 0 0 0
0026H	Reserved			
0027H				
0028H	SMC	Serial mode control register	R/W	0 0 0 0 0 - 0 0
0029H	SRC	Serial rate control register	R/W	- - 0 1 1 0 0 0
002AH	SSD	Serial status and data register	R/W	0 0 1 0 0 - 1 X
002BH	SIDR	Serial input data register	R	X X X X X X X X
	SODR	Serial output data register	W	X X X X X X X X
002CH	UPC	Clock division selection register	R/W	- - - - 0 0 1 0
002DH to 002FH	Reserved			
0030H	ADC1	A/D converter control register 1	R/W	- 0 0 0 0 0 0 0
0031H	ADC2	A/D converter control register 2	R/W	- 0 0 0 0 0 0 1
0032H	ADDH	A/D converter data register H	R	- - - - - - X X
0033H	ADDL	A/D converter data register L	R	X X X X X X X X
0034H	ADEN	A/D enable register	R/W	0 0 0 0 0 0 0 0
0035H	Reserved			
0036H	EIE2	External interrupt 2 control register1	R/W	0 0 0 0 0 0 0 0
0037H	EIF2	External interrupt 2 control register2	R/W	- - - - - - - 0
0038H	Reserved			
0039H	SMR	Serial mode register	R/W	0 0 0 0 0 0 0 0
003AH	SDR	Serial data register	R/W	X X X X X X X X
003BH	SSEL	Serial function switching register	R/W	- - - - - - - 0
003CH to 003FH	Reserved			
0040H	WRARH0	Upper-address setting register	R/W	X X X X X X X X
0041H	WRARL0	Lower-address setting register	R/W	X X X X X X X X
0042H	WRDR0	Data setting register 0	R/W	X X X X X X X X
0043H	WRARH1	Upper-address setting register	R/W	X X X X X X X X
0044H	WRARL1	Lower-address setting register	R/W	X X X X X X X X
0045H	WRDR1	Data setting register 1	R/W	X X X X X X X X
0046H	WREN	Address comparison EN register	R/W	X X X X X X 0 0
0047H	WROR	Wild-register data test register	R/W	- - - - - - 0 0
0048H to 005FH	Reserved			

(Continued)

(Continued)

Address	Register name	Register description	Read/write	Initial value
0060H	PDR6	Port 6 data register	R/W	- - - - - - X X
0061H	DDR6	Port 6 data direction register*	R/W	- - - - - - 0 0
0062H	PUL6	Port 6 pull-up setting register	R/W	- - - - - - 0 0
0063H	PDR7	Port 7 data register	R/W	- - - - - X X X
0064H	DDR7	Port 7 data direction register	R/W	- - - - - 0 0 0
0065H	PUL7	Port 7 pull-up setting register	R/W	- - - - - 0 0 0
0066H to 006FH	Reserved			
0070H	PUL0	Port-0 pull-up setting register	R/W	0 0 0 0 0 0 0 0
0071H	PUL3	Port-3 pull-up setting register	R/W	0 0 0 0 0 0 0 0
0072H	PUL5	Port-5 pull-up setting register	R/W	- - - - - - - 0
0073H to 0078H	Reserved			
0079H	FMCS	Flash memory control status register	R/W	0 0 0 X - - - -
007AH	Reserved			
007BH	ILR1	Interrupt level setting register1	W	1 1 1 1 1 1 1 1
007CH	ILR2	Interrupt level setting register2	W	1 1 1 1 1 1 1 1
007DH	ILR3	Interrupt level setting register3	W	1 1 1 1 1 1 1 1
007EH	ILR4	Interrupt level setting register4	W	1 1 1 1 1 1 1 1
007FH	ITR	Interrupt test register	Not available	- - - - - - 0 0

- : Unused, X : Undefined, M : Set using the mask option

* : No used in MB89F202

Note : Do not use prohibited areas.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
Input voltage*	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage*	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average output current	I_{OLAV1}	—	4	mA	Average value (operating current × operating rate) Pins excluding P40 to P43, P70 to P72
	I_{OLAV2}	—	12	mA	Average value (operating current × operating rate) Pins P40 to P43, P70 to P72
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“H” level maximum output current	I_{OH}	—	–10	mA	Pins excluding P60, P61
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	ΣI_{OH}	—	–50	mA	
Power consumption	Pd	—	200	mW	
Operating temperature	Ta	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : This parameter is based on V_{SS} = 0.0 V.

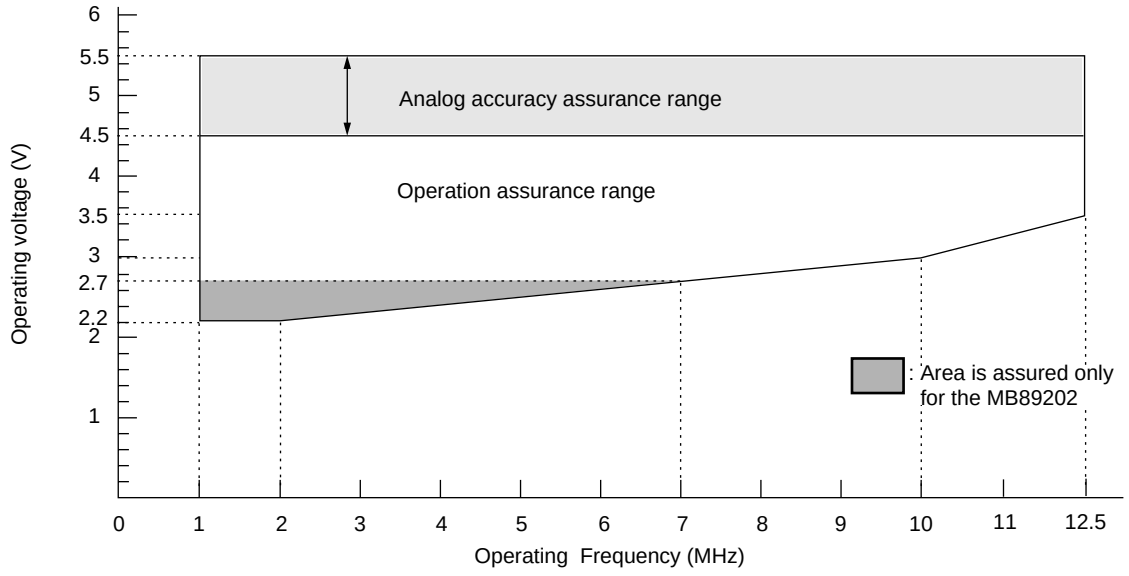
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

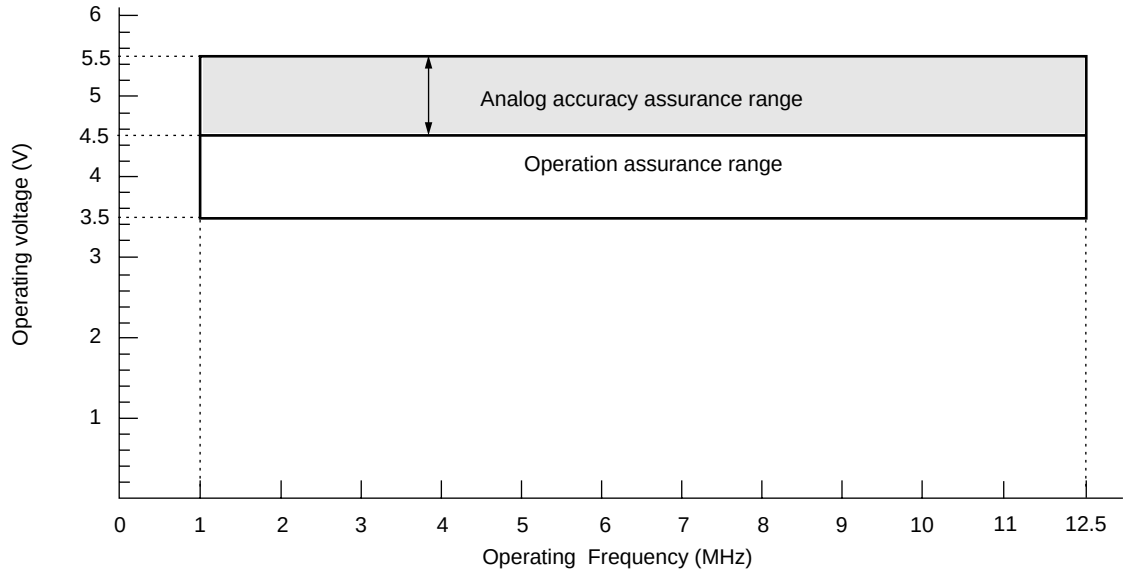
(Vss = 0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.2	5.5	V	MB89202
		3.5	5.5	V	MB89F202
		2.7	5.5	V	MB89V201
		1.5	5.5	V	Retains the RAM state in stop mode
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	P00 to P07, P31, P37, P40 to P43, P50, P60, P61, P70 to P72
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	$\overline{RST}$, EC, $\overline{INT20}$ to $\overline{INT27}$, UCK/SCK, INT10 to INT12, P30, P32 to P36, UI/SI
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	P00 to P07, P31, P37, P40 to P43, P50, P60, P61, P70 to P72
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	$\overline{RST}$, EC, $\overline{INT20}$ to $\overline{INT27}$, UCK/SCK, INT10 to INT12, P30, P32 to P36, UI/SI
Open-drain output pin application voltage	V_D	V_{SS} – 0.3	V_{CC} + 0.3	V	P40 to P43, $\overline{RST}$
Operating temperature	Ta	–40	+85	°C	Room temperature is recommended for programming the flash memory on MB89F202

Operating Assurance for MB89202 and MB89V201



Operating Assurance for MB89F202



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, F_{CH} = 12.5 MHz (External clock) , Ta = –40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P00 to P07, P31, P37, P40 to P43, P50, P60, P61, P70 to P72	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	P30, P32 to P36, $\overline{RST}$ UCK/SCK, UI/SI, EC, $\overline{INT20}$ to $\overline{INT27}$, INT10 to INT12	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P31, P37, P40 to P43, P50, P60, P61, P70 to P72	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	P30, P32 to P36, $\overline{RST}$, UCK/SCK, UI/SI, EC, $\overline{INT20}$ to $\overline{INT27}$, INT10 to INT12	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P40 to P43, $\overline{RST}$	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P00 to P07, P30 to P37, P40 to P43, P50, P70 to P72	I_{OH} = –4.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P30 to P37, P50, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P40 to P43, P70 to P72	I_{OL} = 12.0 mA	—	—	0.4	V	
Input leakage current	I_{LI}	P00 to P07, P30 to P37, P40 to P43, P50 , P60, P61, $\overline{RST}$, P70 to P72	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P30 to P37, P50, $\overline{RST}$, P70 to P72	V_I = 0.0 V	25	50	100	kΩ	MB89202
		P00 to P07, P30 to P37, P50, P70 to P72						MB89F202

(Continued)

(Continued)

Parameter	Sym-bol	Pin name		Condition	Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	I_{CC}	V_{CC}	Normal operation mode (External clock, highest gear speed)	When A/D converter stops	—	8	12	mA	MB89202
					—	6	9	mA	MB89F202
				When A/D converter starts	—	10	15	mA	MB89202
					—	8	12	mA	MB89F202
	I_{CCS}		Sleep mode (External clock, highest gear speed)	When A/D converter stops	—	4	6	mA	MB89202
					—	3	5	mA	MB89F202
	I_{CCH}		Stop mode Ta = +25 °C (External clock)	When A/D converter stops	—	—	1	µA	MB89202
					—	—	10	µA	MB89F202
Input capacitance	C_{IN}	Other than C, V_{CC}, V_{SS}		—	—	10	—	pF	

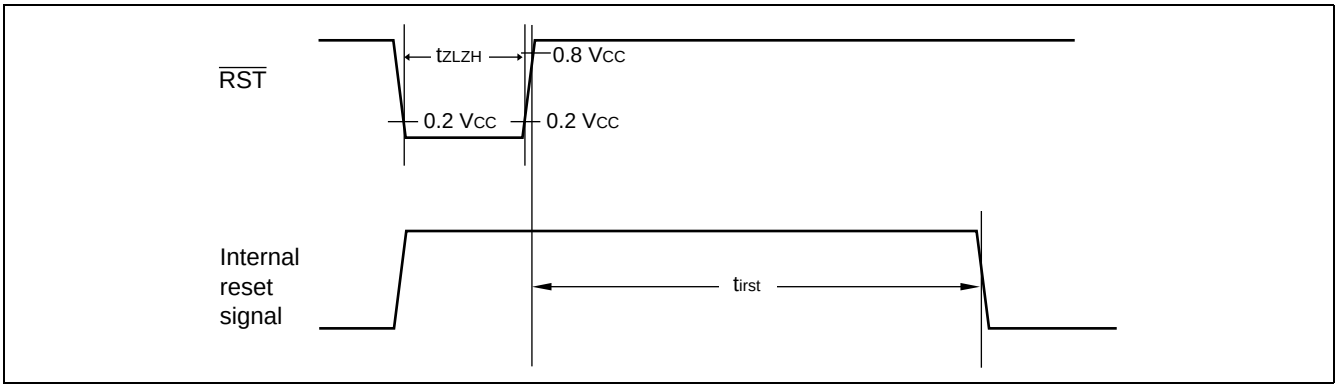
4. AC Characteristics

(1) Reset Timing

(V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	45	—	ns	
Internal reset pulse extension	t_{irst}	—	48 t_{HCYL}*	—	ns	

* : t_{HCYL} 1 oscillating clock cycle time

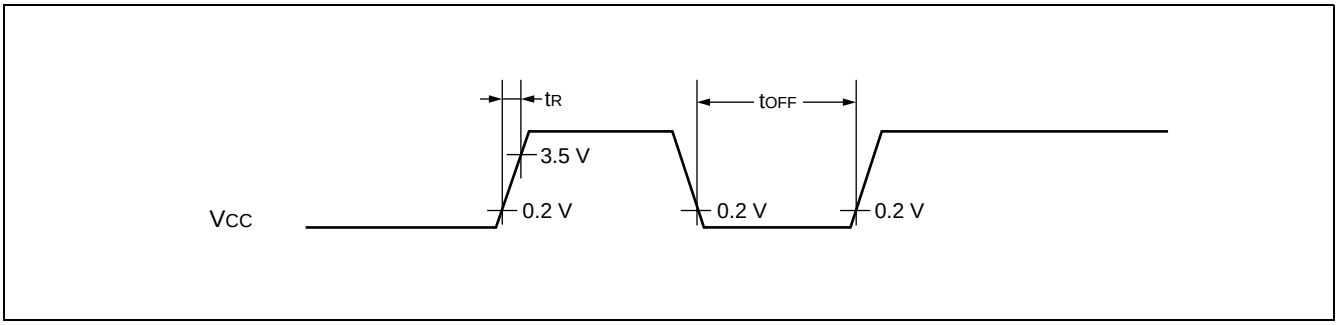


Notes: • When the power-on reset option is not on, leave the external reset on until oscillation becomes stable.
• If the reset pulse applied to the external reset pin ($\overline{RST}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{RST}$).

(2) Power-on Reset

(V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations



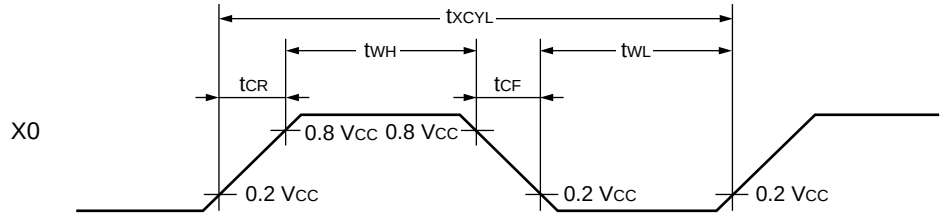
Note : The supply voltage must be set to the minimum value required for operation within the prescribed default oscillation settling time.

(3) Clock Timing

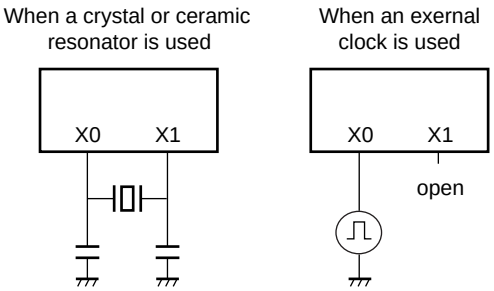
(V_{SS} = 0.0 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Clock frequency	F_{CH}	—	1	12.5	MHz	
Clock cycle time	t_{XCYL}		80	1000	ns	
Input clock pulse width	t_{WH} t_{WL}		20	—	ns	
Input clock rising/falling time	t_{CR} t_{CF}		—	10	ns	

- **X0 and X1 Timing and Conditions**



- **Main Clock Conditions**



(4) Instruction Cycle

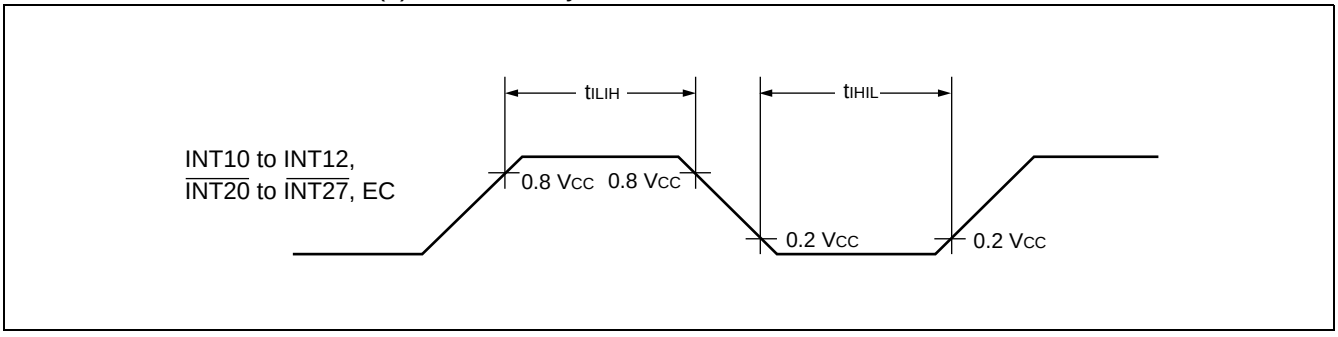
Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{INST}	4/F_{CH}, 8/F_{CH}, 16/F_{CH}, 64/F_{CH}	µs	t_{INST} = 0.32 µs when operating at F_{CH} = 12.5 MHz (4/F_{CH})

(5) Peripheral Input Timing

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

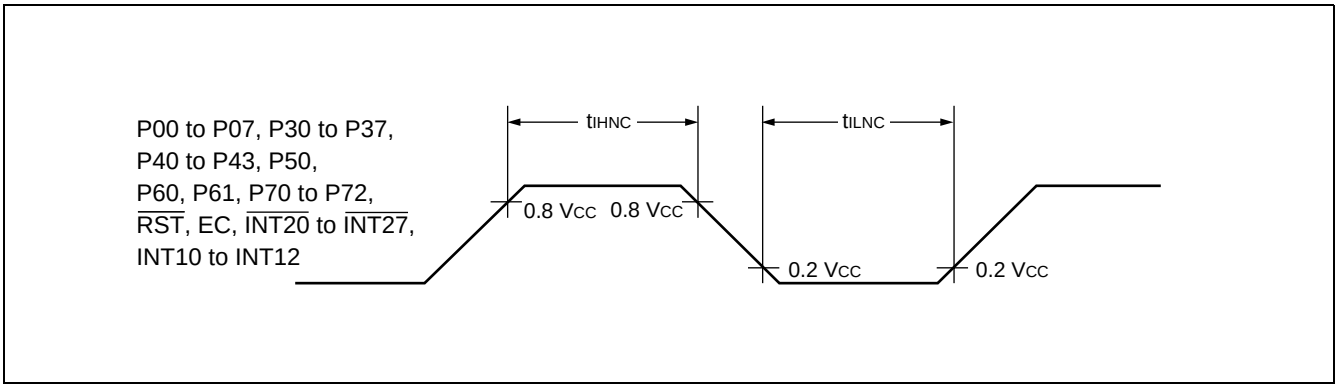
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Peripheral input “H” pulse width	t_{ILIH}	INT10 to INT12, $\overline{INT20}$ to $\overline{INT27}$, EC	2 t_{INST}*	—	µs	
Peripheral input “L” pulse width	t_{IHIL}		2 t_{INST}*	—	µs	

* : For information on t_{INST} see “ (4) Instruction Cycle”.



(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Peripheral input “H” noise limit	t_{IHNC}	P00 to P07, P30 to P37, P40 to P43, P50,P60,P61, P70 to P72, $\overline{RST}$, EC, $\overline{INT20}$ to $\overline{INT27}$, INT10 to INT12	—	45	—	ns	
Peripheral input “L” noise limit	t_{ILNC}		—	45	—	ns	



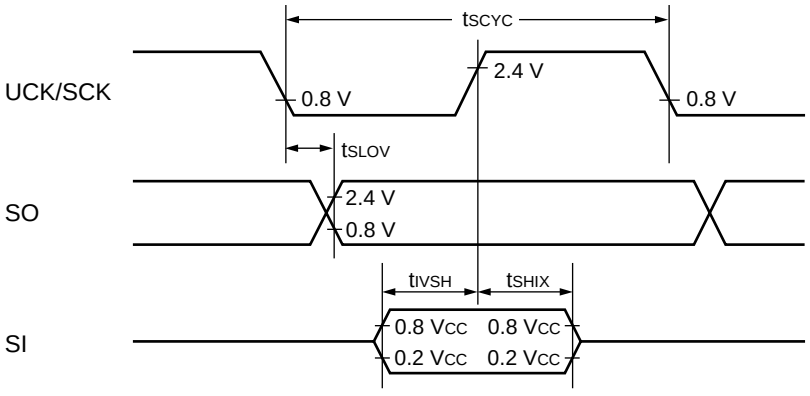
(6) UART, Serial I/O Timing

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

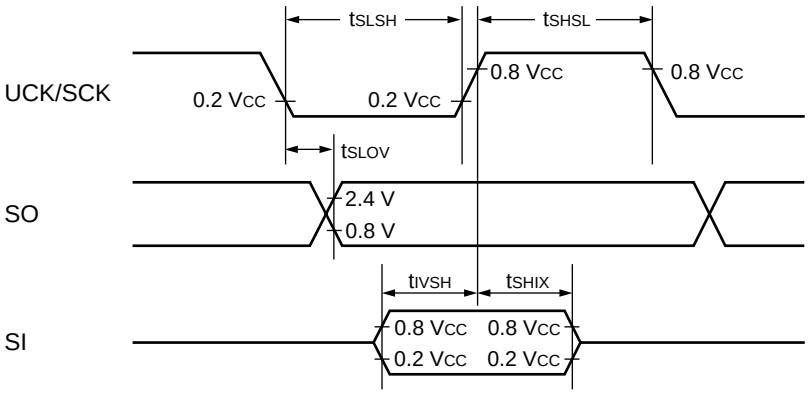
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	UCK/SCK	Internal shift clock mode	2 t_{INST}*	—	µs	
UCK/SCK ↓ → SO time	t_{SLOV}	UCK/SCK, SO		–200	200	ns	
Valid SI → UCK/SCK↑	t_{IVSH}	UCK/SCK, SI		1/2 t_{INST}*	—	µs	
UCK/SCK ↑ → Valid SI hold time	t_{SHIX}	UCK/SCK, SI		1/2 t_{INST}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	UCK/SCK	External shift clock mode	t_{INST}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	UCK/SCK		t_{INST}*	—	µs	
UCK/SCK ↓ → SO time	t_{SLOV}	UCK/SCK, SO		0	200	ns	
Valid SI → UCK/SCK	t_{IVSH}	UCK/SCK, SI		1/2 t_{INST}*	—	µs	
UCK/SCK ↑ → Valid SI hold time	t_{SHIX}	UCK/SCK, SI		1/2 t_{INST}*	—	µs	

* : For information on t_{inst}, see “ (4) Instruction Cycle”.

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**



5. A/D Converter

(1) A/D Converter Electrical Characteristics

(V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

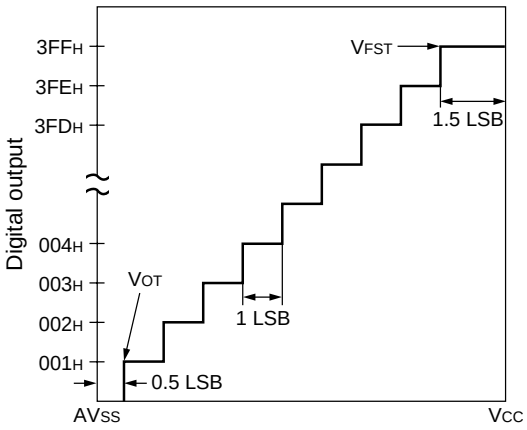
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		–5.0	—	+5.0	LSB	
Linearity error		–3.0	—	+3.0	LSB	
Differential linearity error		–2.5	—	+2.5	LSB	
Zero transition voltage	V_{OT}	V_{SS} – 3.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 4.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} – 6.5 LSB	V_{CC} – 1.5 LSB	V_{CC} + 2.0 LSB	V	
A/D mode conversion time	—	—	—	38 t_{INST}*	µs	
Analog port input current	I_{AIN}	—	—	10	µA	
Analog input voltage range	—	0	—	V_{CC}	V	
Power supply voltage for A/D accuracy assurance	V_{CC}	4.5	—	5.5	V	

* : For information on t_{inst}, see “ (4) Instruction Cycle” in “4. AC Characteristics.”

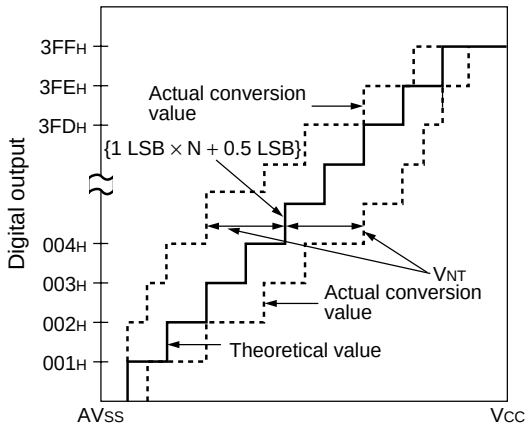
(2) A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics
- Differential linearity error (unit : LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit : LSB)
  The difference between theoretical and actual conversion values

Theoretical I/O characteristics



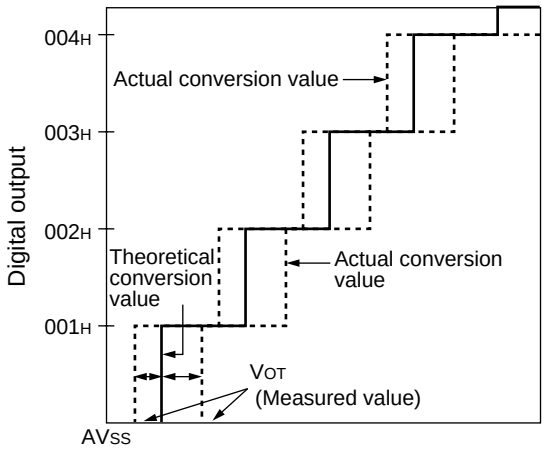
Total error



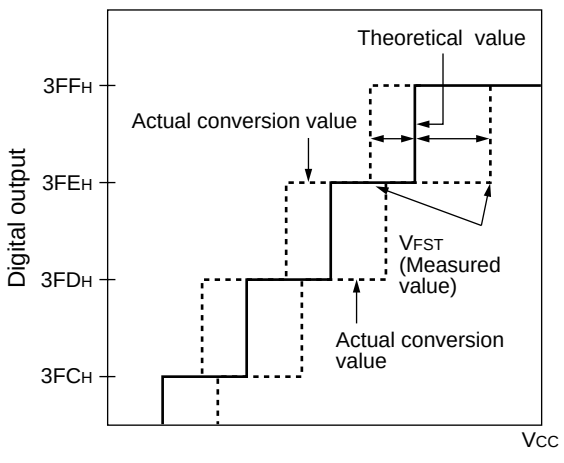
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{(V)}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times \text{N} + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

Zero transition error



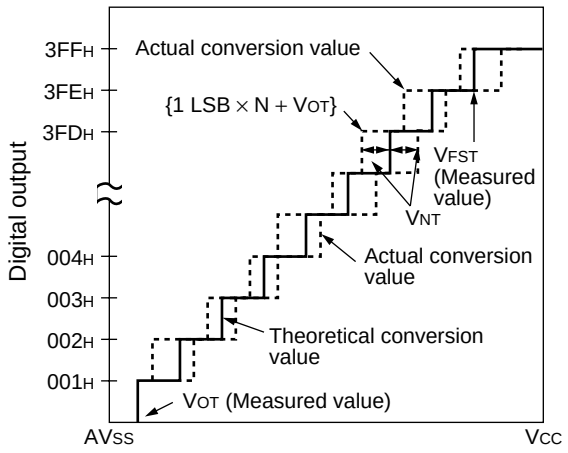
Full-scale transition error



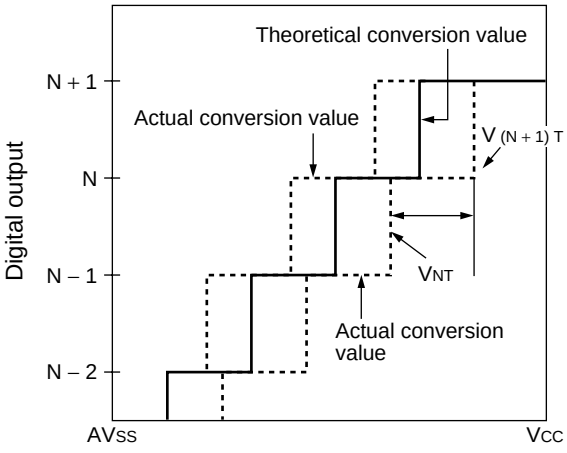
(Continued)

(Continued)

Linearity error



Differential linearity error



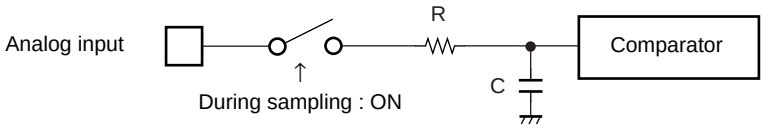
$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

(3) Notes on Using A/D Converter

- **About the external impedance of analog input and its sampling time**
  - A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



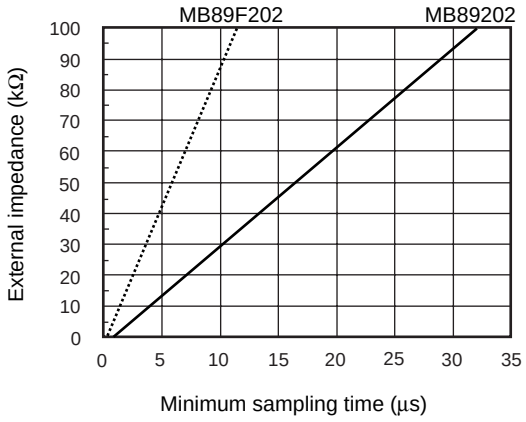
Note : The values are reference values.

	R	C
MB89202	2.2 kΩ (Max)	45 pF (Max)
MB89F202	2.0 kΩ (Max)	16 pF (Max)

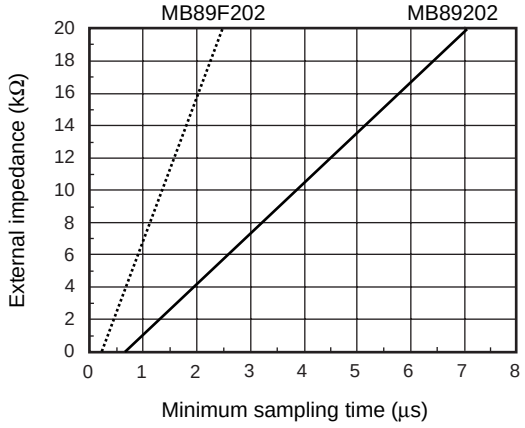
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- **About errors**

As $|V_{CC} - AV_{SS}|$ becomes smaller, values of relative errors grow larger.

6. MB89F202 Flash Memory Program / Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Chip erase time (16 KB)	—	0.5*1	7.5*2	s	Excludes programming prior to erasure
Byte programming time	—	32	3600	µs	Excludes system-level overhead
Program / Erase cycle	10,000	—	—	cycle	

*1: Ta = ＋25 °C, Vcc = 3.0 V, 10,000 cycles

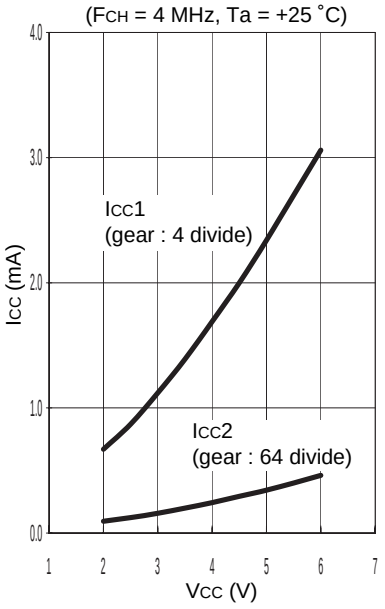
*2: Ta = ＋85 °C, Vcc = 2.7 V, 10,000 cycles

■ EXAMPLE CHARACTERISTICS

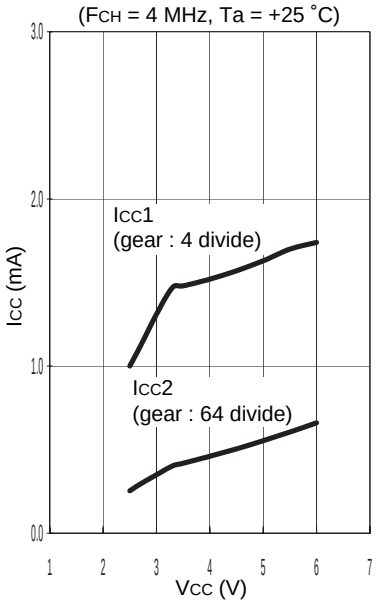
1. Power supply current

- MB89202/F202 : 4 MHz (when external clock are used)

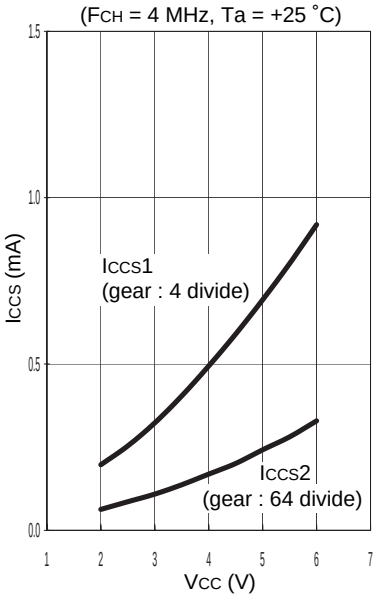
MB89202
Normal operation mode
($I_{CC}1$ – V_{CC}, $I_{CC}2$ – V_{CC})



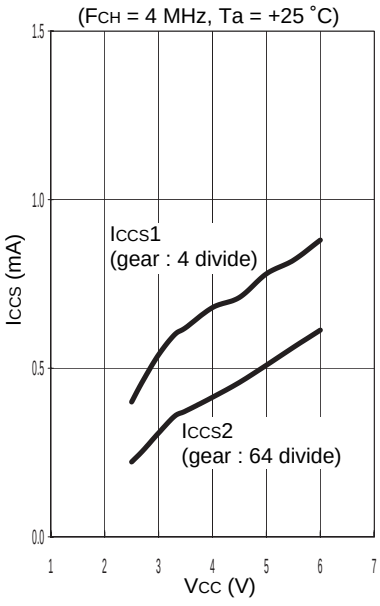
MB89F202
Normal operation mode
($I_{CC}1$ – V_{CC}, $I_{CC}2$ – V_{CC})



MB89202
Sleep mode
($I_{CCS}1$ – V_{CC}, $I_{CCS}2$ – V_{CC})



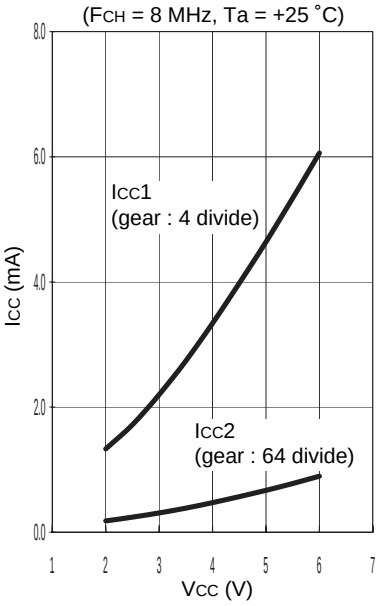
MB89F202
Sleep mode
($I_{CCS}1$ – V_{CC}, $I_{CCS}2$ – V_{CC})



- MB89202/F202 : 8 MHz (when external clock are used)

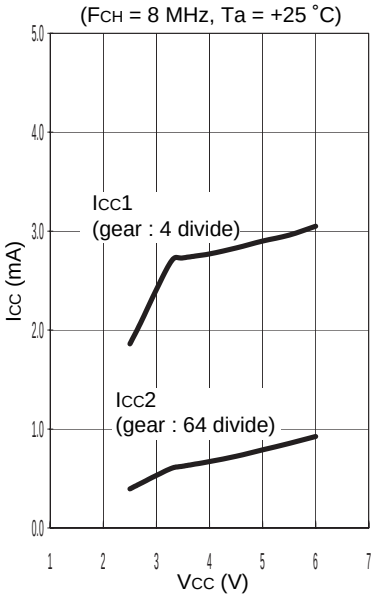
MB89202
Normal operation mode
($I_{CC}1$ – V_{CC}, $I_{CC}2$ – V_{CC})

(F_{CH} = 8 MHz, Ta = +25 ˚C)



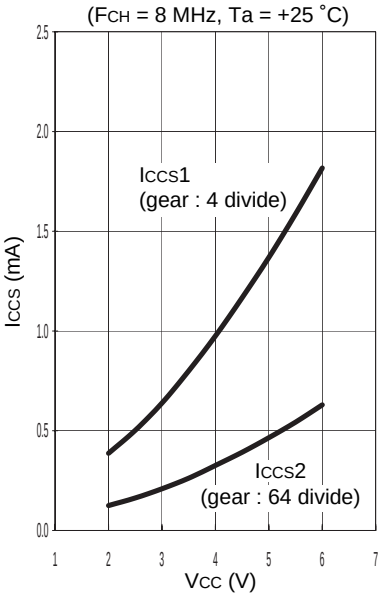
MB89F202
Normal operation mode
($I_{CC}1$ – V_{CC}, $I_{CC}2$ – V_{CC})

(F_{CH} = 8 MHz, Ta = +25 ˚C)



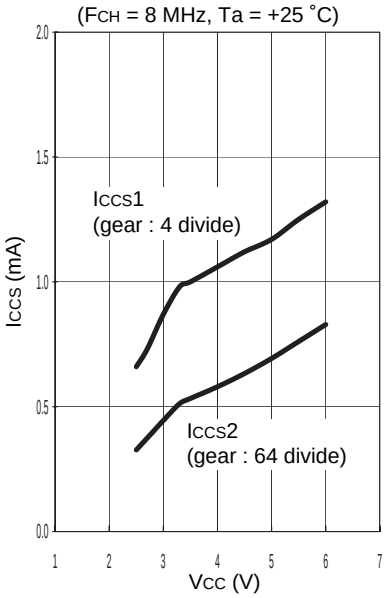
MB89202
Sleep mode
($I_{CCS}1$ – V_{CC}, $I_{CCS}2$ – V_{CC})

(F_{CH} = 8 MHz, Ta = +25 ˚C)



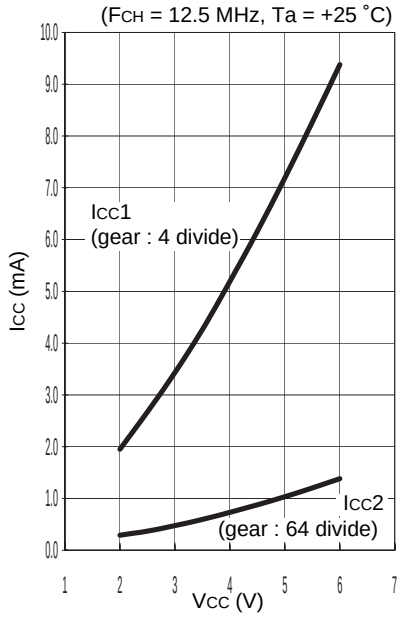
MB89F202
Sleep mode
($I_{CCS}1$ – V_{CC}, $I_{CCS}2$ – V_{CC})

(F_{CH} = 8 MHz, Ta = +25 ˚C)

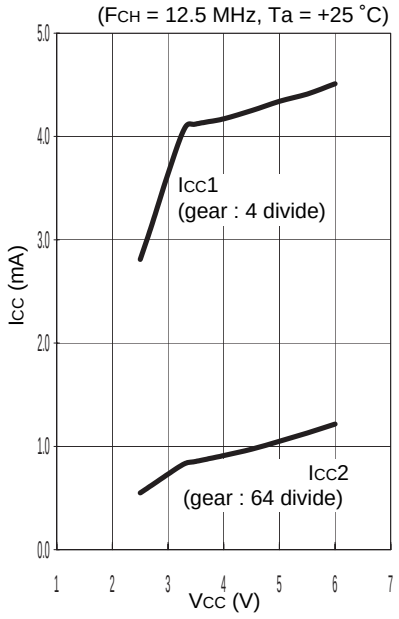


- MB89202/F202 : 12.5 MHz (when external clock is used)

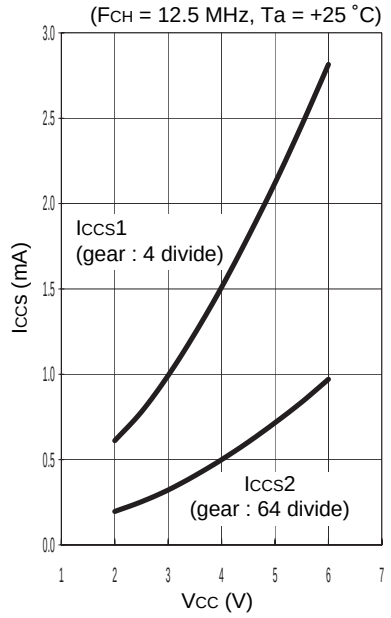
MB89202
Normal operation mode
($I_{CC}1 – V_{CC}$, $I_{CC}2 – V_{CC}$)



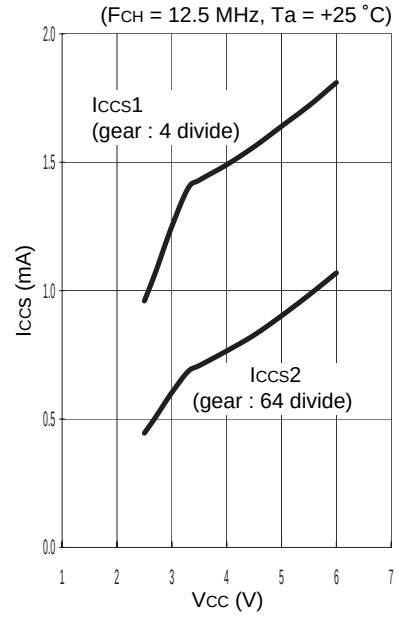
MB89F202
Normal operation mode
($I_{CC}1 – V_{CC}$, $I_{CC}2 – V_{CC}$)



MB89202
Sleep mode
($I_{CCS}1 – V_{CC}$, $I_{CCS}2 – V_{CC}$)



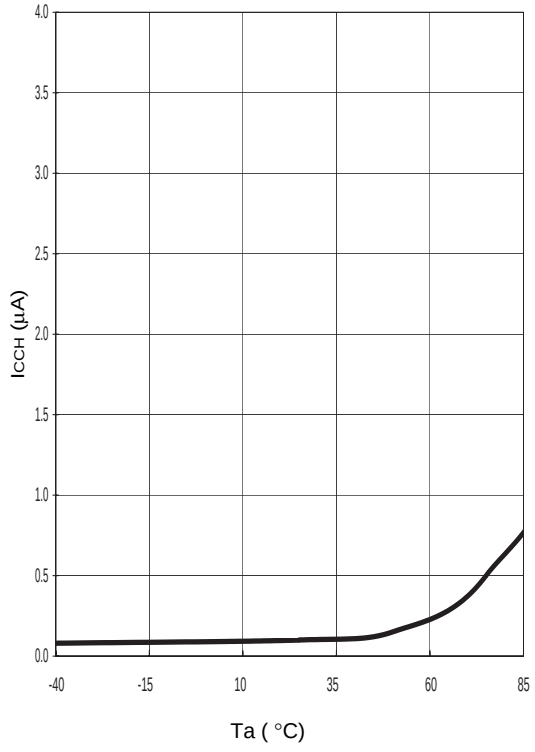
MB89F202
Sleep mode
($I_{CCS}1 – V_{CC}$, $I_{CCS}2 – V_{CC}$)



- MB89202/F202 : 12.5 MHz (when external clock is used)

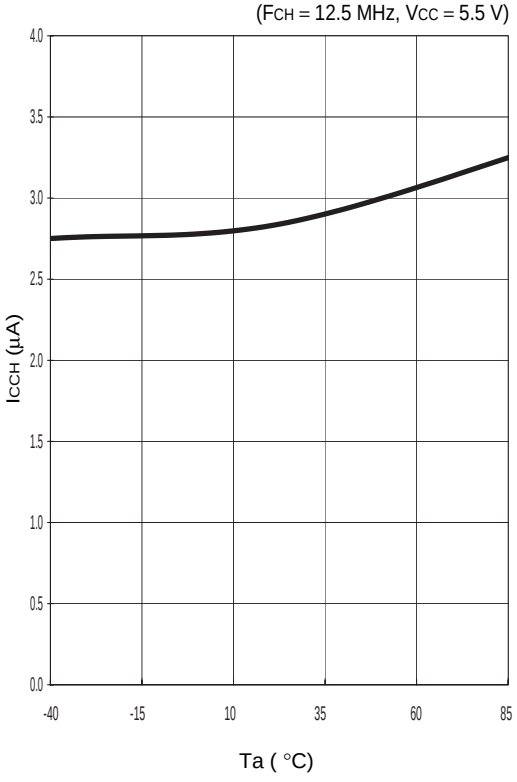
MB89202
Stop mode (I_{CCH} – Ta)

(F_{CH} = 12.5 MHz, V_{CC} = 5.5 V)

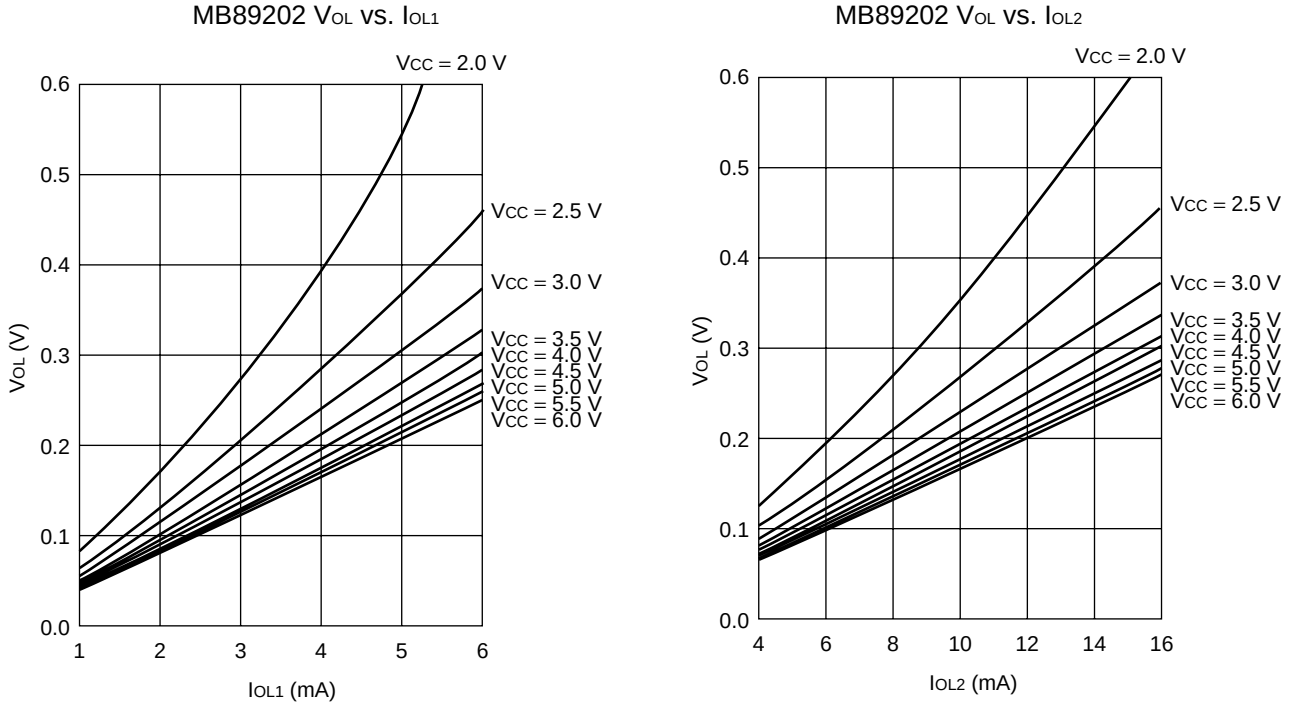


MB89F202
Stop mode (I_{CCH} – Ta)

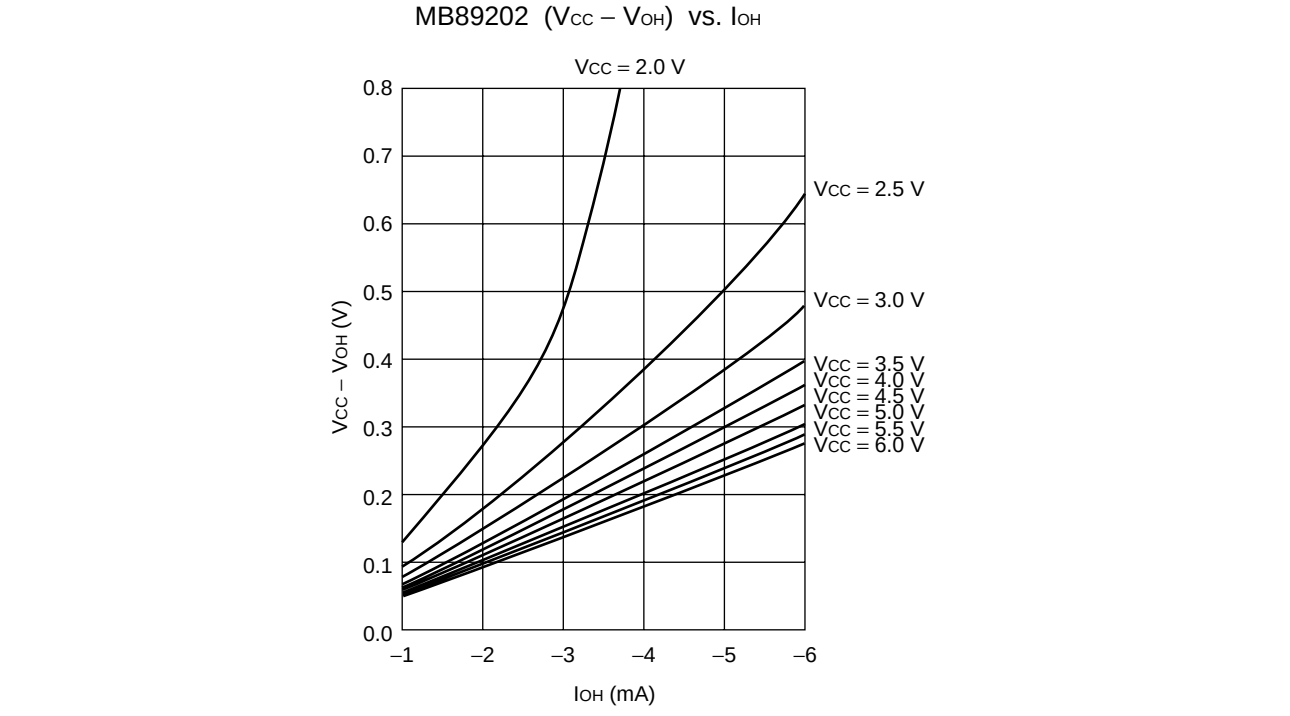
(F_{CH} = 12.5 MHz, V_{CC} = 5.5 V)



2. “L” level output voltage



3. “H” level output voltage



■ MASK OPTIONS

No.	Part number	MB89202	MB89F202	MB89V201
	Specifying procedure	Specify when ordering masking	Specify by part number	
1	Selection of initial value of main clock oscillation settling time* (with F_{CH} = 12.5 MHz) 01 : $2^{14}/F_{CH}$ (Approx.1.31 ms) 10 : $2^{17}/F_{CH}$ (Approx.10.5 ms) 11 : $2^{18}/F_{CH}$ (Approx.21.0 ms)	Selectable	Fixed to $2^{18}/F_{CH}$	Fixed to $2^{18}/F_{CH}$
2	Reset pin output With reset output Without reset output	Selectable	With reset output	With reset output
3	Power on reset selection With power on reset Without power on reset	Selectable	With power on reset	With power on reset

F_{CH} : Main clock oscillation frequency

* : Initial value to which the oscillation settling time bit (SYCC : WT1, WT0) in the system clock control register is set

Note

- Notes on selecting mask option

  Please select “With reset output” by the mask option when power-on reset is generated at the power supply ON, and the device is used without inputting external reset.

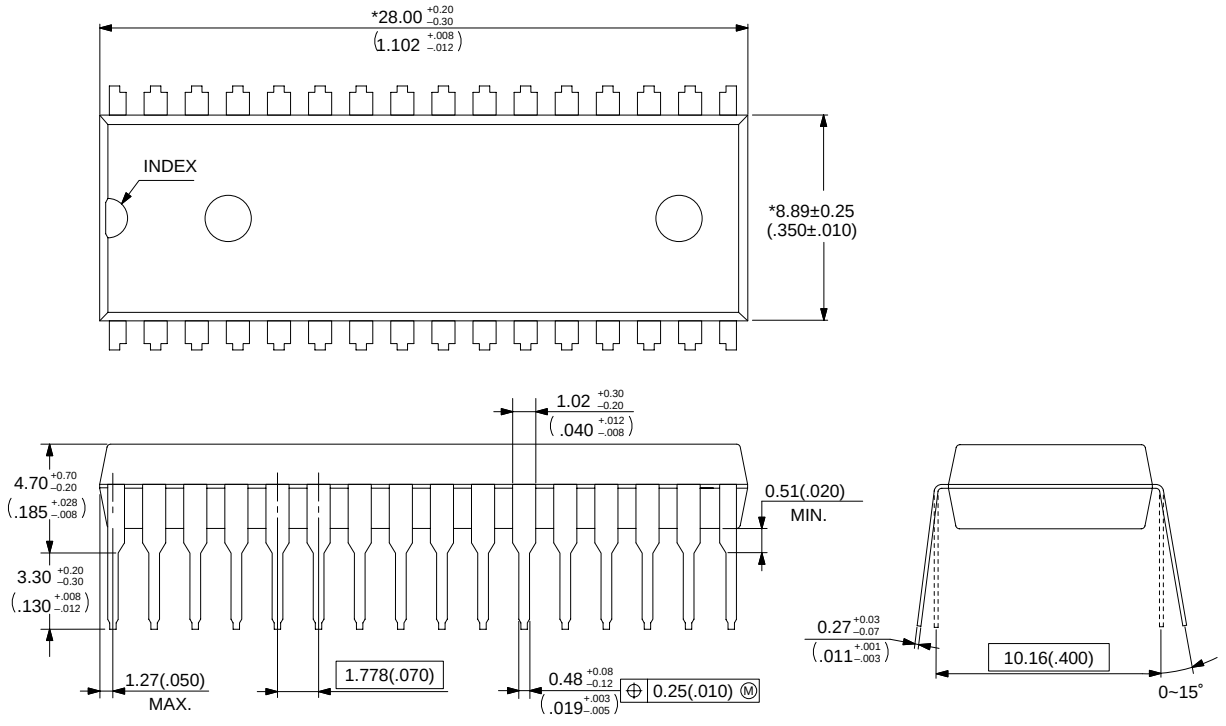
■ ORDERING INFORMATION

Part number	Package	Remarks
MB89202P-SH	32-pin plastic SH-DIP (DIP-32P-M06)	
MB89F202P-SH		
MB89202PFV	34-pin plastic SSOP (FPT-34P-M03)	
MB89F202PFV		
MB89V201PFV	64-pin plastic LQFP (FPT-64P-M03)	

■ PACKAGE DIMENSIONS

32-pin plastic SH-DIP
(DIP-32P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.



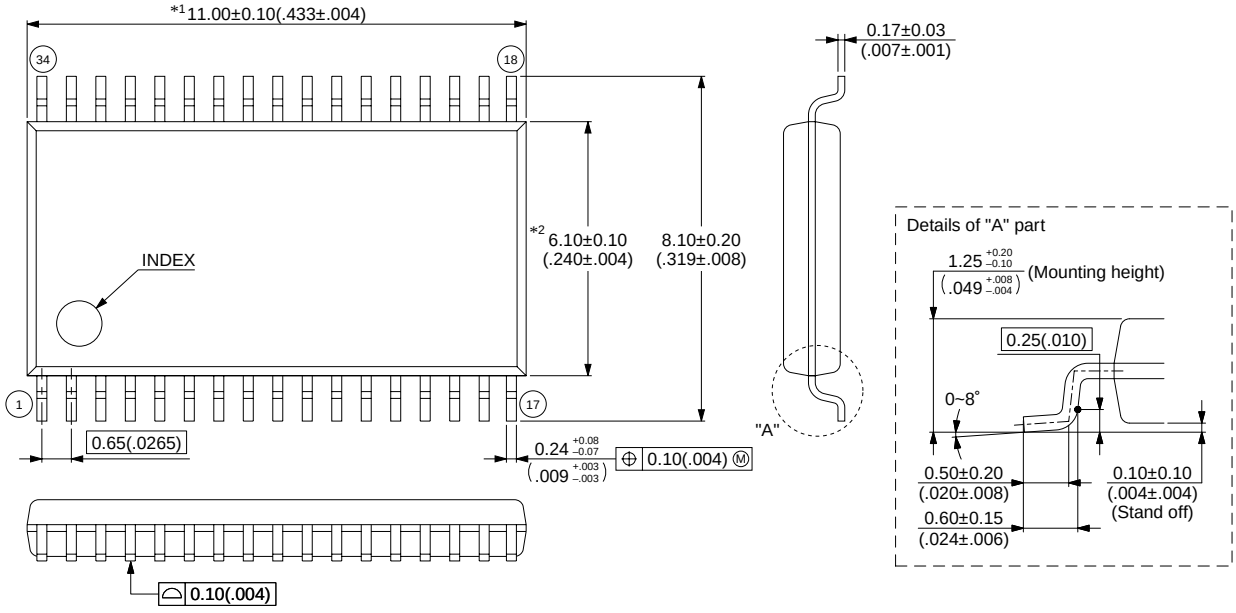
Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

(Continued)

34-pin plastic SSOP
(FPT-34P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

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