AQ112

Ultra-Low Dropout 1A Voltage Regulator

Product Specification | Revision 1.6 | September 13, 2006

General Description

The AQ112 is an ultra-low dropout three terminal voltage regulator, offered in popular fixed options or an adjustable version that can set a precise voltage from 1.22V to 12V with two external resistors.

It drops into the footprint of the popular LM1117 SOT-223 and provides a true 4th pin separated from the output tab which allows a separate bias connection from the pass transistor in order to achieve **enable** and **ultra low dropout** from VIN to VOUT.

The **enable** pin provides a remote turn-off for low power consumption. It draws virtually zero current in shutdown mode and implements Sequential, Ratiometric, or Simultaneous sequencing schemes.

To assure accuracy within 1%, the heart of the AQ112 is a self-correcting AcuRef™ bandgap reference.

On-chip current limit and thermal shutdown with hysteresis protects against any combination of overload and ambient temperature that might cause the junction temperature to exceed safe limits.

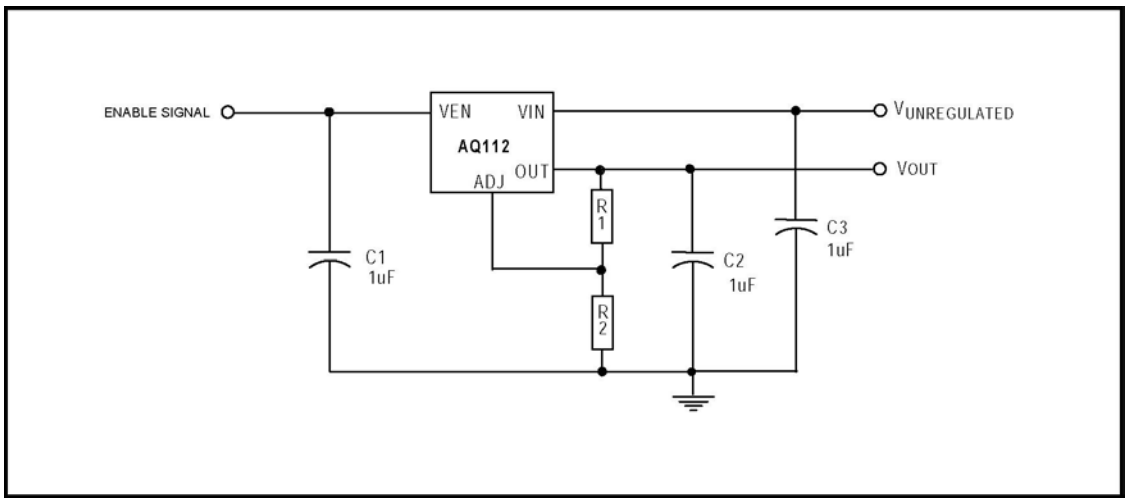
Applications

- Graphic cards
- PC motherboards
- Switching power supply post-regulation
- Telecom equipment
- DVD video player

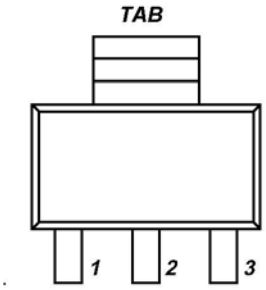
Features

- Ultra Low Dropout (400mV at 1A)
- Enable pin implements sequencing
- Vout tolerance less than **1.5%** over temperature
- Stable with low cost 1uF capacitor
- Thermal protection with hysteresis
- Short circuit protection
- Adjustable output
- The AQ112 is featured in the new **SOT223 4-lead** TetraPack™ package.
- **RoHS compliant** available

Typical Application



Pin Configuration



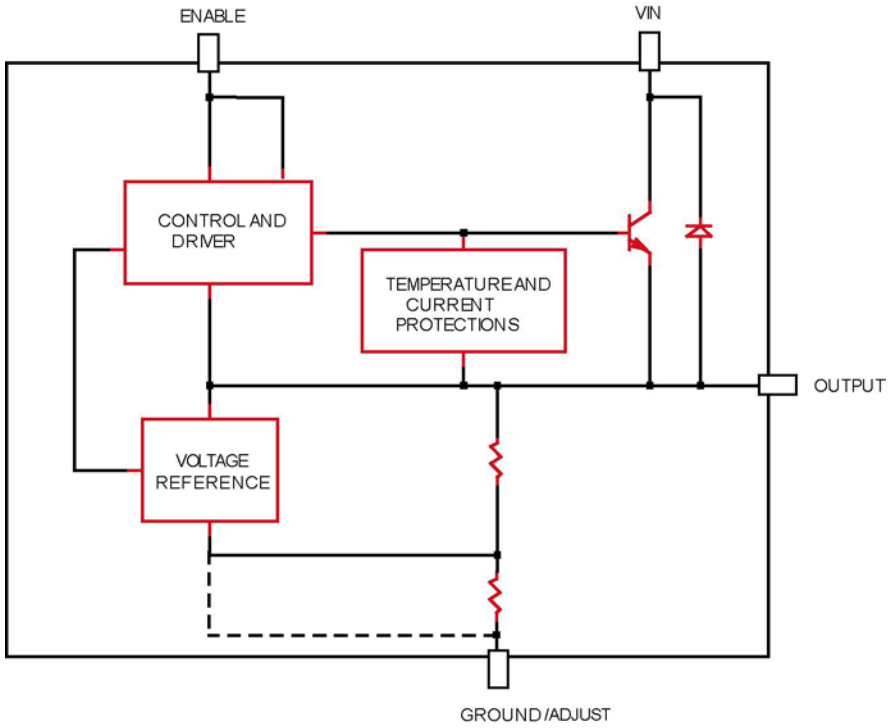
TetraPack™
SOT-223-4

PIN	FUNCTION
1	GND/ADJ
2	Enable
3	VIN
TAB	VOUT

Pin Descriptions

Pin Name	Function
VIN	+ Unregulated Input Voltage, Collector of Pass Transistor
ENABLE	Active high, ENABLE > (0.95V + VOUT), Chip bias circuit supply OFF low, ENABLE < 0.25V
Ground/Adjust	Ground or Adjust pin (Connect to resistive feed back divider)
VOUT	Regulated Output

Functional Block Diagram



Ordering Information

Device	Operating Tj	%Tol	PKG Type	VOUT	Wrap	Ordering Number
AQ112	0C° ≤ 125C°	1.0	SOT-223-4	1.8V	T&R	AQ112CY-S4-18-TR
AQ112	0C° ≤ 125C°	1.0	SOT-223-4	1.8V	T&R	AQ112CY-S4-18-TRL
AQ112	0C° ≤ 125C°	1.0	SOT-223-4	2.5V	T&R	AQ112CY-S4-25-TR
AQ112	0C° ≤ 125C°	1.0	SOT-223-4	2.5V	T&R	AQ112CY-S4-25-TRL
AQ112	0C° ≤ 125C°	1.0	SOT-223-4	3.3V	T&R	AQ112CY-S4-33-TR
AQ112	0C° ≤ 125C°	1.0	SOT-223-4	3.3V	T&R	AQ112CY-S4-33-TRL
AQ112	0C° ≤ 125C°	1.0	SOT-223-4	ADJ	T&R	AQ112CY-S4-AJ-TR
AQ112	0C° ≤ 125C°	1.0	SOT-223-4	ADJ	T&R	AQ112CY-S4-AJ-TRL

Note: The TRL parts are Lead Free and RoHS compliant.

Absolute Maximum Ratings

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under recommended Operating Conditions is not implied. Exposure to "Absolute Maximum Rating" for extended periods may affect device reliability. Use of standard ESD handling precautions is required.

Parameter	Value	Units
Maximum VIN	18	Volts
Maximum VENABLE	18	Volts
Power Dissipation (Internally limited)		
Maximum Junction Temperature	150	°C
Operating Junction Temperature Range	0 to 125	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 4sec.) SOT- 223 package	300	°C

Thermal Management

Thermal Resistance (Junction to TAB)	Typical Value	Units
SOT-223	15	°C/W

Thermal Resistance (Junction to Ambient)	Typical Value	Units
SOT-223 (tab soldered to 1 in^2 1 oz. copper PCB)	46	°C/W

Electrical Specifications

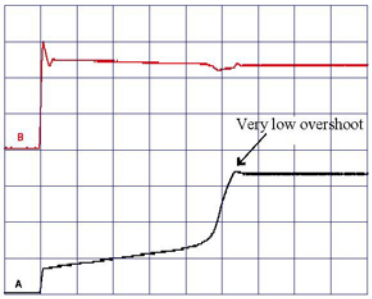
Electrical characteristics are guaranteed over the full temperature range 0ºC <Tj< 125ºC. Ambient temperature must be de-rated based upon power dissipation and package thermal characteristics. Unless otherwise specified: V_{IN} = V_{EN} = (V_{OUT} + 1.5V), I_{OUT} = 10 mA, Tj = 25C. All values in **bold** are over the full temperature range.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VOUT	Output Voltage (1)		-1	V_{OUT}	+1	%
		0°C ≤Tj ≤ 125°C	**-1.5**	V_{OUT}	**+1.5**	%
LNREG	Line Regulation (1)	ΔV_{IN} = V_{OUT} + (1.5V to 10V)		0.035	**0.2**	%
LDREG	Load Regulation (1)	ΔI_{OUT} = (10mA to 1 Amp)		0.2	**0.4**	%
VD	Drop out Voltage (1, 2)	I_{OUT} = 100 mA		50	**80**	mV
		I_{OUT} = 500 mA		200	**250**	mV
		I_{OUT} = 1A		350	**400**	mV
ISC	Current Limit (1)	V_{EN}-V_{OUT} = 2V	1.1	1.5		A
IQ	Quiescent Current	V_{EN} = 5V		7.0	9.0	mA
		0°C ≤Tj ≤ 125°C			**10.0**	mA
VIL	Enable Pin Voltage (OFF)	With respect to GND	**0.25**	0.45		V
VIH	Enable Pin Voltage (ON)	With respect to V_{OUT}		0.92	**0.95**	V
I_{EN}ON	Enable Current ON	I_{OUT} = 10 mA		0.3	**0.5**	mA
		I_{OUT} = 500 mA		2.5	**5.0**	mA
		I_{OUT} = 1A		5.0	**10.0**	mA
VADJ	Reference Voltage	Note (5)	1.208	1.220	1.232	V
		0°C ≤Tj ≤ 125°C	**1.202**		**1.238**	V
IADJ	Adjust Pin Current (5)			20	**40**	µA
Δ IADJ	Adjust Pin Current (5) Change	10mA ≤ I_{OUT}≤ 1Amp 1.4 ≤ V_{IN} ≤ 18V		0.2	**5.0**	µA
I_{QMIN}	Minimum Load Current (5)	To Maintain regulation		0.5	**2.0**	mA
TC	Temperature Coefficient			**0.005**		%/°C
TS	Temperature Stability			**0.5**		%/°C
V_N	RMS Output Noise (3)			0.003		% V_{OUT}
PSRR	Ripple Rejection Ratio (4)	Vin = 5V	**60**	72		dB
TSD	Thermal Shutdown	Junction Temperature		**150**		°C
TSD_{HYST}	TSD Hysteresis			**25**		°C

Notes: (1) Low duty cycle pulse testing with Kelvin connections required.
(2) Measure (V_{IN} - V_{OUT}) when ΔV_{OUT}, OR ΔV_{REF} = 1%
(3) Bandwidth of 10Hz to 10kHz
(4) 120Hz input ripple
(5) Adjustable version only

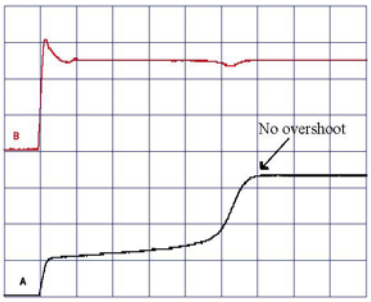
Typical Response Curves

Output Overshoot With Line, 500mA Load



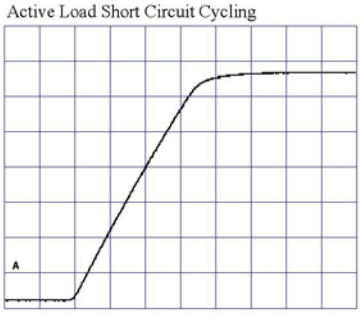
Input Step (B) 0-5V
Output Response (A) 0-3.3V with 500mA load
Horizontal: 100us/div

Output Overshoot With Line, No Load



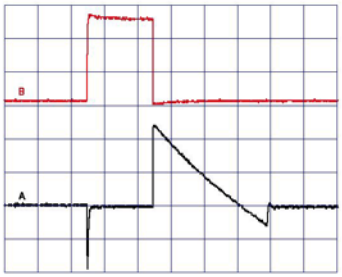
Input Step (B) 0-5V
Output Response (A) 0-3.3V Zero Load
Horizontal: 20us/div

Active Load Short Circuit Cycling



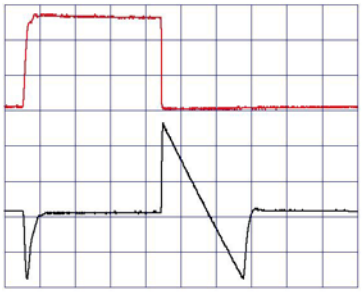
Output Response (A)
Low duty cycle, repetetive, no thermal limit intervention
Horizontal: 10us/div Vertical: 500mV/div

Load Step 0mA to 500mA



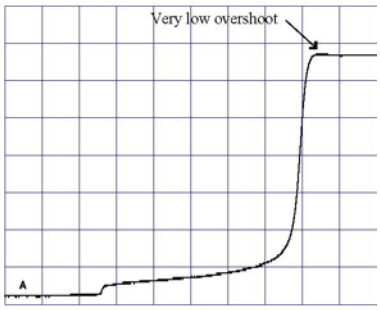
Load Step (B) 0mA to 500mA to 0mA
Output Response (A) 50mV/div (AC coupled)
Horizontal: 500us/div

Load Step 10mA to 500mA



Load Step (B) 10mA to 500mA to 10mA
Output Response (A) 50mV/div (AC coupled)
Horizontal: 100us/div

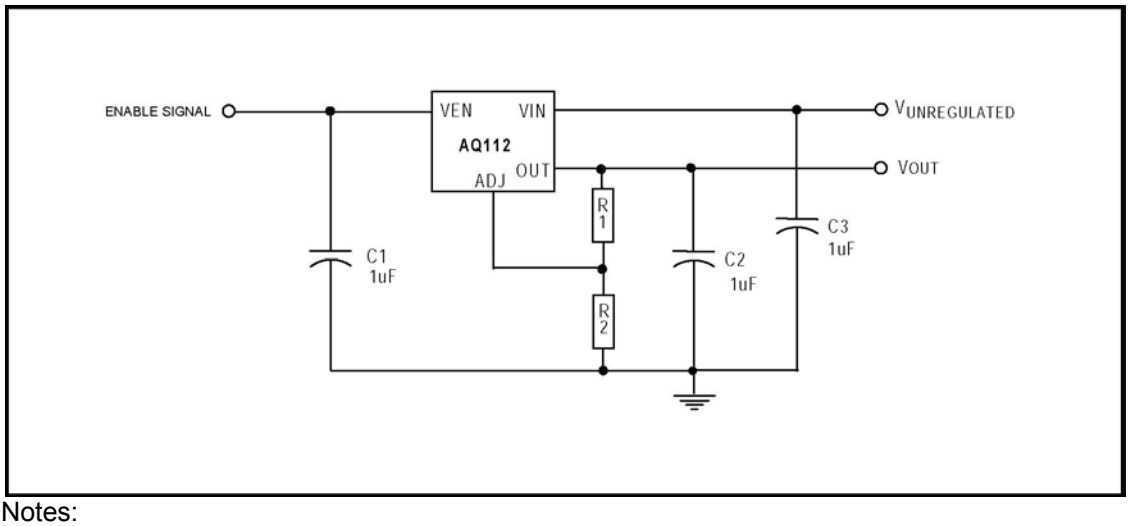
Short Circuit Removal (to no load)



Output Response (A) 0-3.3V
Output grounded to open circuit, single shot
Horizontal: 200us/div Vertical: 500mV/div

Application Notes

1. Typical Application



Notes:

1. Output voltage is 1.22V * (R2 +R1)/R1
2. Input and output capacitors should be located close to the device.
3. The AQ112 will remain stable with C1 and C2 as low as 1.0 µF. Overall transient performance is improved with increased capacitance and the addition of C3.
4. The output is fully enabled when Enable is 950 mV above the expected VOUT. EN may be driven by either a digital or analog signal to control either turn-on time or to give full control of risetime.
5. Enable, tied to any separate source >0.95V + VOUT, will insure Ultra-low drop out voltage (400mV@ 1A) from VIN to VOUT. Or, Enable, tied to Vin will support a low drop out voltage (0.95V).

2. Stability

An Enable capacitor is recommended. A 1.0 µF capacitor on VIN is a suitable input bypass for almost all applications. A larger capacitor is also suitable.

In the adjustable version the “adjust” terminal can be bypassed to ground with a bypass capacitor (C_{ADJ}) to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. At any ripple frequency, the impedance of the C_{ADJ} should be less than R1 (being R1 the resistor between the output and the adjust pin) to prevent the ripple from being amplified:

$$Z = 1/(2\pi * f_{RIPPLE} * C_{ADJ}) < R1$$

R1 is normally in the range of 1KΩ.

The output capacitor is critical in maintaining regular stability. The AQ1541 is stable with an output capacitor greater than 1.0 µF. Of course any increase of the output capacitor will merely improve the loop stability and the load transient response. In the case of the adjustable regulator, when the C_{ADJ} is used, a larger output capacitance may be required. The capacitor C3 may also be necessary if large ripple is present on the VIN line. Tantalum Capacitors exhibit the best stability over a wide range of loads and are recommended.

3. Output Voltage

The AQ112 adjustable version develops a 1.22V reference voltage between the output and the adjust pin terminal. This voltage is applied across the resistor R1 to generate a constant current (I1). The current from the adjust terminal could introduce error to the output, but since it is very small (< 20μA) compared with the current I1 and very constant with line and load changes, the error can be ignored. The constant current I1 then flows through resistor R2 and sets the output voltage to the desired level.

For fixed voltages the resistor R1 and R2 are integrated inside the devices.

The AQ112 regulates the voltage that appears between its output and ground pins or between its output and adjust pins. In some cases, line resistances can introduce errors to the voltage across the load. To obtain the best load regulation a few precautions are needed. For example it is important to minimize the line resistances to the load, so the load itself should be tied directly to the output terminal on the positive side and directly to the ground terminal on the negative side.

When the adjustable regulator is used, the best performance is obtained with the positive side of the resistor R1 tied directly to the output terminal of the regulator rather than near the load. This will eliminate line drops from appearing effectively in series with the reference and degrading regulation. In addition the ground side of the resistor R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation. A capacitor (470pF) between the ADJ pin and system ground will enhance stability.

4. Enable/Sequencing

The AQ112 provides an enable function. The EN pin has to be at least 950 mV higher than the output voltage for the device to be fully turned on. When the voltage of the EN pin is low the device is in shutdown mode and it will not draw any current from the V_{IN} terminal.

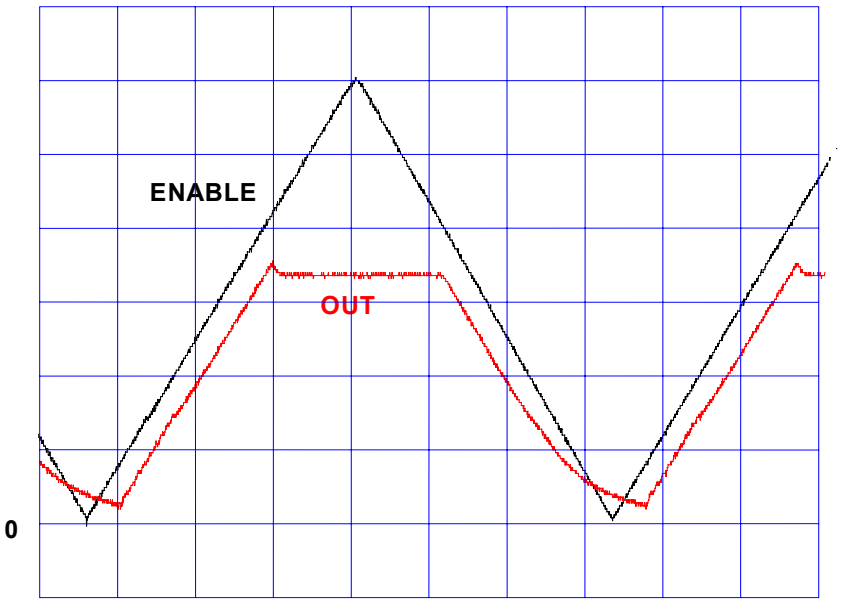


FIG.2 ENABLE 0-5V, Output follows to 3.3V out
(1V/div vertical, 200us/div horizontal)

In addition the enable function includes a sequencing feature, because when the enable pin ramps in voltage the output voltage follows (it will be around 900 mV less than the enable voltage until it reaches the regulation voltage) as shown in Fig. 2 above.

In applications where multiple regulated supply rails are required, it is often required that the relationship between the various supply voltages be controlled during start-up and shutdown. To this end, the AQ112 allows for an analog control of the output voltage via the ENABLE pin. This allows for sequential, ratio-metric and simultaneous sequencing schemes.

4. Protection Diodes

Unlike older regulators, the AQ112 family does not need any protection diodes between the adjustment pin and output or from the output to the input to prevent over-stressing the die. Internal resistors are limiting the internal current paths on the adjustment pin. Therefore, even with capacitors on the adjustment pin, no protection diode is needed to ensure device safety under short circuit conditions. External diodes between the input and output are not usually needed. Only if high value output capacitors are used (> 1000uF) and the input is instantaneously shorted to ground, can damage occur.

5. Thermal Considerations

When an integrated circuit operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits in order to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed circuit board, and eventually to the ambient environment.
The AQ112 regulators have internal thermal shutdown to protect the device from over-heating. Under all possible operating conditions, the junction temperature of the AQ112 must be lower than 125°C. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application.
To determine if a heatsink is needed, the power dissipated by the regulator, P_D, must be calculated:

$$P_D = (V_C - V_{OUT})\, I_L$$

where the I_L is the load current.

The next parameter which must be calculated is the maximum allowable temperature rise, T(max):

$$T(max) = T_J(max) - T_A(max)$$

where T_J(max) is the maximum allowable junction temperature (125°C), and T_A(max) is the maximum ambient temperature which will be encountered in the application.
Using the calculated values for T(max) and P_D, the maximum allowable value for the junction to ambient thermal resistance (θ_{JA}) can be calculated:

$$\theta_{JA} = T(max) / P_D$$

If the maximum allowable value for θ_{JA} is found to be greater than the junction to ambient thermal resistance for the package used, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements.

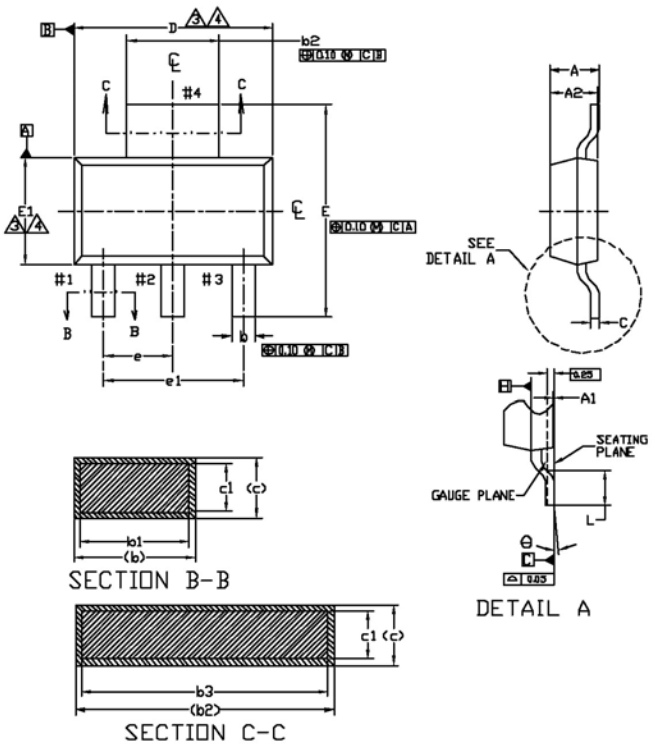
7. Ultra low Dropout Operation

The AQ112 allows for ultra low dropout operation by connecting the pin ENABLE to >0.95V + Vout. This results in a dropout of 100 mV at 150 mA of load current, between Vin and VOUT.

This feature is important when the supply voltage is dropping near the output regulated voltage. Furthermore if the voltage dropout is low, the internal power dissipation is also reduced and the thermal requirements of the device are less stringent.

Package Dimensions

SOT223-4 TetraPack™



Note :

1 DIMENSION ARE IN MILLIMETERS

2 DIMENSIONS b1, b3, AND c1 APPLY TO BASE METAL ONLY. DIMENSIONS b, b2, AND c APPLY TO PLATED LEAD. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08mm AND 0.15mm FROM THE LEAD TIP.

3 DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

4 DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.

5 CONTROLLING DIMENSION IS MILLIMERTER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT

SYMBOL	ALL DIMENSIONS IN MILLIMETERS		ALL DIMENSIONS IN INCH	
	MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
A	1.57	1.75	0.062	0.069
A1	0.02	0.10	0.0008	0.004
A2	1.55	1.65	0.061	0.065
b	0.66	0.84	0.026	0.033
b1	0.60	0.79	0.024	0.031
b2	2.90	3.10	0.114	0.122
b3	2.84	3.05	0.112	0.120
c	0.23	0.33	0.009	0.013
c1	0.23	0.33	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.30 BASIC		0.090 BASIC	
e1	4.60 BASIC		0.180 BASIC	
L	0.90	–	0.035	–
θ	0°	8°	0°	8°

Contact Information

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