A DIVISION OF CIRRUS LOGIC

CS4923

Dolby® Digital Audio Decoder

Features

- Dolby Digital (5.1-channel) decompression
- Dolby Surround Pro Logic® decoder
- Dolby bass manager and crossover filters
- Flexible 6-channel master or slave output
- IEC60958/61937 transmitter for compressed-data or linear-PCM output
- IEC60958/61937 input for compressed-data or linear-PCM input
- Large variable input and output buffers
- DAC clock via analog phase-locked loop
- Dedicated byte wide or serial host interface
- Multiple compressed data input modes
- PES layer decode for A/V synchronization
- 96-kHz-capable PCM I/O, master or slave
- Optional external memory and auto-boot capability
- +3.3-V CMOS low-power, 44-pin package

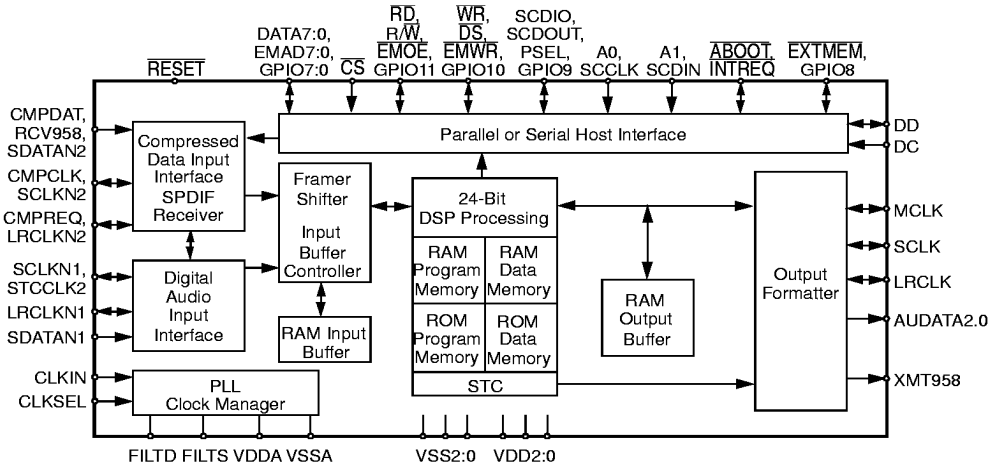
Description

The CS4923 is the first device in a new family of higher-performance digital audio decoders targeted for decompression of multichannel digital audio, such as Dolby Digital, MPEG-2 Surround, and DTS. The CS4923 provides a complete and flexible solution for Dolby Digital audio decoding in laser-disc players, DVD movie players, stereo receivers, out-board decoders, HDTV sets, head-end decoders, set-top boxes, and similar products. The CS4923 is a performance- and feature-enhanced version of the CS4922 audio decoder IC.

Cirrus Logic's Crystal Semiconductor Products Division provides a complete set of audio decoder and auxiliary audio DSP application programs for various applications. For all complementary analog and digital audio I/O, Crystal Semiconductor also provides a complete set of high-quality audio peripherals including: multimedia CODECs, stereo A/D and D/A converters, SPDIF/IEC60958/61937 interfaces, wavetable and FM synthesizers. For example, the CS4226 CODEC provides the following capabilities in one chip: digital receiver, stereo A/D converters, and six 20-bit DACs. Also available is the CRD4923, a reference design for the CS4923 and CS4226.

ORDERING INFORMATION

CS4923xx-CL	44-pin PLCC (xx = ROM revision)
CRD4923	Reference design
CDB4923	Evaluation board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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ABSOLUTE MAXIMUM RATINGS

(AGND, DGND = 0 V; all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Unit
DC power supplies:	Positive digital	VD+	−0.3	3.63	V
	Positive analog	VA+	−0.3	3.63	V
	||VA+| − |VD+||		-	0.4	V
Input current, any pin except supplies		I_{in}	-	±10	mA
Digital input voltage		V_{IND}	−0.3	(VD+) + 0.4	V
Ambient operating temperature (power applied)		T_{Amax}	−55	125	°C
Storage temperature		T_{stg}	−65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0 V; all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Unit
DC power supplies:	Positive digital	VD+	3.13	3.3	3.47	V
	Positive analog	VA+	3.13	3.3	3.47	V
	||VA+| − |VD+||		-	-	0.4	V
Ambient operating temperature		T_A	0	-	70	°C

DIGITAL D.C. CHARACTERISTICS

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.25	-	-	V
Low-level input voltage	V_{IL}	-	-	0.8	V
High-level output voltage at I_O = −4.0 mA	V_{OH}	VD × 0.9	-	-	V
Low-level output voltage at I_O = 4.0 mA	V_{OL}	-	-	VD × 0.1	V
Input leakage current	I_{in}	-	-	1.0	µA

POWER SUPPLY CHARACTERISTICS

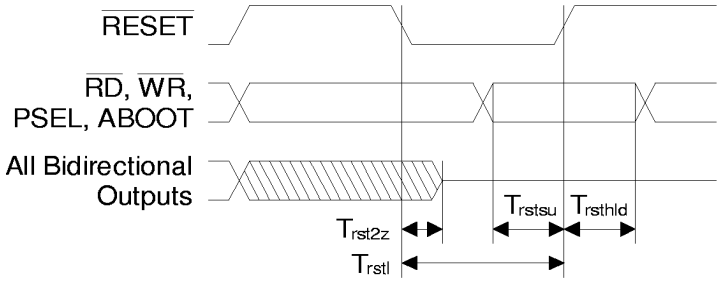
(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

Parameter		Symbol	Min	Typ	Max	Unit
Power supply current:	Digital operating VSS, VDD		-	225	360	mA
	Analog operating VSSA, VDDA		-	25	35	mA

SWITCHING CHARACTERISTICS—$\overline{\text{RESET}}$

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

Parameter	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ minimum pulse width low	T_{rstl}	100	-	ns
All bidirectional pins high-Z after $\overline{\text{RESET}}$ low	T_{rst2z}	-	50	ns
Configuration bits setup before $\overline{\text{RESET}}$ high	T_{rstsu}	50	-	ns
Configuration bits hold after $\overline{\text{RESET}}$ high	T_{rsthld}	15	-	ns

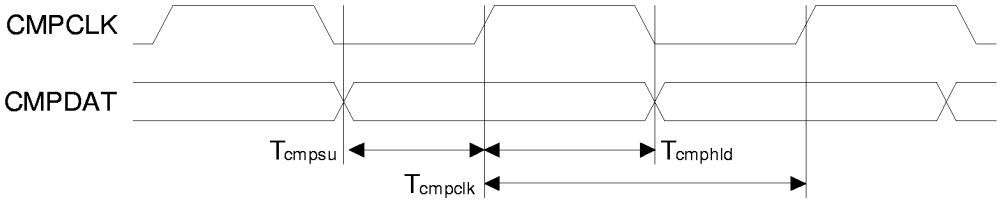


$\overline{\text{RESET}}$ Timing

SWITCHING CHARACTERISTICS—CMPDAT, CMPCLK

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

Parameter	Symbol	Min	Max	Unit
Serial compressed data clock CMPCLK period	T_{cmpclk}	37	-	ns
CMPDAT setup before CMPCLK high	T_{cmpsu}	5	-	ns
CMPDAT hold after CMPCLK high	T_{cmphld}	3	-	ns

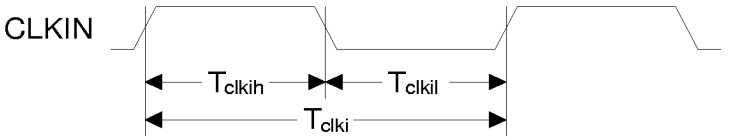


Serial Compressed Data Timing

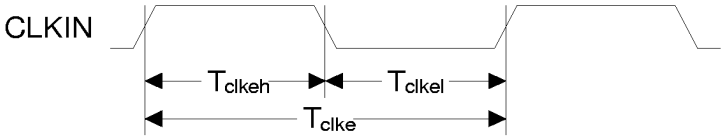
SWITCHING CHARACTERISTICS—CLKIN, MCLK

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

Parameter	Symbol	Min	Max	Unit
CLKIN period for internal DSP clock mode	T_{clki}	33	3800	ns
CLKIN high time for internal DSP clock mode	T_{clkih}	40	60	%
CLKIN low time for internal DSP clock mode	T_{clkil}	40	60	%
CLKIN period for external DSP clock mode	T_{clke}	20	25	ns
CLKIN high time for external DSP clock mode	T_{clkeh}	40	60	%
CLKIN low time for external DSP clock mode	T_{clkel}	40	60	%



CLKIN with CLKSEL = VSS = PLL Enable

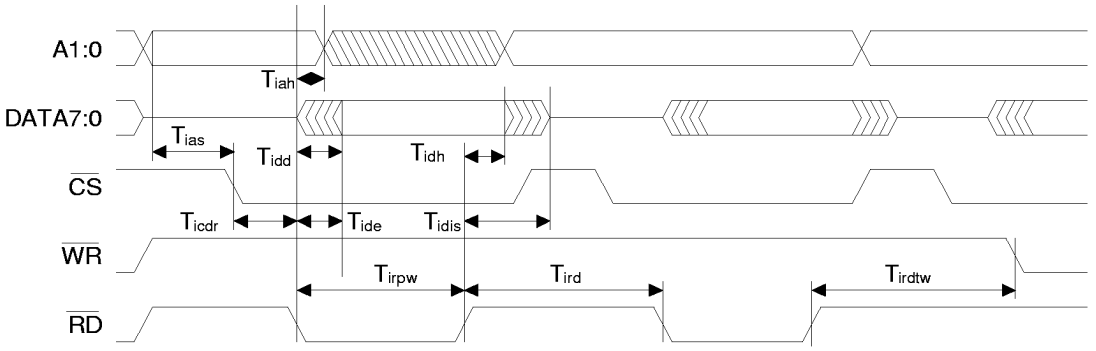


CLKIN with CLKSEL = VDD = PLL Bypass

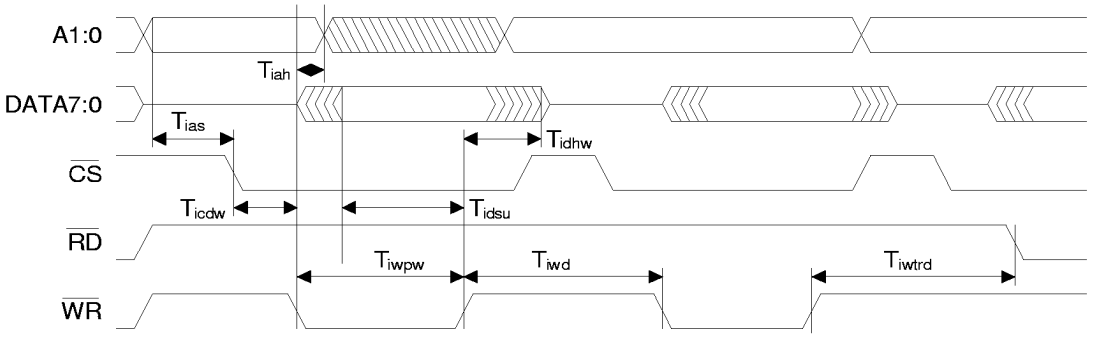
SWITCHING CHARACTERISTICS—INTEL® HOST MODE

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

Parameter	Symbol	Min	Max	Unit
Address valid before $\overline{CS}$ or $\overline{RD}$ low	T_{ias}	5	-	ns
Delay between $\overline{RD}$ then $\overline{CS}$ low or $\overline{CS}$ then $\overline{RD}$ low	T_{icdr}	0	∞	ns
Data valid after $\overline{CS}$ and $\overline{RD}$ low	T_{idd}	-	20	ns
Read pulse width	T_{irpw}	25	-	ns
Data hold time after $\overline{CS}$ or $\overline{RD}$ high	T_{idh}	5	-	ns
Data high-Z after $\overline{CS}$ or $\overline{RD}$ high	T_{idis}	-	15	ns
$\overline{CS}$ or $\overline{RD}$ high to $\overline{CS}$ and $\overline{RD}$ low for next read	T_{ird}	40	-	ns
$\overline{CS}$ or $\overline{RD}$ high to $\overline{CS}$ and $\overline{WR}$ low for next write	T_{irdtw}	40	-	ns
Address hold time after $\overline{CS}$ and $\overline{RD}$ low or $\overline{CS}$ and $\overline{WR}$ low	T_{iah}	5	-	ns
Delay between $\overline{WR}$ then $\overline{CS}$ low or $\overline{CS}$ then $\overline{WR}$ low	T_{icdw}	0	∞	ns
Data valid before end of write	T_{idsu}	20	-	ns
Write pulse width	T_{iwpw}	25	-	ns
Data hold after $\overline{CS}$ or $\overline{WR}$ high	T_{idhw}	5	-	ns
$\overline{CS}$ or $\overline{WR}$ high to $\overline{CS}$ and $\overline{RD}$ low for next read	T_{iwtrd}	40	-	ns
$\overline{CS}$ or $\overline{WR}$ high to $\overline{CS}$ and $\overline{WR}$ low for next write	T_{iwd}	40	-	ns



Intel Parallel Host Mode Read Cycle

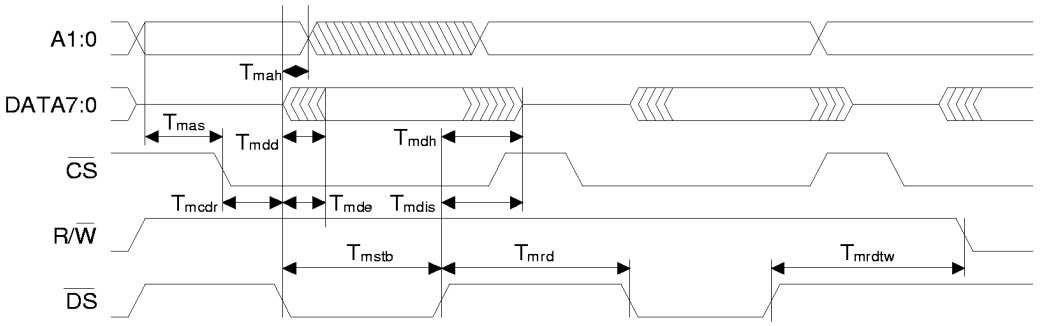


Intel Parallel Host Mode Write Cycle

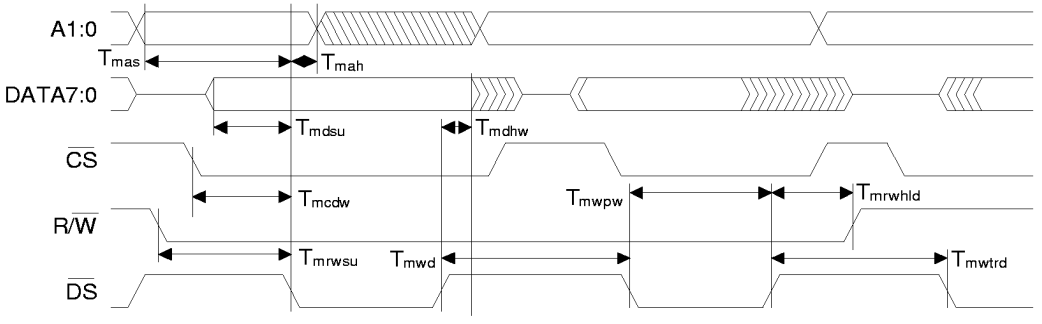
SWITCHING CHARACTERISTICS—MOTOROLA® HOST MODE

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

Parameter	Symbol	Min	Max	Unit
Address valid before $\overline{CS}$ or $\overline{DS}$ low	T_{mas}	5	-	ns
Delay between $\overline{DS}$ then $\overline{CS}$ low or $\overline{CS}$ then $\overline{DS}$ low	T_{mcdr}	0	∞	ns
Data valid after $\overline{CS}$ and $\overline{DS}$ low with R/$\overline{W}$ high	T_{mdd}	-	20	ns
$\overline{CS}$ and $\overline{DS}$ minimum pulse width	T_{mstb}	25	-	ns
Data hold time after $\overline{CS}$ or $\overline{DS}$ high or R/$\overline{W}$ low after read	T_{mdh}	5	-	ns
Data high-Z after $\overline{CS}$ or $\overline{DS}$ high or R/$\overline{W}$ low after read	T_{mdis}	-	15	ns
$\overline{CS}$ or $\overline{DS}$ high to $\overline{CS}$ and $\overline{DS}$ low for next read	T_{mrd}	40	-	ns
$\overline{CS}$ or $\overline{DS}$ high to $\overline{CS}$ and $\overline{DS}$ low for next write	T_{mrdtw}	40	-	ns
Address hold time after $\overline{CS}$ and $\overline{DS}$ low	T_{mah}	5	-	ns
Delay between $\overline{DS}$ then $\overline{CS}$ low or $\overline{CS}$ then $\overline{DS}$ low	T_{mcdw}	0	∞	ns
Data valid before $\overline{CS}$ and $\overline{DS}$ low	T_{mdsu}	20	-	ns
$\overline{CS}$ or $\overline{DS}$ minimum pulse width	T_{mwpw}	25	-	ns
R/$\overline{W}$ setup before $\overline{CS}$ or $\overline{DS}$ low	T_{mrwsu}	5	-	ns
R/$\overline{W}$ hold time after $\overline{CS}$ or $\overline{DS}$ high	T_{mrwhld}	5	-	ns
Data hold after $\overline{CS}$ or $\overline{DS}$ high	T_{mdhw}	5	-	ns
$\overline{CS}$ or $\overline{DS}$ high to $\overline{CS}$ and $\overline{DS}$ low with R/$\overline{W}$ high for next read	T_{mwtrd}	40	-	ns
$\overline{CS}$ or $\overline{DS}$ high to $\overline{CS}$ and $\overline{DS}$ low for next write	T_{mwd}	40	-	ns



Motorola Parallel Host Mode Read Cycle



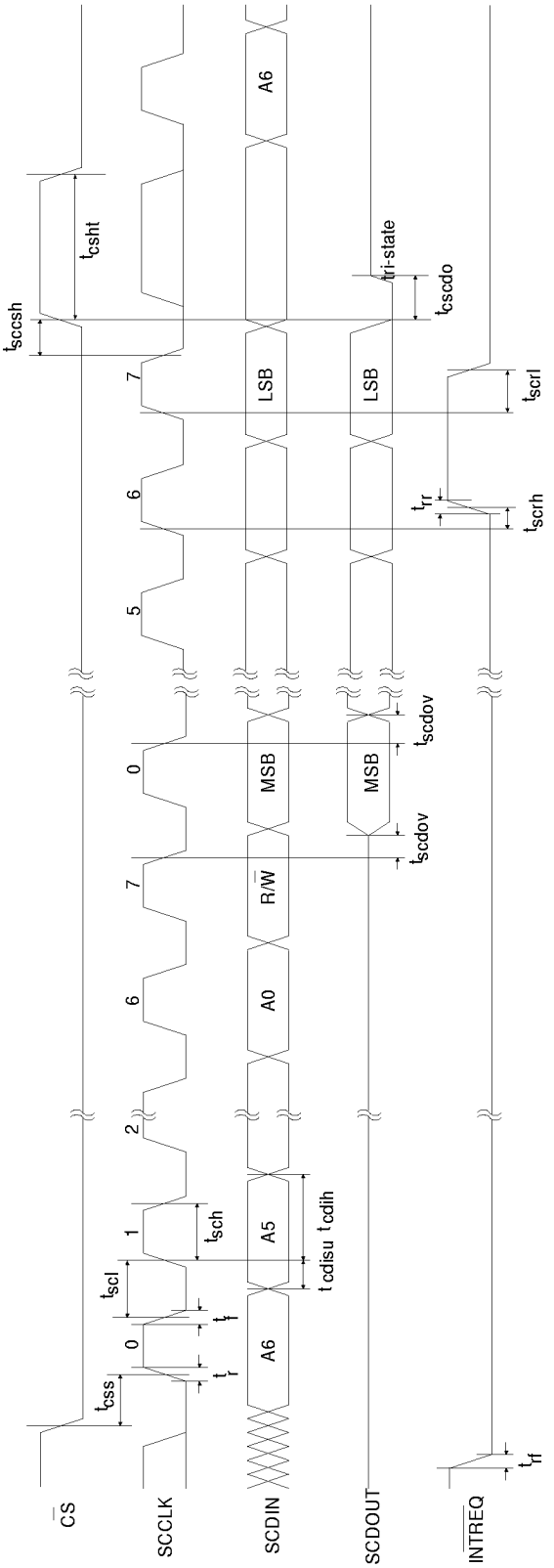
Motorola Parallel Host Mode Write Cycle

SWITCHING CHARACTERISTICS—CONTROL PORT

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20 pF)

Parameter		Symbol	Min	Max	Units
SPI Mode					
SCCLK clock frequency	(Slow mode) (Fast mode)	f_{sck} f_{sck}	- -	350 2000	kHz
$\overline{CS}$ falling to SCCLK rising	(Slow mode)	t_{css}	20	-	ns
Rise time of both SCDIN and SCCLK lines	(Slow mode)	t_r	-	50	ns
Fall time of both SCDIN and SCCLK lines	(Slow mode) (Fast mode)	t_f t_f	- -	300 50	ns ns
SCCLK low time	(Slow mode) (Fast mode)	t_{scl} t_{scl}	1100 150	- -	ns ns
SCCLK high time	(Slow mode) (Fast mode)	t_{sch} t_{sch}	1100 150	- -	ns ns
Setup time SCDIN to SCCLK rising	(Slow mode) (Fast mode)	t_{cdisu}	250 50	- -	ns ns
Hold time SCCLK rising to SCDIN	(Note 1)	t_{cdih}	50	-	ns
Transition time from SCCLK to SCDOUT valid	(Note 2)	t_{scdov}	-	40	ns
Time from SCCLK rising to $\overline{INTREQ}$ rising	(Note 2)	t_{scrh}	-	200	ns
Rise time for $\overline{INTREQ}$	(Note 3)	t_{rr}	-	(Note 5)	ns
Fall time for $\overline{INTREQ}$	(Note 4)	t_{rf}	-	(Note 5)	ns
Hold time for $\overline{INTREQ}$ from SCCLK rising	(Note 4)	t_{scrl}	0	-	ns
Time from SCCLK falling to $\overline{CS}$ rising		t_{sccsh}	20	-	ns
High time between active $\overline{CS}$		t_{csht}	200	-	ns
Time from $\overline{CS}$ rising to SCDOUT high-Z	(Note 6)	t_{cscdo}		10	ns

Notes:
1. Data must be held for sufficient time to bridge the 300(50) ns transition time of SCCLK.
2. SCDOUT should *not* be sampled during this time period.
3. $\overline{INTREQ}$ goes high only if there is no data to be read from the DSP at the rising edge of SCCLK for the second-to-last bit of the last byte of data during a read operation as shown.
4. If $\overline{INTREQ}$ goes high as indicated in Note 3, then $\overline{INTREQ}$ is guaranteed to remain high until the next rising edge of SCCLK. If there is more data to be read at this time, $\overline{INTREQ}$ goes active low again. Treat this condition as a new read transaction. Raise chip select to end the current read transaction and then drop it, followed by the 7-bit address and the R/$\overline{W}$ bit (set to 1 for a read) to start a new read transaction.
5. The rise time of $\overline{INTREQ}$ depends on the pull-up resistor used and the load being driven because this pin is an open-drain output.
6. This time is by design and not tested.



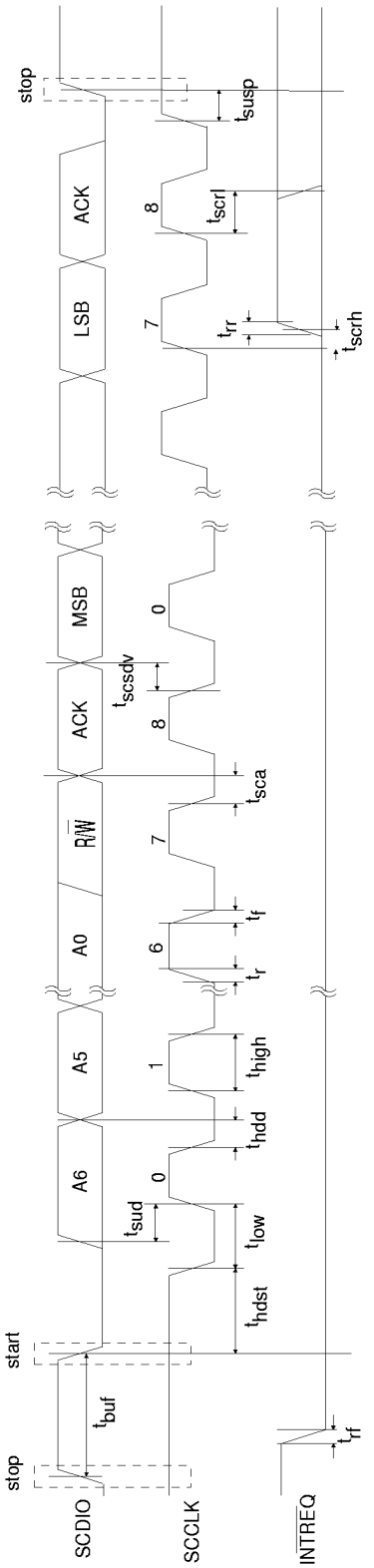
SPI Control Port Timing

SWITCHING CHARACTERISTICS—CONTROL PORT

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; Inputs: Logic 0 = DGND, Logic 1 = VD+, C_L = 20 pF)

Parameter		Symbol	Min	Max	Units
I²C® Mode					
SCCLK clock frequency	(Slow mode) (Fast mode)	f_{scl}		100 400	kHz
Bus free time between transmissions		t_{buf}	4.7		µs
Start-condition hold time (prior to first clock pulse)		t_{hdst}	4.0		µs
Clock low time	(Slow mode) (Fast mode)	t_{low}	4.7 1.2		µs
Clock high time	(Slow mode) (Fast mode)	t_{high}	4.0 1.0		µs
SCDIO setup time to SCCLK rising		t_{sud}	250		ns
SCDIO hold time from SCCLK falling	(Note 7)	t_{hdd}	0		µs
Rise time of both SCDIO and SCCLK	(Note 8)	t_r		50	ns
Fall time of both SCDIO and SCCLK		t_f		300	ns
Time from SCCLK falling to CS4923 ACK		t_{sca}		40	ns
Time from SCCLK falling to SCDIO valid during read operation		t_{scsdv}		40	ns
Time from SCCLK rising to $\overline{\text{INTREQ}}$ rising	(Note 9)	t_{scrh}		200	ns
Hold time for $\overline{\text{INTREQ}}$ from SCCLK rising	(Note 10)	t_{scrl}	0		ns
Rise time for $\overline{\text{INTREQ}}$	(Note 9)	t_{rr}		(Note 11)	ns
Fall time for $\overline{\text{INTREQ}}$	(Note 10)	t_{rf}		(Note 11)	ns
Setup time for stop condition		t_{susp}	4.7		µs

Notes:
7. Data must be held for sufficient time to bridge the 300-ns transition time of SCCLK. This hold time is by design and not tested.
8. This rise time is shorter than that recommended by the I^2C specifications. For more information, see the section on SCP communications.
9. $\overline{\text{INTREQ}}$ goes high only if there is no data to be read from the DSP at the rising edge of SCCLK for the last bit of the last byte of data during a read operation as shown.
10. If $\overline{\text{INTREQ}}$ goes high as indicated in Note 8, then $\overline{\text{INTREQ}}$ is guaranteed to remain high until the next rising edge of SCCLK. If there is more data to be read at this time, $\overline{\text{INTREQ}}$ goes active low again. Treat this condition as a new read transaction. Send a new start condition followed by the 7-bit address and the R/$\overline{\text{W}}$ bit (set to 1 for a read).
11. The rise time of $\overline{\text{INTREQ}}$ depends on the pull-up resistor used and the load being driven because this pin is an open-drain output.



I²C Control Port Timing

SWITCHING CHARACTERISTICS—DIGITAL AUDIO INPUT

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

Parameter		Symbol	Min	Max	Unit
SCLKN1(2) period for both Master and Slave mode		T_{sclki}	40	-	ns
SCLKN1(2) duty cycle for Master and Slave mode			45	55	%
Master Mode	(Note 12)				
LRCLKN1(2) delay after SCLKN1(2) transition	(Note 13)	T_{lrds}	-	10	ns
SDATAN1(2) setup to SCLKN1(2) transition	(Note 14)	T_{sdsum}	5	-	ns
SDATAN1(2) hold time after SCLKN1(2) transition	(Note 14)	T_{sdhm}	5	-	ns
Slave Mode	(Note 15)				
LRCLKN1(2) setup to SCLKN1(2) transition	(Note 13)	T_{lrsus}	5	-	ns
LRCLKN1(2) hold time after SCLKN1(2) transition	(Note 13)	T_{lrhs}	5	-	ns
SDATAN1(2) setup to SCLKN1(2) transition	(Note 14)	T_{sdsus}	5	-	ns
SDATAN1(2) hold time after SCLKN1(2) transition	(Note 14)	T_{sdhs}	5	-	ns

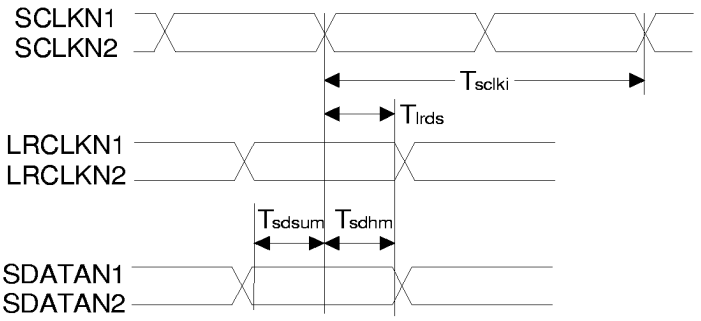
Notes: 12. Master mode is defined as the CS4923 driving LRCLKN1(2) and SCLKN1(2). Master or Slave mode can be programmed. For more information, see the *CS4923 Users Guide*.

13. This timing parameter is defined from the non-active edge of SCLKN1(2). The active edge of SCLKN1(2) is the point at which the data is valid and can be programmed. For more information, see the *CS4923 Users Guide*.

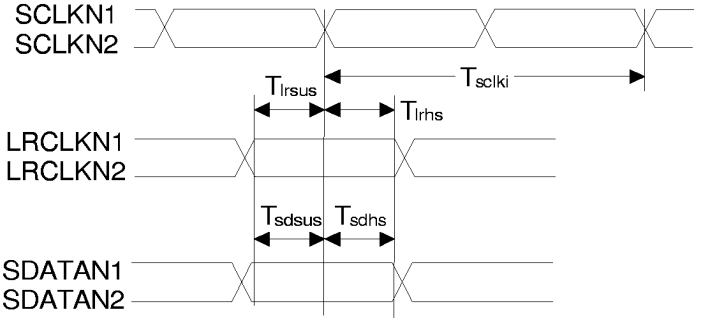
14. This timing parameter is defined from the active edge of SCLKN1(2). The active edge of SCLKN1(2) is the point at which the data is valid and can be programmed. For more information, see the *CS4923 Users Guide*.

15. Slave mode is defined as SCLKN1(2) and LRCLKN1(2) being driven by an external source. Master or Slave mode can be programmed. For more information, see the *CS4923 Users Guide*

MASTER MODE



SLAVE MODE



Digital Audio Input Data, Input and Output Clock Timing

SWITCHING CHARACTERISTICS—DIGITAL AUDIO OUTPUT

(T_A = 25 °C; VA+, VD+ = 3.3 V ±5%; measurements performed under static conditions.)

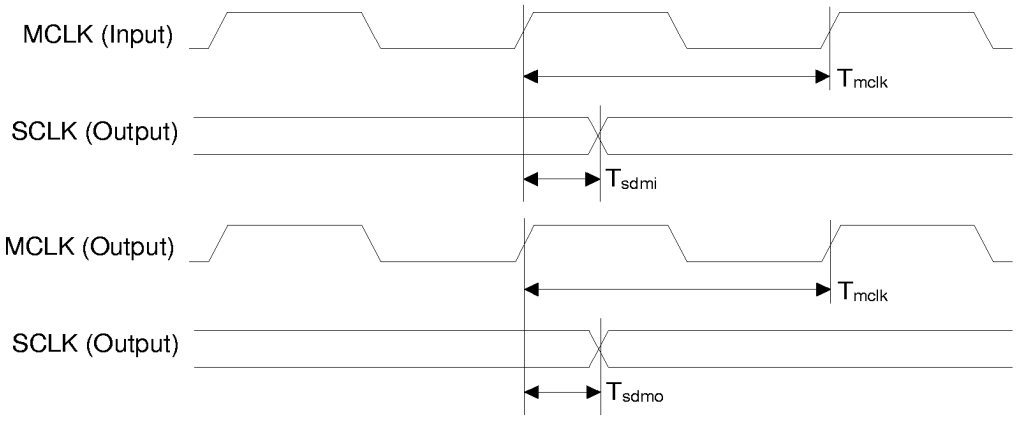
Parameter		Symbol	Min	Max	Unit
MCLK period	(Note 16)	T_{mclk}	40	-	ns
MCLK duty cycle	(Note 16)		40	60	%
SCLK period for Master or Slave mode		T_{sclk}	40	-	ns
SCLK duty cycle for Master or Slave mode			45	55	%
Master Mode	(Note 17)				
SCLK delay from MCLK rising edge, MCLK as an input		T_{sdmi}		10	ns
SCLK delay from MCLK rising edge, MCLK as an output		T_{sdmo}	–5	10	ns
LRCLK delay from SCLK transition	(Note 18)	T_{lrds}		10	ns
AUDATA2–0 delay from SCLK transition	(Note 18)	T_{adsm}		10	ns
Slave Mode	(Note 19)				
LRCLK setup before SCLK transition	(Note 18)	T_{lrss}	5	-	ns
LRCLK hold time after SCLK transition	(Note 18)	T_{lrhs}	5	-	ns
AUDATA2–0 delay from SCLK transition	(Note 18)	T_{adss}		10	ns

Notes: 16. MCLK can be an input or an output. These specifications apply for both cases. Master or Slave mode can be programmed. For more information, see the *CS4923 Users Guide*.

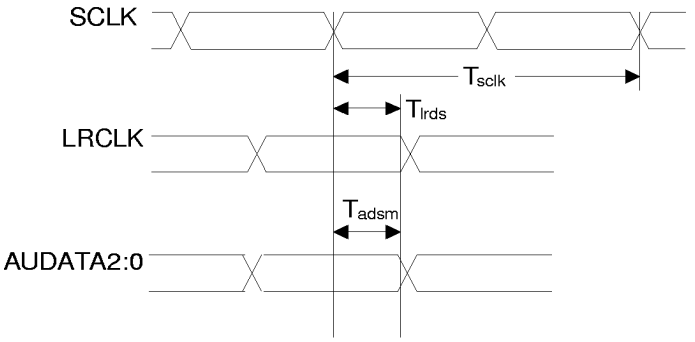
17. Master mode is defined as the CS4923 driving both SCLK and LRCLK. When MCLK is an input, it is divided to produce SCLK and LRCLK.

18. This timing parameter is defined from the non-active edge of SCLK. The active edge of SCLK is the point at which the data is valid and can be programmed. For more information, see the *CS4923 Users Guide*.

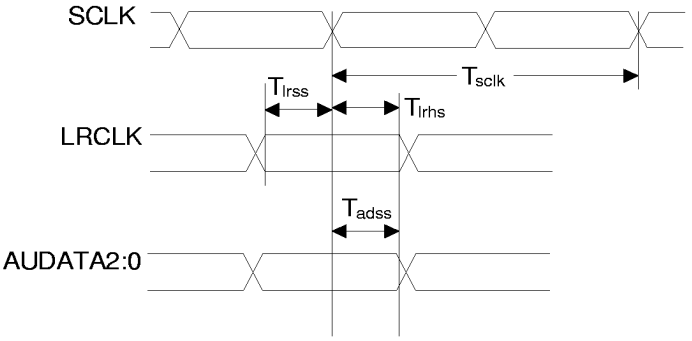
19. Slave mode is defined as SCLK and LRCLK being driven by an external source. Master or Slave mode can be programmed. For more information, see the *CS4923 Users Guide*.



MASTER MODE



SLAVE MODE



Digital Audio Output Data, Input and Output Clock Timing

SYSTEM AND INTERFACE DESCRIPTION

The CS4923 provides comprehensive Dolby Digital audio decompression. In addition to its strict compliance with 5.1-channel audio decoding standards, the CS4923 also features the extra memory and reserve-execution capacity that are necessary to reduce the cost of the entire Dolby subsystem. Additional features include variable surround delays, bass-output management with built-in crossover filters, Dolby Surround Pro Logic decoding, custom audio processing (such as 3D positional effects), robust error concealment, and adjustable audio/video synchronization.

The mixed-signal chip contains the following major functional sub-blocks:

- A processor block with two 24-bit digital signal processors (DSPs)
- A configurable host interface
- A flexible compressed-data-input interface
- An auxiliary digital-audio-input interface
- A multimode digital-audio-output interface
- A programmable, analog phase-locked loop (PLL)

The processor block in the CS4923 accomplishes the audio decoding and post processing with on-chip ROM- and RAM-based DSP software applications supplied by Cirrus Logic's Crystal Semiconductor Products Division. The CS4923 supports two methods of downloading the DSP applications: an external host loading the program through the parallel or serial host interface, or the Automatic Boot mode of the CS4923 with an external memory interface. For complete information on the DSP software-application features and typical operation, see the *CS4923 User's Guide*.

In addition to the processor block, the CS4923 also integrates a complete set of industry-standard audio input/output interfaces. Internal buffers are used to simplify data input and output. To simplify host drivers and enable bursty delivery of high-speed compressed data from data demultiplexers, the CS4923 includes a two-channel, 8-kilobyte input buffer.

The CS4923 DSPs and audio input/output interfaces support clocking of external DAC and ADC interfaces using the on-chip programmable PLL. In addition, the PLL can be driven from an internally recovered, over-sampled clock via a single-wire SPDIF input on the RCV958 pin to perfectly match the output sample rate to the quantity of compressed data received and decoded.

Digital Signal Processing

The CS4923 Dolby Digital decoder takes advantage of a proven 24-bit DSP core that was developed by Cirrus Logic's Crystal Semiconductor Products Division to simplify Dolby Digital Group A decoding. The CS4923 contains program RAM to receive DSP software applications downloaded at initialization by a host microcontroller or read by the CS4923 from an external 8-bit ROM following reset. Nearly all of the CS4923 external interface pins have multiple configurations to allow true flexibility.

The Crystal DSP core uses a high-throughput, 24-bit Harvard architecture that operates from independent on-chip program RAM, program ROM, and data RAM. The DSP core contains dual 48-bit accumulators and a complete 24-bit arithmetic/logic unit (ALU) designed specifically for audio processing. For address generation, the CS4923 contains a dedicated multichannel data address unit and a multichannel program address unit. All of the core I/O peripherals support direct access, many of them 24 bits at a time. Overall, the CS4923 core implements a complete set of DSP instructions equivalent to those commonly found in commercial general-purpose DSPs.

The CS4923 program memory utilizes both ROM and RAM with feature variations to support variable interface requirements. Crystal can furnish software applications under separate licensing

agreements to support audio decoding and advanced player operation. The *CS4923 User's Guide* provides full details of the exact configuration and operation for Dolby Digital audio decoding.

The CS4923 provides over 12 kilowords (36 kilobytes) of data memory. The majority of the data memory is local to the DSP cores. In addition, a large two-channel, 8-kilobyte input buffer simplifies host drivers and accommodates all methods of data delivery.

Host Interface

The host interface to the CS4923 is a bidirectional 8-bit message pipe between the DSP and a configurable serial or parallel host. Whichever host interface is selected, host access to the CS4923 registers is controlled by the application software running on the DSP. Almost all configuration and control of the CS4923 decoder and its peripherals is indirectly executed through the messaging interface or from the initial program download.

The designer can implement the host interface for the CS4923 as any one of four popular industry standards. The CS4923 supports the I^2C and SPI serial-interface modes and the Intel or Motorola byte-wide parallel-host modes. For either the I2C or SPI serial mode the CS4923 can only operate as a slave. The states of the $\overline{RD}$, $\overline{WR}$, and PSEL pins at the rising edge of $\overline{RESET}$ determine the interface type, as shown in Table 1.

In addition, in serial host mode, the DSP can access the GPIO control signals in a predetermined fashion to establish an external memory interface. This interface provides medium-speed optional access to external byte-wide RAM, ROM, EPROM, or Flash memory.

$\overline{RD}$	$\overline{WR}$	PSEL	Host Interface Mode	Signal Pins Used
1	1	1	8-bit Motorola	$\overline{DS}$, R/$\overline{W}$, $\overline{CS}$, DATA7–DATA0, A1, A0, $\overline{INTREQ}$
1	1	0	8-bit Intel	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$, DATA7–DATA0, A1, A0, $\overline{INTREQ}$
0	1	x	Serial I^2C	SCDIO, SCCLK
1	0	x	Serial SPI	$\overline{CS}$, SCDOUT, SCDIN, SCCLK

Table 1. Host Modes

Parallel Host Interface

The parallel host interface supports the downloading of DSP software to configure all of the CS4923 data ports, to deliver compressed data, and to inject linear byte-wide PCM data. In conjunction with the $\overline{INTREQ}$ pin, the parallel host interface provides a robust capability for communication between the DSP and the host to provide for CS4923 configuration, I/O-port setup and run-time messaging for monitoring of error and data-flow transitions. The entire parallel interface is internal to the CS4923, implemented as four 8-bit registers selected by A1 and A0, as shown in Table 2.

A1	A0	Register Name	Register Function
1	1	CMPDATA	8-bit compressed data to input unit (write only)
1	0	PCMDATA	8-bit linear PCM data to input unit (write only)
0	1	CONTROL	Multi-bit control register for setup and handshaking (R/$\overline{W}$)
0	0	HOSTMSG	8-bit control pipe message register (R/$\overline{W}$)

Table 2. Host Memory Map

Host Message (HOSTMSG) Register, A1–A0 = 00b

7	6	5	4	3	2	1	0
HOSTMSG7	HOSTMSG6	HOSTMSG5	HOSTMSG4	HOSTMSG3	HOSTMSG2	HOSTMSG1	HOSTMSG0

HOSTMSG7–0 Host data to and from the DSP. A read or write of this register operates handshake bits between the internal DSP and the external host. This register typically passes multibyte messages carrying microcode, control, and configuration data. HOSTMSG is physically implemented as two independent registers for input and output. (Read and write)

Host Control (CONTROL) Register, A1–A0 = 01b

7	6	5	4	3	2	1	0
Reserved	CMPRST	PCMRST	MFC	MFB	HINBSY	HOUTRDY	HATTN

Reserved Always write to 0 for future compatibility.

CMPRST When set, initializes the CMPDATA compressed data input channel. Writing a one to this bit holds the port in reset. Writing zero enables the port. This bit must be low for normal operation. (Write only)

PCMRST When set, initializes the PCMDATA linear PCM input channel. Writing a one to this bit holds the port in reset. Writing zero enables the port. This bit must be low for normal operation. (Write only)

MFC When high, indicates that the PCMDATA input buffer is almost full. (Read only)

MFB When high, indicates that the CMPDATA input buffer is almost full. (Read only)

HINBSY Set when the host writes to HOSTMSG. Cleared when the DSP reads data from the HOSTMSG register. The host reads this bit to determine if the last host byte written has been read by the DSP. (Read only)

HOUTRDY Set when the DSP writes to the HOSTMSG register. Cleared when the host reads data from the HOSTMSG register. The DSP reads this bit to determine if the last DSP output byte has been read by the host. (Read only)

HATTN Host Attention. Setting this bit generates an interrupt to the DSP. (Write only)

PCM Data Input (PCMDATA) Register, A1–A0 = 10b

7	6	5	4	3	2	1	0
PCMDATA7	PCMDATA6	PCMDATA5	PCMDATA4	PCMDATA3	PCMDATA2	PCMDATA1	PCMDATA0

PCMDATA7–0 The host writes PCM data to the DSP input buffer at this address. (Write only)

Compressed Data Input (CMPDATA) Register, A1–A0 = 11b

7	6	5	4	3	2	1	0
CMPDATA7	CMPDATA6	CMPDATA5	CMPDATA4	CMPDATA3	CMPDATA2	CMPDATA1	CMPDATA0

CMPDATA7–0 The host writes compressed data to the DSP input buffer at this address. (Write only)

Intel 8-Bit Mode

In Intel host interface mode, the host-interface pins perform as an active-low chip select, $\overline{CS}$, and two active-low cycle strobes, $\overline{RD}$ and $\overline{WR}$. $\overline{RD}$ and $\overline{WR}$ have no effect when $\overline{CS}$ is held high. When $\overline{CS}$ is low, $\overline{RD}$ becomes the output enable for DATA7–DATA0. If $\overline{CS}$ and $\overline{RD}$ are low, the contents of register address A1–A0 are driven on the DATA7–DATA0 bus. The address A1–A0 must be valid a minimum time before the later of $\overline{CS}$ and $\overline{RD}$ going low. Driving both $\overline{CS}$ and $\overline{WR}$ low begins an 8-bit write cycle. The address A1–A0 must be valid a minimum time before the later of $\overline{CS}$ and $\overline{WR}$ going low. On the first rising edge of $\overline{CS}$ or $\overline{WR}$, the write cycle ends and DATA7–DATA0 are latched. Data must be valid a minimum time before the end of this Intel write cycle. As a result, data can be invalid at the beginning of the write cycle. The HINBSY and HOUTRDY bits of the CONTROL register are updated at the end of the read or write cycle. During $\overline{RESET}$ low, all control signals have no effect, DATA7–DATA0 are high impedance, and write cycles are disabled.

Motorola 8-Bit Mode

In Motorola host interface mode, the host interface pins act as an active-low chip select, $\overline{CS}$, an active-low data strobe, $\overline{DS}$, and a R/$\overline{W}$ control signal. Internally to the CS4923, $\overline{DS}$ and $\overline{CS}$ are logically ANDed. Therefore, in some cases, $\overline{DS}$ and $\overline{CS}$ can be externally tied together with a common active-low strobe. Otherwise, in long decoder delay scenarios, read or write cycles can be terminated earlier by connecting the microprocessor active-low data-strobe signal to the CS4923 $\overline{DS}$ and a delayed final active-low chip select independently to the $\overline{CS}$ pin.

During read cycles, DATA7–DATA0 are driven when R/$\overline{W}$ is high and $\overline{DS}$ and $\overline{CS}$ are both low. Data is driven until the first signal changes state: R/$\overline{W}$ goes low, $\overline{DS}$ goes high, or $\overline{CS}$ goes high. Write cycles occur with R/$\overline{W}$ low followed by $\overline{DS}$ and $\overline{CS}$ both going low. The A1–A0 address pins select the specific address and DATA7–DATA0 carry the data. For write cycles, the first of $\overline{CS}$ and $\overline{DS}$ going high latches data. During read cycles, DATA7–DATA0 are actively driven when R/$\overline{W}$ is high and $\overline{CS}$ and $\overline{DS}$ are low. DATA7–DATA0 are released with the earliest of $\overline{CS}$ and $\overline{DS}$ going high or R/$\overline{W}$ going low.

I^2C Serial Host Interface

For normal I^2C operation, SCDIO serves as a bidirectional data pin and SCCLK acts as the clock input pin for the CS4923. The CS4923's serial host interface functions as a slave only and always performs an 8-bit data transfer or a series of 8-bit transfers. Data latches on the rising edge of SCCLK. SCCLK is an input only and therefore cannot be stretched by the CS4923 to delay a read or write cycle. Additionally, the CS4923 cannot tolerate slow edges on SCCLK. Care should be taken in driving SCCLK. Figure 1 illustrates the relative timing necessary for an I^2C write operation for a single byte. A write cycle is defined as the transfer of data from an I^2C bus master to the CS4923 serial control port. The host initiates a transfer with a start condition followed by a 7-bit address and a read/write bit (set low for a write). The CS4923 internal 7-bit address is initially assigned to 000 0000b following a reset. In single-slave scenarios, the 7-bit address can be left set to 0. In multislave designs, the CS4923 must be initialized with a unique ID following a reset. Typically, this initialization consists of holding all other devices on the I^2C bus in reset while writing to the CS4923 to initialize the ID. Another way to avoid conflicts is to hold the CS4923 in $\overline{RESET}$ until the host is ready to initialize the ID register.

When the host writes to the CS4923, 8 bits of data on SCDIO shift into the input shift register as shown in Figure 1. When the shift register is full, the 8-bit data transfers to the Serial Control Port Input (SCPIN) register of the CS4923 on the falling

edge of data bit 8. The CS4923 sends an acknowledge (ACK) back to the host and sets an input-ready flag in the internal DSP. The host can continue to send additional data bytes as long as the CS4923 acknowledges each byte. If the CS4923 fails to acknowledge a byte, it is possible that the byte was rejected and the host should transmit it again. If the CS4923 rejects back-to-back byte writes, then the host should reset the CS4923.

When the CS4923 sends a byte to the host, it first writes the byte to the Serial Control Port Output (SCPOUT) register. A write to the SCPOUT register sets the request pin low ($\overline{\text{INTREQ}}$). The host must recognize the request and issue a read operation to the CS4923. Figure 1 illustrates the relative timing of a three byte read. The host must send the 7-bit address of the CS4923 and set the read bit. For the I^2C protocol, it is always the device receiving the transfer that must provide the acknowledgment (ACK). Therefore, the CS4923 acknowledges the address and read bit. After the CS4923 acknowledges, it loads the serial shift register with the byte to be sent to the host and places the most significant bit on the SCDIO line. It then shifts out the 8-bit value in the serial shift register on the rising edges of SCCLK. In I^2C mode, the CS4923 deasserts the $\overline{\text{INTREQ}}$ pin immediately following the rising edge of the last data bit of the current byte being transferred if the SCPOUT register is empty awaiting a write from the DSP. The $\overline{\text{INTREQ}}$ pin is guaranteed to stay deasserted until the rising edge of SCCLK for the acknowledgment (ACK). If there is data written by the DSP into the SCPOUT register before the rising edge of SCCLK for the last data bit, then $\overline{\text{INTREQ}}$ remains asserted, allowing the delivery of multiple bytes. It is important to note that once the data is in the shift register, clocks on the SCCLK pin shift the data bits out of the shift register. A STOP condition on the bus does not prevent this shift from occurring. The host must read the byte before any other bus activity or the data is lost.

If the DSP writes a byte to the SCPOUT register after the rising edge of SCCLK for the last data bit, but before the rising edge of SCCLK for the acknowledgment (ACK), the byte in the SCPOUT is not loaded into the shift register on the falling edge of SCCLK for the acknowledgment. Therefore, reading this byte requires a new read operation.

SPI Serial Host Interface

Normal SPI serial host mode uses the SCCLK, SCDIN, SCDOUT and $\overline{\text{CS}}$ pins along with $\overline{\text{INTREQ}}$. $\overline{\text{CS}}$ is an active-low master enable for this mode and must be held low for serial shifts in or out of the CS4923. SCCLK is an input to the CS4923 and provides a rising edge for the internal serial shift clock. SCDIN is the dedicated serial-data input and SCDOUT is the dedicated serial-data output for the CS4923. $\overline{\text{INTREQ}}$ is the active-low request signal that is driven by the CS4923 when there is valid data in the Serial Control Port Output (SCPOUT) register.

Figure 2 illustrates the relative timing necessary for a single-byte SPI write operation to the CS4923. The host initiates a transfer by driving $\overline{\text{CS}}$ low, followed by a 7-bit address and a read/write bit (set low for writes). The SPI mode typically does not use this address; however, it is still necessary to clock an address across the bus followed by the read/write bit. The CS4923 internal 7-bit address is initially assigned to 000 0000b following a reset.

When the host specifies a write to the CS4923, 8 bits of data on SCDIN shift into the input shift register as shown in Figure 2. When the shift register is full, the 8-bit data transfers to the SCPIN register on the falling edge of the eighth data bit.

When the CS4923 sends a byte to the host, it first writes the byte to the SCPOUT register, which sets the $\overline{\text{INTREQ}}$ pin active low. The host must recognize the request and issue a read operation to the CS4923. Figure 2 illustrates the relative timing of a single-byte read. The host must send the 7-bit ad-

Notes:
1. The ACK for the address byte is driven by the CS4923.
2. The ACKs for the data bytes being read from the CS4923 should be driven by the host.
3. INTREQ is guaranteed to stay low until the rising edge of SCCLK for last bit of the last byte to be transferred out of the CS4923
4. A NOACK should be sent by the host after the last byte to indicate the end of the read cycle.
5. INTREQ is guaranteed ton stay high until the next rising edge of SCCLK (for the ACK/NACK bit) at which point it may go low again if there is new data to be read. The condition of INTREQ going low at this point should be treated as a new read condition and a new start condition followed by an address byte should be sent.

Figure 1. I^2C Timing

dress (and if address checking is enabled, the address must match the value in the SCPCN register) and the read bit. The CS4923 internal 7-bit address is assigned to 000 0000b following a reset. After the falling edge of SCCLK for the read/write bit, the CS4923 loads the serial shift register with the byte to be sent and places the most significant bit on the SCDOUT pin. The host shifts out the 8-bit value in the serial shift register using the rising edge of SCCLK. The data is valid on the rising edge of SCCLK and transitions immediately following the falling edge. In SPI mode, the $\overline{\text{INTREQ}}$ pin is deasserted immediately following the rising edge of the second-to-last data bit of the current byte being transferred if there is no data in the SCPOUT register. The $\overline{\text{INTREQ}}$ pin is guaranteed to stay deasserted (high) until the rising edge of SCCLK for the last data bit.

If there is data placed in the SCPOUT register before the rising edge of SCCLK for the second-to-last data bit, then $\overline{\text{INTREQ}}$ remains asserted low. Immediately following the falling edge of SCCLK for the last data bit, the new data byte loads into the serial shift register. The host should continue to read this new byte. It is important to note that once the data is in the shift register, clocks on the SCCLK line shift the data bits out of the shift register. The host should read the byte before any other bus activity or the data is lost. If $\overline{\text{CS}}$ is deasserted, SCCLK does not shift the data out. However, the data is still in the shift register. After $\overline{\text{CS}}$ is asserted low, each SCCLK shifts the data out of the register.

External Memory Interface

In serial host control port mode, an external memory interface is realizable through the GPIO7–GPIO0, GPIO8, GPIO10, and GPIO11 multifunctional pins, where GPIO7–GPIO0 serve as a multiplexed address and data, EMAD7–EMAD0. The GPIO11 pin functions as $\overline{\text{EMOE}}$, or active-low external-memory data-enable output. The GPIO10 pin functions as $\overline{\text{EMWR}}$, or active-low external write-enable output; and GPIO8 functions as $\overline{\text{EXTMEM}}$, which serves as the active-low chip-select output. Figure 3 illustrates the external memory configuration for the autoboot sequence.

The external memory address is capable of addressing 16 megabytes through a 24-bit address. The address comes from the DSP writing three initial bytes of address consecutively on GPIO7–GPIO0. Each byte of address is externally latched via the $\overline{\text{EMOE}}$ strobe going high with $\overline{\text{EXTMEM}}$ not selected. After the 3-byte address is latched, the CS4923 then drives $\overline{\text{EXTMEM}}$ and $\overline{\text{EMOE}}$ low simultaneously to select the external memory. For specific memory interface timing requirements, see the detailed electrical parameter section of this data sheet. The memory can be implemented as RAM or ROM.

It should be noted that for autoboot the most significant byte is always zero. For this reason a two latch external memory configuration can be used for autoboot. It should also be noted that this two latch external memory architecture may be required for future programs needing external memory.

Additionally, it is possible to configure the CS4923 to automatically load its program from external memory on a hard reset condition with the rising edge of $\overline{\text{RESET}}$. In serial control port mode, holding the $\overline{\text{ABOOT}}$ pin low as the CS4923 leaves the reset state enables an automatic boot. $\overline{\text{ABOOT}}$ can be released following the rising edge of $\overline{\text{RESET}}$. During the automatic boot cycle, the serial control port should remain idle. For more information about communication with the CS4923, see the *CS4923 User's Guide*.

Compressed Data Input

To support varying bitstream input scenarios, the CS4923 can accept compressed data in many forms. The host selects and configures the type of compressed-data input and the delivery mode through a command/message dialog with the inter-

Notes:
1. INTREQ is guaranteed to stay low until the rising edge of SCCLK for the second to last bit of the last byte to be transferred out of the CS4923
2. INTREQ is guaranteed to high until the next rising edge of SCCLK at which point it may go low again if there is new data to be read. The condition of INTREQ going low at this point should be treated as a new read condition and a new start condition followed by an address byte should be sent

Figure 2. SPI Timing

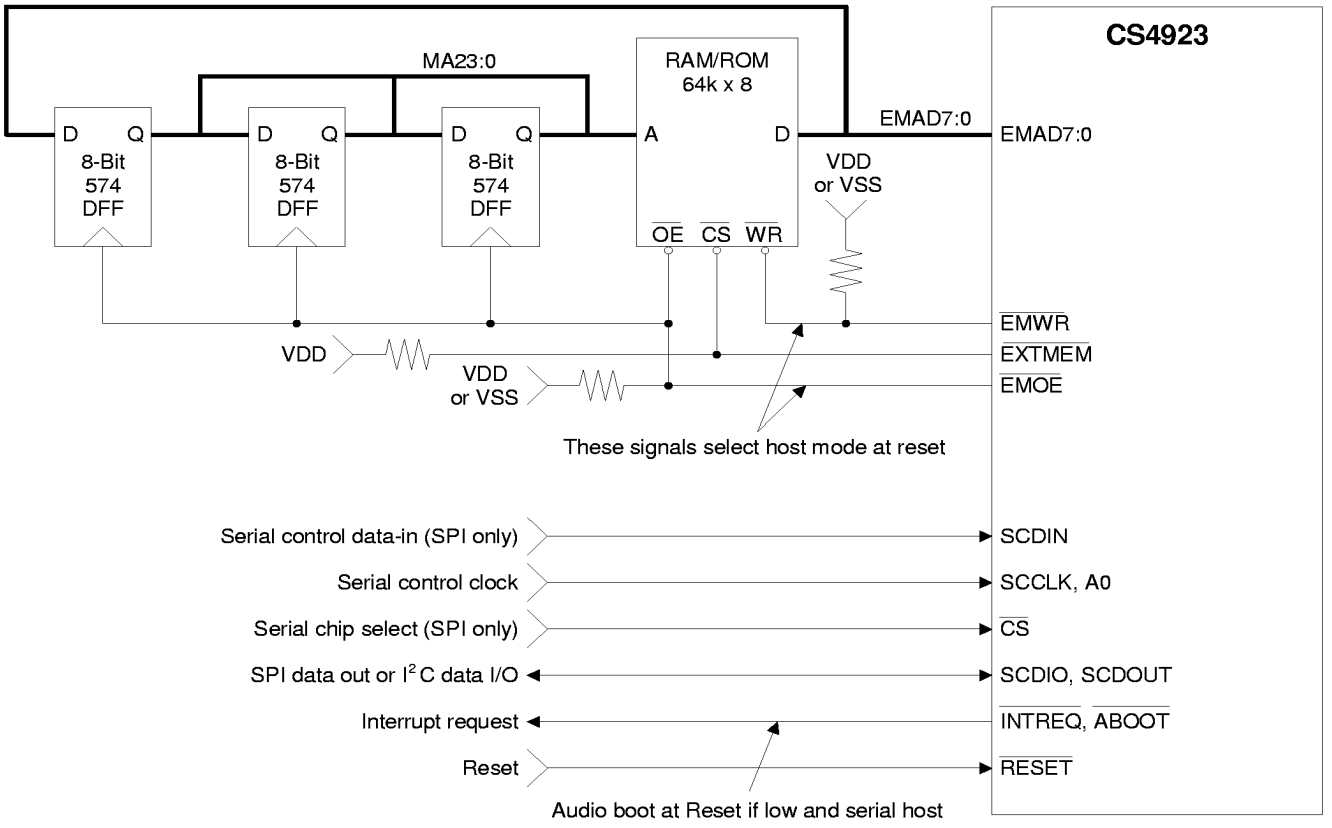


Figure 3. CS4923 Optional External Memory Interface, RAM or ROM

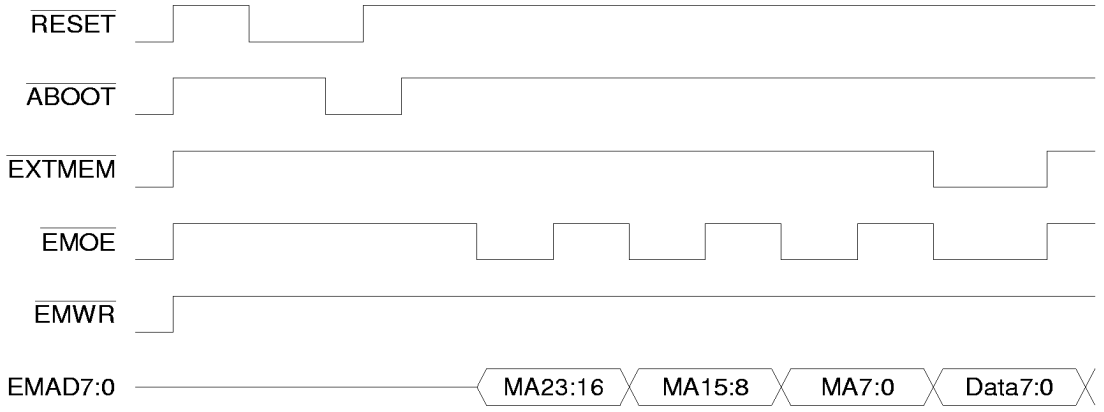


Figure 4. Automatic Boot from External Memory on RESET

nal DSP. DSP application software typically performs the input-data processing of the supported bitstreams, including elementary streams, PES layer packetized elementary streams, program streams, or DVD Pack layer. For the exact command/message dialogue, see the *CS4923 User's Guide*. The most popular and recommended methods of delivering compressed data to the decoder include the following:

1) IEC61937 serial single-wire input on the RCV958 device pin
2) Dedicated serial interface through the CMPDAT, CMPCLK, and $\overline{\text{CMPREQ}}$ device pins
3) Byte-wide through the complete 8-bit host interface polling MFB or MFC in the Host Control register or monitoring $\overline{\text{CMPREQ}}$
4) Universal serial-audio interface on the SCLKN1, LRCLKN1, and SDATAN1 device pins
5) Universal serial-audio interface on the SCLKN2, LRCLKN2, and SDATAN2 device pins

IEC61937 Compressed Data Input through the Single Wire Interface

For Dolby Digital–decoder applications where the CS4923 receives compressed data from another end-user product such as a laser-disc player or a two-channel decoder, the CS4923 can directly accept a serial biphase encoded input on the RCV958 signal pin.

Except for the CMOS input level characteristics of the serial input pin, the input functionality is compatible with the IEC61937 interface, including extended channel-status-bit collection, burst-preamble and burst-info recognition, burst-payload deframing, stuffing-bit removal, null-data-bit removal, and paused-audio-gap processing. The CS4923 provides a dedicated, configurable two-channel input buffer for collecting whole units of the bit stream before batch processing. The internal DSP provides software control of this input in conjunction with dedicated hardware where necessary.

In the IEC61937 mode, the CS4923 recovers the bit clock from the input and provides that clock to the clock manager section of the chip. The clock manager performs overall synchronization of the input rate, derives the DSP clock speed, and selects the output sample-rate clocks. Typically, the sample-rate clock is a phase-locked and divided version of the DSP clock. An oversampled bit-rate clock output can be made available externally on several CS4923 signal pins: MCLK, SCLKN1, and SCLK.

Externally IEC61937 Received Compressed Data Input through SCLKN1, LRCLKN1, and SDATAN1 or SCLKN2, LRCLKN2, and SDATAN2

As an alternative to the single-wire interface, the CS4923 can accept compressed data from an IEC61937 interface that has already passed through an external serial receiver chip (such as the CS8411-12, which performs data decoding and clock recovery). The upstream IEC61937 receiver removes the channel-status information, and that information is therefore unavailable in this input mode. Only one port can be used for compressed data recovery at a time.

Other than the absence of channel-status information, the CS4923's input-data extractor collects all of the data input and automatically locates Dolby Digital frames through the burst-preamble and burst-info fields, performs burst-payload deframing, stuffing-bit removal, null-data-bit removal, and paused-audio-gap processing. The extractor removes all of the discarded data before transferring the data to the input buffer, thereby preserving the large input buffer depth.

Serial Compressed Data Input

The CS4923 implements the serial compressed data input mode with three signal pins: CMPDAT,

CMPCLK, and $\overline{\text{CMPREQ}}$. In this mode, the CS4923 provides a $\overline{\text{CMPREQ}}$ pin, which is level programmable, to request data from the source. If the CS4923 asserts $\overline{\text{CMPREQ}}$, it is ready to accept more compressed data. The CS4923 shifts the serial data MSB first into a configurable input buffer that can provide up to 8192 bytes of storage. The large input buffer simplifies the design of a system employing bursty high-speed delivery. The internal DSP establishes and configures the exact input-buffer-level threshold for controlling the assertion and deassertion of the $\overline{\text{CMPREQ}}$ pin at startup. Serial data on CMPDAT is clocked into the CS4923 with CMPCLK most significant bit first. The active edge of CMPCLK can be programmed to be the rising or falling edge. $\overline{\text{CMPREQ}}$ serves as a FIFO level indicator. CMPCLK must be gated to prevent FIFO overflow when $\overline{\text{CMPREQ}}$ is high.

Byte-Wide Compressed Data Input

To support computer multimedia applications, the CS4923 can accept most-significant-byte-first compressed data through the host 8-bit interface port. The compressed-data interface receives bytes of data when the host interface writes to address 11b (A1 and A0 are both high). The host interface port also utilizes the $\overline{\text{CMPREQ}}$ pin and the MFB and MFC flags in the CONTROL register, which are configurable to supply a data request flag at different input buffer thresholds. Generally, the 8-bit compressed-data interface can accept at least three more bytes as long as the data request ($\overline{\text{CMPREQ}}$) pin is asserted or MFB and MFC are not set. $\overline{\text{CMPREQ}}$ acts as an almost-full flag. The CS4923 can safely receive larger blocks of data in scenarios where $\overline{\text{CMPREQ}}$ or MFB/MFC are configured to be asserted at a lower watermark. In these cases, the CS4923 can accept at least another block of bytes (programmable in units of 512). This mode reduces the polling burden associated with hand-feeding the compressed data.

Linear PCM Digital Audio Input Interfaces

The CS4923 provides three different methods of accepting linear PCM through a total of four PCM ports. The CS4923 has two serial PCM inputs, a serial IEC60958 single-wire port, and an 8-bit interface for PCM data if the parallel host mode is selected. The four PCM ports use the following pin assignments:

1) IEC60958 input on the RCV958 device pin
2) Byte-wide through the complete 8-bit host interface
3) Universal serial-audio interface on the SCLKN1, LRCLKN1, and SDATAN1 device pins
4) Universal serial-audio interface on the SCLKN2, LRCLKN2, and SDATAN2 device pins

The device can accept simultaneously any two independent PCM inputs, each uniquely configured and each at independent sample rates. In all cases, the two independent inputs are routed to the input buffer which is also independently configurable for each logical input. The host messaging interface performs all PCM digital-audio-input-mode configuration by delivering setup values for the input ports.

Serial PCM Input

The CS4923 has two independent serial inputs and each of these PCM interfaces is configurable for master or slave timing. To support all common digital serial modes, the serial PCM can be left flush, right flush, and with or without a 1-bit delay. The PCM sample sizes are also completely programmable with the most common bit lengths being 8, 16, 18, 20, and 24 bits. The active clock edge is also programmable. The input ports can be slaved to external timing or configured in master mode timing. If a serial PCM port is configured for slave mode, the SCLKN1/LRCLKN1 pins, the

SCLKN2/LRCLKN2 pins, or both become inputs. In master mode, these pins become outputs which are slaved to the audio clock manager or the MCLK external device pin. Following reset, both serial PCM input ports default to slave mode to avoid possible external contention. Each PCM serial-input interface can support multiple channels, typically from one to eight. In the simplest scenario, only one channel is accepted uniquely on either subframe. In a more robust scenario, each of the subframes can carry multiple channels, depending on the SCLK oversampling rate and the PCM word size. The CS4923 can accept serial PCM at a different sample rate than that of the PCM output interface. In these cases, the CS4923 can sample-rate convert the PCM input channel to the output rate and variably mix the PCM input into the PCM output. For specific PCM input configuration details, see the *CS4923 User's Guide*.

Byte-Wide PCM Input

In parallel host mode, the CS4923 can accept PCM data through the byte-wide host interface. In this mode, there is a close connection between the run-time CS4923 software and the host processor that is delivering the PCM data. The PCMRST bit of the CONTROL register provides absolute software/hardware synchronization. PCMRST initializes the input channel to uniquely recognize the first write to the byte-wide PCMDATA port. In this fashion, the CS4923 can translate successive byte writes into a variable number of channels with a variable PCM sample size. In the simple case, the CS4923 can receive stereo 8-bit PCM one byte at a time with the internal DSP assigning the first 8-bit write (after PCMRST) to the left channel and the second 8-bit write to the right channel. For 16-bit PCM, it assigns the first two 8-bit writes (after PCMRST) to the left channel and the next two writes to the right channel.

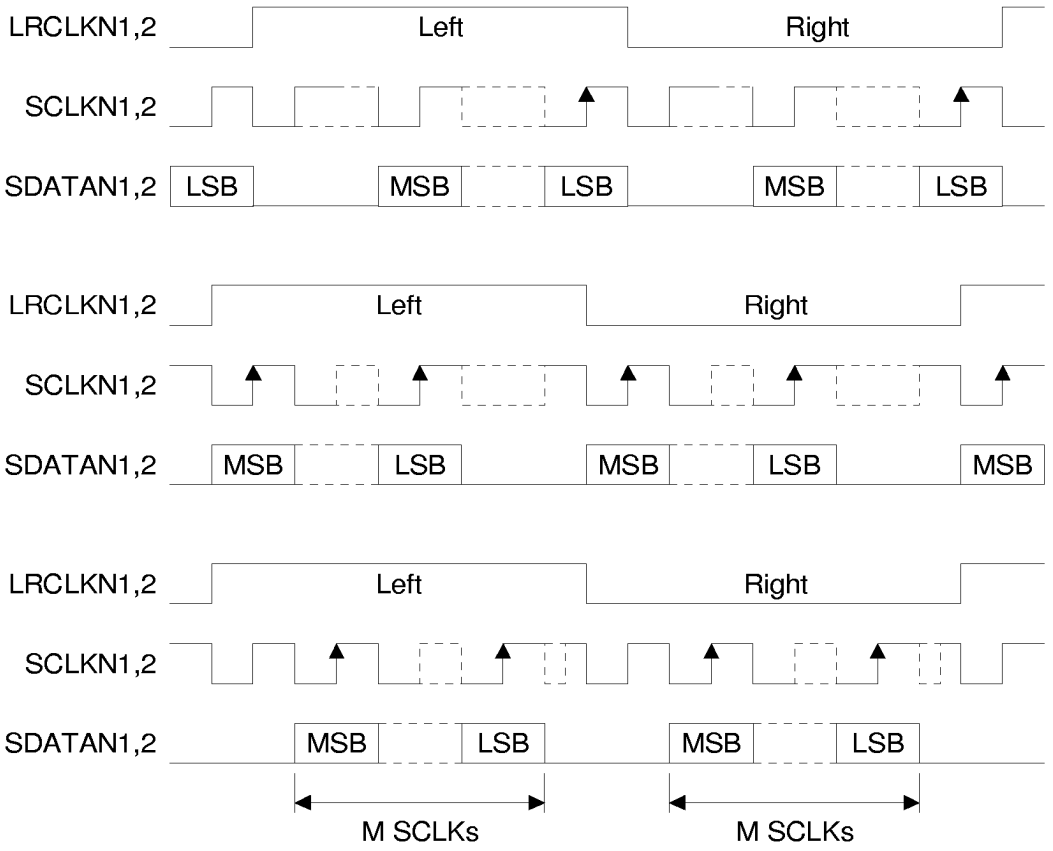
IEC60958 Single-Wire PCM Input

The CS4923 can directly accept a serial, biphase-encoded input on the RCV958 signal pin. Except for the CMOS-level characteristics of the serial-input pin, the input functionality is compatible with the IEC60958 interface, including extended channel-status-bit collection for delivery to the internal DSP. This input port is also configurable to accept: 1) varying PCM word widths of one channel on either subframe, or 2) two channels with one channel accepted from each subframe.

In the IEC60958 mode, the CS4923 recovers the bit clock from the input and provides that clock to the clock manager section of the chip. The clock manager performs overall synchronization of the input rate, derives the DSP clock speed, and selects the output sample-rate clocks. Typically, the sample-rate clock is a phase -locked and divided version of the DSP clock. An oversampled bit-rate clock output can be made available externally on the following CS4923 signal pins: MCLK, SCLKN1, SCLKN2, and SCLK.

Digital Audio/Digital Data Outputs

The CS4923 offers a programmable output interface capable of supporting most industry-standard serial digital interfaces in either master or slave clock modes. The four digital-audio output data pins are AUDATA2, AUDATA1, AUDATA0, and XMT958. The AUDATA2–AUDATA0 output-signal pins are typically connected to external digital-to-analog converters. The CS4923 performs synchronization of the AUDATA2–AUDATA0 output pins with the MCLK, SCLK, and LRCLK bidirectional signal pins. In addition to the common serial-digital interface, the CS4923 has a serial-digital transmitter port that uses the XMT958 output pin. This pin can deliver data with one line in compliance with the IEC-958 specification except that the output is single ended CMOS levels. Typically, the IEC-958 interface connects external audio products.



M = 24 bits maximum, illustrated here with SCLK configured for rising edge.

Figure 5. 2-Channel Per Line Audio Input Formats

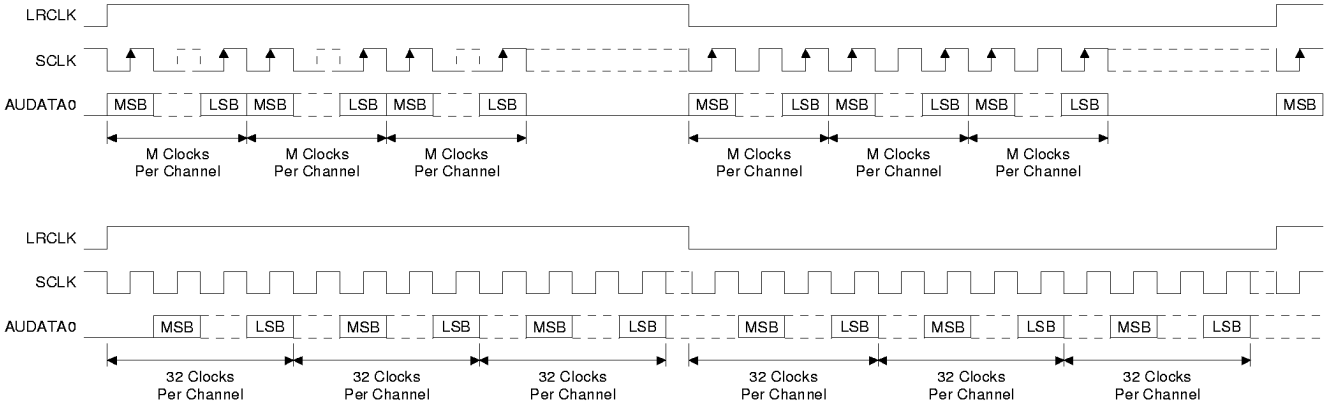


Figure 6. Multichannel Per Line Audio Input Formats

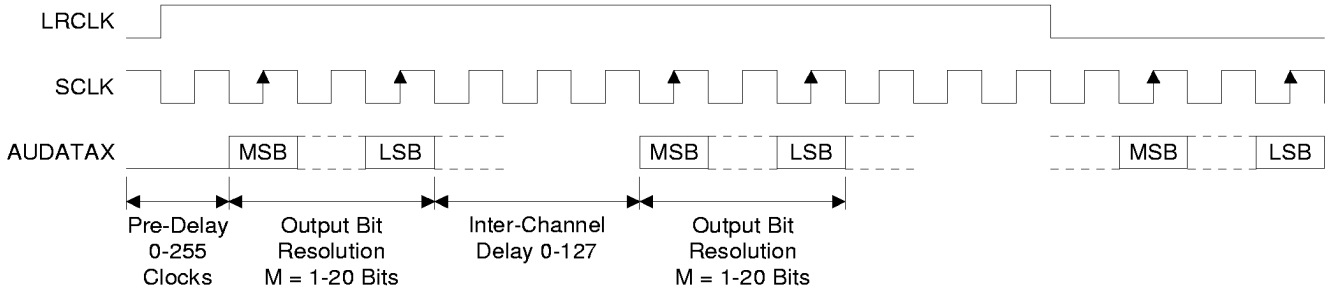


Figure 7. Serial Digital Audio Output Configuration Parameters

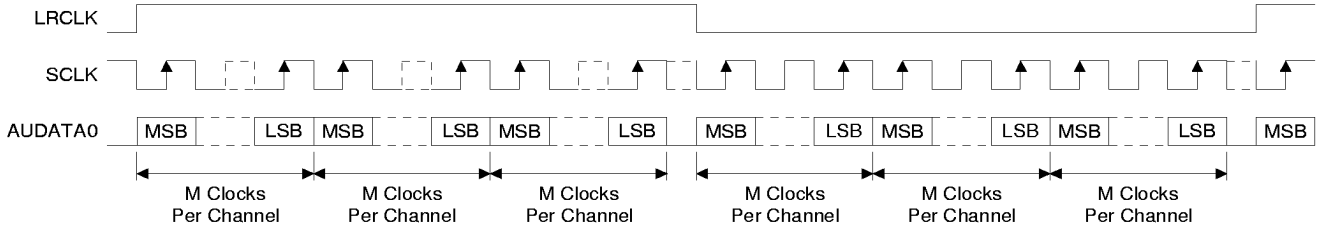


Figure 8. 6-Channel Per Line Serial Audio Output Modes 0 or 4 with Pre-Delay = 0 and Interchannel Delay = 0

Output Mode	LRCLK = 0	LRCLK = 1	Notes
0	AUDATA0 = Channels 1, 3, 5	AUDATA0 = Channels 0, 2, 4	6 channels on one line
1	AUDATA0 = Channels 1, 3 AUDATA1 = Channel 5	AUDATA0 = Channels 0, 2 AUDATA1 = Channel 4	4 channels on one line plus 2 channels on second line
2	AUDATA0 = Channels 1, 3 AUDATA2 = Channel 5	AUDATA0 = Channels 0, 2 AUDATA2 = Channel 4	4 channels on one line plus 2 channels on second line
3	AUDATA0 = Channel 1 AUDATA1 = Channel 3 AUDATA2 = Channel 5	AUDATA0 = Channel 0 AUDATA1 = Channel 2 AUDATA2 = Channel 4	3x (2 channels per line)
4	AUDATA0 = Channels 0, 2, 4	AUDATA0 = Channels 1, 3, 5	6 channels on one line
5	AUDATA0 = Channels 0, 2 AUDATA1 = Channel 4	AUDATA0 = Channels 1, 3 AUDATA1 = Channel 5	4 channels on one line plus 2 channels on second line
6	AUDATA0 = Channels 0, 2 AUDATA2 = Channel 4	AUDATA0 = Channels 1, 3 AUDATA2 = Channel 5	4 channels on one line plus 2 channels on second line
7	AUDATA0 = Channel 0 AUDATA1 = Channel 2 AUDATA2 = Channel 4	AUDATA0 = Channel 1 AUDATA1 = Channel 3 AUDATA2 = Channel 5	3x (2 channels per line)

Table 3. Serial Digital Audio Channel Modes

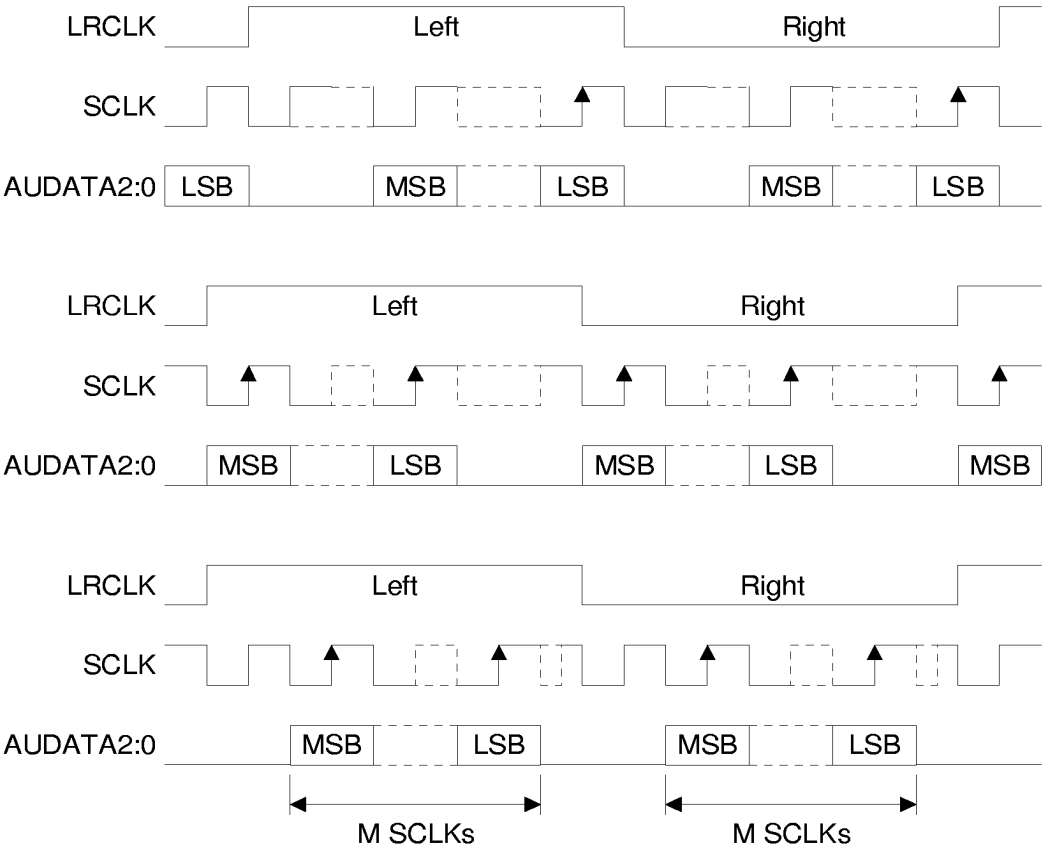


Figure 9. Most Popular 2-Channel Per Line Audio Output Formats in Modes 3 and 7

Notes:
1. Illustrated here—SCLK configured for rising edge valid; SCLK can also be configured for falling edge valid
2. MCLK is the master serial audio clock input/output or the DSP clock output.
3. MCLK as output for serial output can be 128 Fs, 256 Fs, or 512 Fs.
4. MCLK can be input at 128 Fs, 256 Fs, 384 Fs or 512 Fs to divide for SCLK and LRCLK output.
5. SCLK and LRCLK can be input or output and can be asynchronous to MCLK.
6. SCLK can be divided to 32 Fs or 64 Fs for all MCLK rates.
7. SCLK can be divided to 48 Fs if MCLK is 384 Fs.
8. SCLK can be divided to 128 Fs or 256 Fs if MCLK is 256 Fs or 512 Fs.
9. SCLK can be divided to 512 Fs only if MCLK is 512 Fs.
10. M can be a maximum of 20 bits.

PCM Serial Data Outputs

The PCM serial-audio-data port consists of the AUDATA2–AUDATA0 outputs along with the MCLK, SCLK, and LRCLK bidirectional synchronization signal pins. The bidirectionality of the synchronization pins allows the CS4923 to operate in both master and slave modes.

In master mode, the CS4923 clock manager generates the MCLK output signal, which is internally subdivided to create the SCLK and LRCLK outputs, which in turn are used to clock the output FIFOs. As an output, MCLK is firmware configurable to provide either a 128, 256, or 512 Fs clock, where Fs is the output sample rate. LRCLK is the output sample rate, which is internally programmable in the clock manager or provided as an input to the CS4923. In addition, SCLK is also configurable in master mode output. Table 4 lists all of the possible master-mode MCLK and SCLK ratios. For specific PCM digital-audio-output configuration details, see the *CS4923 User's Guide*.

MCLK (Fs)	SCLK (Fs)					
	32	48	64	128	256	512
128	X		X			
384**	X	X	X			
256	X		X	X	X	
512	X		X	X	X	X

Table 4. MCLK/SCLK Master Mode Ratios

** For MCLK as an input only.

There are two different types of slave-mode-output configurations. The external MCLK mode is the capability to input MCLK to the CS4923. In this mode, the SCLK and LRCLK outputs are created by internal division just as though MCLK was delivered from the internal clock manager. The total slave mode is completely independent of MCLK. In the total slave mode, SCLK and LRCLK are inputs to the output block and clock data from the output FIFO ports directly, just as if they were delivered from the output manager.

The serial-digital-output channel mode table lists eight primary output channel configurations. Simply put, the AUDATA0 signal can deliver either six, four, or two channels. AUDATA1 and AUDATA2 are restricted to two channels each. Table 5 lists the PCM output channel allotments.

Mode	AUDATA0	AUDATA1	AUDATA2
Six channels on one line	6	0	0
Quad on one plus two on second	4	2	0
Quad on one plus two on second	4	0	2
Triple stereo	2	2	2

Table 5. PCM Output Channel Allotments

Serial-digital-audio data-bit placement and sample alignment is fully configurable in the CS4923, including left flush, right flush, delay bits or no delay bits, variable sample-word sizes, variable output-channel count, programmable output-channel pin assignments, along with the clock-edge polarity necessary to provide glueless hookup to all popular DACs. Figure 7 provides an overview of the interface functionality. For specific PCM output-configuration details, see the *CS4923 User's Guide*.

IEC-958 Output

The CS4923 has a transmitter port that is fully compatible with IEC-958, except that the output is CMOS level and not a differential or optical output. Typically, the XMT958 output pin is externally connected to a transformer or opto-coupler to solidify the connection of audio equipment. The XMT958 output can be clocked with the internal clock manager or clocked from MCLK in slave mode if MCLK is 256 Fs or 512 Fs. The transmitter functionality is fully programmable by the firmware and can be used for multiple purposes. Simply put, the XMT958 output can consist of two channels of PCM or Dolby Digital compressed data in accordance with ATSC Specification Annex B. The CS4923 can support all channel-status and

user-data modes including all biphase encoding requirements. For specific PCM and Dolby Digital bitstream output-configuration details, see the *CS4923 User's Guide*.

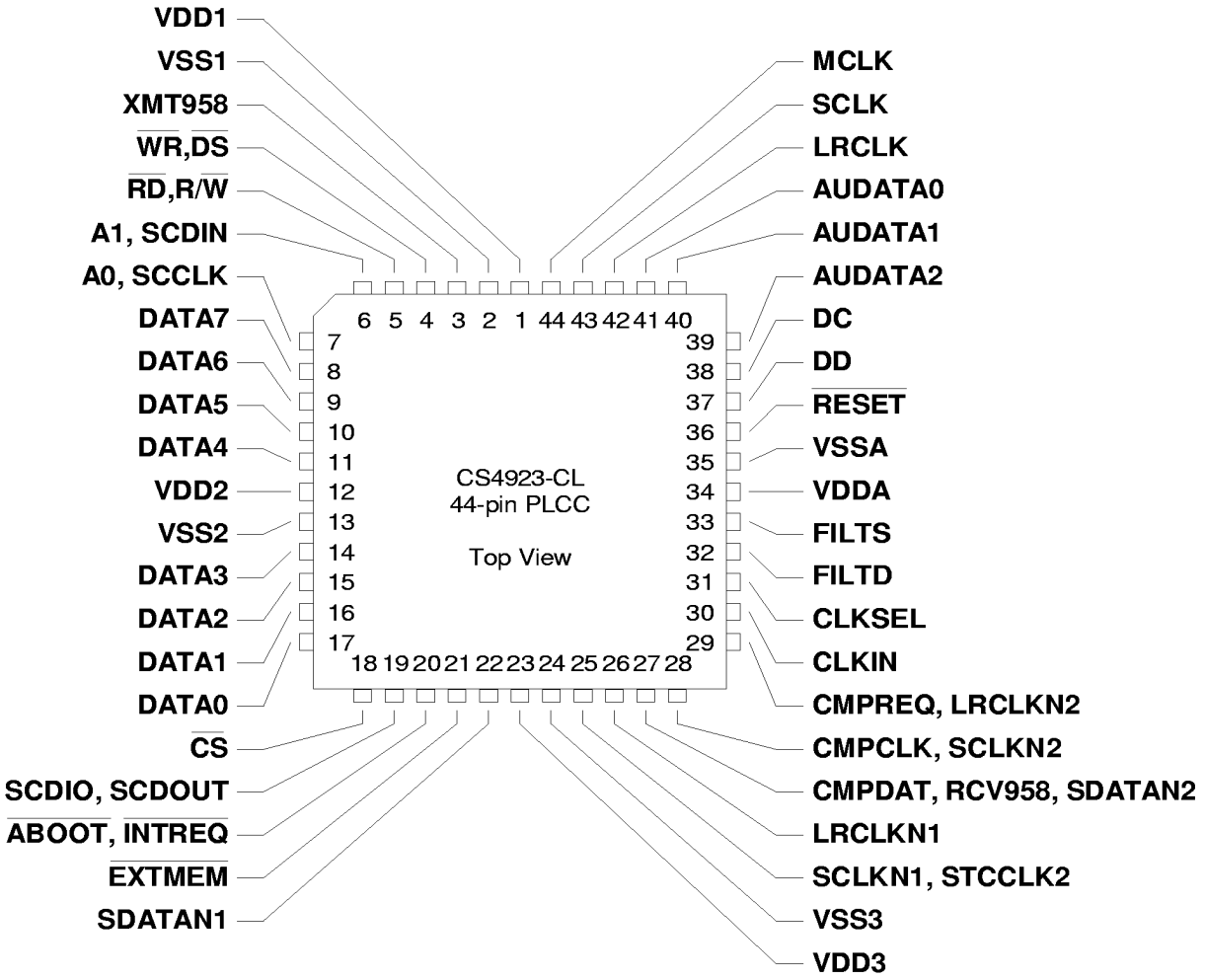
Clock Manager

The CS4923 clock manager is a programmable PLL clock synthesizer that takes an input reference clock and produces all the internal clocks required to run the internal DSP and to provide master mode timing to the audio input/output peripherals. The clock manager also includes a 33-bit system time clock (STC) and a general-purpose timer to support general audio and video synchronization and firmware task scheduling.

The clock manager is completely controllable by the internal DSP with firmware and by host messages. The PLL can be internally bypassed by connecting the CLKSEL pin to VDD. This connection multiplexes the CLKIN pin directly to the DSP core clock. For clocking requirements, see the detailed electrical section of this data sheet.

The PLL reference clock has four possible sources that are routed through a multiplexer controlled by the DSP firmware or host messages: RCV958, SCLKN2, SCLKN1, and CLKIN. Typically, in MPEG environments, the CLKIN pin is connected to 27 MHz. In other scenarios, the PLL can be clocked with even multiples of the desired sampling rate or with an already available clock source. The most common input frequencies range from 32 kHz to 49.152 MHz. Given the total dependence on proper PLL operation, the PLL is only controllable from the DSP application software or the on-chip ROM code. For command setup and control of the internal PLL, see the *CS4923 User's Guide*.

PIN DESCRIPTIONS



VDDA—Analog Positive Supply: Pin 34

Analog positive supply for clock generator. Nominally +3.3 V.

VSSA—Analog Supply Ground: Pin 35

Analog ground for clock generator PLL.

VDD1, VDD2, VDD3—Digital Positive Supply: Pins 1, 12, 23

Digital positive supplies. Nominally +3.3 V.

VSS1, VSS2, VSS3—Digital Supply Ground: Pins 2, 13, 24

Digital ground.

FILTS—Phase-Locked Loop Filter Cap Positive: Pin 33

Connects to an external filter capacitor for the on-chip phase-locked loop.

FILTD—Phase Locked Loop Filter Cap Negative: Pin 32

Connects to an external filter capacitor for the on-chip phase-locked loop.

CLKIN—Master Clock Input: Pin 30

Connects to the input of the clock manager PLL. The DSP clock is connected to the PLL output when the CLKSEL pin is set low. When CLKSEL is high, CLKIN directly connects to the internal DSP clock.

CLKSEL—DSP Clock Select: Pin 31

CLKSEL low selects the clock-manager PLL output as the DSP clock. CLKSEL high selects CLKIN directly from the input as the internal DSP clock.

DATA7 (or EMAD7 or GPIO7)—Pin 8
DATA6 (or EMAD6 or GPIO6)—Pin 9
DATA5 (or EMAD5 or GPIO5)—Pin 10
DATA4 (or EMAD4 or GPIO4)—Pin 11
DATA3 (or EMAD3 or GPIO3)—Pin 14
DATA2 (or EMAD2 or GPIO2)—Pin 15
DATA1 (or EMAD1 or GPIO1)—Pin 16
DATA0 (or EMAD0 or GPIO0)—Pin 17

In parallel host mode, these pins provide bidirectional operation. If a serial host mode is selected, these pins can provide a multiplexed address and data function for connecting an 8-bit external memory. Otherwise, in serial host mode, these pins can act as general-purpose input or output pins that can be individually configured and controlled by the internal DSP.

A0, SCCLK—Host Parallel Address Bit Zero or Serial Control Port Clock: Pin 7

In parallel host mode, this pin serves as an address input pin to help select one of four parallel registers. In serial host mode, this pin serves as the serial data clock signal, specifically as the SPI clock input or the I^2C clock input.

A1, SCDIN—Host Address Bit One or SPI Serial Control Data Input: Pin 6

In parallel host mode, this pin serves as an address input pin to help select one of four parallel registers. In SPI serial host mode, this pin serves as the data input.

$\overline{RD}$, R/$\overline{W}$, $\overline{EMOE}$, GPIO11—Host Parallel Output Enable or Host Parallel R/$\overline{W}$ or External Memory Output Enable or General Purpose Input & Output Number 11: Pin 5

In Intel parallel host mode, this pin serves as the active-low data-bus-enable input. In Motorola parallel host mode, this pin serves as the read-high, write-low input signal. In serial host mode, this pin serves as the external memory active-low data-enable output signal. Also in serial host mode, this pin acts as a DSP-addressable-control-register external input or output bit.

$\overline{WR}$, $\overline{DS}$, $\overline{EMWR}$, GPIO10—Host Write Strobe or Host Data Strobe or External Memory Write Enable or General Purpose Input & Output Number 10: Pin 4

In Intel parallel host mode, this pin serves as the active-low data-write-input strobe. In Motorola parallel host mode, this pin serves as the active-low data-strobe-input signal. In serial host mode, this pin serves as the external-memory active-low write-enable output signal. Also in serial host mode, this pin acts as a DSP-addressable-control-register external input or output bit.

$\overline{CS}$—Host Parallel Chip Select, Host Serial SPI Chip Select: Pin 18

In parallel host mode, this pin serves as the active-low chip-select input signal. In serial host SPI mode, this pin is used as the active-low chip-select input signal.

$\overline{RESET}$—Master Reset Input: Pin 36

Asynchronous active-low master-reset input. Reset should be low at power-up to initialize the CS4923 and to guarantee that the device is not active during initial power-on stabilization periods. Reset can also reinitialize the CS4923 during normal operation with nominal supply voltages. Reset also initializes and selects the host interface and initiates an automatic boot cycle if serial host mode is selected and $\overline{ABOOT}$ is low. Reset being low disables the outputs of all the bidirectional pins, forcing them into a high-Z input mode.

SCDIO, SCDOUT, PSEL, GPIO9—Serial Control Port Data Input and Output, Parallel Port Type Select: Pin 19

In serial control port mode, this pin serves as the open-drain bidirectional data pin for the I^2C serial host control port or the data output pin for the SPI serial host control port. In parallel host mode, this pin is sampled at the rising edge of $\overline{RESET}$ to configure the parallel host mode as an Intel type bus or as a Motorola type bus. In parallel host mode, after the bus mode has been selected, the pin can function as a general-purpose input or output pin that is uniquely addressable by the DSP.

$\overline{EXTMEM}$, GPIO8—External Memory Chip Select or General Purpose Input & Output Number 8: Pin 21

In serial control port mode, this pin acts as an output to provide an independent chip-select capability to connect external byte-wide RAM or ROM. In parallel and serial host mode, this pin can also function as a general-purpose input or output pin that is uniquely addressable by the DSP.

$\overline{INTREQ}$, $\overline{ABOOT}$—Control Port Interrupt Request, Automatic Boot Enable: Pin 20

Open-drain control-port interrupt-request output that is addressable by the DSP. In serial port mode, this pin functions as a request line prompting further communication or for initiating dialog between the host and the DSP. Also in serial host mode, this signal initiates an automatic boot cycle from external memory if it is held low as the CS4923 transitions from a reset state.

AUDATA2—Digital Audio Output 2: Pin 39

PCM multiformat digital-audio data output, capable of only two-channel 20-bit output. This PCM output defaults to VSS as output until enabled by the DSP software.

AUDATA1—Digital Audio Output 1: Pin 40

PCM multiformat digital-audio data output, capable of only two-channel 20-bit output. This PCM output defaults to VSS as output until enabled by the DSP software.

AUDATA0—Digital Audio Output 0: Pin 41

PCM multiformat digital-audio data output, capable of two-, four-, or six-channel 20-bit output. This PCM output defaults to VSS as output until enabled by the DSP software.

MCLK—Audio Master Clock: Pin 44

Bidirectional master audio clock. In audio master timing mode, MCLK is an output from the CS4923 that provides an oversampled audio-output clock at either 128 Fs, 256 Fs, or 512 Fs. MCLK is used by the output formatter and the XMT958 digital transmitter port. In slave mode, the user can input MCLK at 128 Fs, 256 Fs, 384 Fs, or 512 Fs, which then can be used to sequence the digital-audio output interface, including the division and output of SCLK and LRCLK.

SCLK—Audio Output Bit Clock: Pin 43

Bidirectional digital-audio output bit clock. In output master timing mode or MCLK slave mode, SCLK is an output that is divided from MCLK to provide 32 Fs, 64 Fs, 128 Fs, 256 Fs, or 512 Fs, depending on the MCLK rate and the digital-output configuration. In total slave mode, SCLK is an input and can be any common bit clock rate. In total slave mode, SCLK is totally independent of MCLK. SCLK defaults to an input upon reset.

LRCLK—Audio Output Sample Rate Clock: Pin 42

Bidirectional digital-audio output-sample-rate clock that is always synchronous with SCLK. In output master timing mode or MCLK slave mode, LRCLK is an output that is divided from MCLK to provide the output sample rate depending on the output configuration. In total slave mode, LRCLK is an input and can be totally asynchronous to the other clocks, including MCLK. LRCLK defaults to an input upon $\overline{\text{RESET}}$ low.

XMT958—SPDIF Transmitter Output: Pin 3

Logic-level output that contains a biphase-encoded clock for synchronously outputting two channels of PCM digital audio or a Dolby Digital compressed-data interface or both. This output typically connects to the input of an RS-422 transmitter or to the input of an optical transmitter.

SCLKN1, STCCLK2—PCM Audio Input Bit Clock: Pin 25

Bidirectional digital-audio PCM bit clock that is an output in master mode and an input in slave mode. SCLKN1 defaults to an input upon $\overline{\text{RESET}}$ low. In slave mode, SCLKN1 can operate totally asynchronous from the CS4923 clock generator. In master mode, SCLKN1 is derived from the CS4923 internal clock generator. In either master or slave mode, the active edge of SCLKN1 can be programmed by the DSP. For applications supporting MPEG playback where a system time clock (STC) is required to support audio/video synchronization and CLKIN is not driven with a 27-MHz clock, this pin functions as STCCLK2, which provides a path for connecting the 27-MHz time-base clock directly to the internal STC counter.

LRCLKN1—PCM Audio Input Sample Rate Clock: Pin 26

Bidirectional digital-audio PCM input sample-rate clock that is an output in master mode and an input in slave mode. LRCLKN1 defaults to an input upon RESET low. LRCLKN1 delineates audio subframes. LRCLKN1 is derived from the CS4923 internal clock generator for master mode. In slave mode, LRCLKN1 can operate totally asynchronously from the CS4923 clock generator. In either master or slave mode, LRCLKN1 can be sampled with either edge of SCLKN1, depending on the SCLKN1 active-edge configuration.

SDATAN1—PCM Audio Data Input Number One: Pin 22

Multiformat/multichannel digital-audio PCM data input that can input from one to six channels of PCM, as well as inputting compressed data. SDATAN1 can be sampled with either edge of SCLKN1, depending on the SCLKN1 configuration. Data format for SDATAN1 is programmable.

CMPCLK, SCLKN2—PCM Audio Input Bit Clock: Pin 28

Bidirectional digital-audio PCM bit clock or compressed-data clock that is an output in master mode and an input in slave mode. SCLKN2 defaults to an input upon RESET low. In slave mode, SCLKN2 can operate totally asynchronously from the CS4923 clock generator. In master mode, SCLKN2 is derived from the CS4923 internal clock generator. In either master or slave mode, the active edge of SCLKN2 can be programmed by the DSP. If this pin is configured as CMPCLK, then it is used to clock CMPDAT into the CS4923 input buffer.

CMPREQ, LRCLKN2—PCM Audio Input Sample Rate Clock: Pin 29

Bidirectional multimode signal that can be used as a programmable-polarity compressed-data-request output signal (CMPREQ) in the serial compressed data input mode or the parallel host compressed data mode. If it is used for a digital-audio interface, LRCLKN2 functions as a bidirectional digital-audio PCM bit clock that is an output in master mode and an input in slave mode. LRCLKN2, CMPREQ defaults to an input upon RESET low. In slave digital audio mode, LRCLKN2 can operate totally asynchronously from the CS4923 clock generator. In master mode, LRCLKN2 is derived from the CS4923 internal clock generator. In either master or slave mode, LRCLKN2 can be sampled with either edge of SCLKN2 depending on the SCLKN2 configuration.

CMPDAT, RCV958, SDATAN2—PCM Audio Data Input Number Two: Pin 27

Multiformat/multichannel digital-audio PCM data input that can input from one to six channels of PCM as well as inputting compressed data. SDATAN2 can be sampled with either edge of SCLKN2 depending on the SCLKN2 configuration. SDATAN2 input can be programmed to be flush left or flush right. If configured for RCV958 mode, this pin provides an input for IEC60958/61937, accepting biphase-encoded compressed data or PCM or both. If the RCV958 input is used to recover data, then the CS4923 clock manager is slaved to the 64 Fs sample-rate clock recovered from the input.

DC—Reserved: Pin 38

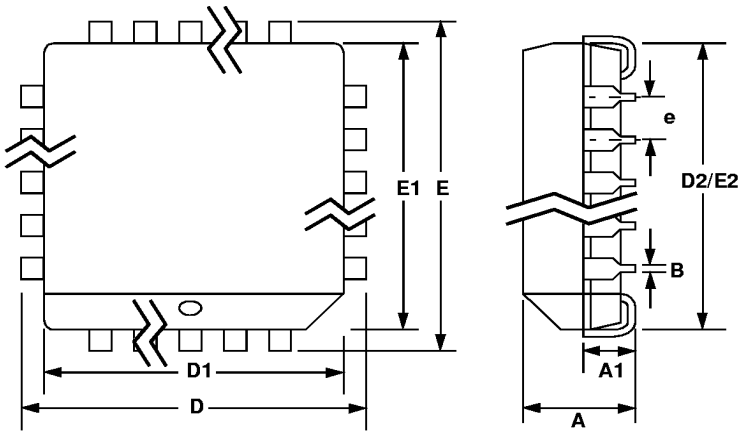
This pin is reserved and should be pulled up with an external 10k resistor.

DD—Reserved: Pin 37

This pin is reserved and should be pulled up with an external 10k resistor.

PACKAGE DIMENSIONS

44L PLCC PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.165	0.180	4.043	4.572
A1	0.090	0.120	2.205	3.048
B	0.013	0.021	0.319	0.533
D	0.685	0.695	16.783	17.653
D1	0.650	0.656	15.925	16.662
D2	0.590	0.630	14.455	16.002
E	0.685	0.695	16.783	17.653
E1	0.650	0.656	15.925	16.662
E2	0.590	0.630	14.455	16.002
e	0.040	0.060	0.980	1.524