Final

Am7960

Coded Data Transceiver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Universal Networking Transceiver
- High impedance interface to coupling transformer
  - User transparent Manchester encoding/decoding
  - Glitch-free power up/down
- "Modem-like" controller interface
- 32 dB dynamic range (transmit to receive)
- Transmit edge rate control
- Up to 3 Mbps data rate

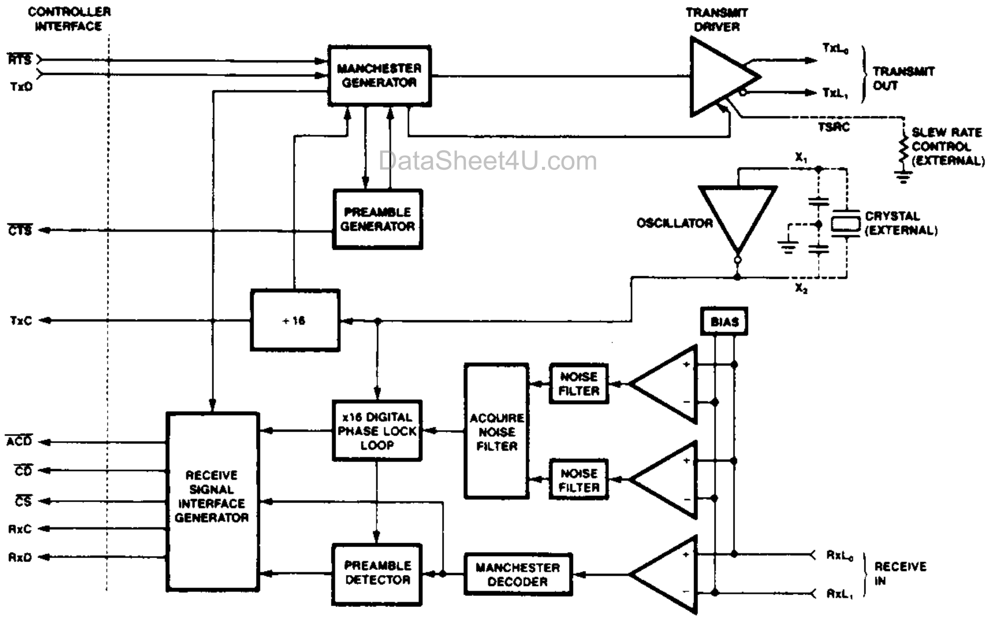
GENERAL DESCRIPTION

The Am7960 is a combined Manchester encoder/decoder and transceiver. It is designed for use in synchronous communications systems which require common mode isolation in point-to-point or common bus architecture, supporting data rates of up to 3 Mbps. This 5 V device provides 32 dB of dynamic range, and guarantees 2 V output into 37.5 Ω. A single external component controls the slew rate of the transmitter, and a signal qualifier in the receiver minimizes false starts improving reliability.

The Am7960 has a modem-like controller interface which makes it compatible with nearly every existing synchronous communications controller (USARTs, SCCs, etc).

The use of ECL circuitry to process signals internal to the Am7960 chip enhances device speed. I/O pins operate at TTL/MOS logic levels to allow convenient interfacing with other devices such as the AmZ8530* Serial Communications Controller.

BLOCK DIAGRAM



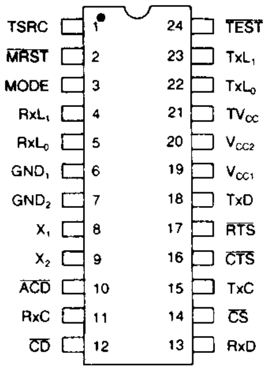
BD005440

RELATED AMD PRODUCTS

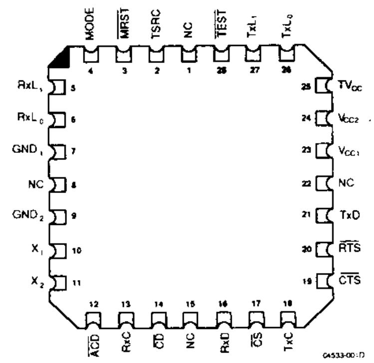
Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7992B	Serial Interface Adapter
Am7996	Ethernet Transceiver
AmZ8530	Serial Communications Controller
Am79C900	Integrated Local Area Communications Controller (ILACC)

Publication# 04533 Rev. D Amendment/0
Issue Date: June 1990

CONNECTION DIAGRAM
Top View



CD007050



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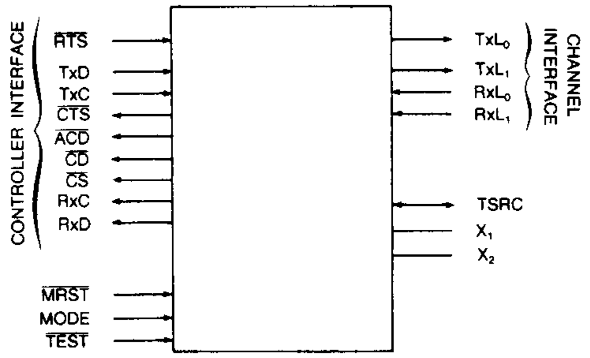
LOGIC SYMBOL



LS001951

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM7960 D C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
M = Military* (−55 to +125°C)

c. PACKAGE TYPE
D = 24-Pin Ceramic DIP (CD 024)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am7960 Coded Data Transceiver

Valid Combinations	
AM7960	DC, DCB, DMB, LC, LMB

*Military range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Controller Transmit Interface Signals

TxC Transmit Clock (Output)

Transmit Clock is the data transmit clock. All transmit interface signals are synchronized to this clock. This signal is always active.

TxD Transmit Data (Input)

Transmit Data is the serial data that will be Manchester encoded.

$\overline{\text{RTS}}$ $\overline{\text{Request to Send}}$ (Input)

The communication controller indicates that it wishes to transmit data by asserting Request to Send. Once started, only negating Request to Send can stop transmission.

$\overline{\text{CTS}}$ $\overline{\text{Clear to Send}}$ (Output)

The Am7960 asserts Clear to Send when it is ready to encode Transmit Data as line data.

Controller Receiver Interface Signals

RxC Receive Clock (Output)

Receive Clock is the data receive bit clock. All controller receive interface signals with the exception of Advance Carrier Detect are synchronized to this clock. It is negated after either End of Message or quiet line.

RxD Receive Data (Output)

Receive Data is the decoded serial receive data.

$\overline{\text{ACD}}$ $\overline{\text{Advance Carrier Detect}}$ (Output)

Advance Carrier Detect is asserted whenever the receiver has detected line activity. It is negated after there has been no line activity for 2 bit times (quiet line). During transmission Advance Carrier Detect is internally negated. This signal is asynchronous with both Transmit Clock and Receive Clock.

$\overline{\text{CD}}$ $\overline{\text{Carrier Detect}}$ (Output)

Carrier Detect is asserted after internal clock acquisition and immediately before asserting Receive Clock. It is negated after either End of Message or quiet line.

$\overline{\text{CS}}$ $\overline{\text{Carrier Sense}}$ (Output)

Carrier Sense is asserted immediately before the first receive data bit and negated after either a Manchester coding violation or quiet line.

Channel Interface Signals

TxL_0, TxL_1 Transmit Outputs (Output)

The difference between these outputs (TxL_0 - TxL_1) is the channel transmit signal. A single external resistor controls the slew rate of the transmitter.

TV_{CC} Transmit Power Supply

The transmitter has a separate 5.0-volt nominal power supply input.

TSRC Slew Rate Control (I/O)

This pin is used to control the transmit slew rate with an external resistor (typically 1 kΩ to 3 kΩ for 1 Mbps operation) connected to ground.

RxL_0, RxL_1 Receiver Inputs (Input)

The difference between these inputs (RxL_0 - RxL_1) is the channel receive signal.

Global Signals

$\overline{\text{MRST}}$ $\overline{\text{Master Reset}}$ (Input)

Master Reset is an asynchronous transceiver reset. When asserted, all interface signals will be inhibited with the exception of Transmit Clock. It has an internal pullup resistor, internal discharge clamp diode, and input hysteresis to provide power-on reset with a single external capacitor to ground.

MODE Mode Control (Input)

Mode Control determines if the Am7960 will internally generate and recognize line preamble. When LOW, the Mode Control is in Mode 0 and uses preamble. When HIGH, the Mode Control is in Mode 1 and is preamble transparent. This input has an internal pullup resistor.

$\overline{\text{TEST}}$ $\overline{\text{Test Control}}$ (Input)

Test Control is not a user function. This input is used to functionally test the device. It has an internal pullup resistor connected to V_{CC} and should always be left open or tied high during normal operation.

X_1, X_2 Crystal Oscillator Connections

X_1 and X_2 are the Crystal Oscillator Connections. The Am7960 can be operated either by using a crystal or by driving the X_1 pin with an external TTL clock.

V_{CC1}, V_{CC2} Power Supply

V_{CC1} and V_{CC2} are 5.0-volt nominal power supply pins. V_{CC1} powers TTL and V_{CC2} powers ECL circuitry.

GND_1 Ground Pin (TTL and Transmit)

GND_2 Ground Pin (ECL)

FUNCTIONAL DESCRIPTION

The Am7960 encodes data and clock into a standard Manchester serial bit stream. Every bit cell is divided into two parts with a logic level transition at its midpoint. The direction of the transition represents the cell's logic state. Thus, a "1" bit is encoded as a 0 followed by a 1; a "0" bit is represented as a 1 followed by a 0. Line End of Message is encoded into an illegal Manchester signal–transmit output is held at a logic 1 level for two entire bit times. In Mode 0, the 32-bit preamble consists of a Manchester 1 followed by 30 bits of alternating Manchester 0 and 1 bits followed by a final 1 (i.e., the last four bits of preamble will be Manchester 1011).

The Am7960 has two operating modes: Mode 0 and Mode 1. When transmitting, Mode 0 i nserts a 32-bit preamble, Manchester encodes the transmit data, and appends End Of Message. When receiving, Mode 0 identifies and removes preamble, decodes the Manchester line data, and removes End Of Message. Mode 1 is identical to Mode 0 except preamble is neither generated on transmit nor detected upon reception; the Coded Data Transceiver simply passes data (bit for bit) onto the media and recovers it at the destination. Mode 1 requires an externally generated preamble of at least 5 bits, with the first four or more bits alternating between 0 and 1 or 1 and 0. The sixth bit received is the first to appear on RxD. One of these two modes will interface to almost all existing synchronous controllers.

Transmit

The Am7960 has a modem-like controller interface. Transmission is initiated by asserting Request To Send. Once started, only negating Request To Send or bringing $\overline{MRST}$ low can stop transmission. All receive signals are active with the exception of Advance Carrier Detect which will be off for the duration of the transmission. In either mode, Clear-To-Send is activated one transmit clock cycle before Transmit Data (TxD) is encoded as line data.

Receive

The Receiver has three status lines: Advance Carrier Detect, Carrier Detect, and Carrier Sense. Advance Carrier Detect indicates that the receiver is detecting line activity. It is asynchronous with both Transmit Clock and Receive Clock. Advance Carrier Detect is asserted for line signals above the Positive Presence Level or below the Negative Presence Level. Once asserted, Advance Carrier Detect will remain active until line signal is absent for 2 bit times (quiet line).

After the Am7960 has detected an active line, it attempts to acquire Receive Clock. Clock qualification is achieved by sampling the Presence Levels. To qualify, a line signal must either be above the Positive Presence Level and then go below the Negative Presence Level or below the Negative Presence Level and then go above the Positive Presence Level in ¾ to 1¼ bit times (i.e., two adjacent line transitions must be separated by between ¾ and 1¼ bit times).

Advance Carrier Detect indicates that the Am7960 has an internally acquired clock. Receive Clock will be active whenever Carrier Detect is active. Carrier Detect will remain active until either the line is quiet or End Of Message is detected.

Carrier Sense becomes active when the Am7960 intends to transmit Receive Data to the controller. Carrier Sense stays active until either the line is quiet or an invalid Manchester cell is detected. Receive Data is OFF until Carrier Sense becomes active and remains active until Carrier Detect becomes inactive.

The Am7960 decodes the line data by sampling the ¼ and ¾ bit intervals with respect to the start of the cell. If these samples are opposite, valid Manchester data has been decoded. If these samples are the same and the next ¼ sample is the same, the receiver has detected End Of Message.

In Mode 0, valid preamble is defined as at least seven receive clocks, the last four as decoded Manchester 1 0 1 1. Until this criteria is met, the Am7960 will continue to hunt for preamble.

Channel

The transmitter/receiver interface has been designed to provide a high impedance, low capacitance channel interface. There is a provision to externally control the slew rate of the transmit signals. Slew limiting the transmit signal decreases the presence of undesired harmonic frequencies, reducing the amount of energy radiating from the transmission media. Transmit outputs are optimized to drive transformer-isolated data lines, providing high common mode isolation between nodes.

The receiver provides a high impedance input over the total input operating range. A common mode voltage reference minimizes the number of external components needed for use with coupling or isolation transformers. The receiver's high input sensitivity and large dynamic range allows reception of both large (near end) and small (far end) signals. Its range also allows for operation immediately adjacent to an active transmitter without overload damage.

Oscillator

The internal oscillator runs at 16 times the data rate. This oscillator can be driven from an external clock source or can operate with a crystal in either the fundamental or third overtone parallel resonance mode. AMD recommends crystals with a tolerance better than ±0.05%.

APPLICATIONS

Design Guidelines for the Am7960

Transformer Isolation and Data Encoding

The Am7960 is optimized to drive isolation transformers. Static shielded transformers provide high common mode isolation between each Am7960 and the network media, supply a discharge path for high AC voltages caused by lightning or static discharge, and are effective narrow band filters, preventing low frequency noise from reaching the receive inputs and improving a network's signal-to-noise ratio.

Several transformer configurations are acceptable for use with the Am7960. A single-secondary transformer may be used (with receiver and transmitter connected in parallel) to provide low-cost isolation. Some improvement in isolation and common mode range may be achieved using a dual-secondary transformer at higher cost.

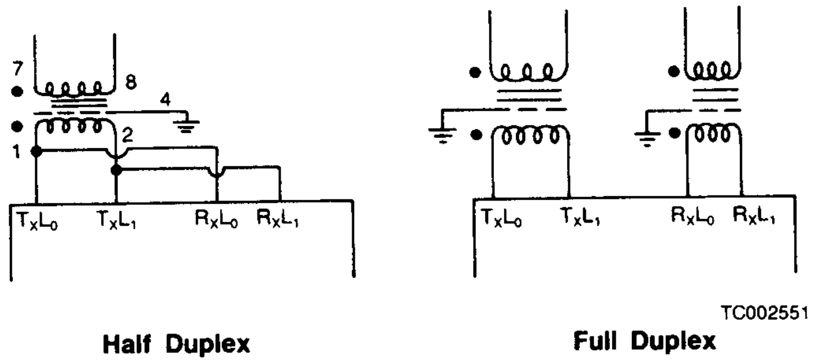


Figure 1. Pulse Engineering PE5156X or Equivalent Transformer (For 1 Mbps or Greater Data Rate)

To gain the benefit of transformer isolation, the Am7960 incorporates data encoding which bandlimits the frequencies of transmitted information. This is necessary because transformers act as a bandpass filter - they cannot pass DC or extremely high frequencies. NRZ data can change states at a rate anywhere from 0 Hz (many "1's" or "0's" strung together) to the data rate (alternating "1's" and "0's"). Any encoding scheme which is self-clocking (clock and data combined into one signal) eliminates the problem of trying to pass DC through an isolation transformer. Manchester encoding was selected for use in the Am7960 for several reasons:

1. The modulation rate (rate at which the signal changes states) of Manchester data is tightly limited. It ranges from a low equal to the data rate (alternating "1's" and "0's") to a high of twice the data rate (all "1's" or all "0's").

2. In each bit cell, the signal is high for half the time and low for the other half. Therefore, Manchester data has a constant DC component and is less likely to suffer from low frequency "bias" distortion ("line twist").

3. Manchester encoding/decoding is relatively inexpensive to realize in silicon.

Since ideal Manchester data has limited low-frequency content, noise immunity of the receiver is improved. The receiver needs only to look for high-frequency information in a narrow band (f to 2f).

Slew Rate Control

A single external resistor (R_{SRC}) connected from pin 1 (TSRC) to ground controls the Am7960's transmit slew rate. A fast slew rate minimizes power consumption of the Coded Data Transceiver and reduces the amount of a network's jitter budget allocated for line noise.

However, in applications where EMI/RFI radiation is a problem, each state transition should slew for approximately 33% of a data period. This produces a straight-line approximation of a sine wave. Since a sine wave by definition has no harmonic content, the straight-line approximation ensures that few higher order harmonics are generated and less energy is radiated.

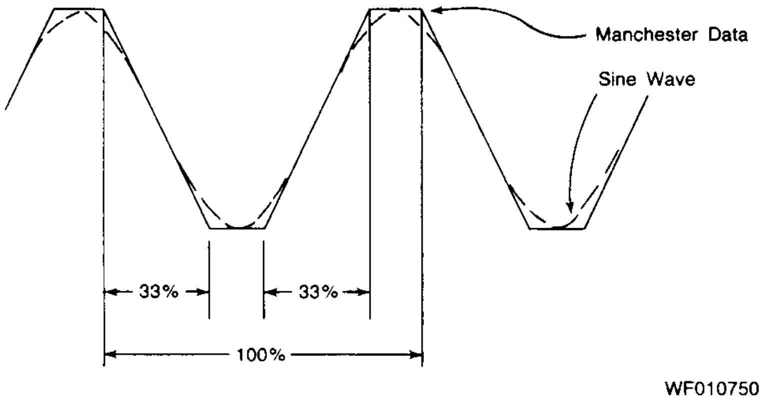


Figure 2. Manchester Data and Sine Wave

The actual slew rate realized in a network depends on the load capacitance driven by the transmitter as well as the value chosen for R_{SRC}. Since the slew rate is influenced by such network variables as cable type and length, the following equation should be used only to get an approximate value for R_{SRC}. This equation is correct when driving a purely resistive load and assumes that the user wishes the transmitted waveform to slew for 33% of a data period.

$$R_{SRC} \cong \frac{4.0}{\text{Data Rate (in Mbps)}} \text{ k}\Omega$$

where $500 \text{ Kbps} \leq \text{Data Rate} \leq 3 \text{ Mbps}$
and $1 \text{ k}\Omega \leq R_{SRC} \leq 8.0 \text{ k}\Omega$

The range of slew rate control on the Am7960 is limited. R_{SRC} must be above 0.5 kΩ; bit transitions can be adjusted to meet the 33% rule for data rates of 500 Kbps to 3 Mbps. The device can be used outside this range, but transmitted data will have higher than optimal harmonic content.

Oscillator

The Am7960 contains an inverting amplifier intended to form the basis of a pierce oscillator. The oscillator synchronizes internal logic and runs at 16 times the data rate. In designing this oscillator, it is necessary to consider several factors related to the application.

The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the Am7960 is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystals are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO).

Absolute frequency accuracy must also be considered. The resonant frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32 pF), or to specify the load when ordering a special crystal. It is then possible to determine from the crystal characteristics the load tolerance to maintain a given accuracy. If the "set-on" error due to load tolerance is unacceptable, a trimmer capacitor should be incorporated for fine adjustment.

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained, crystal oscillators operate at their fundamental frequency. However, crystals are not generally available with fundamental frequencies above 20 - 25 MHz. At higher frequencies, an overtone oscillator must be used. In this case, the crystal is designed to oscillate efficiently at one of its odd harmonic frequencies, and additional components are included in the oscillator circuit to prevent it from oscillating at lower harmonics.

First Harmonic (Fundamental) Oscillator: The circuit of a typical first harmonic oscillator is shown in Figure 3. The crystal load is comprised of the two 56-pF capacitors in series. This 28 pF plus stray capacitances approximates the standard 32-pF crystal load. If a closer match is required, then one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer. The nominal value of the combination should be 60 pF to provide proper crystal loading.

A typical crystal specification for use in this circuit is:

Frequency Range:	6 - 24 MHz
Resonance:	Parallel Mode
Load:	32 pF
Stability:	.01% or to match system requirements

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.

Third Harmonic Oscillator: For frequencies greater than 24 MHz, a crystal can be operated at its third harmonic. A typical circuit is shown in Figure 4. Two additional components are included: an inductor (L_1) and a capacitor (C_3). The purpose of the capacitor is to block the DC path through the inductor and thereby maintain the correct amplifier bias. C_3 should be large (> 1000 pF).

The inductor forms a parallel tuned circuit with C_1. This circuit has its resonance set between the first and third harmonics of the crystal and is used to prevent the oscillator from operating at the first harmonic. In the first harmonic oscillator, the crystal appears as an inductor and forms a π-network with the two capacitors, thus providing the necessary phase shift for oscillation. In the third harmonic oscillator, L_1 and C_1 are chosen such that at the third harmonic the impedance of the circuit is equivalent to that of the capacitor C_2 in the first harmonic oscillator (Figure 5-b.). Thus, the same π-network is formed (Figure 5-c.) and oscillation is possible. At the first harmonic the tuned circuit appears as an inductor (Figure 5-a.), the π-network is not formed and oscillation is not possible.

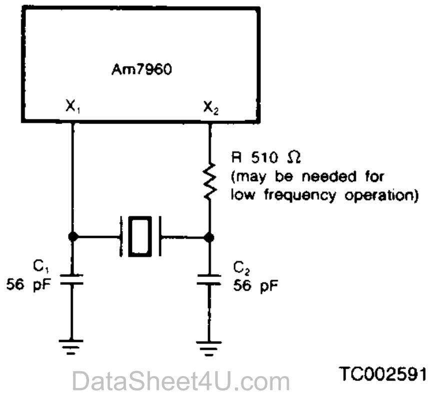


Figure 3. Connections for 6 - 24 MHz

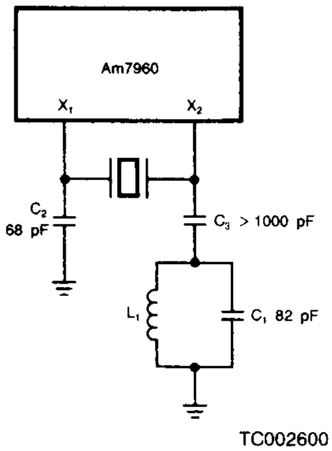
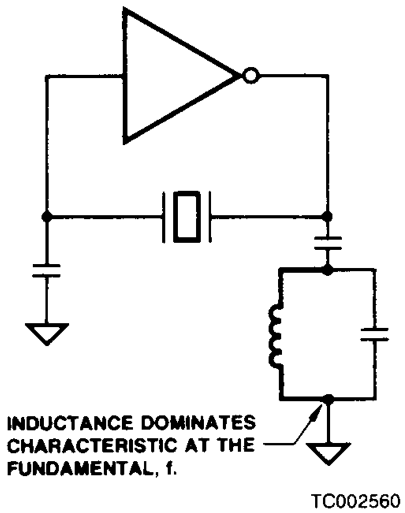
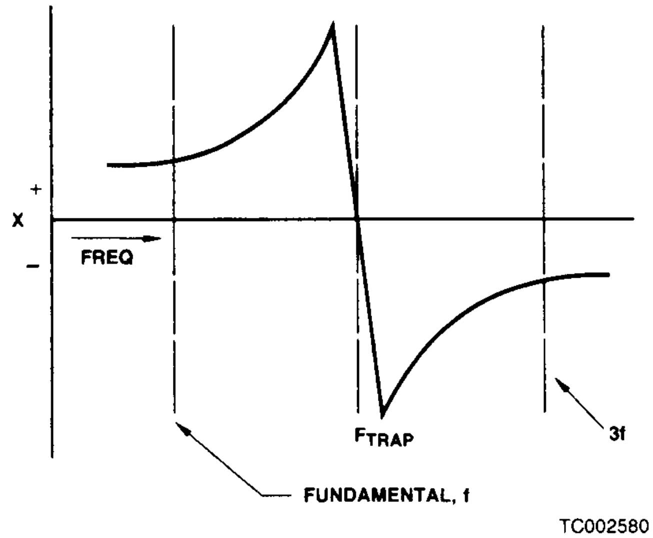


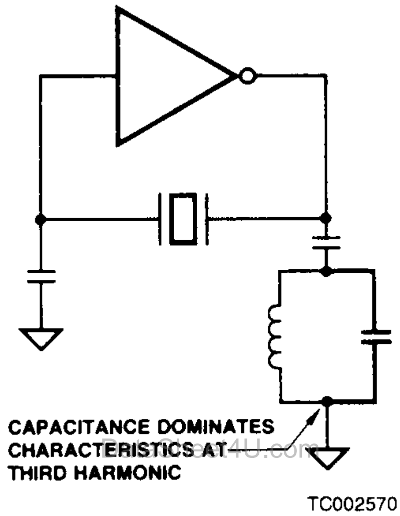
Figure 4. Connections for Frequencies Above 24 MHz (Commercial Application only)



a) Fundamental Equivalent



b) Trap Impedance



c) Harmonic Equivalent

Figure 5. Forcing Third Harmonic Oscillation (Commercial Application only)

The following specification is typical for a crystal to be used in a third harmonic oscillator (commercial application only):

Frequency Range:	> 24 MHz
Resonance:	Parallel Mode
Load:	32 pF
Stability:	.01% or to match systems requirements

Again, it is good practice to ground the crystal case and keep connections short.

Design Procedure:

1. Assume C_1 = 82 pF and C_2 = 68 pF (this gives a sensible inductor value). L_1 is calculated according to the formula:

   $$L_1 = \frac{1151}{f_o^2} \qquad f_o = \text{Crystal frequency in MHz}, \; L_1 \text{ in } \mu H$$

   This sets the resonant frequency of the L-C combination at 0.52 f_o.

2. Select the closest standard value inductor for L_1. Using this value, calculate C_1 such that the resulting crystal load at the third harmonic is 32 pF.

   $$C_1 = 60 + 25{,}330/[L_1(f_o^2)] \quad C_1 \text{ in pF}$$

   Choose the closest standard capacitor value to this.

Using standard values, both the resonant frequency to the L-C circuit (f_r) and the crystal load are non-optimal. This will cause a slight error in the oscillating frequency. If this is not permissible, C_1 may be a fixed capacitor in parallel with a trimmer, such that the range of adjustment includes the calculated value for C_1. This is then set to give the desired frequency.

External Clock Drive: An external clock used to drive the Am7960 must be a TTL signal which comes from a Schottky output and drives nothing else. This assures fast rise and fall times (< 2.5 ns) and minimal jitter. The duty cycle should be between 40% and 60%. The external TTL signal drives X_1 with X_2 left unconnected.

We do not specify or guarantee any phase relationship between the X_1 input and the TxC output.

Operating the Am7960 at Data Rates Below 500 Kbits Per Second

Slew Rate: Output transition times of more than 660 ns are not possible. This means that the 33% rule cannot be met at data rates less than 500 Kbps. However, a 660-ns slew rate should provide more than adequate suppression of EMI radiation in low data rate applications.

Oscillator: Crystals below 6 MHz may not be used with the Am7960, but there is no lower frequency bound on the 7960's range of clock rate with an external TTL clock.

Isolation Transformer: The size of an appropriate transformer for low frequency operation increases with low data rates.

Receiver Section

The received differential signal is fed to three comparators. One detects zero crossings and is used for clock recovery and data decoding. The other two comparators are biased so that together they discriminate between positive and negative differential signals - rejecting as noise anything smaller than ±20 mV and accepting signals greater than ±35 mV. The outputs from these "Presence Level" Comparators are filtered to screen out infrequent noise pulses less than 1/16 data period wide. The resulting presence level signals are synchronized with the internal 16x clock and used to determine whether valid Manchester data is present on the line. A signal must be either above the Positive Presence Level and then go below the Negative Presence Level or vice versa in 3/4 to 1 1/4 bit times to qualify as Manchester preamble. After this occurs, the next level transition brings the internal clock recovery circuitry into action.

The Am7960 must see a quiet line (less than ±20 mV) for at least 2.4 TxC periods before $\overline{ACD}$ will go inactive before allowing the device to begin receiving another message. It must be remembered, however, that the line does not become quiet immediately after the transmission of a data packet. This is because "End of Message" is encoded into an illegal Manchester signal–transmit output is held high for two entire bit times. During the "End of Message" signal, the isolation transformer's inductance stores energy which must be discharged onto the transmission line before the line can become quiet. This is known as transformer kickback. The amount of time that transformer kickback disturbs the line depends on the amount of energy stored during "End of Message" (dependent on data rate), the LR time constant of transformer inductance, and load resistance. Once the transmission line becomes quiet after an "End of Message," the Am7960 must wait 2.4 additional bit times before it can begin receiving a data packet.

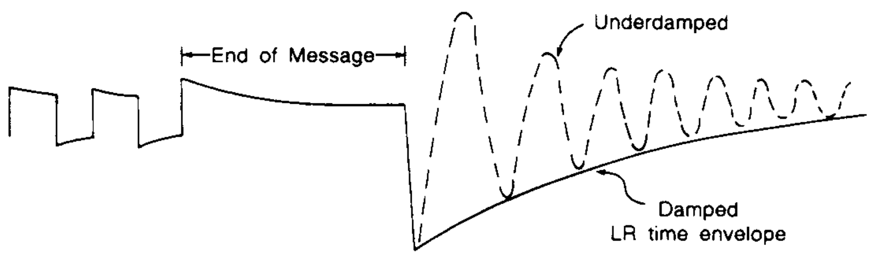


Figure 6. Transformer Kickback

Clock Recovery: When receiving data, the oscillator runs at 16x the data rate. Once it has been determined that Manchester data is on the line, the receive clock tracks the input data by creating three windows at 5/16 to 7/16, 1/2, and 9/16 to 11/16 of each perceived data cell. Any zero-crossing within these respective windows sets a SHORTEN, CENTER, or LENGTHEN bit. This tells the Phase-Locked Loop circuitry to change the next clock period by 1/16 if needed. Since the receive clock period is changed in increments of 1/16, the Phase-Locked Loop is minimally susceptible to jitter.

Data Decoding: The Am7960 decodes line data by sampling the 1/4 and 3/4 bit intervals. If these samples are opposite, valid Manchester data has been decoded. If these samples are the same and the next 1/4 sample is also the same, the receiver has detected "End of Message."

General Network Considerations

Well-conceived network design demands consideration of such variables as data transfer rate, error rate, line length, and maximum number of nodes. Once these system parameters are defined, the designer should first select the transmission media and then shift attention to devices within individual nodes.

Media Selection: Cable characteristics limit network size, complexity, and cost as well as the speed and accuracy of data communication. Conformance to FCC/VDE radiation specifications is also determined in part by the transmission media.

The selected cable should have low DC resistance to minimize intersymbol interference. AC line loss (Ld) must be measured in dB/ (unit of length) at three times the desired data rate. If shielded cable is chosen, it is important to have a foil shield with overlap and copper center conductor. The cable should be terminated at each end with its characteristic impedance to minimize reflections and should be grounded at just one point to prevent circulating ground currents.

The Am7960 is guaranteed to meet its specifications over the entire operating temperature range with transmitter loads of at least 37.5 ohms (terminated 75-ohm cable). Terminated 50-ohm cable may be used only under controlled environmental conditions or with resistors added to present a 37.5-ohm load to the transmitter.

Transformer Selection: Open circuit impedance, measured over the range from 0.2 to 5 times the data rate, should be relatively high (at least 10 times the cable impedance). Signal attenuation should be low over this range. Static shielded transformers are mandatory in electrically hostile environments. The static shield provides both line isolation and protection for the Am7960 by supplying a discharge path for high AC voltages (i.e., lightning, static discharges). The PE 5156X (Pulse Engineering) is acceptable for data rates of 1 Mbps or higher.

Power Budget: The power budget calculation shows how the Am7960's dynamic range (ratio of transmitter power to receiver sensitivity) is allocated among the various points of signal attenuation in a network.

$P_b = L_x + L_i(N\text{-}2) + (L_d)L + L_r$ + Receiver Overdrive

where:

P_b = Power Budget. For the Am7960 this figure is 32 dB (the dynamic range of the device)

L_x = Loss from transmitter to line

L_i* = Insertion loss for any node between transmitter and receiver (parallel connection of the transformer and Am7960 at 5 MHz)

L_r = Loss from line to receiver

L_d = Line loss in dB/length

N = Number of stations

L = Maximum line length

*Note: Insertion loss (L_i) must be under 0.2 dB if the designer wishes to ignore node reflections in his calculations.

The power budget is consumed by network parameters such as receiver overdrive, cable length, and the number of nodes on the network. These three variables are interdependent; that is, a designer wishing to maximize any one of these variables (such as cable length) does so at the expense of the other two:

Receiver Overdrive: This figure is inversely proportional to the error rate of any communication system. A value of 6 dB generally assures good performance. Error rate can be improved by increasing the signal-to-noise ratio, but this will reduce the maximum cable length or number of stations allowed on the network.

Cable Length: Any type of cable has associated with it a certain amount of line loss per unit of length. The longer a network is, the more power budget this parameter consumes.

Number of Nodes: Every node on a network contributes some insertion loss to the system. This reduces the proportion of power budget which can be allocated to S/N ratio and network length.

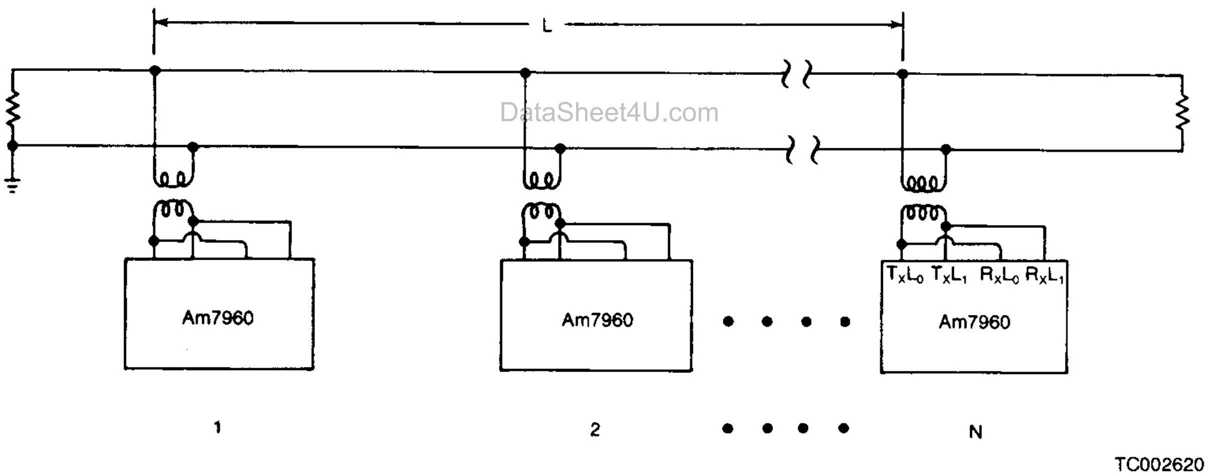


Figure 7. Am7960 Common Bus Party Line Applications

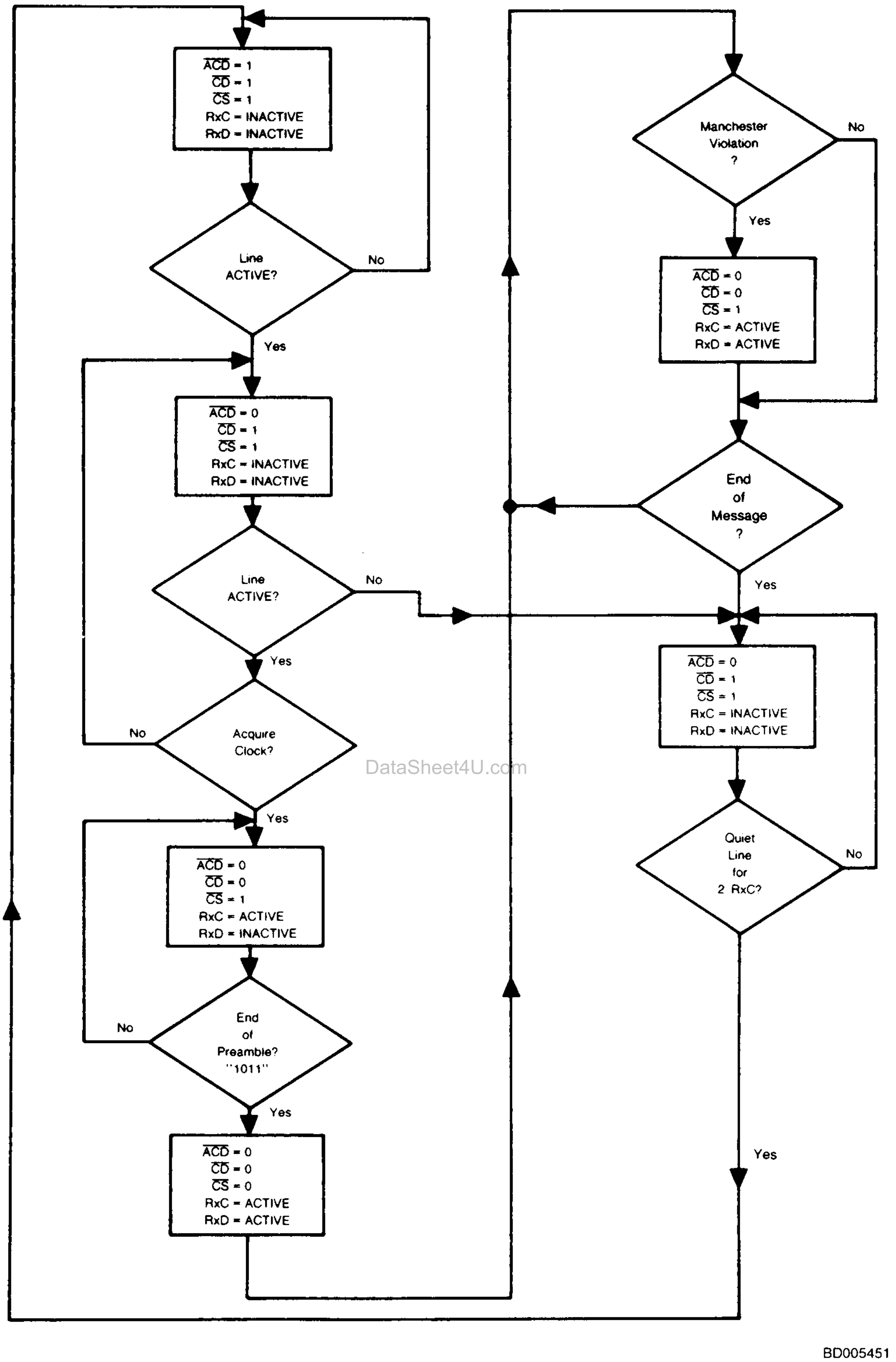


Figure 8. Am7960 Receive Flow Chart–Mode 0

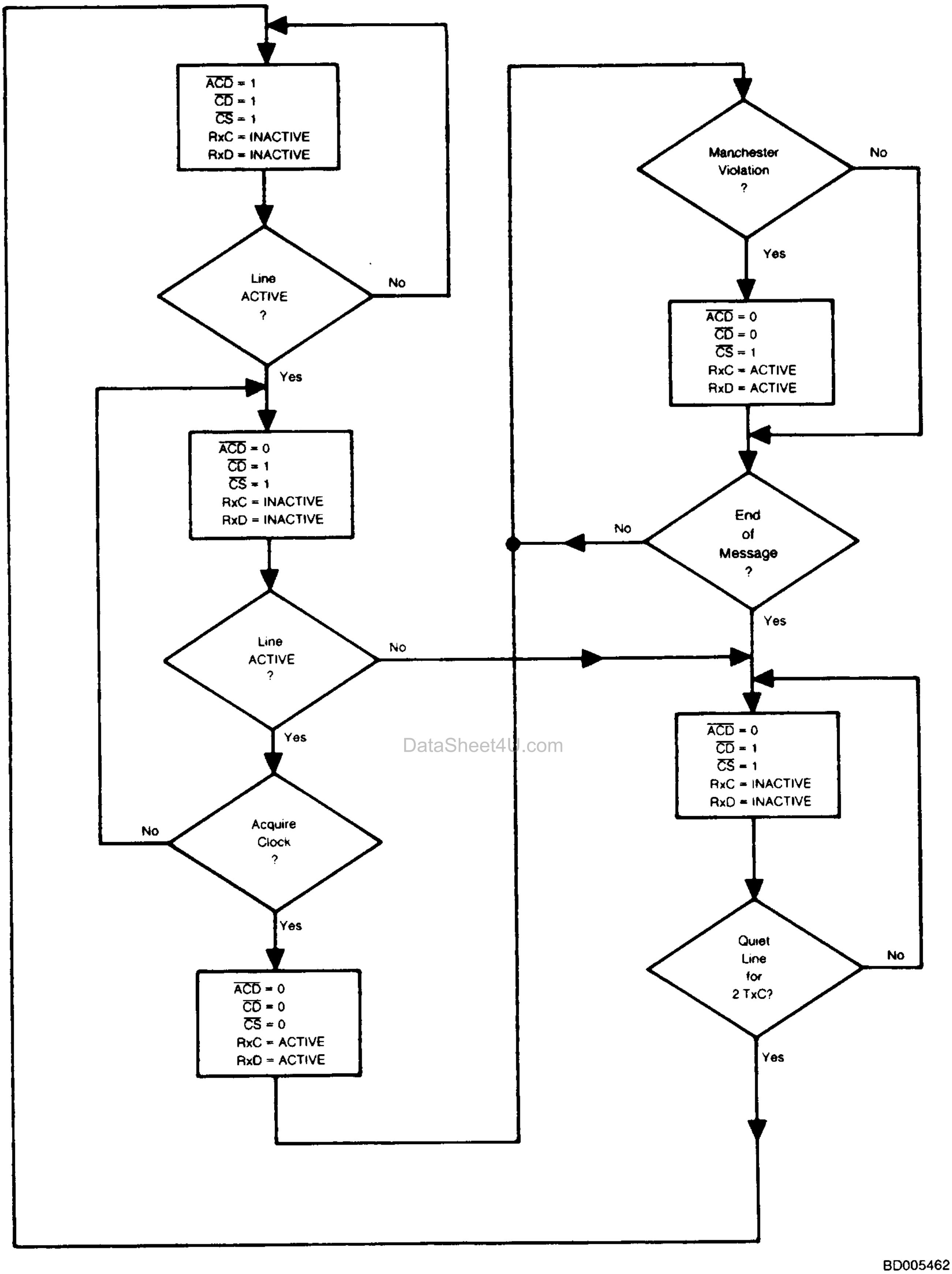


Figure 9. Am7960 Receive Flow Chart–Mode 1

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Supply Voltage Above Ground Potential . −0.5 V to +7.0 V
Receiver Common Mode Voltage .... −10.0 V to +6.0 V
Transmitter Common Mode Voltage ...... −0.5 V to +5.5 V
DC Output Current, Into Outputs (Logic Outputs) .... 30 mA
DC Input Voltage (Logic Inputs) .... −0.5 V to +5.5 V
DC Input Current (Logic Inputs) .... −30 mA to +5.0 mA
Power Dissipation .... 1.5 W
Lead Soldering Temperature (10 seconds) .... 300°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) .... 0 to +70°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Military (M) Devices
Temperature (T_C) .... −55 to +125°C
Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter	Description		Test Conditions	Min.	Typ.*	Max.	Units
Controller Interface Signals							
V_{OH}	Output HIGH Voltage	(Note 1)	I_{OH} = −1 mA	2.4			V
V_{OL}	Output LOW Voltage	(Note 1)	I_{OL} = −8 mA			0.5	V
V_{OH}	Output MOS HIGH Voltage	(Note 2)	I_{OH} = −.4 mA	3.9			V
V_{OL}	Output MOS LOW Voltage	(Note 2)	I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Voltage	(Notes 3 & 4)		2.0			V
V_{IL}	Input LOW Voltage	(Notes 3 & 4)				0.8	V
V_{RIH}	Reset Input HIGH Voltage	(Notes 5 & 14)	V_{CC} = Max.	1.9		2.95	V
V_{RIL}	Reset Input LOW Voltage	(Notes 5 & 14)			1.7	0.8	V
V_{RH}	Reset Input Hysteresis	(Notes 5 & 14)	V_{CC} = Min.		0.60		V
V_L	Input Clamp Voltage	(Notes 3 & 5)	I_{IN} = −18 mA			−1.2	V
		(Note 4)	I_{IN} = −5 mA			−1.2	
I_{IL}	Input LOW Current	(Notes 3, 4 & 5)	V_{IN} = 0.5 V			−500	μA
I_{IH}	Input HIGH Current	(Notes 3 & 4)	V_{IN} = 2.4 V			50	μA
		(Note 5)				50	
I_I	Input HIGH Current	(Notes 3 & 4)	V_{CC} = Min., V_{IN} = 5.5 V			1.0	mA
		(Note 5)	V_{CC} = Max., V_{IN} = 5.5 V				
I_{SC}	Short Circuit Current	(Notes 1, 2 & 6)	V_{CC} = Max.	−40		−120	mA
R_p	Pull-up Resistor to V_{CC}	(Notes 4, 5 & 14)			20		kΩ
Transmit Channel Interface Signals							
$\overline{V_T}$	Differential Transmit Output Voltage	(Notes 7 & 14)	R_L = 37.5 Ω	−2.0	−2.7	−3.5	V
V_T				2.0	2.7	3.5	
$\overline{V_{OS}}$	Commom Mode ransmit Output Voltage	(Note 8)	R_L = 37.5 Ω	1.0		3.0	V
V_{OS}							
V_{TO}	$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$ Difference in Differential Output Voltage	(Note 7)	R_L = 37.5 Ω	−75		75	mV
V_{OSO}	$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$ Difference in Common Mode Output Voltage	(Note 8)	R_L = 37.5 Ω	−75		75	mV
I_{OSC}	Transmit Output Short Circuit Current		V_{CC} = Max.			−250	mA
I_{OX}	Off State Leakage Currents		V_{CC} = Max. V_{OX} = $V_{CC/2}$	−100		100	μA
C_T	Differential Transmit Input Capacitance	(Note 14)	Transmit OFF		4		pF

Notes: See next page for notes.

* Typical values listed are for V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.

DC CHARACTERISTICS (Cont.)

Parameter	Description		Test Conditions	Min.	Typ.*	Max.	Units
Receive Channel Interface Signals							
V_{TH}	Differential Receiver Offset Voltage	(Notes 10, 14 & 22)		−5	±2	5	mV
V_{CM}	Common Mode Receiver Input Voltage	(Note 11)		1.0		3.0	V
V_{CPP}	Positive Static Carrier Presence Level	(Notes 9 & 14)	$0°C \leq T_A \leq 70°C$	20	+27	35	mV
V_{CPN}	Negative Static Carrier Presence Level	(Notes 9 & 14)	$0°C \leq T_A \leq 70°C$	−20	−27	−35	mV
R_R	Differential Receiver Input Resistance	(Note 14)	$\overline{V_T} < V_{IN} < V_T$ $0 < V_{CC} <$ Max.		25		kΩ
C_R	Differential Receiver Input Capacitance	(Note 14)	$\overline{V_T} < V_{IN} < V_T$		2		pF
Global Signals							
R_N	Differential Node Resistance	(Notes 12 & 14)	$\overline{V_T} < V_{IN} < V_T$ $0 < V_{CC} <$ Max.		25		kΩ
C_N	Differential Node Capacitance	(Notes 12, 14)	$\overline{V_T} < V_{IN} < V_T$ $0 < V_{CC} <$ Max.		6		pF
I_{CC}	Power Supply Current (Static)	(Note 13)	V_{CC} = Max., f = 0, $R_L = \infty$			190	mA

Notes:
1. Output signals $\overline{ACD}$, $\overline{CD}$, $\overline{CS}$ and $\overline{CTS}$.
2. Output signals TxC, RxC and RxD.
3. Inputs TxD and $\overline{RTS}$.
4. Inputs $\overline{TEST}$ and MODE.
5. Input $\overline{MRST}$ only.
6. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
7. V_T and $\overline{V_T}$ are the differential output signals TxL_0–TxL_1 depending upon signal polarity.
8. V_{OS} and $\overline{V_{OS}}$ are the average of TxL_0 and TxL_1 depending upon signal polarity.
9. V_{IN} is the differential input signal RxL_0–RxL_1 .
10. Offsets are for differential input signals (See Receiver Thresholds waveform diagram).
11. V_{CM} is the average RxL_0 and RxL_1.
12. Node impedance is with transmitter and receiver connected.
13. Dynamic I_{CC} is a function of load, slew rate, data rate, V_{CC}, and temperature as shown in Typical Performance Curves.
14. Typical values. Not tested.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

No.	Parameter	Description		Test Conditions	Min.	Typ.	Max.	Units
Transmit Clock								
1	t_P	Transmit Clock Period	(Notes 2, 21, 22)		330	250		ns
2	t_{PW}	Transmit Clock Width LOW	(Note 2)		45%		55%	TxC
3	t_{PW}	Transmit Clock Width HIGH	(Note 2)		45%		55%	TxC
4	t_r/t_f	Transmit Clock Rise and Fall Time	(Notes 2 & 15)	C_L = 50 pF			8	ns
			(Notes 2, 16 & 21)	C_L = 15 pF		3		
Transmit Control								
5	t_S	Setup $\overline{RTS}$ to ↑ TxC	(Notes 1 & 2)		15			ns
6	t_h	Hold $\overline{RTS}$ to ↑ TxC	(Notes 1 & 2)		5			ns
7	t_D	Minimum Inter-Packet Delay	(Notes 18 & 21)			3		TxC
8	t_{PLH}	↑ TxC to $\overline{ACD}$ Inhibit	(Notes 1 & 2)		0.3		0.5	TxC
9	t_{PHL}	↑ TxC to $\overline{ACD}$ Enable	(Notes 1 & 2)		2.25			TxC
10	t_{PHL}	↑ TxC to $\overline{CTS}$ Enable	(Notes 1 & 2)				0.4	TxC
11	t_{PHL}	↑ TxC to $\overline{CTS}$ Disable	(Notes 1 & 2)				0.4	TxC
12	t_S	Setup TxD to ↑ TxC	(Notes 1 & 2)		15			ns
13	t_h	Hold TxD to ↑ TxC	(Notes 1 & 2)		5			ns
Transmit Latency								
14	t_{PD}	↑ TxC to Encoded Data Line Clock Transition	(Notes 4, 17, 23)		0.75		1.0	TxC
15	t_{HZ}	↑ TxC to Transmitter Disable	(Notes 5, 17, 24)		2.25			TxC

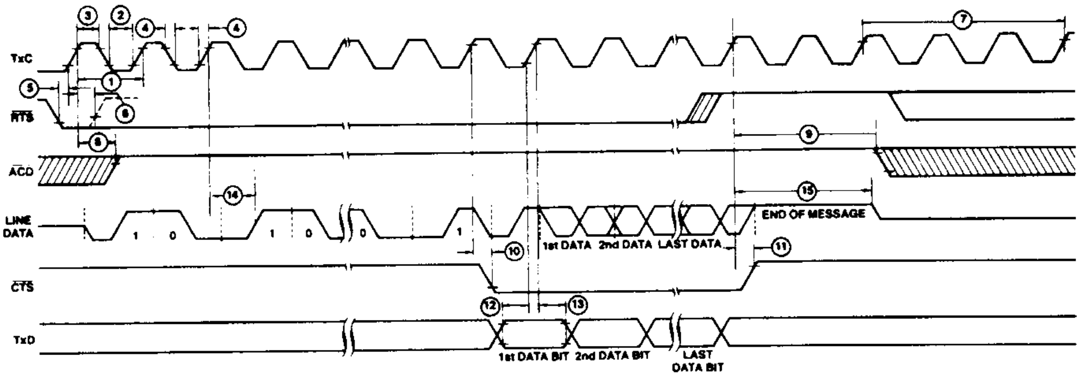
Notes: See next page for notes.

SWITCHING CHARACTERISTICS (Cont.)

No.	Parameter	Description		Test Conditions	Min.	Typ.	Max.	Units
Receive Clock and Data								
16	t_P	Receive Clock Period	(Note 2)		92%		108%	TxC
17	t_{PW}	Receive Clock Width LOW	(Note 2)		42%		58%	TxC
18	t_{PW}	Receive Clock Width HIGH	(Note 2)		42%		58%	TxC
19	t_r/t_f	Receive Clock Rise and Fall Time	(Notes 2 & 15)	C_L = 50 pF			8	ns
			(Notes 2, 16 & 21)	C_L = 15 pF		3		ns
20	t_{PD}	↑ RxC to Valid RxD	(Note 2)		−5		20	ns
21	t_r/t_f	Receive Data Rise and Fall Time	(Notes 2 & 15)	C_L = 50 pF			10	ns
			(Notes 2, 16 & 21)	C_L = 15 pF		3		ns
Receive Control								
22	t_{PHL}	Line Active to $\overline{ACD}$ Active	(Notes 1 & 6)		0.1		0.4	TxC
23	t_{PLH}	Line Quiet to $\overline{ACD}$ Inactive	(Notes 1 & 7)		2.15		2.4	TxC
24	t_{PW}	$\overline{ACD}$ Width LOW	(Note 1)		0.1			TxC
25	t_{PW}	$\overline{ACD}$ Width HIGH	(Note 1)		0.1			TxC
26	t_{PHL}	$\overline{ACD}$ Active to $\overline{CD}$ Active	(Notes 1 & 9)		1.5			TxC
			(Notes 1 & 8)		3.5			
27	t_{PLH}	$\overline{CD}$ Inactive to $\overline{ACD}$ Inactive	(Note 1)		0			ns
28	t_{PLH}	1st Line Data Transition to ↑ RxC	(Notes 2 & 8)		3.5			TxC
			(Notes 2 & 9)		1.0			
29	t_{PLH}	$\overline{CD}$ Active to ↑ RxC	(Notes 1 & 2)		0.41			TxC
30	t_{PLH}	↓ RxC to Inactive $\overline{CD}$	(Notes 1 & 2)		0		0.1	TxC
31	t_{PLH}	$\overline{CS}$ Active to ↑ RxC	(Notes 1, 2 & 8)		60			ns
32	t_{PLH}	↓ RxC to $\overline{CS}$ Active	(Notes 1, 2 & 9)		0		0.1	TxC
33	t_{PLH}	↓ RxC to $\overline{CS}$ Inactive	(Notes 1 & 2)		0		0.1	TxC
34	t_{PLH}	$\overline{CD}$ Active to $\overline{CS}$ Active	(Notes 1 & 9)		7			TxC
35	t_{PHL}	$\overline{CD}$ Inactive to RxC Inactive	(Note 21)			.95		TxC
Channel Transmit Signals								
36	t_{slew}	Transmit Slew Rate Coefficient	(Notes 20 & 21))			75		ns/kΩ
37	t_r	Transmit Rise Time	(Notes 3, 10, 21, 23)			30%		TxC
38	t_f	Transmit Fall Time	(Notes 3, 10, 21)			30%		TxC
39	t_p	Bit Cell Edge to Bit Cell Center	(Note 11)		48%		52%	TxC
40	t_p	Bit Cell Center to Bit Cell Center	(Note 11)		98%		102%	TxC
41	t_p	Bit Cell Center to Bit Cell Edge	(Note 11)		48%		52%	TxC
42		Transmit Waveform	(Notes 12 & 21)			Mono-tonic		
Channel Receive Signals								
43	t_{PW}	Receiver Positive Line Active Pulse Width	(Notes 13 & 24)		.10			TxC
44	t_{PW}	Receiver Negative Line Active Pulse Width	(Notes 13 & 24)		.10			TxC
45	t_J	Receiver Total Jitter Error Tolerance	(Notes 14, 21, 24)		−12.5	±18	12.5	%TxC
Global Signals								
46	f	Xtal Frequency	(Notes 19, 24)				50	MHz
47	t_{PW}	Master Reset Pulse Width	(Note 21, 24)		3.0	2.5		TxC

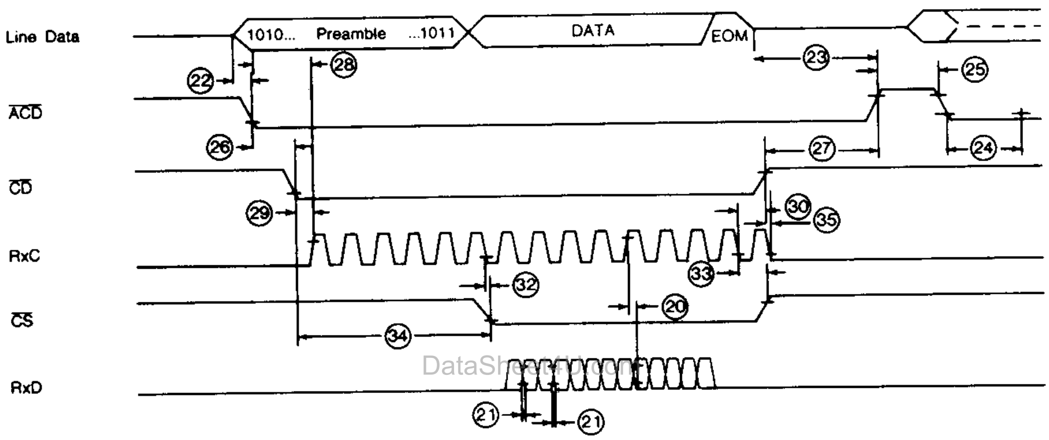
Notes:
1. TTL levels (Test Circuit A). Applies to $\overline{ACD}$, $\overline{CD}$, $\overline{CS}$, $\overline{CTS}$.
2. MOS levels (Test Circuit B). Applies to TxC, RxC, RxD.
3. Transmit slew rate set nominally at 30% TxC at 1 MHz. V_{CC} = +5.0 V, T_A = +25°C, R_{SRC} = 4K.
4. Measurements mode with Test Circuit C at $V_A - V_B = V_{CMA}$ ±5 mV.
5. Differential output starts to approach 0 volts.
6. Line active from differential receive signal has to meet minimum active width timing.
7. Line inactive is from the last differential signal to meet the minimum active width timing.
8. For Mode 1 only.
9. For Mode 0 only.
10. Transmit signals measured with Test Circuit C at $V_A - V_B$ = 10% and 90%.
11. Transmit Skew is measured with Test Circuit D at ±5 mV.
12. Transmitter shall be monotonic for both rise and fall.
13. Differential receive signals less than the maximum filtered pulse width are guaranteed to be rejected by the receiver. Differential receive signal greater than the minimum active pulse width are guaranteed to turn on the receiver.
14. The Am7960 receiver jitter is defined as the percentage edge displacement from the ideal transmit signal at the transceiver data bit frequency over the period of the transceiver data bit frequency (Figure 2).The jitter has been divided into two areas: characteristic and random. Characteristic jitter is edge displacement due to asymmetry and intersymbol interference. Random jitter is gaussion edge displacement of mean 0 and sigma at 1/3 the maximum random deviation.
15. Rise and fall times measured between 0.8 V and 2.0 V.
16. Rise and fall times measured between 1.0 V and 3.5 V.
17. R_{SRC} = 1 kΩ and data rate = 1 Mbps.
18. Interpacket delay is the amount of time that the receive inputs must see a "quiet" line before a message can be accepted. Cable and transformer characteristics determine the length of time required for the line to become quiet after End of Message.
19. This device should be used with crystals which have a frequency tolerance of 0.1% or better.
20. Measured with Test Circuit D.
21. Typical values. Not tested.
22. Transmit Clock Period, t_{P1} is 1/16 of X_1. The ATE tests this parameter at X_1 = 100 ns
23. ATE RSRC = 6.2K ohm and data rate = 625 KHz
24. Not tested.

SWITCHING WAVEFORMS



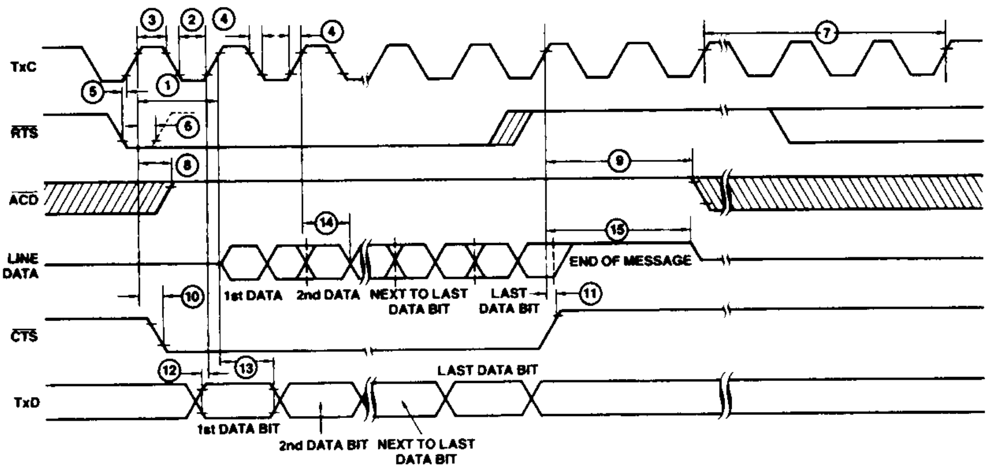
WF001642

Transmit Mode 0



WF010760

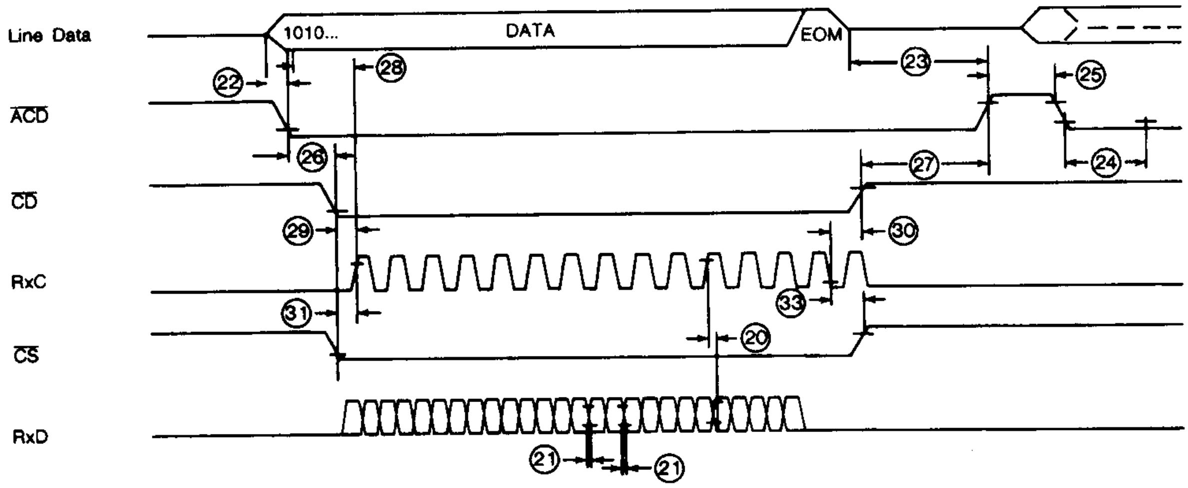
Receive Mode 0



WF001671

Transmit Mode 1

SWITCHING WAVEFORMS (Cont.)

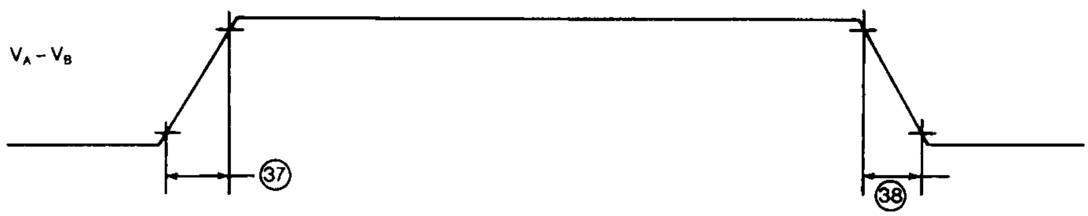


WF010771

Receive Mode 1

WF010780

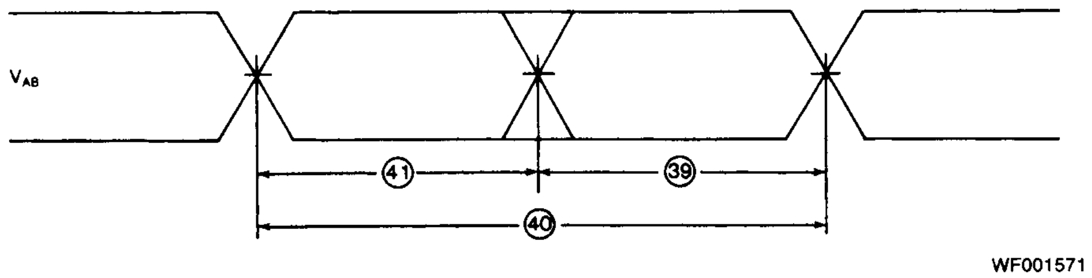
Receive Clock Waveform



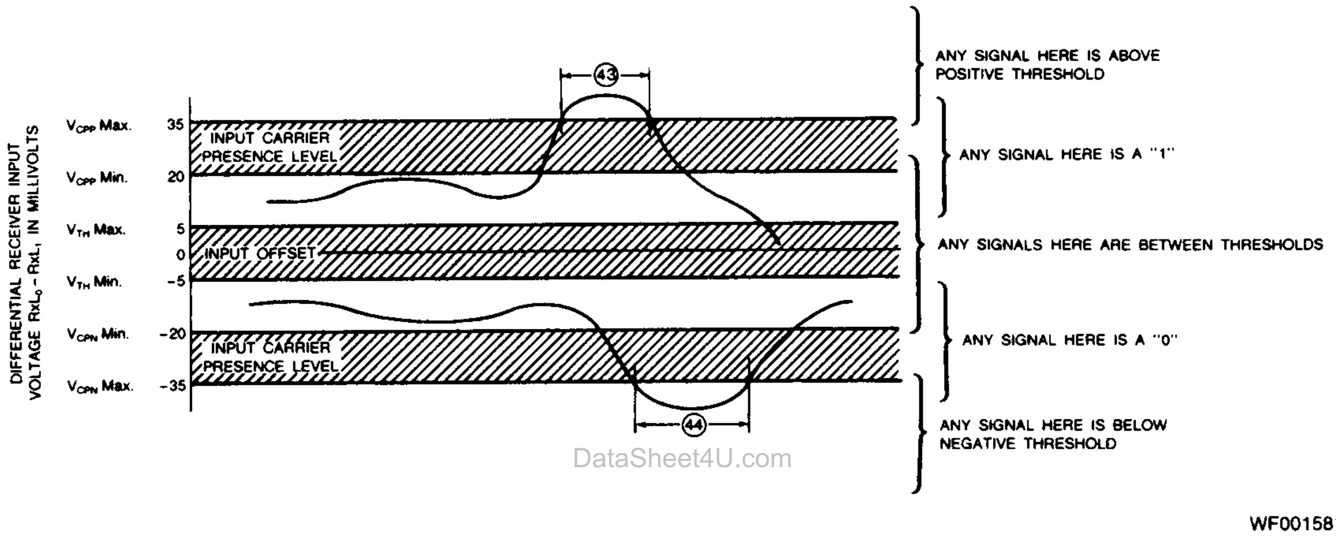
WF001551

Transmit Rise/Fall Time

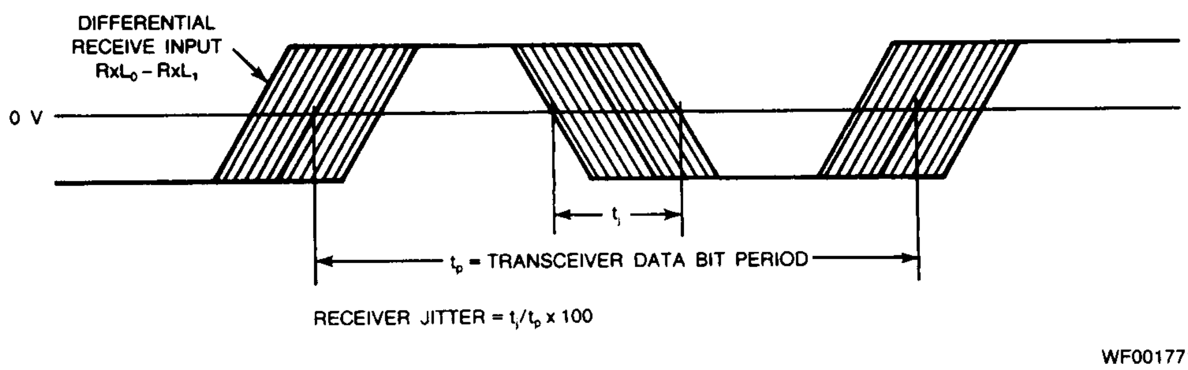
SWITCHING WAVEFORMS (Cont.)



Transmit Latency

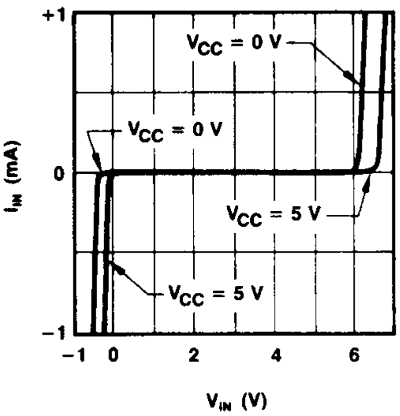


Receiver Thresholds



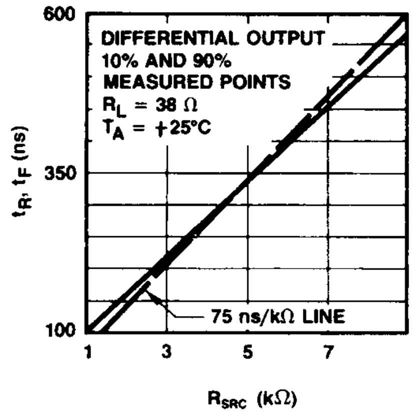
Receiver Jitter

TYPICAL PERFORMANCE CURVES*



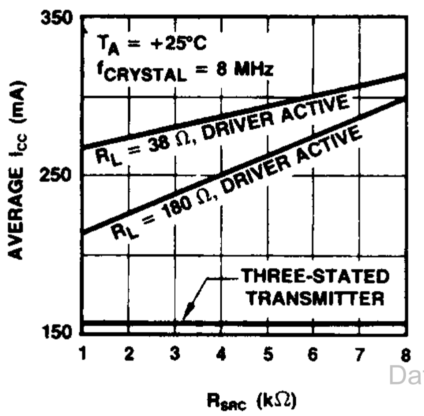
OP001850

Differential Transmit Input Characteristics with Three-State Driver



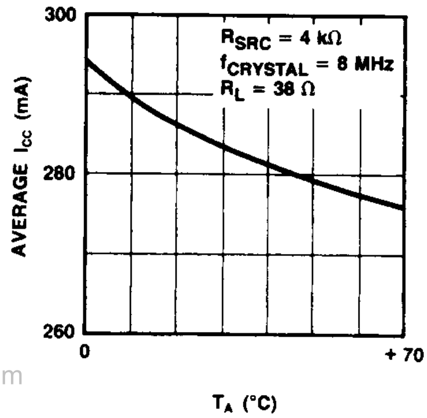
OP001860

Transmit Rise and Fall Times as a Function of R_{SRC}



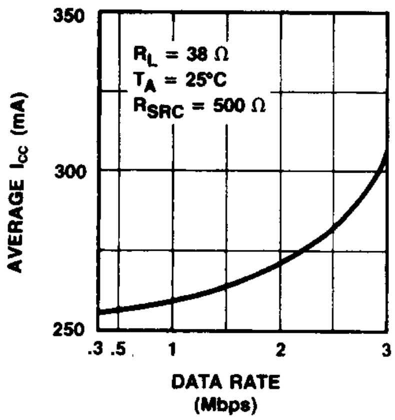
OP001870

Average I_{CC} as a Function of R_{SRC}



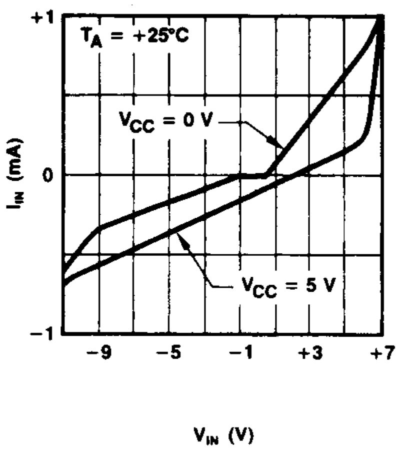
OP001880

Average I_{CC} as a Function of T_A



OP001890

Average I_{CC} as a Function of Data Rate

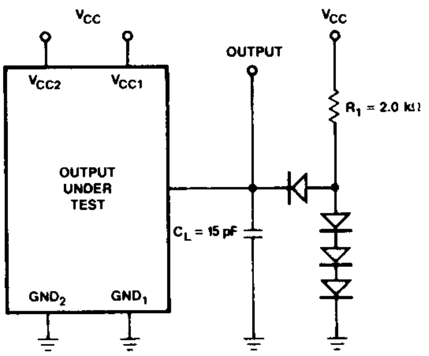


OP001900

Receiver Input Characteristics

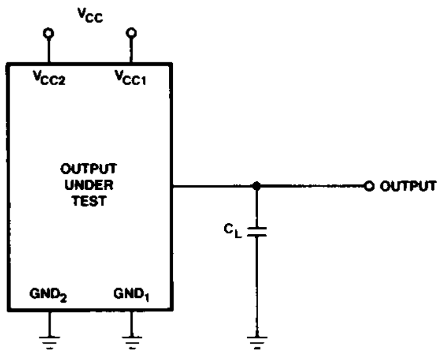
*Typical values are derived from characterization data. Production devices are not 100% tested to typical specifications.

SWITCHING TEST CIRCUITS



TC000781

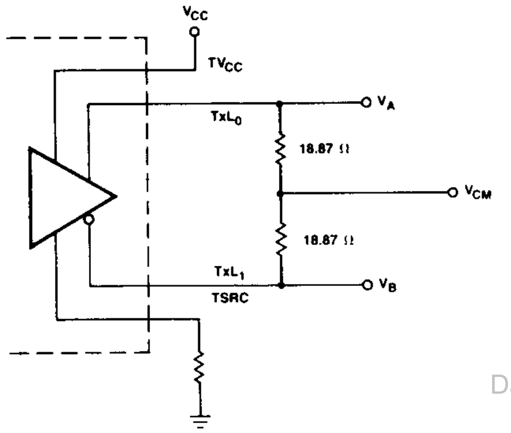
A. TTL Outputs (Note 1)



TC000771

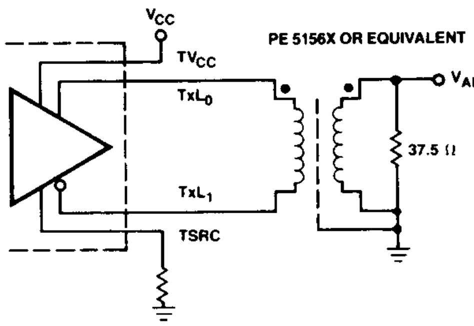
B. MOS Outputs (Notes 1 & 2)

Notes: 1. C_1 includes test fixture capacitance.
2. $C_L = 50$ pF unless otherwise specified.



TC000762

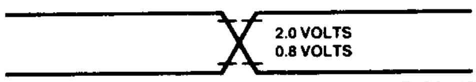
C. Transmitter Outputs



TC000751

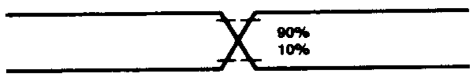
D. Transmitter Asymmetry

SWITCHING TEST WAVEFORMS



WF002140

A. TTL Outputs

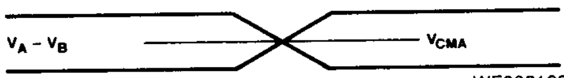


WF002181

B. MOS Outputs

WF002150

Rise and Fall Times



WF002160

Transmit Latency

C. Transmitter Outputs

WF002220

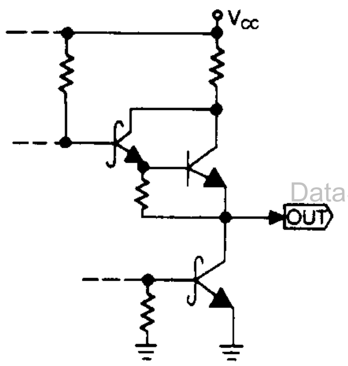
D. Transmitter Asymmetry

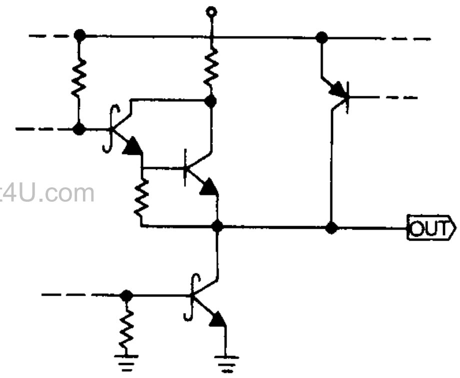
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

INPUT/OUTPUT CURRENT DIAGRAMS

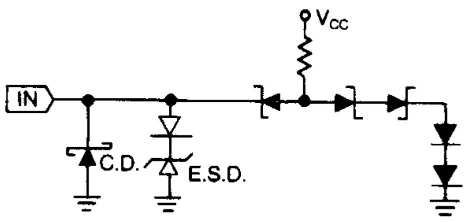




TC002631

TTL Outputs
($\overline{CTS}$, $\overline{ACD}$, $\overline{CD}$, $\overline{CS}$)

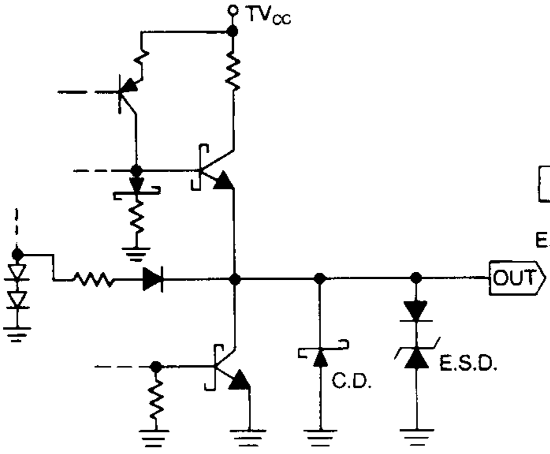
MOS Outputs
(RxC, RxD, TxC)

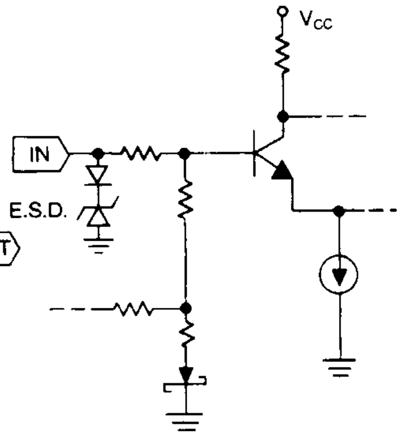


TC002641

TTL Inputs
($\overline{RTS}$, TxD)

INPUT/OUTPUT DIAGRAMS (Cont.)

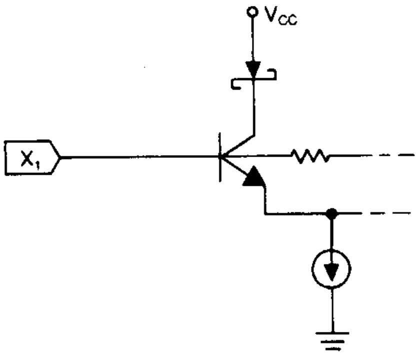




TC002651

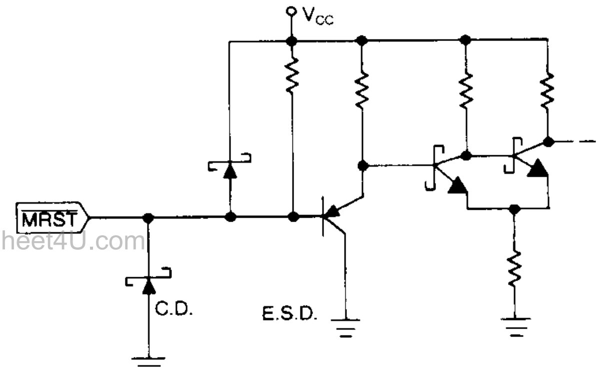
Transmit Outputs
(TxL_0, TxL_1)

Receiver Inputs
(RxL_0, RxL_1)



TC002780

X_1 Input

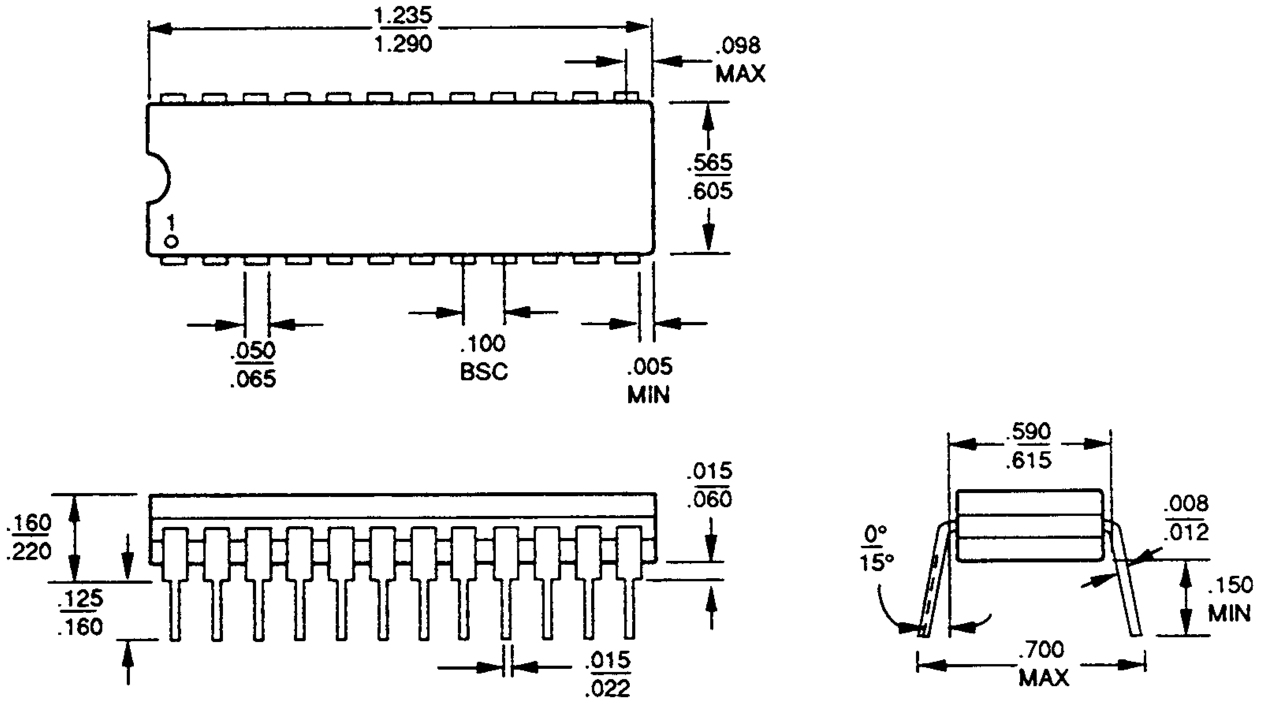


TC002661

$\overline{\text{MRST}}$ Inputs

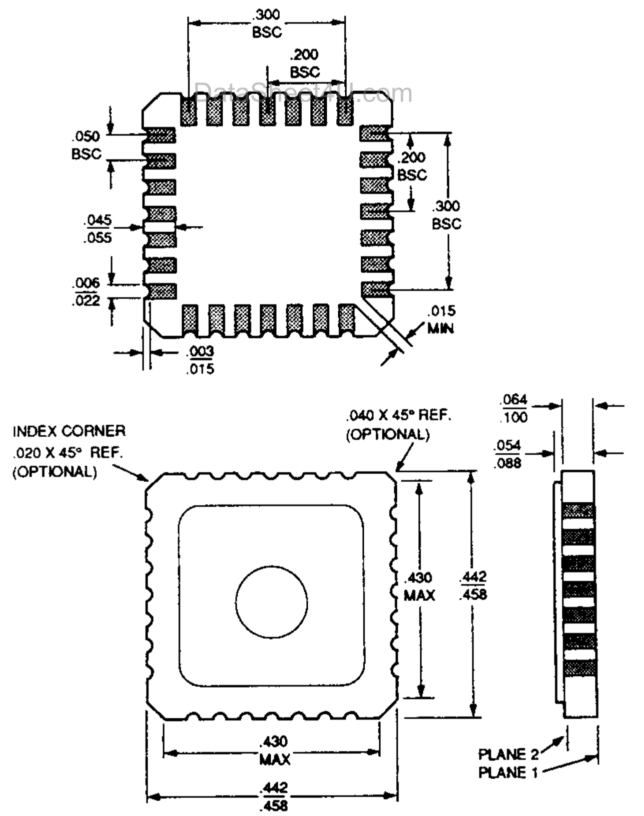
PHYSICAL DIMENSIONS

CD 024



PID# 07156B

CL 028



PID# 06595G