ADJD-S312-CR999

Miniature Surface-Mount RGB Digital Color Sensor

Data Sheet

Description

The ADJD-S312-CR999 is a cost effective, CMOS digital output RGB color sensor in miniature surface-mount package with a mere size of 3x3x0.77mm. The IC comes with integrated RGB filters, an analog-to-digital converter and a digital core for communication and sensitivity control. The output allows direct interface to micro-controller or other logic control for further signal processing without the need of any additional components.

This device is designed to cater for wide dynamic range of illumination level and is ideal for applications like portable or mobile devices which demand higher integration, smaller size and low power consumption. Sensitivity control is performed by the serial interface and can be optimized individually for the different color channel. The sensor can also be used in conjunction with a white LED for reflective color management.

Features

- Fully integrated RGB digital color sensor
- Digital I/O via 2-wire serial interface
- Industry's smallest form factor – CSP 3x3x0.77mm
- Adjustable sensitivity for different levels of illumination
- Uniformly distributed RGB photodiode array
- 7 bit resolution per channel output
- Built in internal oscillator
- Sleep function when not in use
- No external components
- Low supply voltage (VDD) 2.6V
- 0°C to 70°C operating temperature
- Lead free package

Applications

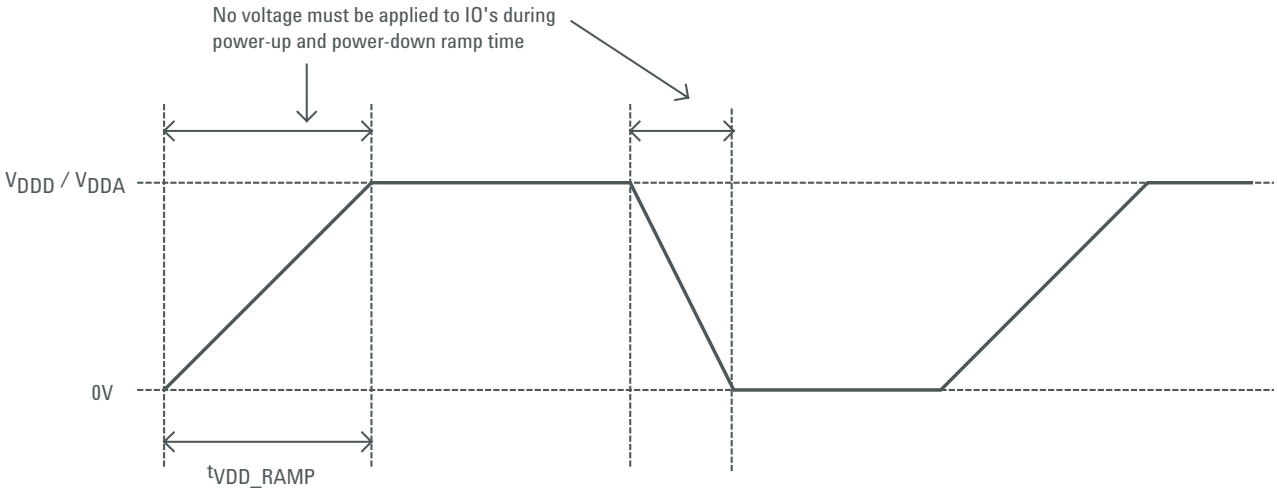
- General color detection and measurement
- Mobile appliances such as mobile phones, PDAs, MP3 players,etc
- Consumer appliances
- Portable medical equipments
- Portable color detector/reader

ESD WARNING: *Standard CMOS handling precautions should be observed to avoid static discharge.*

General Specifications

Feature	Value
Interface	100kHz serial interface
Supply	2.6V digital (nominal), 2.6V analog (nominal)

Powering the Device



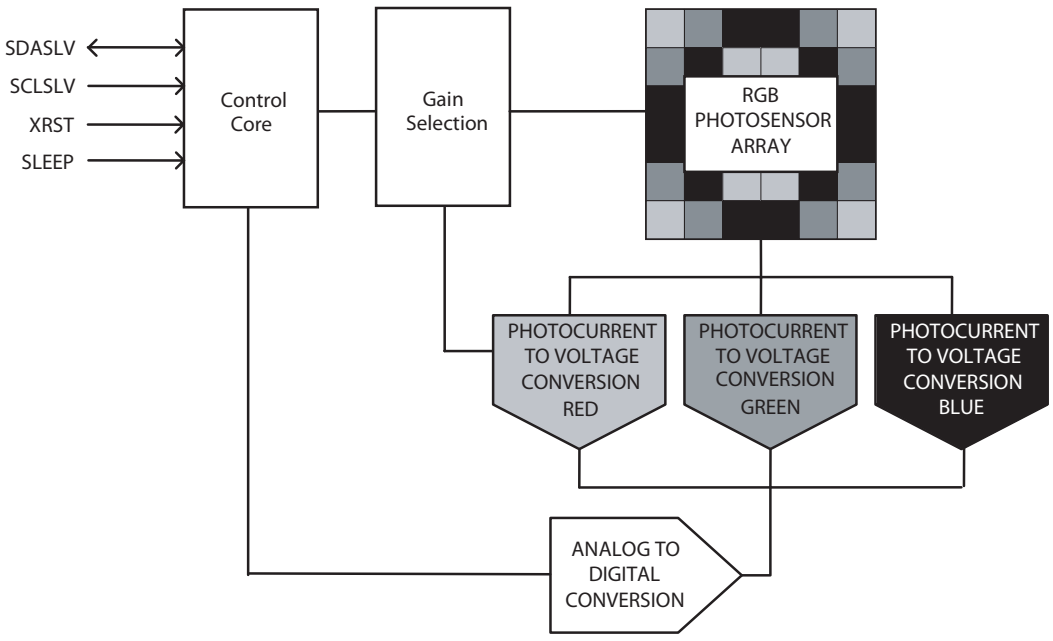
ESD Protection Diode Turn-On During Power-Up and Power-Down

A particular power-up and power-down sequence must be used to prevent any ESD diode from turning on inadvertently. The figure above describes the sequence. In general, AVDD and DVDD should power-up and power-down together to prevent ESD diodes from turning on inadvertently. During this period, no voltage should be applied to the IO's for the same reason.

Ground Connection

AGND and DGND must both be set to 0V and preferably star-connected to a central power source as shown in the application diagram. A potential difference between AGND and DGND may cause the ESD diodes to turn on inadvertently.

Block Diagram



Electrical Specifications

Absolute Maximum Ratings (Notes 1 & 2)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage temperature	T_{STG_ABS}	-40	85	C	
Digital supply voltage, DVDD to DVSS	V_{DDD_ABS}	-0.5	3.7	V	
Analog supply voltage, AVDD to AVSS	V_{DDA_ABS}	-0.5	3.7	V	
Input voltage	VI_{N_ABS}	-0.5	V_{DDD}+0.5	V	All I/O pins
Solder Reflow Peak temperature	T_{L_ABS}		245	C	
Human Body Model ESD rating	ESD_{HBM_ABS}		2	kV	All pins, human body model per JESD22-A114-B

Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units	Notes
Free air operating temperature	TA	0	25	70	C
Digital supply voltage, DVDD to DVSS	V_{DDD}	2.5	2.6	3.6	V
Analog supply voltage, AVDD to AVSS	V_{DDA}	2.5	2.6	3.6	V
Output current load high	I_{OH}			3	mA
Output current load low	I_{OL}			3	mA
Input voltage high level (Note 4)	V_{IH}	0.7 V_{DDD}		V_{DDD}	V
Input voltage low level (Note 4)	V_{IL}	0		0.3 V_{DDD}	V

DC Electrical Specifications

Over Recommended Operating Conditions (unless otherwise specified)

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Output voltage high level (Note 5)	V_{OH}	I_{OH} = 3mA	V_{DDD}-0.8	V_{DDD}-0.4		V
Output voltage low level (Note 6)	V_{OL}	I_{OL} = 3mA		0.2	0.4	V
Dynamic supply current (Note 7,8)	I_{DD_DYN}	(Note 9)		9.4	14	mA
Static supply current (Note 8)	I_{DD_STATIC}	(Note 9)		2.7		mA
Sleep-mode supply current (Note 8)	I_{DD_SLP}	(Note 9)		0.2	15	uA
Input leakage current	I_{LEAK}		-10		10	uA

AC Electrical Specifications

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Internal clock frequency	f_{CLK}		16	26	38	MHz

Optical Specification

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Dark offset*	V_D	Ee = 0		65		LSB

*code is from dark code to (dark code + 128LSB)

Minimum sensitivity (note 3)

Parameter	Symbol	Conditions		Minimum	Typical (Note 3)	Maximum	Units
Irradiance Responsivity	Re	λ_P = 460 nm Refer Note 10	B		36		LSB/ ($mWcm^{-2}$)
		λ_P = 542 nm Refer Note 11	G		52		
		λ_P = 645 nm Refer Note 12	R		79		

Maximum sensitivity (note 3)

Parameter	Symbol	Conditions		Minimum	Typical (Note 3)	Maximum	Units
Irradiance Responsivity	Re	λ_P = 460 nm Refer Note 10	B		1150		LSB/ ($mWcm^{-2}$)
		λ_P = 542 nm Refer Note 11	G		1640		
		λ_P = 645 nm Refer Note 12	R		2310		

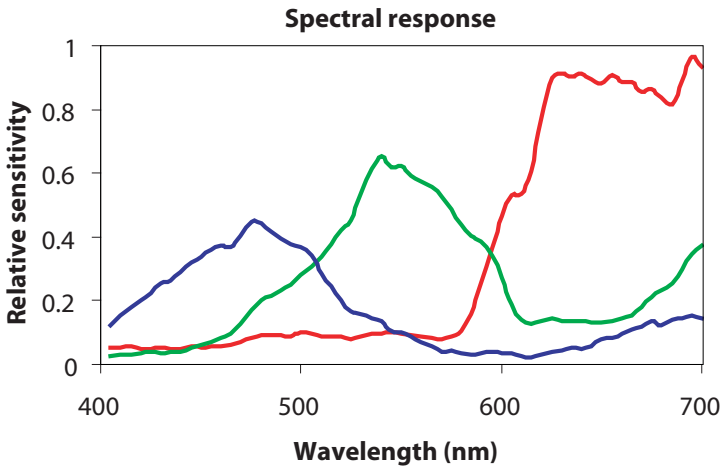
Minimum sensitivity (note 13)

Parameter	Symbol	Conditions		Minimum	Typical (Note 3)	Maximum	Units
Saturation Irradiance		λ_P = 460 nm Refer Note 10	B		4.17		$mWcm^{-2}$
		λ_P = 542 nm Refer Note 11	G		2.88		
		λ_P = 645 nm Refer Note 12	R		1.90		

Maximum sensitivity (note 13)

Parameter	Symbol	Conditions		Minimum	Typical (Note 3)	Maximum	Units
Saturation Irradiance		λ_P = 460 nm Refer Note 10	B		0.13		$mWcm^{-2}$
		λ_P = 542 nm Refer Note 11	G		0.09		
		λ_P = 645 nm Refer Note 12	R		0.06		

Notes:
1. The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The device should not be operated at these limits. The parametric values defined in the "Electrical Specifications" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Specified at room temperature (25°C) and VDDD = VDDA = 2.6V.
4. Applies to all DI pins.
5. Applies to all DO pins. SDASLV go tri-state when output logic high. Minimum VOH depends on the pull-up resistor value.
6. Applies to all DO and DIO pins.
7. Dynamic testing is performed with the IC operating in a mode representative of typical operation.
8. Refers to total device current consumption.
9. Output and bidirectional pins are not loaded.
10. Test condition is blue light of peak wavelength (λ_P) 460 nm and spectral half width ($\Delta\lambda$½) 25 nm.
11. Test condition is green light of peak wavelength (λ_P) 542 nm and spectral half width ($\Delta\lambda$½) 35 nm
12. Test condition is red light of peak wavelength (λ_P) 645 nm and spectral half width ($\Delta\lambda$½) 20 nm
13. Saturation irradiance = (MSB)/(Irradiance responsivity)



Typical spectral response when the gains for all the color channels are set at equal.

Serial Interface Timing Information

Parameter	Symbol	Minimum	Maximum	Units
SCL clock frequency	f_{scl}	0	100	kHz
(Repeated) START condition hold time	$t_{HD:STA}$	4	-	µs
Data hold time	$t_{HD:DAT}$	0	3.45	µs
SCL clock low period	t_{LOW}	4.7	-	µs
SCL clock high period	t_{HIGH}	4.0	-	µs
Repeated START condition setup time	$t_{SU:STA}$	4.7	-	µs
Data setup time	$t_{SU:DAT}$	250	-	ns
STOP condition setup time	$t_{SU:STO}$	4.0	-	µs
Bus free time between START and STOP conditions	t_{BUF}	4.7	-	µs

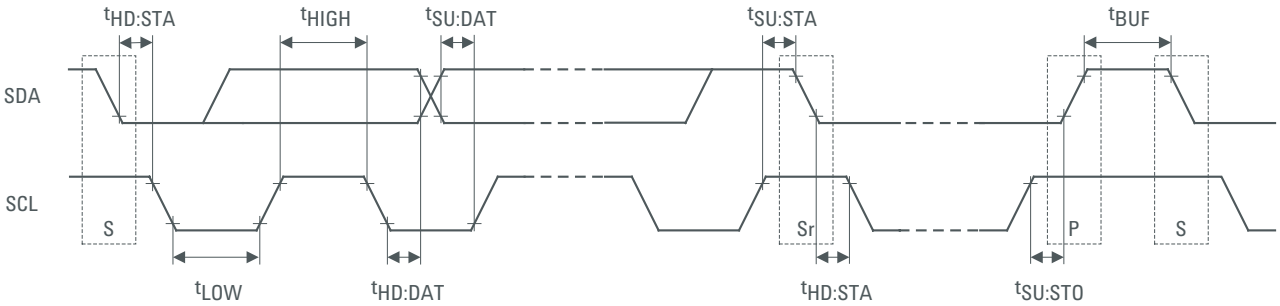
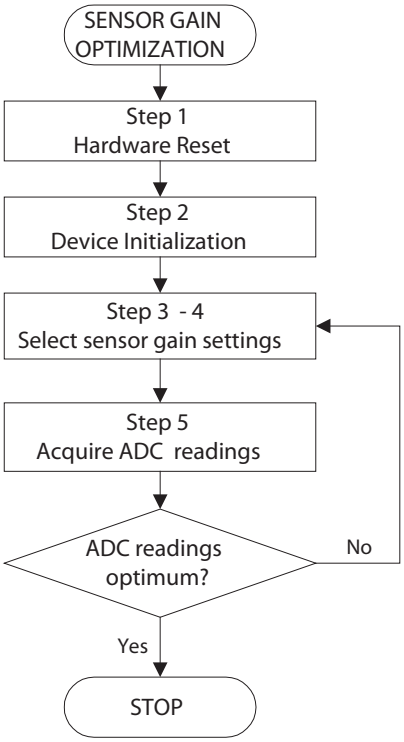


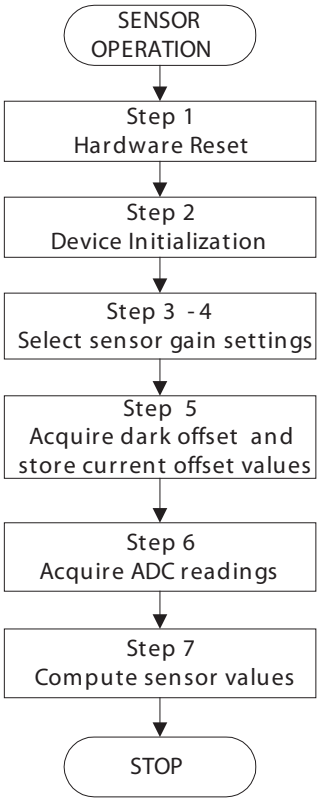
Figure 1. Serial Interface Bus Timing Waveforms

High Level Description

The sensor needs to be configured before it can be used. The gain selection needs to be set for optimum performance depending on light levels. The flowcharts below describe the different procedures required.



Sensor gain optimization flowchart



Sensor operation flowchart

* Please refer to application note for more detailed information.

Detail Description

A hardware reset (by asserting XRST) should be performed before starting any operation.

The user controls and configures the device by programming a set of internal registers through a serial interface. At the start of application, the following setup data must be written to the setup registers:

Address (Hex)	Register	Setup Data (Hex)
03	SETUP0	01
04	SETUP1	01
0C	SETUP2	01
0D	SETUP3	01
0E	SETUP4	01

Sensor Gain Settings

The sensor gain can be adjusted by varying the photodiode size and integration time of the sensor manually through the following registers.

Sensor Sensitivity ~ Photodiode Size x Integration Time Slot

Address (Hex)	Register	Description
0B	PDASR	Red Channel Photodiode Size
0A	PDASG	Green Channel Photodiode Size
09	PDASB	Blue Channel Photodiode Size
11	TINTR	Red Channel Integration Time
10	TINTG	Green Channel Integration Time
0F	TINTB	Blue Channel Integration Time

Setup Value for Photodiode Size

The following value can be written to each of the photodiode size registers to adjust the gain of the sensor. The default value after reset for these registers is 07H.

Value (Hex)	Photodiode Size
01	¼
03	½
07	¾
0F	Full

Setup Value for Integration Time

The following value can be written to each of the integration time registers to adjust the gain of the sensor. The default value after reset for these registers is 07H.

Value (Hex)	Integration Time Slot
00	1
01	2
02	3
03	4
04	5
05	6
06	7
07	8
08	9
09	10
0A	11
0B	12
0C	13
0D	14
0E	15
0F	16

Sensor ADC Output Registers

To obtain sensor ADC value, '02' Hex must be written to ACQ register before reading the Sensor ADC Output Registers.

Address (Hex)	Register	Description
02	ACQ	Acquire sensor analog to digital converter (ADC) values when 02H is written. Reset to 00H when sensor acquisition is completed
44	ADCR	Sensor Red channel ADC value.
43	ADCG	Sensor Green channel ADC value.
42	ADCB	Sensor Blue channel ADC value.

Serial Interface Reference

Description

The programming interface to the ADJD-S312 is a 2-wire serial bus. The bus consists of a serial clock (SCL) and a serial data (SDA) line. The SDA line is bi-directional on ADJD-S312 and must be connected through a pull-up resistor to the positive power supply. When the bus is free, both lines are HIGH.

The 2-wire serial bus on ADJD-S312 requires one device to act as a master while all other devices must be slaves. A master is a device that initiates a data transfer on the bus, generates the clock signal and terminates the data transfer while a device addressed by the master is called a slave. Slaves are identified by unique device addresses.

Both master and slave can act as a transmitter or a receiver but the master controls the direction for data transfer. A transmitter is a device that sends data to the bus and a receiver is a device that receives data from the bus.

The ADJD-S312 serial bus interface always operates as a slave transceiver with a data transfer rate of up to 100kbit/s.

START/STOP Condition

The master initiates and terminates all serial data transfers. To begin a serial data transfer, the master must send a unique signal to the bus called a START condition. This is defined as a HIGH to LOW transition on the SDA line while SCL is HIGH.

The master terminates the serial data transfer by sending another unique signal to the bus called a STOP condition. This is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH.

The bus is considered to be busy after a START (S) condition. It will be considered free a certain time after the STOP (P) condition. The bus stays busy if a repeated START (Sr) is sent instead of a STOP condition.

The START and repeated START conditions are functionally identical.

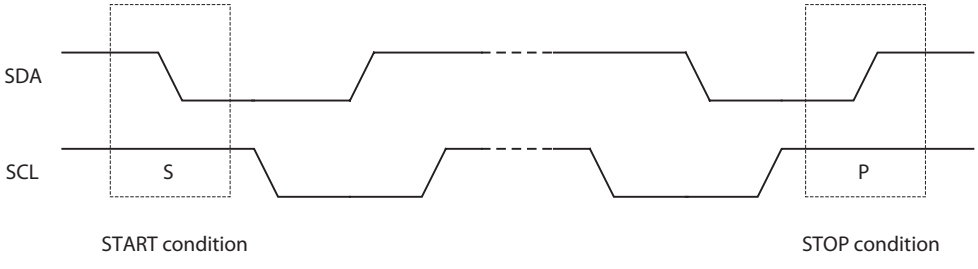


Figure 1: START/STOP Condition

Data Transfer

The master initiates data transfer after a START condition. Data is transferred in bits with the master generating one clock pulse for each bit sent. For a data bit to be valid, the SDA data line must be stable during the HIGH period of the SCL clock line. Only during the LOW period of the SCL clock line can the SDA data line change state to either HIGH or LOW.

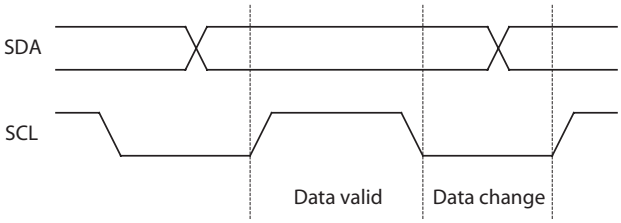


Figure 2: Data Bit Transfer

The SCL clock line synchronizes the serial data transmission on the SDA data line. It is always generated by the master. The frequency of the SCL clock line may vary throughout the transmission as long as it still meets the minimum timing requirements.

The master by default drives the SDA data line. The slave drives the SDA data line only when sending an acknowledge bit after the master writes data to the slave or when the master requests the slave to send data.

The SDA data line driven by the master may be implemented on the negative edge of the SCL clock line. The master may sample data driven by the slave on the positive edge of the SCL clock line. Figure shows an example of a master implementation and how the SCL clock line and SDA data line can be synchronized.

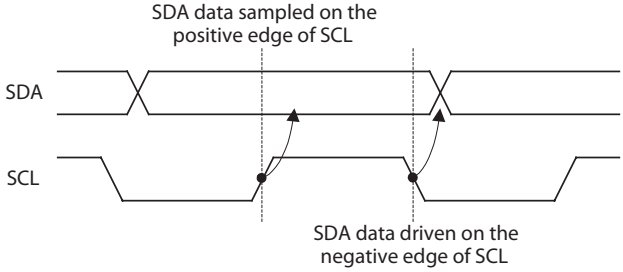


Figure 3: Data Bit Synchronization

A complete data transfer is 8-bits long or 1-byte. Each byte is sent most significant bit (MSB) first followed by an acknowledge or not acknowledge bit. Each data transfer can send an unlimited number of bytes (depending on the data format). See Figure 4.

Acknowledge/Not acknowledge

The receiver must always acknowledge each byte sent in a data transfer. In the case of the slave-receiver and master-transmitter, if the slave-receiver does not send an acknowledge bit, the master-transmitter can either STOP the transfer or generate a repeated START to start a new transfer. See Figure 5.

In the case of the master-receiver and slave-transmitter, the master generates a not acknowledge to signal the end of the data transfer to the slave-transmitter. The master can then send a STOP or repeated START condition to begin a new data transfer.

In all cases, the master generates the acknowledge or not acknowledge SCL clock pulse. See Figure 6.

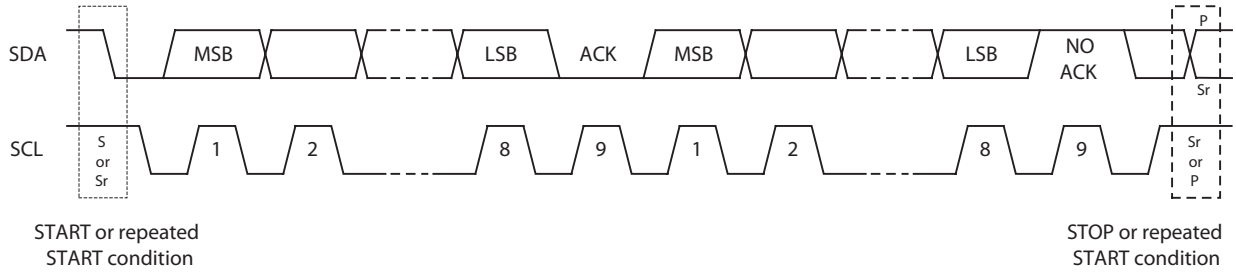


Figure 4: Data Byte Transfer

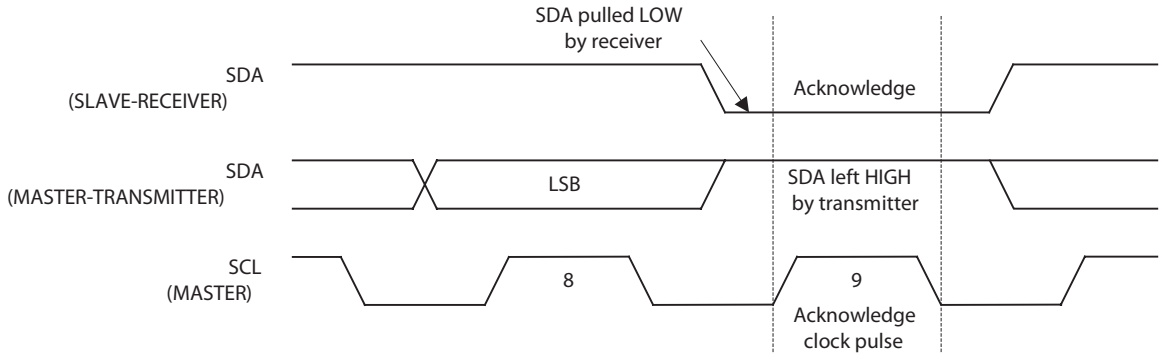


Figure 5: Slave-Receiver Acknowledge

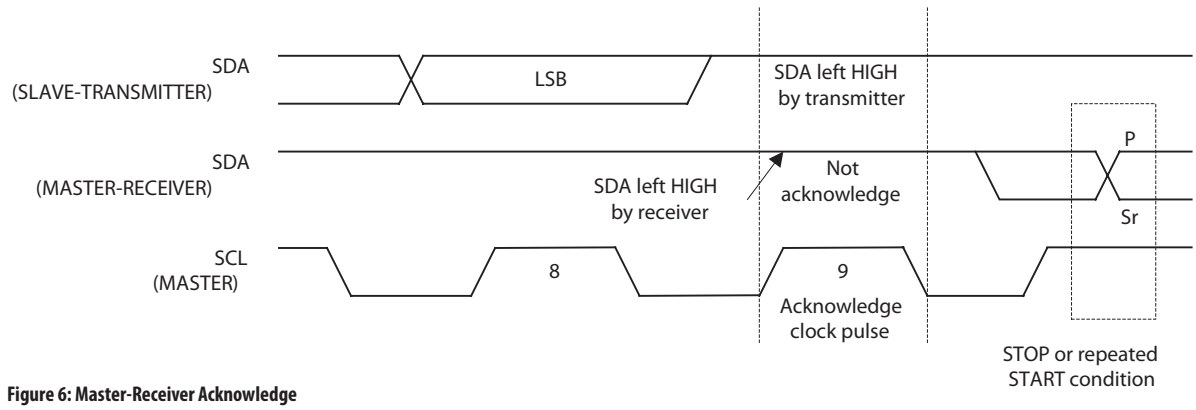


Figure 6: Master-Receiver Acknowledge

Addressing

Each slave device on the serial bus needs to have a unique address. This is the first byte that is sent by the master-transmitter after the START condition. The address is defined as the first seven bits of the first byte.

The eighth bit or least significant bit (LSB) determines the direction of data transfer. A 'one' in the LSB of the first byte indicates that the master will read data from the addressed slave (master-receiver and slave-transmitter). A 'zero' in this position indicates that the master will write data to the addressed slave (master-transmitter and slave-receiver).

A device whose address matches the address sent by the master will respond with an acknowledge for the first byte and set itself up as a slave-transmitter or slave-receiver depending on the LSB of the first byte.

The slave address on ADJD-S312 is 0x58 (7-bits).

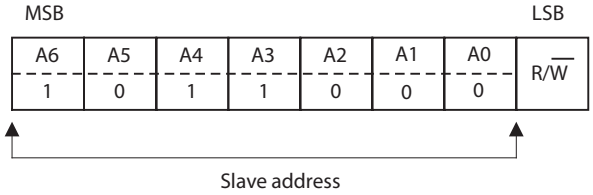


Figure 7: Slave Addressing

Data format

ADJD-S312 uses a register-based programming architecture. Each register has a unique address and controls a specific function inside the chip.

To write to a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then writes the new register data. Once the slave acknowledges, the master generates a STOP condition to end the data transfer. See figure 8.

To read from a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then generates a repeated START condition and resends the slave address sent previously. The least significant bit (LSB) of the slave address must indicate that the master wants to read from the slave. The addressed device will then acknowledge the master.

The master reads the register data sent by the slave and sends a no acknowledge signal to stop reading. The master then generates a STOP condition to end the data transfer. See figure 9.

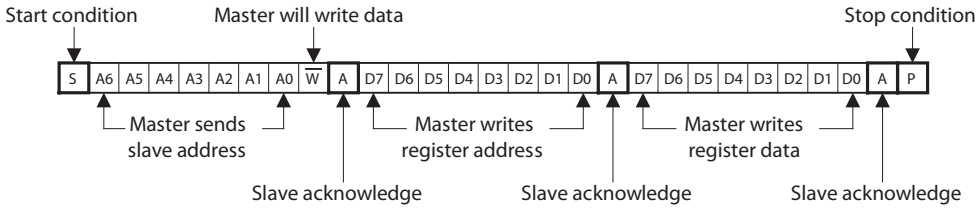


Figure 8: Register Byte Write Protocol

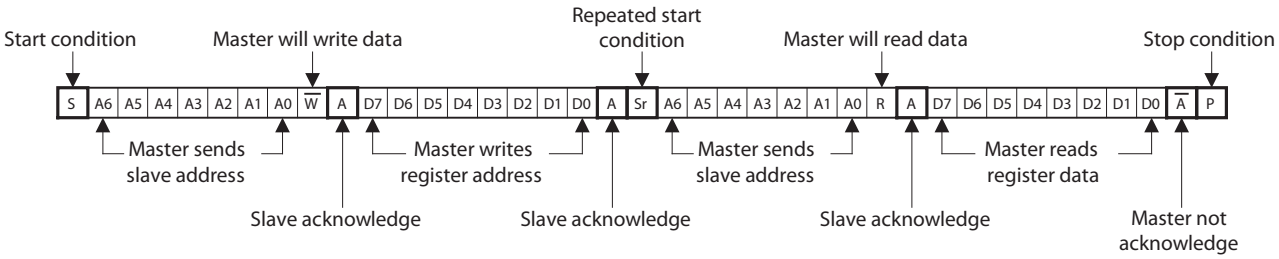


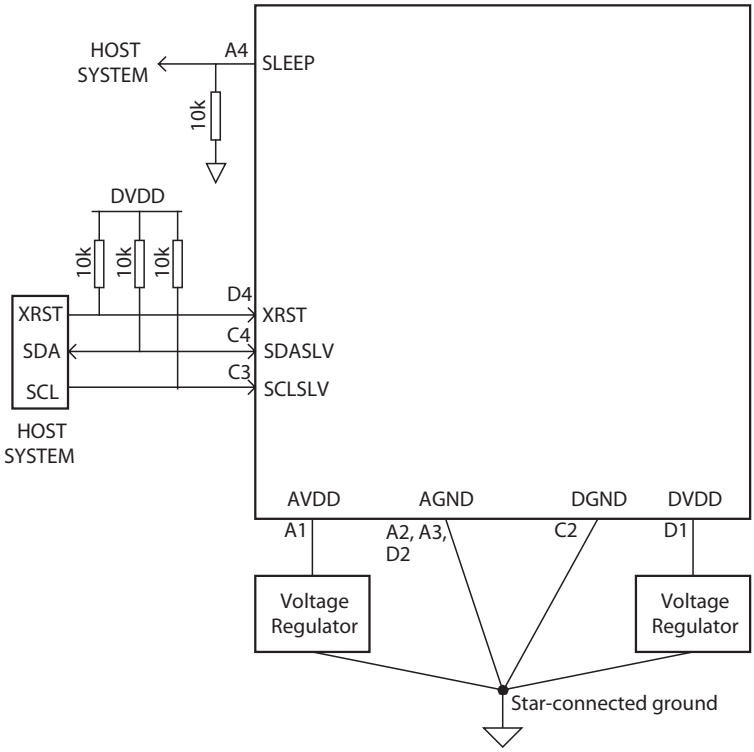
Figure 9: Register Byte Read Protocol

Powering the Device

Ground Connection

AGND and DGND must both be set to 0V and preferably star-connected to a central power source as shown in the application diagram. A potential difference between AGND and DGND may cause the ESD diodes to turn on inadvertently.

Application Diagrams



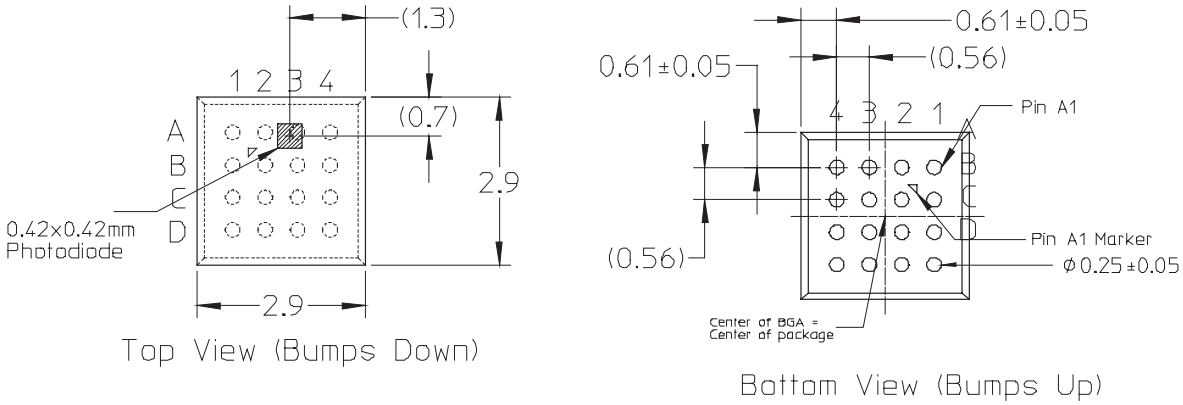
Pin Information

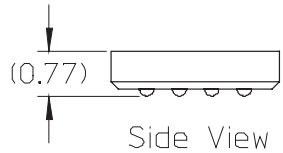
Pin	Name	Type	Description
A1	AVDD	Power	Analog power pin.
A2	AGND	Ground	Tie to analog ground.
A3	AGND	Ground	Tie to analog ground.
A4	SLEEP	Input	When SLEEP=1, the device goes into sleep mode. In sleep mode, all analog circuits are powered down and the clock signal is gated away from the core logic resulting in very low current consumption.
B1	NC	No connect	No connect. Leave floating.
B2	NC	No connect	No connect. Leave floating.
B3	NC	No connect	No connect. Leave floating.
B4	NC	No connect	No connect. Leave floating.
C1	NC	No connect	No connect. Leave floating
C2	DGND	Ground	Tie to digital ground.
C3	SCLSLV	Input	SDASLV and SCLSLV are the serial interface communications pins. SDASLV is the bidirectional data pin and SCLSLV is the interface clock. A pull-up resistor should be tied to SDASLV because it goes tri-state to output logic 1.
C4	SDASLV	Input/ Output(tri-state high)	
D1	DVDD	Power	Digital power pin.
D2	AGND	Ground	Tie to analog ground.
D3	NC	No connect	No connect. Leave floating.
D4	XRST	Input	Global, asynchronous, active-low system reset. When asserted low, XRST resets all registers. Minimum reset pulse low is 1 us and must be provided by external circuitry.

Pin Configuration

	1	2	3	4
A	AVDD	AGND	AGND	SLEEP
B	NC	NC	NC	NC
C	NC	DGND	SCLSLV	SDASLV
D	DVDD	AGND	NC	XRST

Package Dimensions

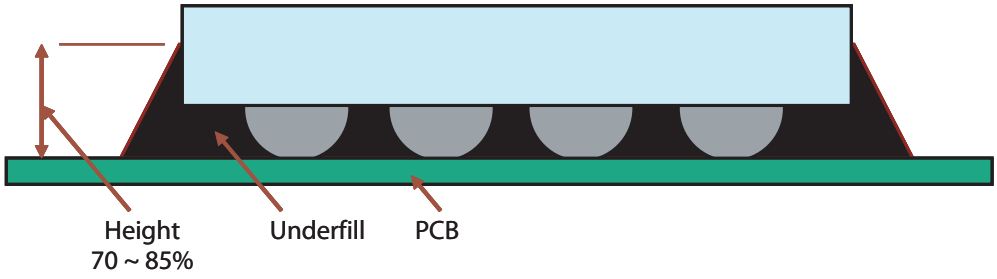




Note:
1. Dimensions are in milimeters (mm)
2. Standard tolerances (unless otherwise specified)
   a. Linear tolerance = +/-0.1mm
   b. Angular tolerance = +/-1°

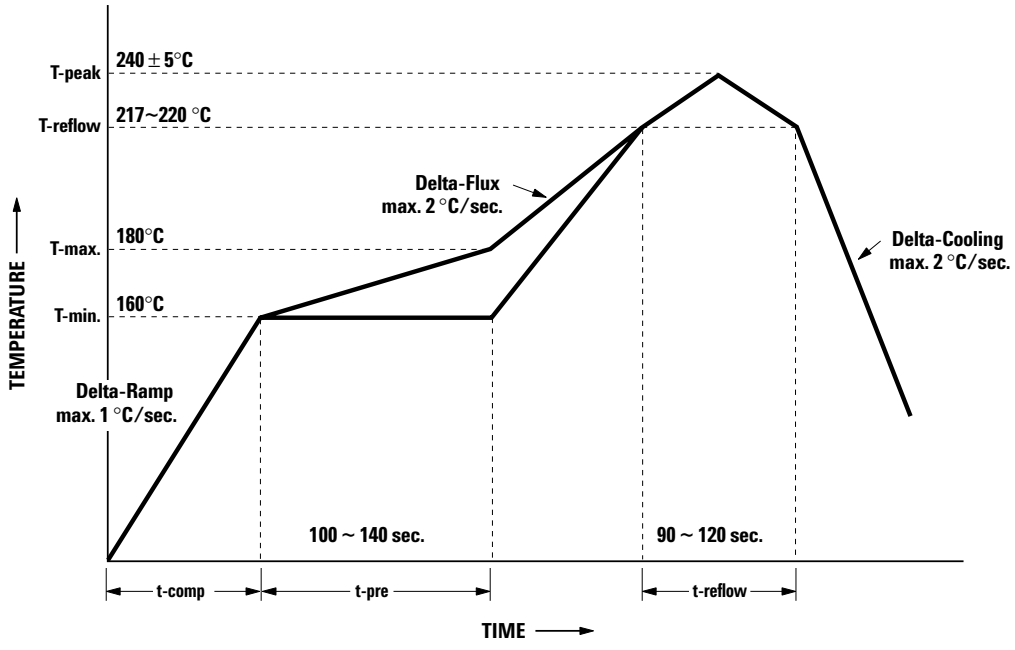
Recommended Underfill Type and Characteristic

- Low moisture absorption type
- Total height of underfill from PCB plane to cover up 70 – 85 %
- Underfill to cover all 4 side of the package



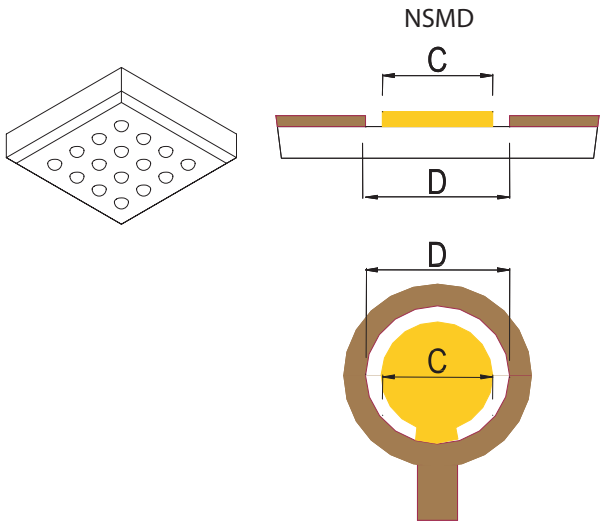
Recommended Reflow Profile

It is recommended that Henkel Pb-free solder paste LF310 be used for soldering ADJD-S312-CR999. Below is the recommended reflow profile.



Recommended PCB land pad design

- NiAu flash over copper pad
- Pad Diameter (C)= 0.20 mm
- NSMD Diameter (D)= 0.25 ~ 0.30 mm

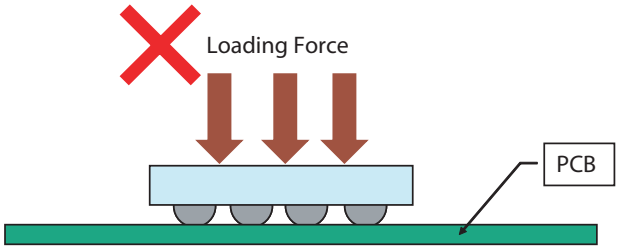


After soldering or mounting precaution

Please ensure that all soldered or reflowed CSP package that is mounted on the PCB is not exposed to compression or loading force directly perpendicular to the flat top surface.

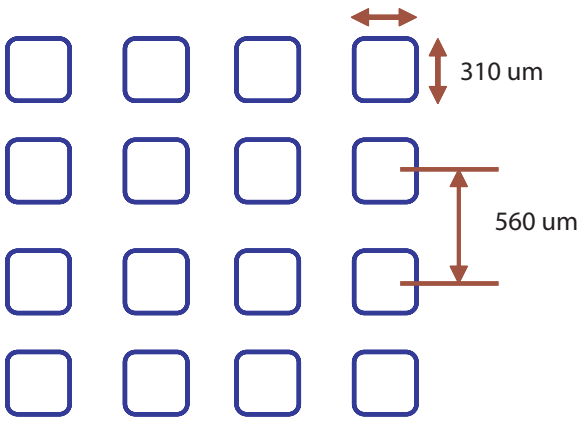
Precaution:

Excessive loading force directly perpendicular to the flat top surface may cause pre-mature failure.



Recommended Stencil Design

- Stencil thickness 5 mils
- Stencil type Ni Electroforming
- Stencil Aperture Type Square
- Stencil Aperture 310 um
- Additional Feature Rounded square edge



Recommendations for Handling and Storage of ADJD-S312

This product is qualified as Moisture Sensitive Level 3 per Jedec J-STD-020. Precautions when handling this moisture sensitive product is important to ensure the reliability of the product. Do refer to Avago Application Note AN5305 Handling Of Moisture Sensitive Surface Mount Devices for details.

A. Storage before use

- Unopened moisture barrier bag (MBB) can be stored at 30°C and 90%RH or less for maximum 1 year
- It is not recommended to open the MBB prior to assembly (e.g. for IQC)
- It should also be sealed with a moisture absorbent material (Silica Gel) and an indicator card (cobalt chloride) to indicate the moisture within the bag

B. Control after opening the MBB

- The humidity indicator card (HIC) shall be read immediately upon opening of MBB
- The components must be kept at <30°C/60%RH at all time and all high temperature related process including soldering, curing or rework need to be completed within 168hrs

C. Control for unfinished reel

- For any unused components, they need to be stored in sealed MBB with desiccant or desiccator at <5%RH

D. Control of assembled boards

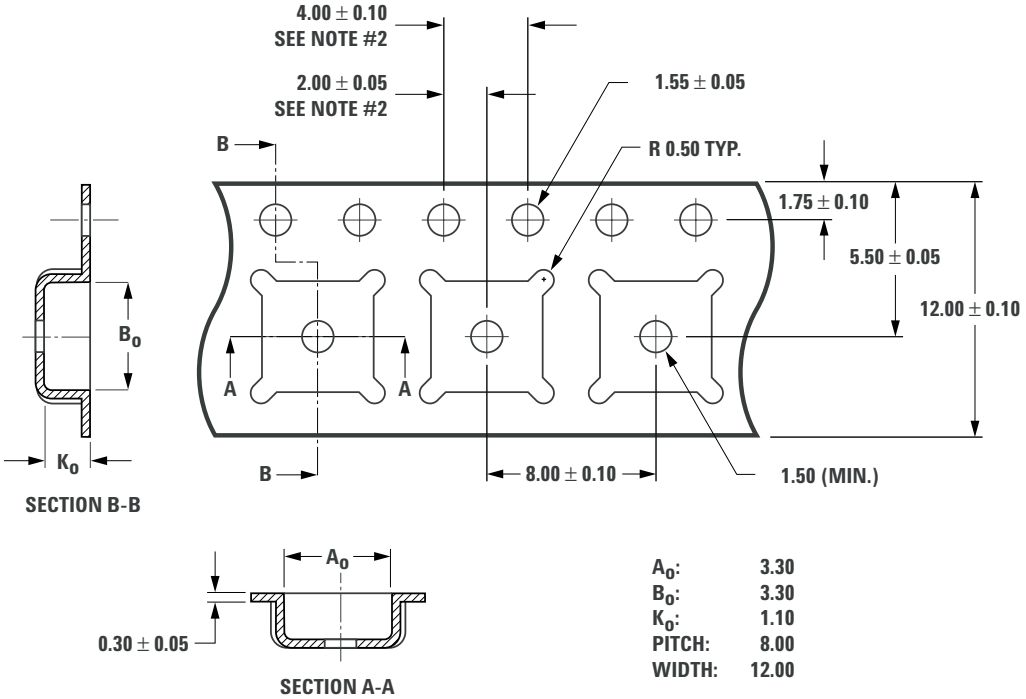
- If the PCB soldered with the components is to be subjected to other high temperature processes, the PCB need to be stored in sealed MBB with desiccant or desiccator at <5%RH to ensure no components have exceeded their floor life of 168hrs

E. Baking is required if:

- "10%" or "15%" HIC indicator turns pink
- The components are exposed to condition of >30°C/60%RH at any time.
- The components floor life exceeded 168hrs
- Recommended baking condition (in component form): 125°C for 24hrs

Package Tape and Reel Dimensions

Carrier Tape Dimensions

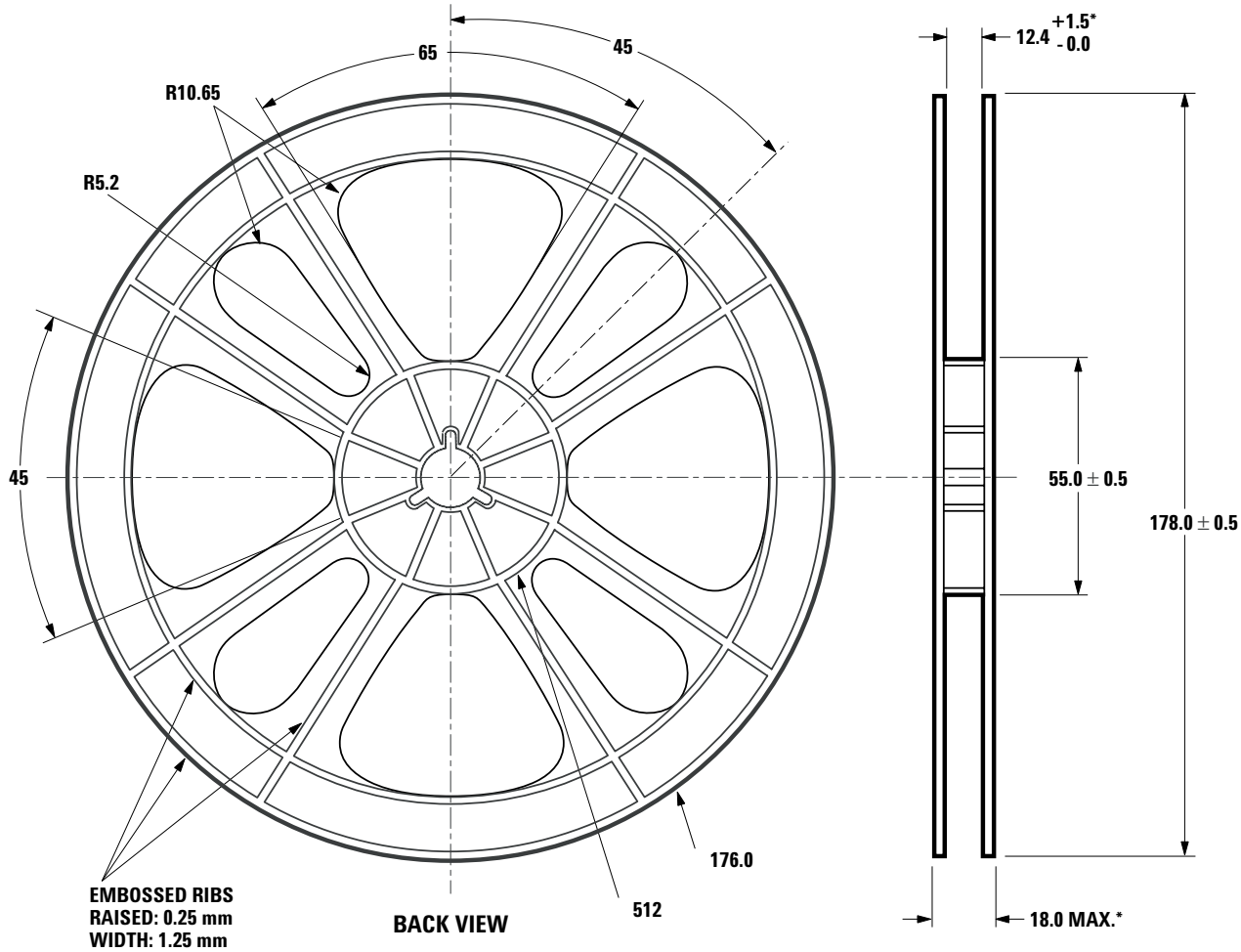


A_0:	3.30
B_0:	3.30
K_0:	1.10
PITCH:	8.00
WIDTH:	12.00

NOTES:

1. A_0 AND B_0 MEASURED AT 0.3 mm ABOVE BASE OF POCKET.
2. 10 PITCHES CUMULATIVE TOLERANCE IS ± 0.2 mm.
3. DIMENSIONS ARE IN MILLIMETERS (mm).

Reel Dimensions



NOTES:
1. *MEASURED AT HUB AREA.
2. ALL FLANGE EDGES TO BE ROUNDED.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0637EN - July 30, 2007