P4C151
ULTRA HIGH SPEED 1K x 4 RESETTABLE CACHE-TAG STATIC CMOS RAM (SCRAM)

FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  - 10/12/15/20/25 ns (Commercial)
  - 15/20/25/35 ns (Military)
- Fast Comparison Operation
  - 12 ns (Commercial)
  - 19 ns (Military)
- Chip Clear Function
- Low Power Operation (Commercial Military)
  - 660 mW — 10/12 (Commercial)
  - 550/660 mW — 15/20/25/35
- Single Power Supply
  - 5V ±10%
- Common Data I/O
- Three-State Data Outputs
- Open-Drain MATCH Output
- Fully TTL Compatible Inputs and Outputs
- Produced with PACE II Technology™
- Compact Package
  - 20-Pin 300 mil DIP

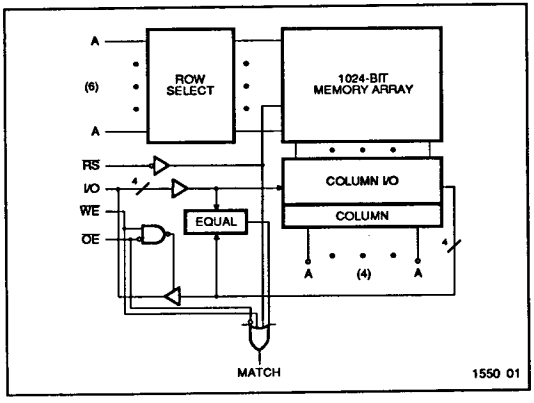
DESCRIPTION

The P4C151 is a 4,096-bit ultra high-speed static RAM with a built-in 4-bit comparator, organized as 1K x 4 for high speed cache-tag applications. The RAM can be used to determine if a 14-bit address consisting of the 10-bit RAM address and the 4-bit tag data is in the cache. A single reset control clears all tag words in the RAM to zero when activated, for flash-clearing of the cache-tag memory during system operation or system reset. The comparison output MATCH is open-drain for wired-OR expandability. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs and outputs are fully TTL-compatible. The RAM operates from a single 5V ± 10% tolerance power supply.

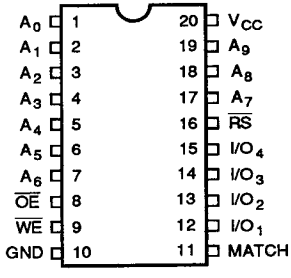
Access times as fast as 10 nanoseconds with comparison times of 12 ns are available, permitting greatly enhanced system operating speeds. The time required for reset is only 20 ns for the 10 ns SRAM. CMOS is utilized to reduce power consumption to a low level. The P4C151 is a member of a family of PACE RAM™ products offering super fast access times never before available at these complexity levels in TTL-compatible bipolar or CMOS technologies. The P4C151 is manufactured using PACE II Technology™.

The P4C151 is available in a 20-pin 300 mil DIP package providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

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Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Military	–55 to +125°C	0V	5.0V ± 10%

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Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions	P4C151		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage		–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC}–0.2	V_{CC}+0.5	V
V_{LC}	CMOS Input Low Voltage		–0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA	—	–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +10 mA, V_{CC} = Min. I_{OL} = +8 mA, V_{CC} = Min.	— —	0.5 0.4	V
V_{OLC}	Output Low Voltage (CMOS Load)	I_{OLC} = +100 µA, V_{CC} = Min.		0.2	V
V_{OH}	Output High Voltage (TTL Load) except MATCH output	I_{OH} = –4 mA, V_{CC} = Min.	2.4	—	V
V_{OHC}	Output High Voltage (CMOS Load) except MATCH output	I_{OHC} = –100 µA, V_{CC} = Min.	V_{CC}–0.2	—	V
I_{LI}	Input Leakage Current	V_{CC} = Max. Mil. V_{IN} = GND to V_{CC} Com'l.	–10 –5	+10 +5	µA +5
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{OE}$ = V_{IH}, Mil. V_{OUT} = GND to V_{CC} Com'l.	–10 –5	+10 +5	µA

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CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF

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Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

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Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20 ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions		P4C150 Min	P4C150 Max	Unit
I_{CC}	Dynamic Operating Current – 10, 12	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	n/a	mA
			Com'l.	—	120	
I_{CC}	Dynamic Operating Current – 15, 20, 25, 35	V_{CC} = Max., f = Max., Outputs Open	Mil.	—	120	mA
			Com'l.	—	100	

n/a = Not Applicable

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AC CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-10* Min	-10* Max	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	-25 Min	-25 Max	-35 Min	-35 Max	Unit
t_{RC}	Read Cycle Time	10		12		15		20		25		35		ns
t_{AA}	Address Access Time		10		12		15		20		25		35	ns
t_{OH}	Output Hold from Address Change	2		2		2		2		2		2		ns
t_{OE}	Output Enable to Data Valid		7		9		10		14		15		20	ns
t_{OLZ}	Output Enable to Output in Low Z	1		1		1		2		2		2		ns
t_{OLZ}	Output Disable to Output in High Z		5		7		9		11		13		17	ns

*V_{CC} = 5V ± 5% for -10

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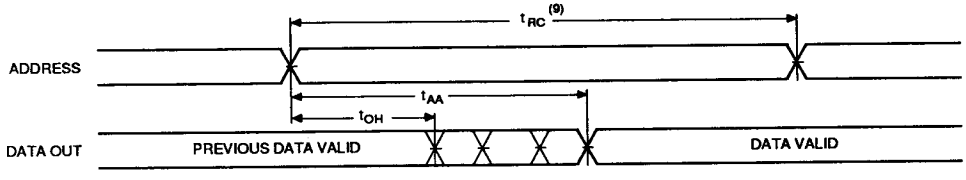
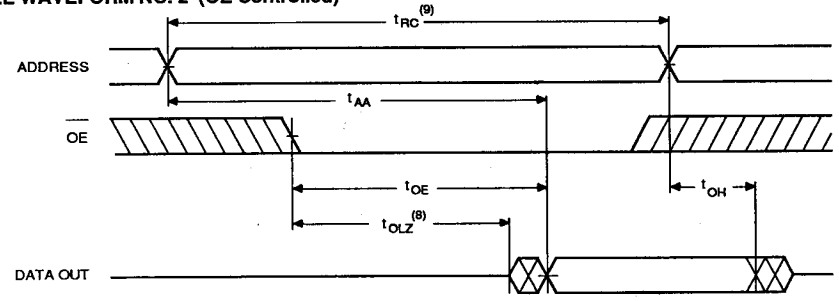
TIMING WAVEFORM OF READ CYCLE NO. 1 (ADDRESS Controlled) [5,6]



1550 03

Notes:
5. $\overline{WE}$ is high for READ cycle.
6. $\overline{CS}$ and $\overline{OE}$ are low for READ cycle.

READ CYCLE WAVEFORM NO. 2 ($\overline{OE}$ Controlled) [5]



1550 04

Notes:

7. ADDRESS must be valid prior to, or concident with, $\overline{CS}$ transition low, t_{AA} must still be met.
8. Transition is measured ±200 mV from steady state voltage prior to change, with loading as specified in Figure 1.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

AC CHARACTERISTICS—RESET CYCLE

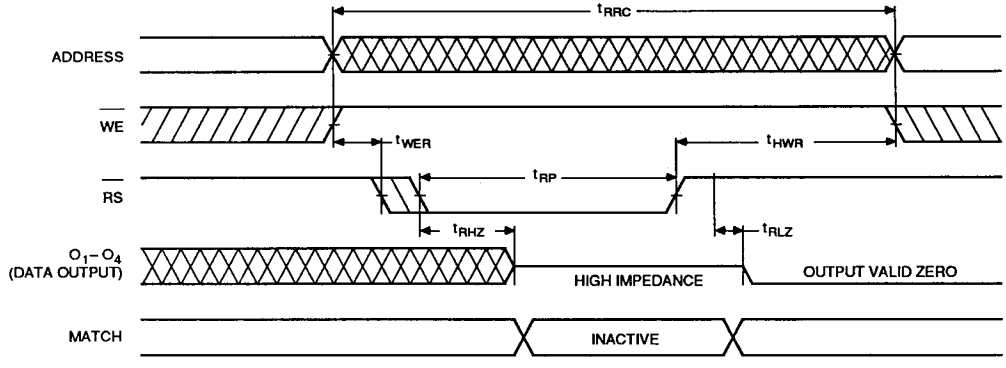
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RRC}	Reset Cycle Time	20		24		30		40		50		70		ns
t_{WER}	Write Enable High to Beginning of Reset	0		0		0		0		0		0		ns
t_{RP}	Reset Pulse Width	10		12		15		20		25		30		ns
t_{HWR}	Write Enable Hold after End of Reset	10		12		15		20		25		40		ns
t_{RLZ}	Reset High to Output in Low Z	0		0		0		0		0		0		ns
t_{RHZ}	Reset Low to Output in High Z	0	8	0	10	0	12	0	16	0	20	0	25	ns

*V_{CC} = 5V ± 5% for -10

1550 Tbl 10

TIMING WAVEFORM OF RESET CYCLE



1550 05

AC CHARACTERISTICS—COMPARE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{CC}	Compare Cycle Time	12		15		19		25		30		40		ns
t_{RCS}	Read Command Set–up	0		0		0		0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		0		0		0		ns
t_{CCS}	Compare Command Set–up	3		4		5		7		8		10		ns
t_{CCH}	Compare Command Hold	0		0		0		0		0		0		ns
t_{DCA}	Compare Access after Data–in Valid		6		8		9		12		15		20	ns
t_{ACA}	Compare Access after Address Valid		12		15		19		25		30		35	ns
t_{DCH}	Compare Hold after Data–in Change	1		1		2		3		3		3		ns
t_{ACH}	Compare Hold after Address Change	3		3		4		5		5		5		ns

*V_{cc} = 5V ± 5% for -10

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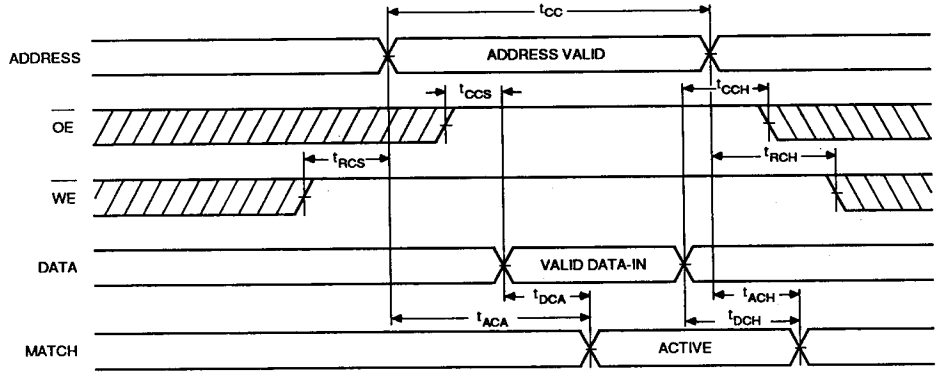
COMPARE CYCLE WAVEFORM



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AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10		12		15		20		25		35		ns
t_{AW}	Address Valid to End of Write	8		10		13		16		20		30		ns
t_{AS}	Address Set-up Time	0		1		1		1		2		3		ns
t_{WP}	Write Pulse Width	8		10		11		13		15		20		ns
t_{AH}	Address Hold Time	0		1		1		1		2		3		ns
t_{WR}	Write Recovery Time	0		1		1		1		2		3		ns
t_{DW}	Data Valid to End of Write	5		8		11		13		15		20		ns
t_{DH}	Data Hold Time	0		1		1		1		2		3		ns
t_{WZ}	Write Enable to Output in High Z		5		8		12		15		20		25	ns
t_{OW}	Output Active from End of Write	2		2		2		3		3		3		ns

*V_{CC} = 5V ± 5% for -10

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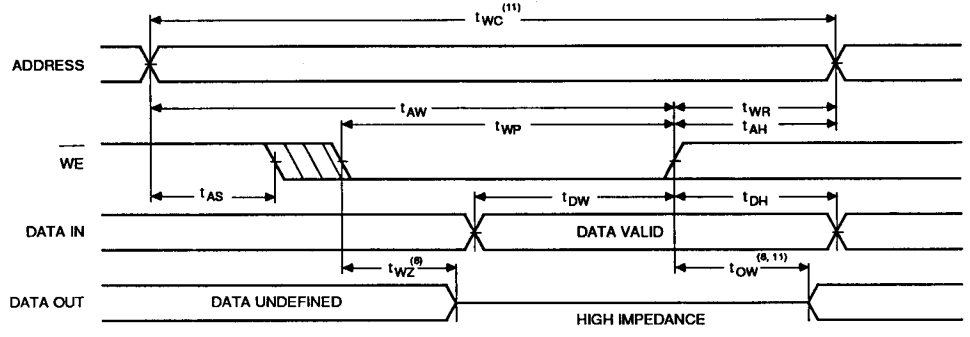
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled) [10]



1550 07

Notes:
10. $\overline{WE}$ must be low for WRITE cycle.
11. Write Cycle Timing is measured from the last valid address to the first transitioning address.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

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TRUTH TABLE

Mode	$\overline{RS}$	$\overline{OE}$	$\overline{WE}$	MATCH	Output
COMPARE	H	H	H	Valid	High Z
READ	H	L	H	Invalid	D_{OUT}
WRITE	H	X	L	Invalid	High Z
RESET	L	X	H	Invalid	High Z

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Note:
MATCH "Valid" means output is OFF if HIT, output voltage is V_{OL} if MISS. Match output is forced high during test.

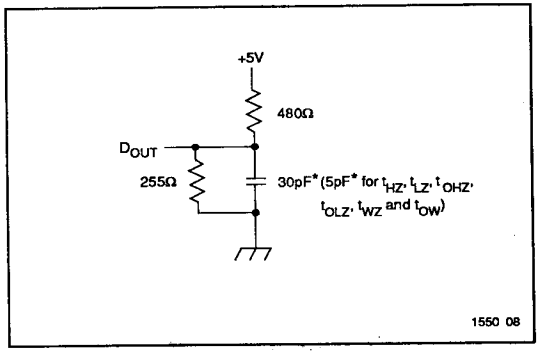


Figure 1. Output Load

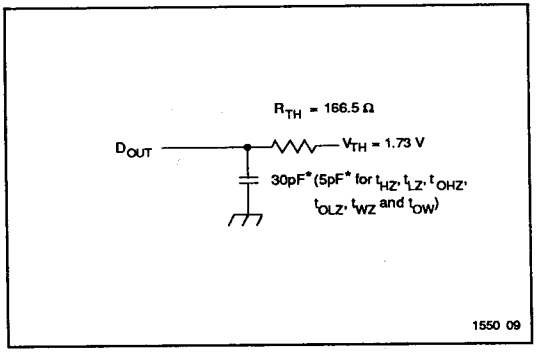


Figure 2. Thevenin Equivalent

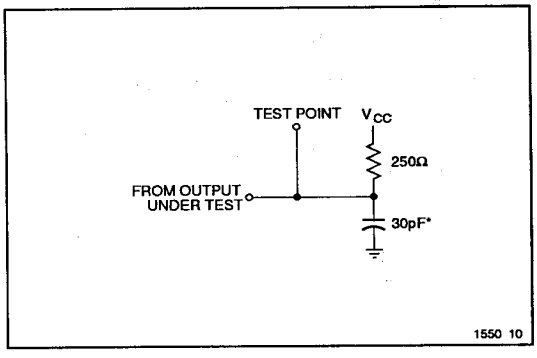


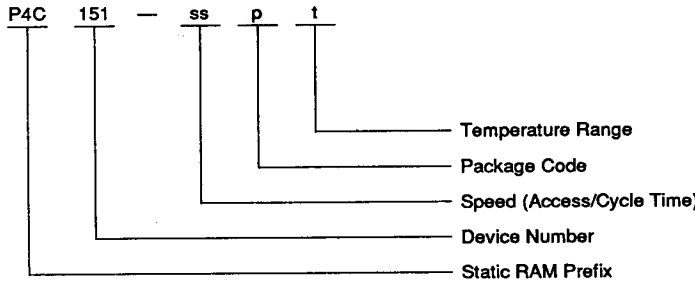
Figure 3. Match Output Load Circut

* including scope and test fixture.

Note:
Due to the ultra-high speed of the P4C151, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{cc} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{cc} and ground.

To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



ss = Speed (access/cycle time in ns), e.g., 10, 15
p = Package code, i.e., P, D.
t = Temperature range, i.e., C, M, MB.

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PACKAGE SUFFIX

Package Suffix	Description
P	Plastic DIP, 300 mil wide standard
D	CERDIP, 300 mil wide standard

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TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C – +70°C.
M	Military Temperature Range, –55°C – +125°C.
MB	Mil. Temp. with MIL-STD-883C Class B compliance

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SELECTION GUIDE

The P4C151 is available in the following temperature, speed and package options.

Temperature Range	Speed (ns) / Package	10	12	15	20	25	35
Commercial	Plastic DIP	-10PC	-12PC	-15PC	-20PC	-25PC	N/A
	CERDIP	N/A	-12DC	-15DC	-20DC	-25DC	N/A
Military Temp.	CERDIP	N/A	N/A	-15DM	-20DM	-25DM	-35DM
Military Processed*	CERDIP	N/A	N/A	-15DMB	-20DMB	-25DMB	-35DMB

* Military temperature range with MIL-STD-883 Revision C, Class B processing.
N/A = Not available

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TECHDOC 1550