Lattice Semiconductor Corporation

ispGDX® Device Datasheet

June 2010

All Devices Discontinued!

Product Change Notification (PCN) #09-10 has been issued to discontinue all devices in this data sheet.

The original datasheet pages have not been modified and do not reflect those changes. Please refer to the table below for reference PCN and current product status.

Product Line	Ordering Part Number	Product Status	Reference PCN
ispGDX80A	ispGDX80A-5T100	**Discontinued**	PCN#09-10
	ispGDX80A-7T100		
ispGDX120A	ispGDX120A-5Q160		
	ispGDX120A-7Q160		
	ispGDX120A-5T176		
	ispGDX120A-7T176		
ispGDX160A	ispGDX160A-5B272		
	ispGDX160A-7B272		
	ispGDX160A-5Q208		
	ispGDX160A-7Q208		

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Lattice Semiconductor Corporation

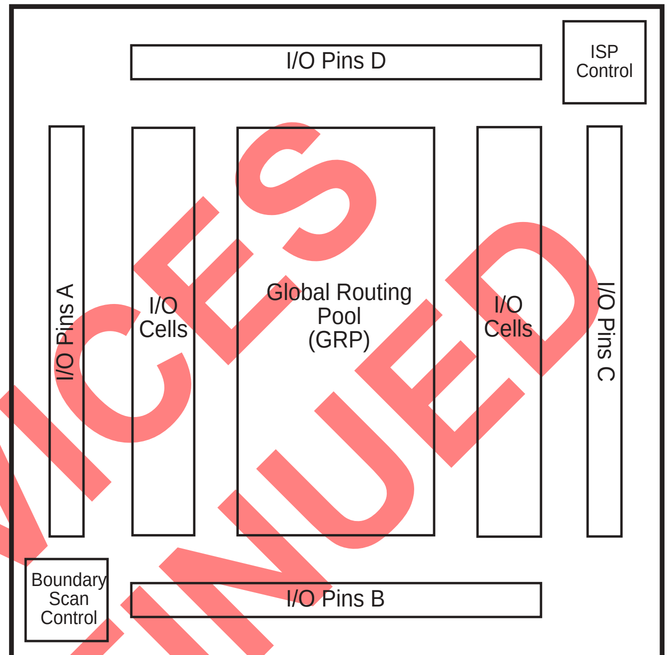
ispGDX® Family

In-System Programmable Generic Digital Crosspoint

Features

- **IN-SYSTEM PROGRAMMABLE GENERIC DIGITAL CROSSPOINT FAMILY**
  - **— Advanced Architecture Addresses Programmable PCB Interconnect, Bus Interface Integration and Jumper/Switch Replacement**
  - **— Three Device Options: 80 to 160 Programmable I/O Pins**
  - **— "Any Input to Any Output" Routing**
  - **— Fixed HIGH or LOW Output Option for Jumper/DIP Switch Emulation**
  - **— Space-Saving TQFP, PQFP and BGA Packaging**
  - **— Dedicated IEEE 1149.1-Compliant Boundary Scan Test**
  - **— PCI Compliant Output Drive**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 5V Power Supply**
  - **— 5.0ns Input-to-Output/5.0ns Clock-to-Output Delay**
  - **— Low-Power: 40mA Quiescent Icc**
  - **— Balanced 24mA Output Buffers with Programmable Slew Rate Control**
  - **— Schmitt Trigger Inputs for Noise Immunity**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E²CMOS Technology**
  - **— 100% Tested**
- **ispGDX OFFERS THE FOLLOWING ADVANTAGES**
  - **— In-System Programmable**
  - **— Lattice ISP or JTAG Programming Interface**
  - **— Only 5V Power Supply Required**
  - **— Change Interconnects in Seconds**
  - **— Reprogram Soldered Devices**
- **FLEXIBLE ARCHITECTURE**
  - **— Combinatorial/Latched/Registered Inputs or Outputs**
  - **— Individual I/O Tri-state Control with Polarity Control**
  - **— Dedicated Clock Input Pins (two or four) or Programmable Clocks from I/O Pins (from 20 up to 40)**
  - **— Up to 4:1 Dynamic Path Selection**
  - **— Programmable Output Pull-up Resistors**
  - **— Outputs Tri-state During Power-up ("Live Insertion" Friendly)**

Functional Block Diagram



Description

The ispGDX architecture provides a family of fast, flexible programmable devices to address a variety of system-level digital signal routing and interface requirements including:

- Multi-Port Multiprocessor Interfaces
- Wide Data and Address Bus Multiplexing (e.g. 4:1 High-Speed Bus MUX)
- Programmable Control Signal Routing (e.g. Interrupts, DMAREQs, etc)
- Board-Level PCB Signal Routing for Prototyping or Programmable Bus Interfaces

The ispGDX Family consists of three members with 80, 120 and 160 Programmable I/Os. These devices are available in packages ranging from the 100-pin TQFP to the 208-pin PQFP. The devices feature fast operation, with input-to-output signal delays (Tpd) of 5ns and clock-to-output delays of 5ns.

The architecture of the devices consists of a series of programmable I/O cells interconnected by a Global Rout-

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November 2003

Description (Continued)

ing Pool (GRP). All I/O pin inputs enter the GRP directly or are registered or latched so they can be routed to the required I/O outputs. I/O pin inputs are defined as four sets (A,B,C,D) which have access to the four MUX inputs found in each I/O cell. Each output has individual, programmable I/O tri-state control (OE), output latch clock (CLK) and two multiplexer control (MUX0 and MUX1) inputs. Polarity for these signals is programmable for each I/O cell. The MUX0 and MUX1 inputs control a fast 4:1 MUX, allowing dynamic selection of up to four signal sources for a given output. OE, CLK and MUX0 and MUX1 inputs can be driven directly from selected sets of I/O pins. Optional dedicated clock input pins give minimum clock-to-output delays.

Through in-system programming, connections between I/O pins and architectural features (latched or registered inputs or outputs, output enable control, etc.) can be defined. In keeping with its data path application focus, the ispGDX devices contain no programmable logic arrays. All input pins include Schmitt trigger buffers for noise immunity. These connections are programmed into the device using non-volatile E^2CMOS technology. Non-volatile technology means the device configuration is saved even when the power is removed from the device.

In addition, there are no pin-to-pin routing constraints for 1:1 or 1:n signal routing. That is, *any* I/O pin configured as an input can drive one or more I/O pins configured as outputs.

The device pins also have the ability to set outputs to fixed HIGH or LOW logic levels (Jumper or DIP Switch mode). Device outputs are specified for 24mA sink and source current and can be tied together in parallel for greater drive. Programmable output slew rate can be defined independently for each I/O pin to reduce overall ground bounce and switching noise.

All I/O pins are equipped with IEEE1149.1-compliant Boundary Scan Test circuitry for enhanced testability. In addition, in-system programming is supported through the Test Access Port via a special set of private commands or through Lattice's industry-standard ISP protocol. The BSCAN/$\overline{\text{ispEN}}$ pin is used to make this selection.

The ispGDX I/Os are designed to withstand "live insertion" system environments. The I/O buffers are disabled during power-up and power-down cycles. When designing for "live insertion," absolute maximum rating conditions for the Vcc and I/O pins must still be met. For additional information, an application note about using Lattice devices in hot swap environments can be downloaded from the Lattice web site at www.latticesemi.com.

Table 1. ispGDX Family Members

	ispGDX DEVICE		
	ispGDX80A	ispGDX120A	ispGDX160A
I/O Pins	80	120	160
I/O-OE Inputs*	20	30	40
I/O-Clk Inputs*	20	30	40
I/O-MUXsel1 Inputs*	20	30	40
I/O-MUXsel2 Inputs*	20	30	40
Dedicated Clock Pins	2	4	4
BSCAN / $\overline{\text{ispEN}}$	1	1	1
TOE	1**	1	1
BSCAN / ISP Interface	4	4	4
$\overline{\text{RESET}}$	1	1	1
Power/GND	12	25	33
Pin Count/Package	100-Pin TQFP	176-Pin TQFP/ 160-Pin PQFP	208-Pin PQFP 272-Ball BGA

* The CLK, OE, MUX0 and MUX1 terminals on each I/O cell can each access 25% of the I/Os.
** MUXed with Y1.

Architecture

The ispGDX architecture is different from traditional PLD architectures, in keeping with its unique application focus. The block diagram is shown below. The programmable interconnect consists of a single Global Routing Pool (GRP). Unlike ispLSI® devices, there are no programmable logic arrays on the device. Control signals for OEs, Clocks and MUX Controls must come from designated sets of I/O pins. The polarity of these signals can be independently programmed in each I/O cell.

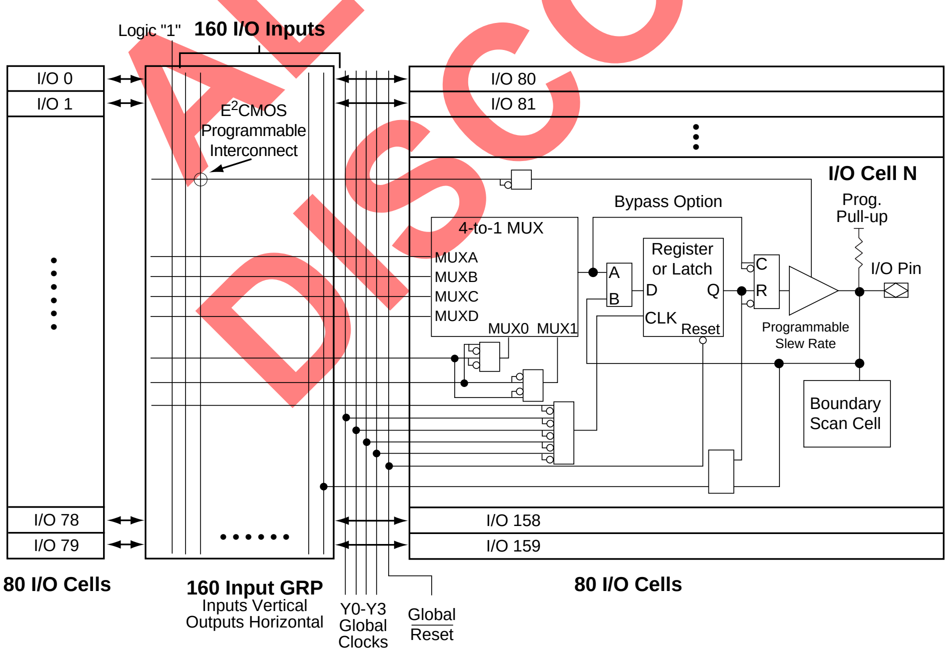
Each I/O cell drives a unique pin. The OE control for each I/O pin is independent and may be driven via the GRP by one of the designated I/O pins (I/O-OE set). The I/O-OE set consists of 25% of the total I/O pins. Boundary Scan test is supported by dedicated registers at each I/O pin. The in-system programming process uses either a Boundary Scan based or Lattice ISP protocol. The programming protocol is selected by the BSCAN/ispEN pin as described later.

The various I/O pin sets are also shown in the block diagram below. The A, B, C, and D I/O pins are grouped together with one group per side.

I/O Architecture

Each I/O cell contains a 4:1 dynamic MUX controlled by two select lines called MUX0 and MUX1 as shown in Figure 1. The four data inputs to the MUX (called MUXA, MUXB, MUXC and MUXD) come from I/O signals found in the GRP. Each MUX data input can access one quarter of the total I/Os. For example, in a 160 I/O ispGDX, each data input can connect to one of 40 I/O pins. MUX0 and MUX1 can be driven by designated I/O pins called MUXsel1 and MUXsel2. Each MUXsel input covers 25% of the total I/O pins (e.g. 40 out of 160). MUX0 and MUX1 can be driven from either MUXsel1 or MUXsel2. The I/O cell also includes a programmable flow-through latch or register that can be placed in the input or output path and bypassed for combinatorial outputs. As shown in Figure 1, when both register/latch control MUXes select the “A” path, the register/latch gets its inputs from the 4:1 MUX and drives the I/O output. When selecting the “B” path, the register/latch is directly driven by the I/O input while its output feeds the GRP. The programmable polarity Clock to the latch or register can be connected to any I/O in the I/O-Clock set (one-quarter of total I/Os) or to one of the dedicated clock input pins (Y_X). Use of the dedicated clock inputs gives minimum clock-to-output delays and minimizes delay variation with fanout. Combinatorial output mode may be implemented by a dedicated architecture bit and bypass MUX. I/O cell output polarity can be programmed as active high or active low.

Figure 1. ispGDX I/O Cell and GRP Detail (160 I/O Device)



I/O MUX Operation

MUX1	MUX0	DATA INPUT SELECTED
0	0	MUXA
0	1	MUXB
1	1	MUXC
1	0	MUXD

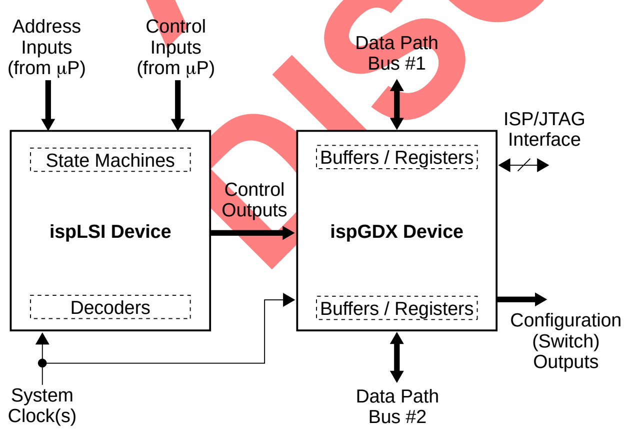
Applications

The ispGDX family architecture has been developed to deliver an in-system programmable signal routing solution with high speed and high flexibility. The devices are targeted for three similar but distinct classes of end-system applications:

Programmable, Random Signal Interconnect (PRSI)
This class includes PCB-level programmable signal routing and may be used to provide arbitrary signal swapping between chips. It opens up the possibilities of programmable system hardware. It is characterized by the need to provide a large number of 1:1 pin connections which are statically configured, i.e., the pin-to-pin paths do not need to change dynamically in response to control inputs.

Programmable Data Path (PDP)
This application area includes system data path transceiver, MUX and latch functions. With today's 32- and 64-bit microprocessor buses, but standard data path glue components still relegated primarily to eight bits, PCBs are frequently crammed with a dozen or more data path glue chips that use valuable real estate. Many of these applications consist of "on-board" bus and memory interfaces that do not require the very high drive of standard glue functions but can benefit from higher integration. Therefore, there is a need for a flexible means to integrate these on-board data path functions in an analogous way to programmable logic's solution to control logic integration. Lattice's ispLSI High-Density PLDs make an ideal control logic complement to the ispGDX in-system programmable data path devices as shown below.

Figure 2. ispGDX Complements Lattice ispLSI



Programmable Switch Replacement (PSR)
Includes solid-state replacement and integration of mechanical DIP Switch and jumper functions. Through in-system programming, pins of the ispGDX devices can be driven to HIGH or LOW logic levels to emulate the traditional device outputs. PSR functions do not require any input pin connections.

These applications actually require somewhat different silicon features. PRSI functions require that the device support arbitrary signal routing on-chip between any two pins with no routing restrictions. The routing connections are static (determined at programming time) and each input-to-output path operates independently. As a result, there is little need for dynamic signal controls (OE, clocks, etc.). Because the ispGDX device will interface with control logic outputs from other components (such as ispLSI) on the board (which frequently change late in the design process as control logic is finalized), there must be no restrictions on pin-to-pin signal routing for this type of application.

PDP functions, on the other hand, require the ability to dynamically switch signal routing (MUXing) as well as latch and tri-state output signals. As a result, the programmable interconnect is used to define *possible* signal routes that are then selected dynamically by control signals from an external MPU or control logic. These functions are usually formulated early in the conceptual design of a product. The data path requirements are driven by the microprocessor, bus and memory architecture defined for the system. This part of the design is the earliest portion of the system design frozen, and will not usually change late in the design because the result would be total system and PCB redesign. As a result, the ability to accommodate *arbitrary* any pin-to-any pin re-routing is not a strong requirement as long as the designer has the ability to define his functions with a reasonable degree of freedom initially.

As a result, the ispGDX architecture has been defined to support PSR and PRSI applications (including bidirectional paths) with no restrictions, while PDP applications (using dynamic MUXing) are supported with a minimal number of restrictions as described below. In this way, speed and cost can be optimized and the devices can still support the system designer's needs.

The following diagrams illustrate several ispGDX applications.

Applications (Cont.)

Figure 3. Address Demultiplex/Data Buffering

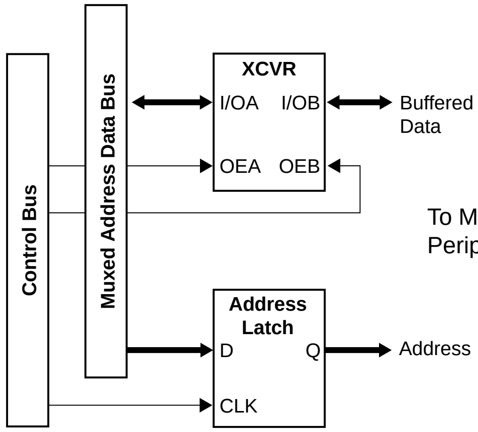


Figure 4. Data Bus Byte Swapper

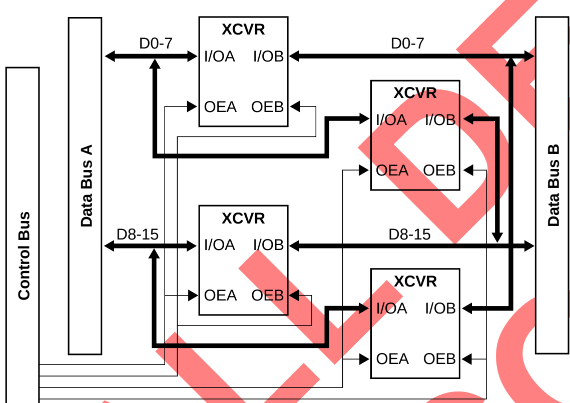
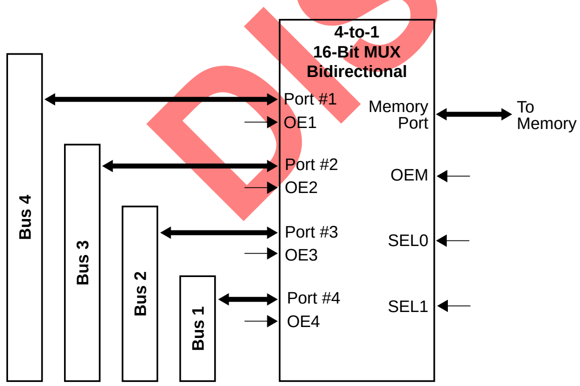


Figure 5. Four-Port Memory Interface



Note: All OE and SEL lines driven by external arbiter logic (not shown).

Designing with the ispGDX

As mentioned earlier, this architecture satisfies the PRSI class of applications without restrictions: any I/O pin as a single input or bidirectional can drive any other I/O pin as output.

For the case of PDP applications, the designer does have to take into consideration the limitations on pins that can be used as control (MUX0, MUX1, OE, CLK) or data (MUXA-D) inputs. The restrictions on control inputs are not likely to cause any major design issues because the input possibilities span 25% of the total pins.

The MUXA-D input partitioning requires that designers consciously assign pinouts so that MUX inputs are in the appropriate, disjoint groups. For example, since the MUXA group includes I/O0-19 (80 I/O device), it is not possible to use I/O0 and I/O9 in the same MUX function. As previously discussed, data path functions will be assigned early in the design process and these restrictions are reasonable in order to optimize speed and cost.

User Electronic Signature

The ispGDX Family includes dedicated User Electronic Signature (UES) E^2CMOS storage to allow users to code design-specific information into the devices to identify particular manufacturing dates, code revisions, or the like. The UES information is accessible through the boundary scan or Lattice ISP programming port via a specific command. This information can be read even when the security cell is programmed.

Security Bit

The ispGDX Family includes a security bit feature that prevents reading the device program once set. Even when set, it does not inhibit reading the UES or device ID code. It can be erased only via a device bulk erase.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} .... -0.5 to +7.0V

Input Voltage Applied .... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature .... -65 to 150°C

Case Temp. with Power Applied .... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Conditions

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial T_A = 0°C to +70°C	4.75	5.25	V
V_{IL}[1]	Input Low Voltage		0	0.8	V
V_{IH}[1]	Input High Voltage		2.0	V_{CC} + 1	V

1. Typical 100mV of input hysteresis.

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	8	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Dedicated Clock Capacitance	10	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2 - 0006

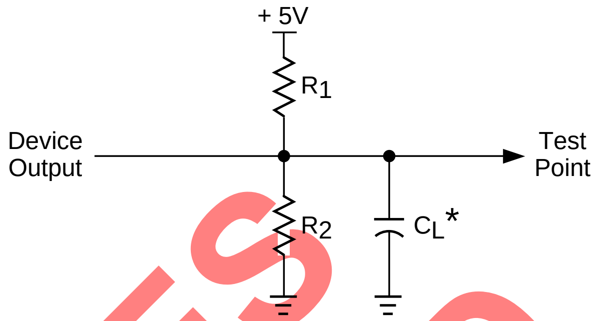
Erase/Reprogram Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
ispGDX Erase/Reprogram Cycles	10,000	–	Cycles

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure at right

3-state levels are measured 0.5V from steady-state active level.



*C_L includes Test Fixture and Probe Capacitance.

Output Load Conditions

TEST CONDITION		R1	R2	CL
A		160Ω	90Ω	35pF
B	Active High	∞	90Ω	35pF
	Active Low	160Ω	90Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	90Ω	5pF
	Active Low to Z at V_{OL}+0.5V	160Ω	90Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =24 mA	–	–	0.55	V
V_{OH}	Output High Voltage	I_{OH} =-24 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	–	–	10	µA
$I_{IL\text{-}isp}$	ispEN Input Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	–	–	-150	µA
$I_{IL\text{-}PU}$	I/O Active Pull-Up Current	$0V \le V_{IN} \le V_{IL}$	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V, T_A = 25°C	-100	–	-250	mA
I_{CCQ}	Quiescent Power Supply Current	V_{IL} = 0.5V, V_{IH} = V_{CC}	–	25	40	mA
I_{CC}	Dynamic Power Supply Current per Input Switching	One input toggling @ 50% duty cycle, outputs open.	–	See Note 3	–	mA/MHz

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Typical values are at V_{CC} = 5V and T_A = 25°C.
3. I_{CC} / MHz = (0.0114 x I/O cell fanout) + 0.06
   e.g. An input driving four I/O cells at 40 MHz results in a dynamic I_{CC} of approximately ((0.0114 x 4) + 0.06) x 40 = 4.2 mA.

External Timing Parameters

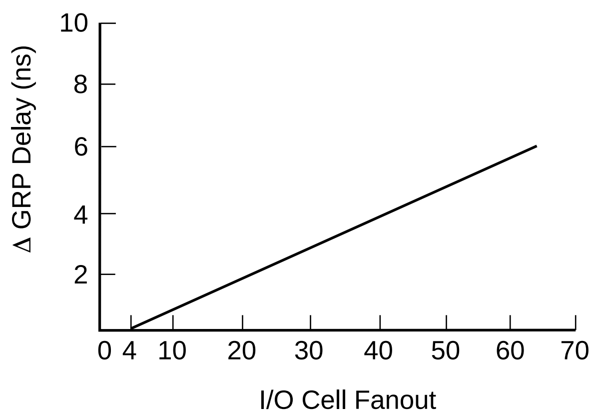
Over Recommended Operating Conditions

PARAMETER	TEST[1] COND.	#	DESCRIPTION	-5		-7		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd	A	1	Data Propagation Delay from any I/O pin to any I/O pin	–	5.0	–	7.0	ns
tsel	A	2	Data Propagation Delay from MUXsel Inputs to any Output	–	6.5	–	9.0	ns
fmax(ext)	–	3	Clock Frequency with External Feedback $\left(\frac{1}{tsu2+tgco1}\right)$	111	–	80.0	–	MHz
tsu1	–	4	Input Latch or Register Setup Time before any Clk	4.0	–	5.5	–	ns
tsu2	–	5	Output Latch or Register MUX Data Setup Time before any Clk	4.0	–	5.5	–	ns
th	–	6	Latch or Register Hold Time after any Clk	0.0	–	0.0	–	ns
tgco1	A	7	Output Latch or Register Clk (from Y_x) to Output Delay	–	5	–	7.0	ns
tgco2	A	8	Input Latch or Register Clk (from Y_x) to Output Delay	–	8.5	–	11.0	ns
tco1	A	9	Output Latch or Register Clk (from I/O pin) to Output Delay		6.0		9.0	ns
tco2	A	10	Input Latch or Register Clock (from I/O pin) to Output Delay	–	9.5	–	13.0	ns
ten	B	11	Input to Output Enable	–	6.0	–	8.5	ns
tdis	C	12	Input to Output Disable	–	6.0	–	8.5	ns
ttoeen	B	13	Test OE Output Enable	–	9.0	–	12.0	ns
ttoedis	C	14	Test OE Output Disable	–	9.0	–	12.0	ns
twh	–	15	Clock Pulse Duration, High	3.5	–	5.0	–	ns
twl	–	16	Clock Pulse Duration, Low	3.5	–	5.0	–	ns
trst	–	17	Register Reset Delay from RESET Low	–	14.0	–	18.0	ns
trw	–	18	Reset pulse width	10.0	–	14.0	–	ns
tsl	A	19	Output Delay Adder for Output Timings Using Slow Slew Rate	–	5.0	–	7.0	ns
tsk	A	20	Output Skew (tgco1 across chip)	–	0.5	–	0.5	ns

1. All timings measured with one output switching, fast output slew rate setting, except tsl.

ispGDX timings are specified with a GRP load (fanout) of four I/O cells. The figure at right shows the Maximum Δ GRP Delay with increased GRP loads. These deltas apply to any signal path traversing the GRP (MUXA-D, OE, CLK, MUXsel0-1). Global Clock signals, which do not use the GRP, have no fanout delay adder.

Maximum Δ GRP Delay vs. I/O Cell Fanout



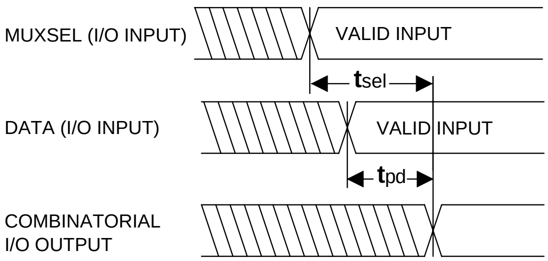
Internal Timing Parameters[1]

Over Recommended Operating Conditions

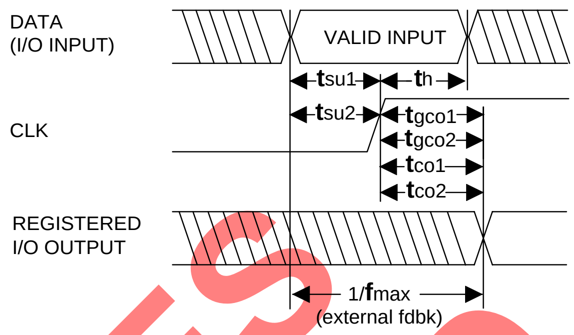
PARAMETER	#[2]	DESCRIPTION[1]	-5 MIN.	-5 MAX.	-7 MIN.	-7 MAX.	UNITS
Inputs							
t_{io}	21	Input Buffer Delay	—	0.7	—	1.3	ns
GRP							
t_{grp}	22	GRP Delay	—	2.0	—	2.5	ns
MUX							
t_{muxd}	23	I/O Cell MUX A/B/C/D Data Delay	—	1.0	—	1.4	ns
t_{muxs}	24	I/O Cell MUX A/B/C/D Data Select	—	2.5	—	3.4	ns
Register							
t_{iolat}	25	I/O Latch Delay	—	1.6	—	2.2	ns
t_{iosu}	26	I/O Register Setup Time Before Clock	—	1.6	—	1.8	ns
t_{ioh}	27	I/O Register Hold Time After Clock	—	2.4	—	3.6	ns
t_{ioco}	28	I/O Register Clock to Output Delay	—	1.6	—	2.2	ns
t_{ior}	29	I/O Reset to Output Delay	—	0.7	—	1.0	ns
Data Path							
t_{rfdbk}	30	I/O Register Feedback Delay	—	0.2	—	0.3	ns
t_{iobp}	31	I/O Register Bypass Delay	—	0.4	—	0.6	ns
t_{ioob}	32	I/O Register Output Buffer Delay	—	0.1	—	0.7	ns
t_{muxc} (Yx Clk)	33	I/O Register Data Input MUX Delay	—	1.1	—	1.2	ns
t_{muxc} (I/O Clk)	34	I/O Register Data Input MUX Delay	—	2.1	—	3.2	ns
t_{iod} (Yx Clk)	35	I/O Register I/O Input MUX Delay	—	4.1	—	5.1	ns
t_{iod} (I/O Clk)	36	I/O Register I/O Input MUX Delay	—	5.1	—	7.1	ns
Outputs							
t_{ob}	37	Output Buffer Delay	—	0.9	—	1.3	ns
t_{obs}	38	Output Buffer Delay, Slow Slew	—	5.9	—	8.3	ns
t_{oen}	39	I/O Cell OE to Output Enabled	—	0.8	—	1.1	ns
t_{oedis}	40	I/O Cell OE to Output Disabled	—	0.8	—	1.1	ns
t_{goe}	41	Global Output Enable Delay	—	2.5	—	3.6	ns
t_{toe}	42	Test OE Enable Delay	—	8.2	—	10.9	ns
Clocks							
t_{cio}	43	I/O Clock Delay	—	0.7	—	1.0	ns
$t_{gy0/1/2/3}$	44	Clock Delay, Y0/1/2/3	—	2.4	—	2.8	ns
Global Reset							
t_{gr}	45	Global Reset to I/O Register/Latch	—	12.3	—	15.0	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to the Timing Model in this data sheet for further details.

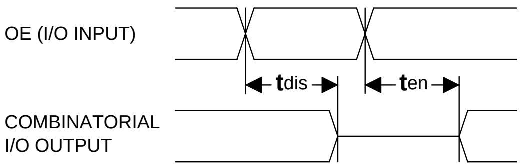
Switching Waveforms



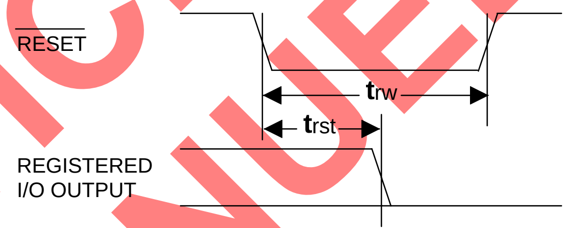
Combinatorial Output



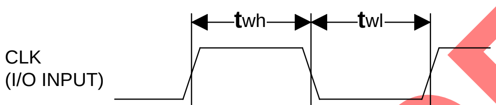
Registered Output



I/O Output Enable/Disable

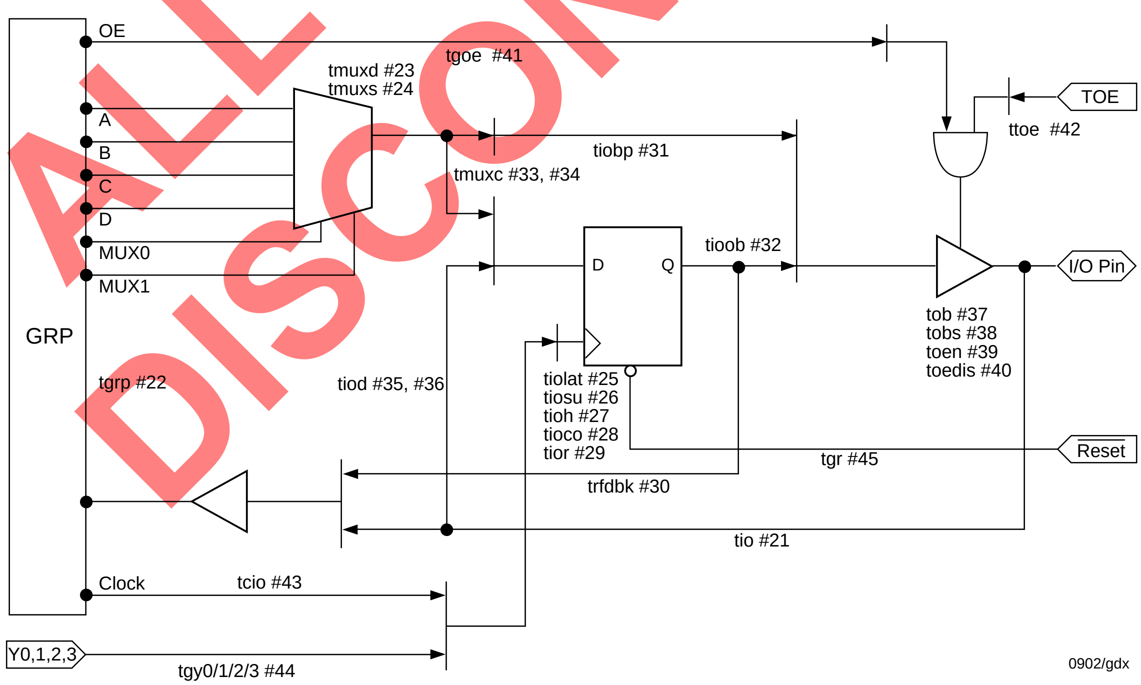


Reset



Clock Width

ispGDX Timing Model



ispLEVER Development System

The ispLEVER Development System supports ispGDX design using a VHDL or Verilog language syntax. From creation to in-system programming, the ispLEVER system is an easy-to-use, self-contained design tool.

Features

- VHDL and Verilog Synthesis Support Available
- ispGDX Design Compiler
  - Design Rule Checker
  - I/O Connectivity Checker
  - Automatic Compiler Function
- Industry Standard JEDEC File for Programming
- Min/Max Timing Report
- Interfaces To Popular Timing Simulators
- User Electronic Signature (UES) Support
- Detailed Log and Report Files For Easy Design Debug
- On-line Help
- Windows® XP, Windows 2000, Windows 98 and Windows NT® Compatible
- Solaris® and HP-UX Versions Available

In-System Programmability

All necessary programming of the ispGDXV/VA is done via four TTL level logic interface signals. These four signals are fed into the on-chip programming circuitry where a state machine controls the programming.

On-chip programming can be accomplished using an IEEE 1149.1 boundary scan protocol. The IEEE 1149.1-compliant interface signals are Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS) control. The EPEN pin is also used to enable or disable the JTAG port.

The embedded controller port enable pin (EPEN) is used to enable the JTAG tap controller and in that regard has similar functionality to a TRST pin. When the pin is driven high, the JTAG TAP controller is enabled. This is also true when the pin is left unconnected, in which case the pin is pulled high by the permanent internal pullup. This allows ISP programming and BSCAN testing to take place as specified by the Instruction Table.

When the pin is driven low, the JTAG TAP controller is driven to a reset state asynchronously. It stays there while the pin is held low. After pulling the pin high the JTAG controller becomes active. The intent of this feature is to allow the JTAG interface to be directly controlled by the data bus of an embedded controller (hence the name Embedded Port Enable). The EPEN signal is used as a “device select” to prevent spurious programming and/or testing from occurring due to random bit patterns on the data bus. Figure 9 illustrates the block diagram for the ispJTAG™ interface.

Figure 5. ISP Device Programming Interface

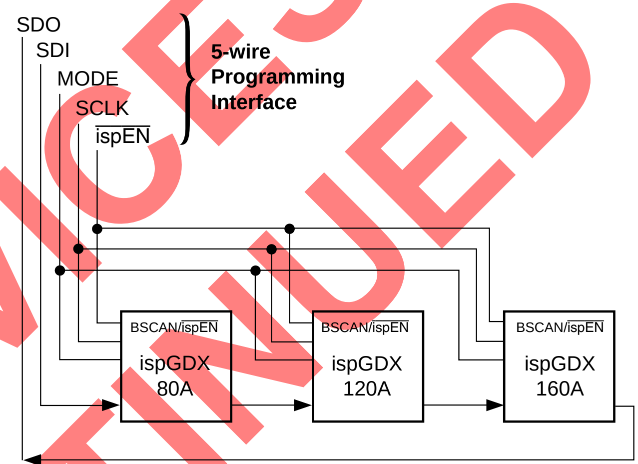


Figure 6. ispJTAG Device Programming Interface

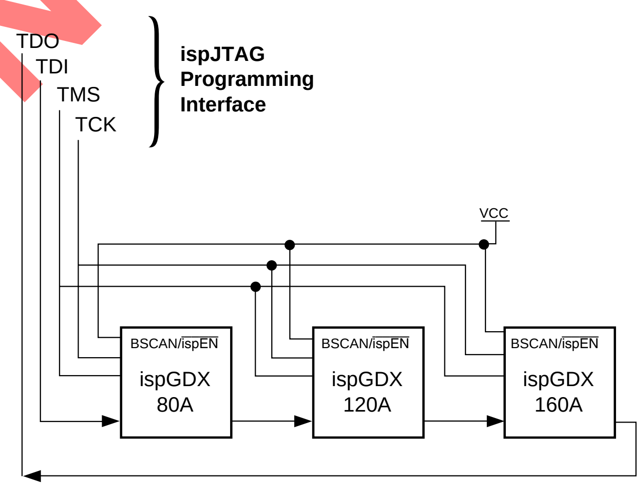


Table 3. I/O Shift Register Order

DEVICE	I/O SHIFT REGISTER ORDER
ispGDX80A	SDI/TDI, I/O B10 .. B19, I/O C0 .. C19, I/O D0 .. D9, $\overline{\text{RESET}}$, Y1/TOE, Y0, I/O B9 .. B0, I/O A19.. A0, I/O D19 .. D10, SDO/TDO
ispGDX120A	SDI/TDI, I/O B15 .. B29, I/O C0 .. C29, I/O D0 .. D14, TOE, Y2, Y3, $\overline{\text{RESET}}$, Y1, Y0, I/O B14 .. B0, I/O A29.. A0, I/O D29 .. D15, SDO/TDO
ispGDX160/A	SDI/TDI, I/O B20 .. B39, I/O C0 .. C39, I/O D0 .. D19, TOE, Y2, Y3, $\overline{\text{RESET}}$, Y1, Y0, I/O B19 .. B0, I/O A39.. A0, I/O D39 .. D20, SDO/TDO

I/O Shift Reg Order/ispGDX

Table 4. ispGDX Device ID Codes

DEVICE	8-BIT ISP ID	32-BIT BOUNDARY SCAN IDCODE
ispGDX80A	0111 0111	0000 0000 0010 0101 0001 0000 0100 0011
ispGDX120A	0111 1000	0000 0000 0010 0101 0010 0000 0100 0011
ispGDX160/A	0111 1001	0000 0000 0010 0101 0011 0000 0100 0011

GDX ID Codes

Boundary Scan

The ispGDXV/VA devices provide IEEE1149.1a test capability and ISP programming through a standard Boundary Scan Test Access Port (TAP) interface.

The boundary scan circuitry on the ispGDXV/VA Family operates independently of the programmed pattern. This allows customers using boundary scan test to have full test capability with only a single BSDL file.

The ispGDXV/VA devices are identified by the 32-bit JTAG IDCODE register. The device ID assignments are listed in Table 4.

The ispJTAG programming is accomplished by executing Lattice private instructions under the Boundary Scan State Machine.

Contact Lattice Technical Support to obtain more detailed programming information.

Figure 7. Boundary Scan I/O Register Cell

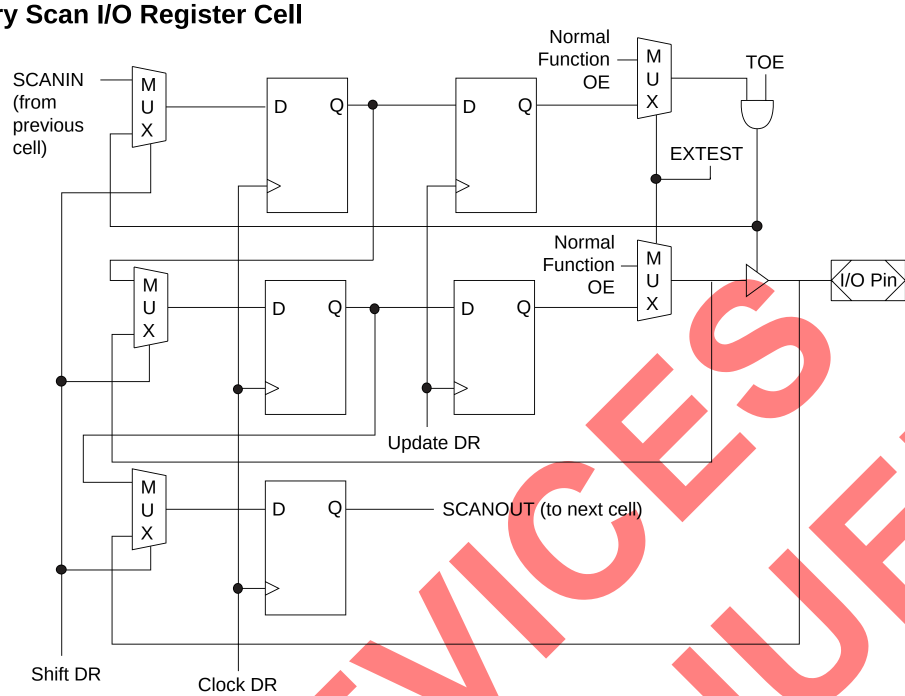
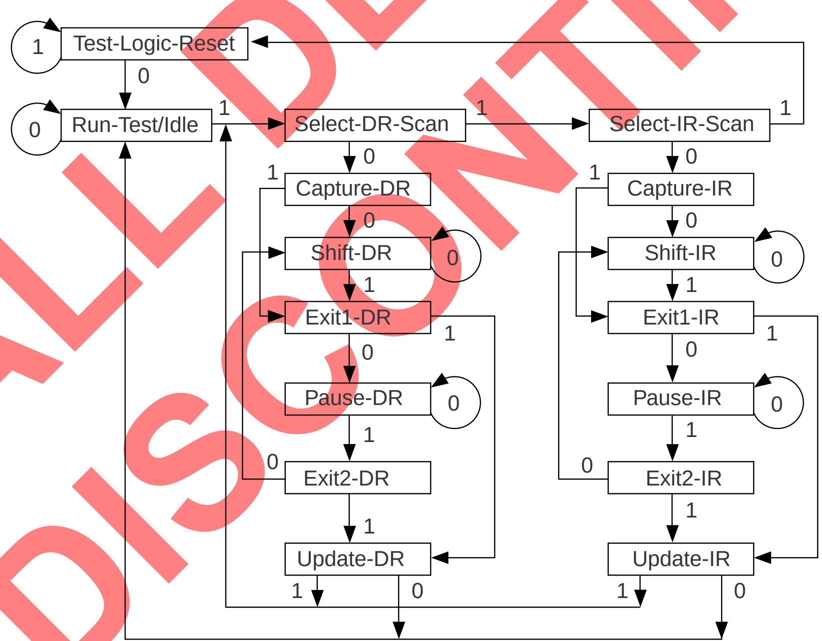
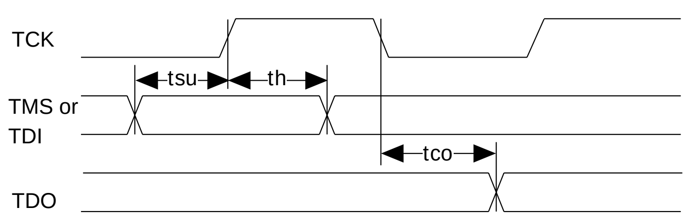


Figure 8. Boundary Scan State Machine





t_{su} = 0.1µs (min.) th = 0.1µs (min.) tco = 0.1µs (min.)

Signal Descriptions

Signal Name	Description
I/O	Input/Output Pins – These are the general purpose bidirectional data pins. When used as outputs, each may be independently latched, registered or tristated. They can also each assume one other control function (OE, CLK and MUXsel as described in the text).
TOE	Test Output Enable pin – This pin tristates all I/O pins when a logic low is driven.
$\overline{\text{RESET}}$	Active LOW Input Pin – Resets all I/O register outputs when LOW.
Y0, Y1, Y2, Y3	Input Pins – Dedicated clock input pins. Each pin can drive any or all I/O cell registers.
BSCAN/$\overline{\text{ispEN}}$	Input Pin – When HIGH, this pin enables the Boundary Scan Test and Programming Interface. When LOW, this pin enables the Lattice ISP protocol for programming and tristates all I/O pins, except those used for the programming interface.
TDI/SDI	Input/Input Pin – Serial data input during ISP programming or Boundary Scan mode.
TCK/SCLK	Input/Input Pin – Serial data clock during ISP programming or Boundary Scan mode.
TMS/MODE	Input/Input Pin – Control input during ISP programming or Boundary Scan mode.
TDO/SDO	Output/Output Pin – Serial data output during ISP programming or Boundary Scan mode.
GND	Ground (GND)
VCC	Vcc – Supply voltage (5V).
NC[1]	No Connect.

1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Locations: ispGDX160A

Signal	208-Pin PQFP	272-Ball BGA
TOE	178	A12
$\overline{\text{RESET}}$	185	D10
Y0, Y1, Y2, Y3,	75, 76, 180, 181	V10, Y10, C11, A11
BSCAN/$\overline{\text{ispEN}}$	183	B10
TDI/SDI	81	Y12
TCK/SCLK	80	U11
TMS/MODE	79	V11
TDO/SDO	78	W11
GND	6, 15, 25, 35, 44, 54, 63, 77, 91, 100, 110, 119, 129, 139, 148, 159, 168, 182, 195, 204	A1, D4, D8, D13, D17, H4, H17, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, U4, U8, U13, U17
VCC	1, 17, 33, 49, 65, 89, 105, 121, 137, 153, 170, 184 193	D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15
NC[1]	73, 74, 156, 179	A2, A6, A7, A10, A15, A19, A20, B1, B2, B4, B11, B14, B18, B19, B20, C2, C3, C10, C18, D2, D3, D16, E2, E17, E19, H1, H3, H18, H20, K20, L1, N1, N3, N18, N20, T2, T4, T19, U5, U18, U19, V3, V14, V18, V19, W1, W2, W3, W7, W10, W14, W19, W20, Y1, Y2, Y6, Y9, Y11, Y18, Y20

1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Locations: ispGDX160A

Signal	208 PQFP	272 BGA	Signal	208 PQFP	272 BGA	Signal	208 PQFP	272 BGA	Signal	208 PQFP	272 BGA	Signal	208 PQFP	272 BGA
I/O A0	2	E4	I/O A32	40	R2	I/O B24	86	W13	I/O C16	125	M20	I/O D8	164	A16
I/O A1	3	C1	I/O A33	41	T1	I/O B25	87	V13	I/O C17	126	L19	I/O D9	165	C15
I/O A2	4	D1	I/O A34	42	P4	I/O B26	88	Y14	I/O C18	127	L18	I/O D10	166	D14
I/O A3	5	E3	I/O A35	43	R3	I/O B27	90	Y15	I/O C19	128	L20	I/O D11	167	B15
I/O A4	7	E1	I/O A36	45	U1	I/O B28	92	W15	I/O C20	130	K19	I/O D12	169	C14
I/O A5	8	F3	I/O A37	46	T3	I/O B29	93	Y16	I/O C21	131	K18	I/O D13	171	A14
I/O A6	9	G4	I/O A38	47	U2	I/O B30	94	U14	I/O C22	132	K17	I/O D14	172	C13
I/O A7	10	F2	I/O A39	48	V1	I/O B31	95	V15	I/O C23	133	J20	I/O D15	173	B13
I/O A8	11	F1	I/O B0	50	U3	I/O B32	96	W16	I/O C24	134	J19	I/O D16	174	A13
I/O A9	12	G3	I/O B1	51	V2	I/O B33	97	Y17	I/O C25	135	J18	I/O D17	175	D12
I/O A10	13	G2	I/O B2	52	W4	I/O B34	98	V16	I/O C26	136	J17	I/O D18	176	C12
I/O A11	14	G1	I/O B3	53	V4	I/O B35	99	W17	I/O C27	138	H19	I/O D19	177	B12
I/O A12	16	H2	I/O B4	55	Y3	I/O B36	101	U16	I/O C28	140	G20	I/O D20	186	A9
I/O A13	18	J4	I/O B5	56	Y4	I/O B37	102	V17	I/O C29	141	G19	I/O D21	187	B9
I/O A14	19	J3	I/O B6	57	V5	I/O B38	103	W18	I/O C30	142	F20	I/O D22	188	C9
I/O A15	20	J2	I/O B7	58	W5	I/O B39	104	Y19	I/O C31	143	G18	I/O D23	189	D9
I/O A16	21	J1	I/O B8	59	Y5	I/O C0	106	T17	I/O C32	144	F19	I/O D24	190	A8
I/O A17	22	K2	I/O B9	60	V6	I/O C1	107	V20	I/O C33	145	E20	I/O D25	191	B8
I/O A18	23	K3	I/O B10	61	U7	I/O C2	108	U20	I/O C34	146	G17	I/O D26	192	C8
I/O A19	24	K1	I/O B11	62	W6	I/O C3	109	T18	I/O C35	147	F18	I/O D27	194	B7
I/O A20	26	L2	I/O B12	64	V7	I/O C4	111	T20	I/O C36	149	D20	I/O D28	196	C7
I/O A21	27	L3	I/O B13	66	Y7	I/O C5	112	R18	I/O C37	150	E18	I/O D29	197	B6
I/O A22	28	L4	I/O B14	67	V8	I/O C6	113	P17	I/O C38	151	D19	I/O D30	198	A5
I/O A23	29	M1	I/O B15	68	W8	I/O C7	114	R19	I/O C39	152	C20	I/O D31	199	D7
I/O A24	30	M2	I/O B16	69	Y8	I/O C8	115	R20	I/O D0	154	D18	I/O D32	200	C6
I/O A25	31	M3	I/O B17	70	U9	I/O C9	116	P18	I/O D1	155	C19	I/O D33	201	B5
I/O A26	32	M4	I/O B18	71	V9	I/O C10	117	P19	I/O D2	157	B17	I/O D34	202	A4
I/O A27	34	N2	I/O B19	72	W9	I/O C11	118	P20	I/O D3	158	C17	I/O D35	203	C5
I/O A28	36	P1	I/O B20	82	W12	I/O C12	120	N19	I/O D4	160	A18	I/O D36	205	A3
I/O A29	37	P2	I/O B21	83	V12	I/O C13	122	M17	I/O D5	161	A17	I/O D37	206	D5
I/O A30	38	R1	I/O B22	84	U12	I/O C14	123	M18	I/O D6	162	C16	I/O D38	207	C4
I/O A31	39	P3	I/O B23	85	Y13	I/O C15	124	M19	I/O D7	163	B16	I/O D39	208	B3

Signal Configuration: ispGDX160A

ispGDX160A 272-Ball BGA Signal Diagram

ispGDX160A

Bottom View

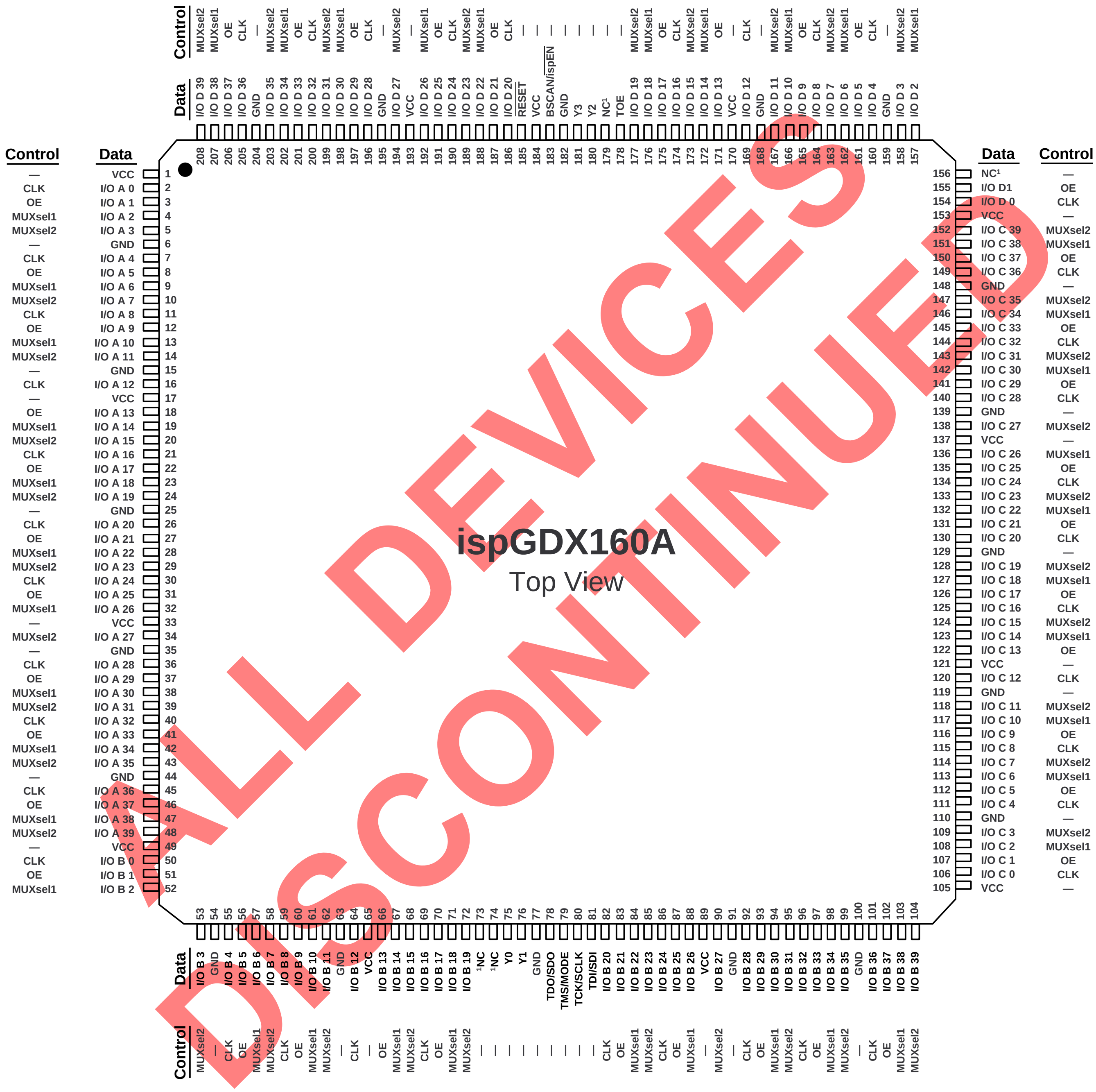
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	NC[1]	NC[1]	I/O D4	I/O D5	I/O D8	NC[1]	I/O D13	I/O D16	TOE	Y3	NC[1]	I/O D20	I/O D24	NC[1]	NC[1]	I/O D30	I/O D34	I/O D36	NC[1]	GND	A
B	NC[1]	NC[1]	NC[1]	I/O D2	I/O D7	I/O D11	NC[1]	I/O D15	I/O D19	NC[1]	BSCAN/ ispEN	I/O D21	I/O D25	I/O D27	I/O D29	I/O D33	NC[1]	I/O D39	NC[1]	NC[1]	B
C	I/O C39	I/O D1	NC[1]	I/O D3	I/O D6	I/O D9	I/O D12	I/O D14	I/O D18	Y2	NC[1]	I/O D22	I/O D26	I/O D28	I/O D32	I/O D35	I/O D38	NC[1]	NC[1]	I/O A1	C
D	I/O C36	I/O C38	I/O D0	GND	NC[1]	VCC	I/O D10	GND	I/O D17	VCC	$\overline{\text{RESET}}$	I/O D23	GND	I/O D31	VCC	I/O D37	GND	NC[1]	NC[1]	I/O A2	D
E	I/O C33	NC[1]	I/O C37	NC[1]													I/O A0	I/O A3	NC[1]	I/O A4	E
F	I/O C30	I/O C32	I/O C35	VCC													VCC	I/O A5	I/O A7	I/O A8	F
G	I/O C28	I/O C29	I/O C31	I/O C34													I/O A6	I/O A9	I/O A10	I/O A11	G
H	NC[1]	I/O C27	NC[1]	GND													GND	NC[1]	I/O A12	NC[1]	H
J	I/O C23	I/O C24	I/O C25	I/O C26					GND	GND	GND	GND					I/O A13	I/O A14	I/O A15	I/O A16	J
K	NC[1]	I/O C20	I/O C21	I/O C22					GND	GND	GND	GND					VCC	I/O A18	I/O A17	I/O A19	K
L	I/O C19	I/O C17	I/O C18	VCC					GND	GND	GND	GND					I/O A22	I/O A21	I/O A20	NC[1]	L
M	I/O C16	I/O C15	I/O C14	I/O C13					GND	GND	GND	GND					I/O A26	I/O A25	I/O A24	I/O A23	M
N	NC[1]	I/O C12	NC[1]	GND													GND	NC[1]	I/O A27	NC[1]	N
P	I/O C11	I/O C10	I/O C9	I/O C6													I/O A34	I/O A31	I/O A29	I/O A28	P
R	I/O C8	I/O C7	I/O C5	VCC													VCC	I/O A35	I/O A32	I/O A30	R
T	I/O C4	NC[1]	I/O C3	I/O C0													NC[1]	I/O A37	NC[1]	I/O A33	T
U	I/O C2	NC[1]	NC[1]	GND	I/O B36	VCC	I/O B30	GND	I/O B22	TCK/ SCLK	VCC	I/O B17	GND	I/O B10	VCC	NC[1]	GND	I/O B0	I/O A38	I/O A36	U
V	I/O C1	NC[1]	NC[1]	I/O B37	I/O B34	I/O B31	NC[1]	I/O B25	I/O B21	TMS/ MODE	Y0	I/O B18	I/O B14	I/O B12	I/O B9	I/O B6	I/O B3	NC[1]	I/O B1	I/O A39	V
W	NC[1]	NC[1]	I/O B38	I/O B35	I/O B32	I/O B28	NC[1]	I/O B24	I/O B20	TDO/ SDO	NC[1]	I/O B19	I/O B15	NC[1]	I/O B11	I/O B7	I/O B2	NC[1]	NC[1]	NC[1]	W
Y	NC[1]	I/O B39	NC[1]	I/O B33	I/O B29	I/O B27	I/O B26	I/O B23	TDI/ SDI	NC[1]	Y1	NC[1]	I/O B16	I/O B13	NC[1]	I/O B8	I/O B5	I/O B4	NC[1]	NC[1]	Y
	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Pin Configuration: ispGDX160A

ispGDX160A 208-Pin PQFP (with Heat Spreader) Pinout Diagram



1. No Connect Pins (NC) are not to be connected to any active signal, Vcc or GND.

Signal Locations: ispGDX120A

Signal	176-Pin TQFP	160-Pin PQFP
TOE	150	136
$\overline{\text{RESET}}$	156	142
Y0, Y1, Y2, Y3,	63, 64, 152, 153	57, 58, 138, 139
BSCAN/$\overline{\text{ispEN}}$	154	140
TDI/SDI	69	63
TCK/SCLK	68	62
TMS/MODE	67	61
TDO/SDO	66	60
GND	8, 17, 27, 37, 50, 65, 77, 91, 101, 110, 120, 129, 144, 161, 170	6, 15, 25, 35, 44, 59, 71, 81, 91, 100, 110, 119, 130, 147, 156
VCC	3, 19, 35, 55, 79, 99, 115, 136, 155, 159	1, 17, 33, 49, 73, 89, 105, 122, 141, 145
NC[1]	1, 2, 43, 44, 45, 46, 61, 62, 87, 88, 89, 90, 130, 131, 132, 133, 134, 151, 175, 176	55, 56, 120, 137

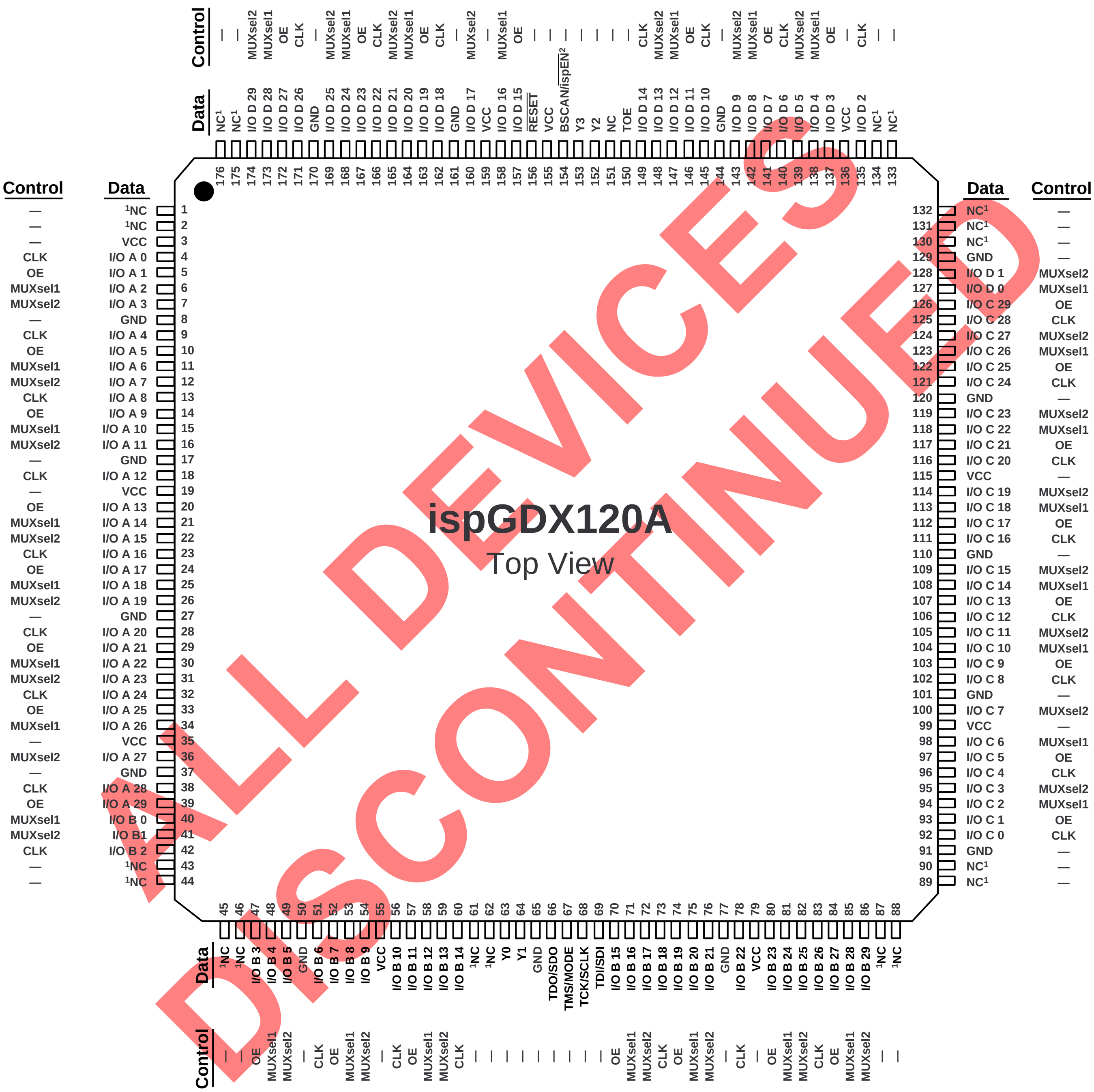
1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Locations: ispGDX120A

Signal	176 TQFP	160 PQFP	Signal	176 TQFP	160 PQFP	Signal	176 TQFP	160 PQFP	Signal	176 TQFP	160 PQFP	Signal	176 TQFP	160 PQFP
I/O A0	4	2	I/O A24	32	30	I/O B18	73	67	I/O C12	106	96	I/O D6	140	126
I/O A1	5	3	I/O A25	33	31	I/O B19	74	68	I/O C13	107	97	I/O D7	141	127
I/O A2	6	4	I/O A26	34	32	I/O B20	75	69	I/O C14	108	98	I/O D8	142	128
I/O A3	7	5	I/O A27	36	34	I/O B21	76	70	I/O C15	109	99	I/O D9	143	129
I/O A4	9	7	I/O A28	38	36	I/O B22	78	72	I/O C16	111	101	I/O D10	145	131
I/O A5	10	8	I/O A29	39	37	I/O B23	80	74	I/O C17	112	102	I/O D11	146	132
I/O A6	11	9	I/O B0	40	38	I/O B24	81	75	I/O C18	113	103	I/O D12	147	133
I/O A7	12	10	I/O B1	41	39	I/O B25	82	76	I/O C19	114	104	I/O D13	148	134
I/O A8	13	11	I/O B2	42	40	I/O B26	83	77	I/O C20	116	106	I/O D14	149	135
I/O A9	14	12	I/O B3	47	41	I/O B27	84	78	I/O C21	117	107	I/O D15	157	143
I/O A10	15	13	I/O B4	48	42	I/O B28	85	79	I/O C22	118	108	I/O D16	158	144
I/O A11	16	14	I/O B5	49	43	I/O B29	86	80	I/O C23	119	109	I/O D17	160	146
I/O A12	18	16	I/O B6	51	45	I/O C0	92	82	I/O C24	121	111	I/O D18	162	148
I/O A13	20	18	I/O B7	52	46	I/O C1	93	83	I/O C25	122	112	I/O D19	163	149
I/O A14	21	19	I/O B8	53	47	I/O C2	94	84	I/O C26	123	113	I/O D20	164	150
I/O A15	22	20	I/O B9	54	48	I/O C3	95	85	I/O C27	124	114	I/O D21	165	151
I/O A16	23	21	I/O B10	56	50	I/O C4	96	86	I/O C28	125	115	I/O D22	166	152
I/O A17	24	22	I/O B11	57	51	I/O C5	97	87	I/O C29	126	116	I/O D23	167	153
I/O A18	25	23	I/O B12	58	52	I/O C6	98	88	I/O D0	127	117	I/O D24	168	154
I/O A19	26	24	I/O B13	59	53	I/O C7	100	90	I/O D1	128	118	I/O D25	169	155
I/O A20	28	26	I/O B14	60	54	I/O C8	102	92	I/O D2	135	121	I/O D26	171	157
I/O A21	29	27	I/O B15	70	64	I/O C9	103	93	I/O D3	137	123	I/O D27	172	158
I/O A22	30	28	I/O B16	71	65	I/O C10	104	94	I/O D4	138	124	I/O D28	173	159
I/O A23	31	29	I/O B17	72	66	I/O C11	105	95	I/O D5	139	125	I/O D29	174	160

Pin Configuration: ispGDX120A

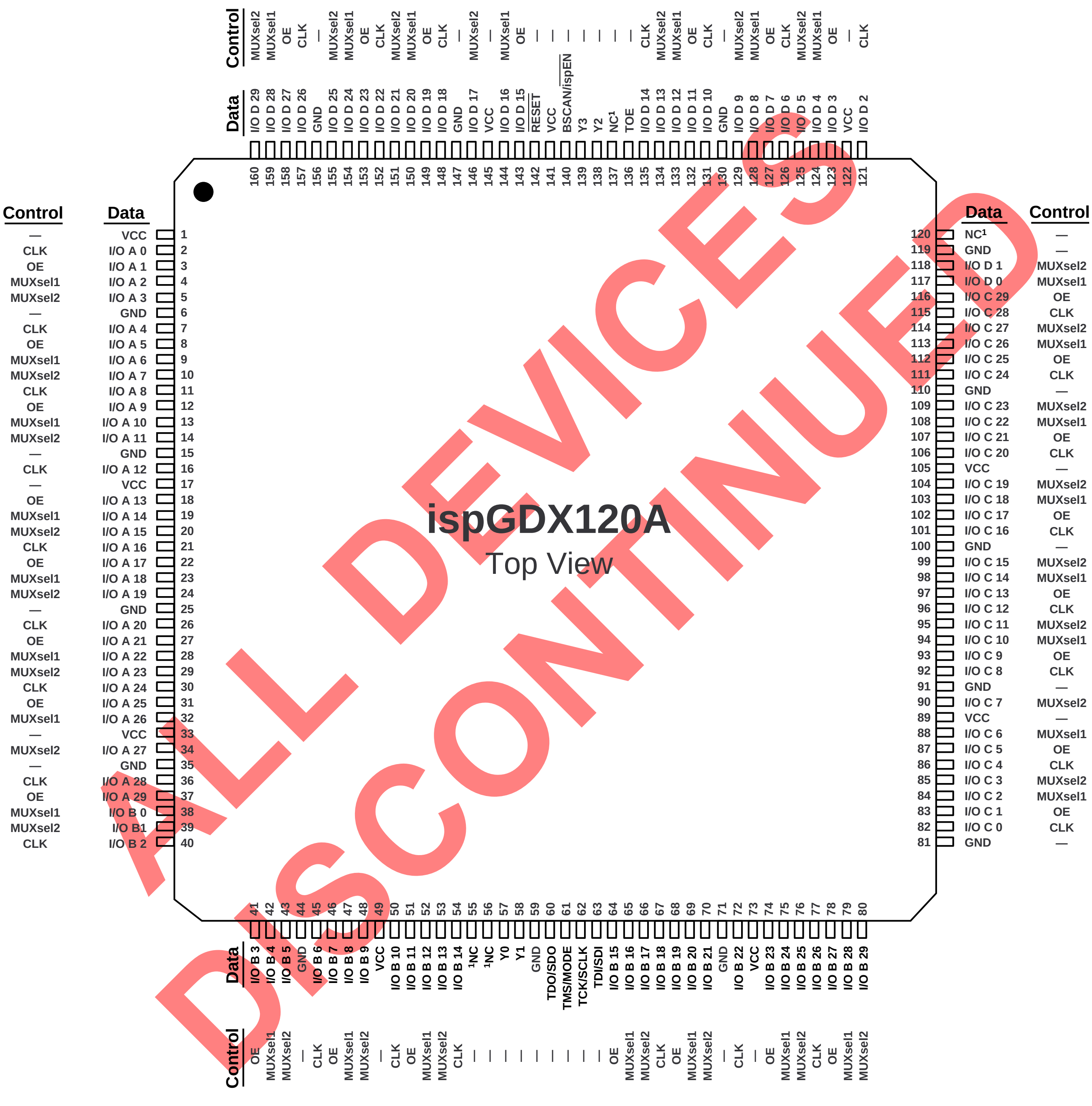
ispGDX120A 176-Pin TQFP Pinout Diagram



1. NC pins are not to be connected to any active signals, VCC or GND.

Pin Configuration: ispGDX120A

ispGDX120A 160-Pin PQFP Pinout Diagram



1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Locations: ispGDX80A

Signal	100-Pin TQFP
Y1/TOE	87
Y0	38
$\overline{\text{RESET}}$	89
BSCAN/$\overline{\text{ispEN}}$	35
TDI/SDI	39
TCK/SCLK	36
TMS/MODE	86
TDO/SDO	85
GND	6, 18, 29, 45, 56, 68, 79, 95
VCC	12, 37, 62, 88

I/O Locations: ispGDX80A

Signal	100 TQFP	Signal	100 TQFP	Signal	100 TQFP	Signal	100 TQFP
I/O A0	1	I/O B0	24	I/O C0	51	I/O D0	74
I/O A1	2	I/O B1	25	I/O C1	52	I/O D1	75
I/O A2	3	I/O B2	26	I/O C2	53	I/O D2	76
I/O A3	4	I/O B3	27	I/O C3	54	I/O D3	77
I/O A4	5	I/O B4	28	I/O C4	55	I/O D4	78
I/O A5	7	I/O B5	30	I/O C5	57	I/O D5	80
I/O A6	8	I/O B6	31	I/O C6	58	I/O D6	81
I/O A7	9	I/O B7	32	I/O C7	59	I/O D7	82
I/O A8	10	I/O B8	33	I/O C8	60	I/O D8	83
I/O A9	11	I/O B9	34	I/O C9	61	I/O D9	84
I/O A10	13	I/O B10	40	I/O C10	63	I/O D10	90
I/O A11	14	I/O B11	41	I/O C11	64	I/O D11	91
I/O A12	15	I/O B12	42	I/O C12	65	I/O D12	92
I/O A13	16	I/O B13	43	I/O C13	66	I/O D13	93
I/O A14	17	I/O B14	44	I/O C14	67	I/O D14	94
I/O A15	19	I/O B15	46	I/O C15	69	I/O D15	96
I/O A16	20	I/O B16	47	I/O C16	70	I/O D16	97
I/O A17	21	I/O B17	48	I/O C17	71	I/O D17	98
I/O A18	22	I/O B18	49	I/O C18	72	I/O D18	99
I/O A19	23	I/O B19	50	I/O C19	73	I/O D19	100

Pin Configuration: ispGDX80A

ispGDX80A 100-Pin TQFP Pinout Diagram

ispGDX80A
Top View

	Data	Control
1	I/O A0	CLK
2	I/O A1	OE
3	I/O A2	MUXsel1
4	I/O A3	MUXsel2
5	I/O A4	CLK
6	GND	—
7	I/O A5	OE
8	I/O A6	MUXsel1
9	I/O A7	MUXsel2
10	I/O A8	CLK
11	I/O A9	OE
12	VCC	—
13	I/O A10	MUXsel1
14	I/O A11	MUXsel2
15	I/O A12	CLK
16	I/O A13	OE
17	I/O A14	MUXsel1
18	GND	—
19	I/O A15	MUXsel2
20	I/O A16	CLK
21	I/O A17	OE
22	I/O A18	MUXsel1
23	I/O A19	MUXsel2
24	I/O B0	CLK
25	I/O B1	OE
26	I/O B2	MUXsel1
27	I/O B3	MUXsel2
28	I/O B4	CLK
29	GND	—
30	I/O B5	OE
31	I/O B6	MUXsel1
32	I/O B7	MUXsel2
33	I/O B8	CLK
34	I/O B9	OE
35	BSCAN/$\overline{ispEN}$	—
36	[1]TCK/SCLK	—
37	VCC	—
38	Y0	—
39	[1]TDI/SDI	—
40	I/O B10	MUXsel1
41	I/O B11	MUXsel2
42	I/O B12	CLK
43	I/O B13	OE
44	I/O B14	MUXsel1
45	GND	—
46	I/O B15	MUXsel2
47	I/O B16	CLK
48	I/O B17	OE
49	I/O B18	MUXsel1
50	I/O B19	MUXsel2
51	I/O C0	CLK
52	I/O C1	OE
53	I/O C2	MUXsel1
54	I/O C3	MUXsel2
55	I/O C4	CLK
56	GND	—
57	I/O C5	OE
58	I/O C6	MUXsel1
59	I/O C7	MUXsel2
60	I/O C8	CLK
61	I/O C9	OE
62	VCC	—
63	I/O C10	MUXsel1
64	I/O C11	MUXsel2
65	I/O C12	CLK
66	I/O C13	OE
67	I/O C14	MUXsel1
68	GND	—
69	I/O C15	MUXsel2
70	I/O C16	CLK
71	I/O C17	OE
72	I/O C18	MUXsel1
73	I/O C19	MUXsel2
74	I/O D0	CLK
75	I/O D1	OE
76	I/O D2	MUXsel1
77	I/O D3	MUXsel2
78	I/O D4	CLK
79	GND	—
80	I/O D5	OE
81	I/O D6	MUXsel1
82	I/O D7	MUXsel2
83	I/O D8	CLK
84	I/O D9	OE
85	TDO/SDO[1]	—
86	TMS/MODE[1]	—
87	Y1/TOE[1]	—
88	VCC	—
89	$\overline{RESET}$	—
90	I/O D10	MUXsel1
91	I/O D11	MUXsel2
92	I/O D12	CLK
93	I/O D13	OE
94	I/O D14	MUXsel1
95	GND	—
96	I/O D15	MUXsel2
97	I/O D16	CLK
98	I/O D17	OE
99	I/O D18	MUXsel1
100	I/O D19	MUXsel2

1. Pins have dual function capability.

Part Number Description

ispGDX XXXX – X XXXX X

Device Family — ispGDX

Device Number — XXXX
160A
120A
80A

Speed — X
5 = 5ns Tpd
7 = 7ns Tpd

Package — XXXX
Q208 = PQFP (with Heat Spreader)
T176 = TQFP
Q160 = PQFP
B272 = BGA
T100 = TQFP

Grade — X
Blank = Commercial

0212/ispGDX

Ordering Information

COMMERCIAL

I/O PINS	tpd (ns)	ORDERING NUMBER	PACKAGE
160A	5	ispGDX160A-5Q208	208-Pin PQFP
	5	ispGDX160A-5B272	272-Ball BGA
	7	ispGDX160A-7Q208	208-Pin PQFP
	7	ispGDX160A-7B272	272-Ball BGA
120	5	ispGDX120A-5T176	176-Pin TQFP
	5	ispGDX120A-5Q160	160-Pin PQFP
	7	ispGDX120A-7T176	176-Pin TQFP
	7	ispGDX120A-7Q160	160-Pin PQFP
80	5	ispGDX80A-5T100	100-Pin TQFP
	7	ispGDX80A-7T100	100-Pin TQFP

Table 2-0041/ispGDX