LH6P81

PRELIMINARY

CMOS 8M (512K × 16) SF-ASIC RAM

FEATURES

- 524,288 x 16 bit organization
- Power Supply: +3.3 V ±0.3 V
- Available for static column mode using A_1 - A_7, $\overline{UB}$ and $\overline{LB}$ pins
- Access time:
  Normal mode: 100 ns
  Page mode (static column mode): 55 ns
- Cycle time: 200 ns
- Power consumption:
  Operating: 130 mW (MAX.)
  Standby: 110 µW (MAX.)
  Self refresh: 1.1 mW (MAX.)
- LVTTL compatible I/O
- Available for address refresh, auto-refresh, and self-refresh modes
- 4,096 refresh cycles within 64 ms
- Available for byte access mode using $\overline{UB}$ and $\overline{LB}$ pins
- Package: 48-pin TSOP (Type I)

DESCRIPTION

The LH6P81 is a CMOS 8M bit SF-ASIC RAM memory organized as 524,288 x 16 bits. On the SF-ASIC RAM chip, RAM and ROM can be freely mapped into the memory space. Thus, SF-ASIC RAM is very suitable for storing application software such as ROM-executable DOS or other.

The architecture of the RAM space is equivalent to a Pseudo SRAM. The memory cell is the same as a DRAM cell (1T1C). Therefore, refreshing is necessary to retain RAM data. The architecture of the ROM space is equivalent to a Mask ROM, and the ROM data is programmed by the factory. Even if a CPU writes data into a ROM address, the ROM data never changes.

The access to ROM and RAM is executed with common control pins ($\overline{CE}$,$\overline{OE}$,$\overline{WE}$), common address pins, and common I/O pins, using the same timing scheme. The read operations are identical for both ROM and RAM. Access time is the same in both the ROM and the RAM address space.

The read/write timing scheme is the same as a Pseudo SRAM. Also, the refresh function and the data retention function are the same as those of a Pseudo SRAM.

The LH6P81 has a continuous 1M byte of memory space consisting of sixteen blocks (Figure 1). Each block contains 64K bytes or 256 pages of memory. A page contains 256 bytes, and each page can be used as either ROM or RAM. Users can map RAM and ROM randomly into the 1M byte memory space in minimum units of 256 bytes or one page. Page Mode (i.e., Static column mode) is available inside the page of 256 bytes or 128 words.

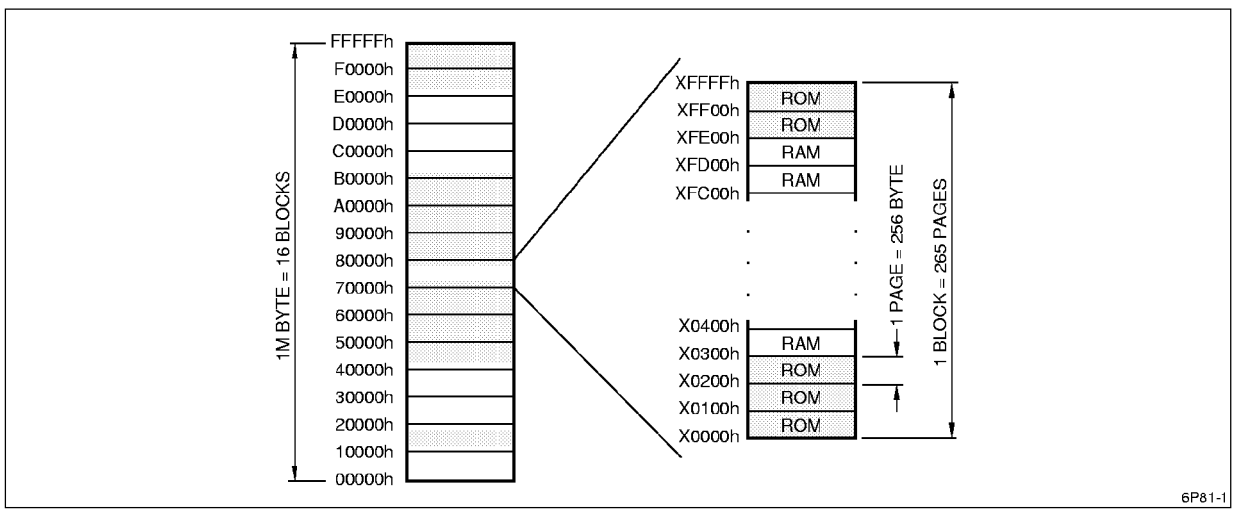


Figure 1. 1M Byte of Continuous Memory Space

PIN DESCRIPTIONS

SIGNAL	PIN NAME
A_1 - A_{19}	Address input
$\overline{UB}$, $\overline{LB}$	Upper/Lower byte select input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
$\overline{RFSH}$	Refresh input
$\overline{CE}$	Chip enable input
CS	Chip select input
I/O_0 - I/O_{15}	Data input/output
Reset	Reset input
V_{CC}	Power supply
GND	Ground

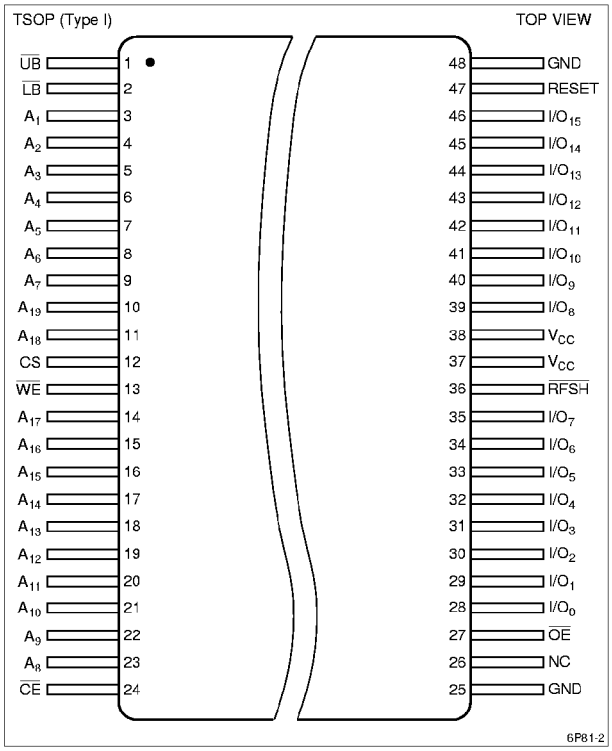


Figure 2. Pin Connections for TSOP Package

TRUTH TABLE

$\overline{CE}$	CS	$\overline{RFSH}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	MODE		I/O_0 - I/O_7	I/O_8 - I/O_{15}
L	H	H	H	L	H	L	Read	Lower byte access	Output data	High-Z
					L	H		Upper byte access	High-Z	Output data
					L	L		Word access	Output data	Output data
					H	H		Invalid	High-Z	High-Z
L	H	H	L	X	H	L	Write	Lower byte access	Input data	High-Z
					L	H		Upper byte access	High-Z	Input data
					L	L		Word access	Input data	Input data
					H	H		Invalid	High-Z	High-Z
H	X	L	X	X	X	X	Auto Refresh		High-Z	High-Z
L	L	H	X	X	X	X	CS Standby		High-Z	High-Z
H	X	H	X	X	X	X	Standby		High-Z	High-Z

NOTES:
H = High, L = Low, X = Don't care

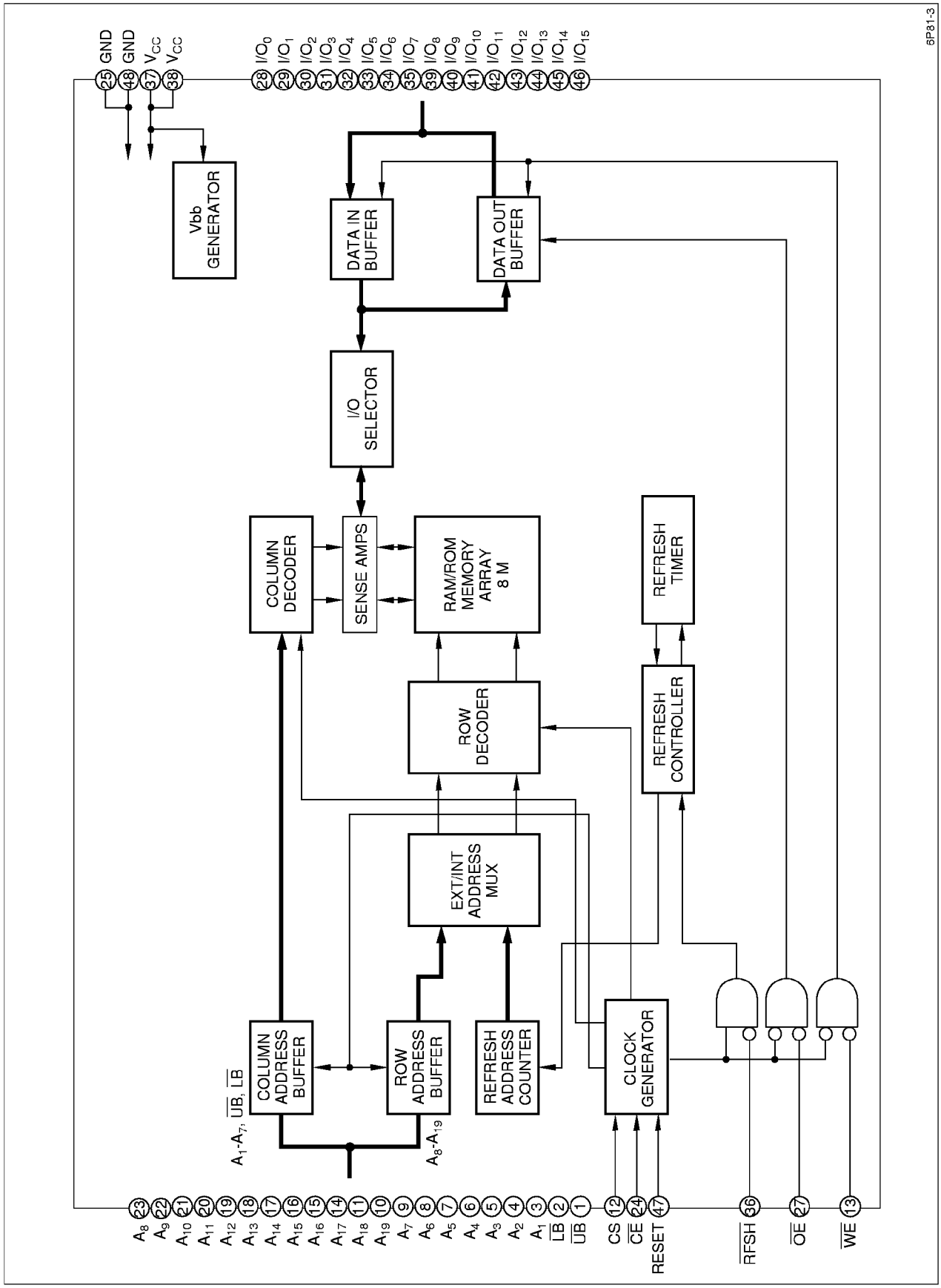


Figure 3. LH6P81 Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_T	-0.5 to +4.6	V	1
Output short circuit current	I_O	50	mA	
Power dissipation	P_D	600	mW	
Operating temperature	T_{OPR}	0 to +70	°C	
Storage temperature	T_{STG}	-65 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.0		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1M, V_{CC} = 3.3 V ±0.3 V)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_1 - A_{19}, $\overline{UB}$ /$\overline{LB}$	C_{IN1}		8	pF
	$\overline{WE}$, $\overline{OE}$, $\overline{RFSH}$	C_{IN2}		8	pF
	$\overline{CE}$, CS, RESET	C_{IN3}		8	pF
Input/output capacitance	I/O_0 - I/O_{15}	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current in normal operation	I_{CC1}	t_{RC} = t_{RC} (MIN.)		35	mA	1, 2
Operating current in static column mode	I_{CCSC1}	t_{SRC} = t_{SRC} (MIN.) or t_{SWC} = t_{SWC} (MIN.)		TBD	mA	1, 2
Standby current	I_{CC2}	$\overline{CE}$, $\overline{OE}$, $\overline{RFSH}$ = V_{IH} (MIN.) RESET, CS = V_{IL} (MAX.)		1	mA	1
		$\overline{CE}$, $\overline{OE}$, $\overline{RFSH}$ = V_{CC} - 0.2 V RESET, CS = 0.2 V		30	µA	1
Self-refresh average current	I_{CC3}	$\overline{CE}$, $\overline{OE}$ = V_{IH} (MIN.), $\overline{RFSH}$, RESET = V_{IL} (MAX.)		1	mA	1
		$\overline{CE}$, $\overline{OE}$ = V_{CC} - 0.2 V, $\overline{RFSH}$, RESET = 0.2 V		300	µA	1, 3
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V (0 V on all other test pins)	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V (outputs in High-Z state)	-10	10	µA	
Output High voltage	V_{OH}	IOUT = -1 mA	2.4		V	
		I_{OUT} = 100 µA	V_{CC} - 0.2			
Output Low voltage	V_{OL}	IOUT = 1 mA		0.4	V	
		I_{OUT} = 100 µA		0.2		

NOTES:

1. The output pins are in high-impedance state.
2. I_{CC1} and I_{CCSC1} depend on the cycle time.
3. I_{CC3} at CMOS input level depends on RAM/ROM mapping. It is given by I_{CC3} = {0.8 × (N/16) + 0.2} × 300 µA, where N is the total number of blocks that include RAM page(s).
   Example: In case of 50% RAM and 50% ROM, I_{CC3} (MAX.) = 180 µA.

AC CHARACTERISTICS (Notes 1, 2) (T_A = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Random read, write cycle time	t_{RC}	200		ns	
Random read modify write cycle time	t_{RMW}	260		ns	
Static column mode read cycle time	t_{SRC}	60		ns	
Static column mode write cycle time	t_{SWC}	60		ns	
$\overline{CE}$ pulse width	t_{CE}	100	10,000	ns	
$\overline{CE}$ precharge time	t_P	90		ns	
Address setup time	t_{AS}	0		ns	3
Row address hold time from $\overline{CE}$	t_{RAH}	20		ns	3
Column address hold time from $\overline{CE}$	t_{CAH}	100		ns	
CS setup time from $\overline{CE}$	t_{CSS}	0		ns	
CS hold time from $\overline{CE}$	t_{CSH}	20		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
$\overline{CE}$ access time	t_{CEA}		100	ns	4
Address access time	t_{AA}		55	ns	4
$\overline{OE}$ access time	t_{OEA}		45	ns	4
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		ns	
Write disable to output in Low-Z	t_{WLZ}	0		ns	
Chip disable to output in High-Z	t_{CHZ}	0	25	ns	
Output disable to output in High-Z	t_{OHZ}	0	25	ns	
$\overline{WE}$ to output in High-Z	t_{WHZ}	0	25	ns	
Write command pulse width	t_{WCP}	20		ns	
Write command setup time	t_{WCS}	20	10,000	ns	
Write command hold time	t_{WCH}	65	10,000	ns	
Data setup time from $\overline{WE}$	t_{DSW}	25		ns	5
Data setup time from $\overline{CE}$	t_{DSC}	25		ns	5
Data hold time from write disable	t_{DHW}	0		ns	5
Data hold time from chip disable	t_{DHC}	0		ns	5
Data hold time from column address	t_{OH}	0		ns	
Column address setup time from $\overline{WE}$	t_{ASW}	0		ns	
Column address hold time from chip disable	t_{AHC}	0		ns	5
Column address hold time from write disable	t_{AHW}	0		ns	5
Transition time (rise and fall)	t_T	3	50	ns	
Output disable set-up time	t_{ODS}	0		ns	
Output disable hold time	t_{ODH}	15		ns	
Refresh time interval	t_{REF}		64	ms	6, 7
Auto refresh cycle time	t_{FC}	200		ns	6, 7
Refresh delay time from $\overline{CE}$	t_{RFD}	90		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		ns	
$\overline{CE}$ delay time from refresh disable (Auto refresh)	t_{FCE}	200		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	200		ns	

NOTES:

1. AC characteristics are measured at t_T = 5 ns.
2. AC characteristics are measured per the conditions indicated in Figure 4.
3. Row address signals are latched in the memory at the falling edge of $\overline{CE}$.
4. Measured with a load equivalent to 50 pF.
5. Input data is latched in the memory at the earlier rising edge of $\overline{CE}$ and $\overline{WE}$. One of t_{AHW}, t_{DSW}, t_{DHW} and t_{AHC}, t_{DSC}, t_{DHC} needs to be satisfied, and the other is "Don't care".
6. Address refresh or auto-refresh needs to be executed 4,096 times within 64 ms.
7. Regardless of the memory type (ROM or RAM), it is necessary to refresh all row addresses every 64 ms (MAX) interval.

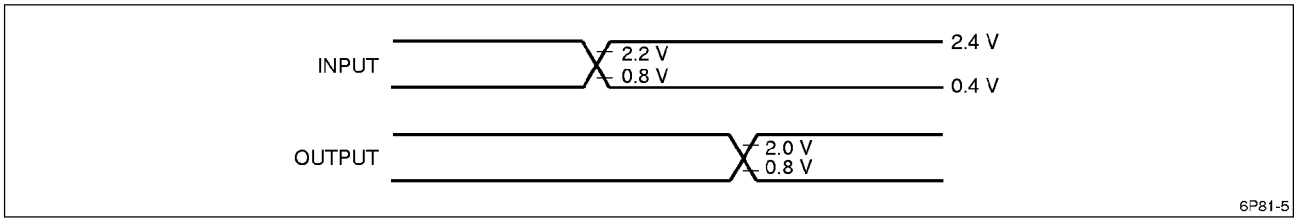


Figure 4. AC Characteristics Measuring Conditions

REQUIREMENTS FOR SF-ASIC RAM OPERATION

RESET Operation

- The initial reset operation is a special mode for the SF-ASIC RAM. In this mode, internal memory circuits are all reset and all RAM data are cleared to zero.
- To ensure normal operation of the SF-ASIC RAM, a minimum of 1 ms reset time is necessary after power-on. To initialize the internal memory circuits, RESET, $\overline{CE}$, and $\overline{RFSH}$ must be kept HIGH for more than 1 ms after V_{CC} reaches the operating voltage level. And after RESET goes LOW, $\overline{CE}$ and $\overline{RFSH}$ must stay HIGH for more than 200 ns.
- In normal use of the memory, a reset operation must be executed only once right after power-on.
- All RAM data are cleared to zero whenever a reset operation is executed.
- A reset operation is also necessary when supply voltage falls below the recommended supply voltage by temporary power down.
- When refresh time interval (t_{REF}) cannot be kept at a minimum of 64 ms, a reset operation is necessary to ensure correct ROM data read out.
- Regardless of ROM or RAM memory mapping, refresh time interval (t_{REF}) must be kept immediately after the reset operation.

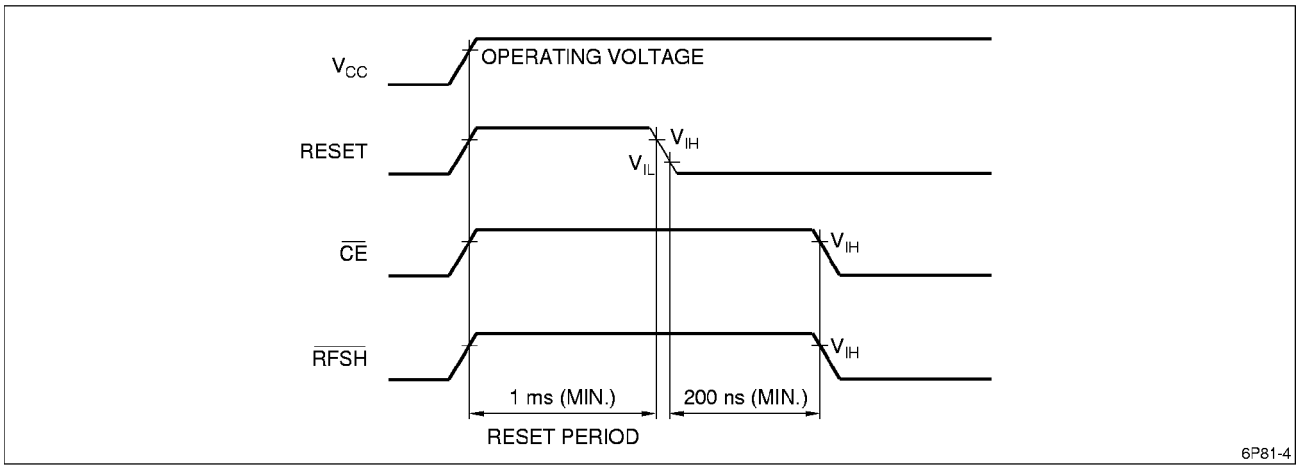


Figure 5. Reset Requirements for Power-on

Return From Data Retention Mode With Address Refresh or Auto-Refresh

As long as refresh time interval is kept and supply voltage is kept within the recommended voltage range, it is not necessary to execute a reset when returning from data retention mode with address refresh or auto-refresh.

Return From Self-Refresh Mode

As long as refresh time is kept and supply voltage is kept within the recommended voltage range, it is not necessary to execute a reset operation when returning from self-refresh mode.

Refresh After Self-Refresh or Reset

- If address refresh is used during normal read/write cycles, the first address refresh must be executed within 15 µs after self-refresh or reset ends and the address refresh must be executed continuously for 4096 refresh cycles.
- If distributed auto-refresh is used during normal read/write cycles, the first auto-refresh must be executed within 15 µs after self-refresh or reset ends.
- If burst auto-refresh is used during normal read/write cycles, the first auto-refresh must be executed within 15 µs after self-refresh or reset ends, and the auto-refresh must be executed continuously for 4096 refresh cycles.

Bypass Capacitor for Power Supply Noise Reduction

- Because the SF-ASIC RAM operates dynamically like a DRAM, it is recommended to put bypass capacitors between V_{CC} and GND to absorb power supply noise due to the peak current.

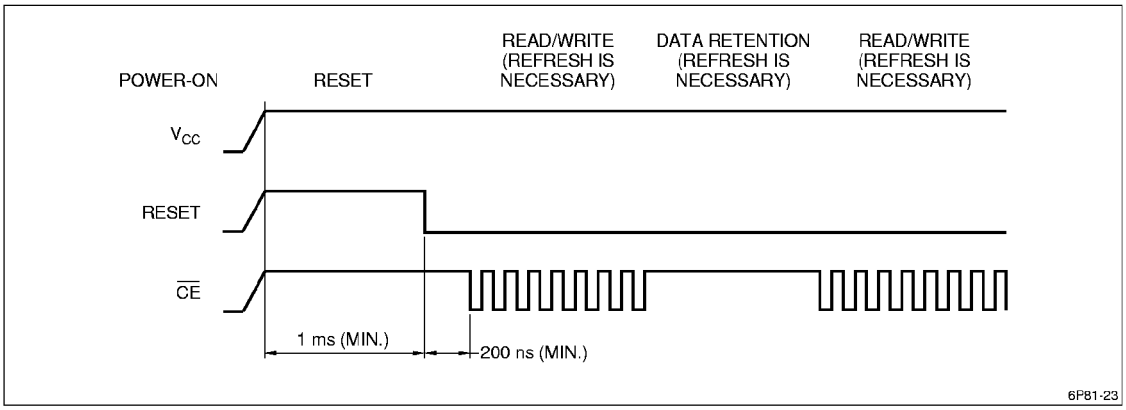


Figure 6. Return From Data Retention Mode

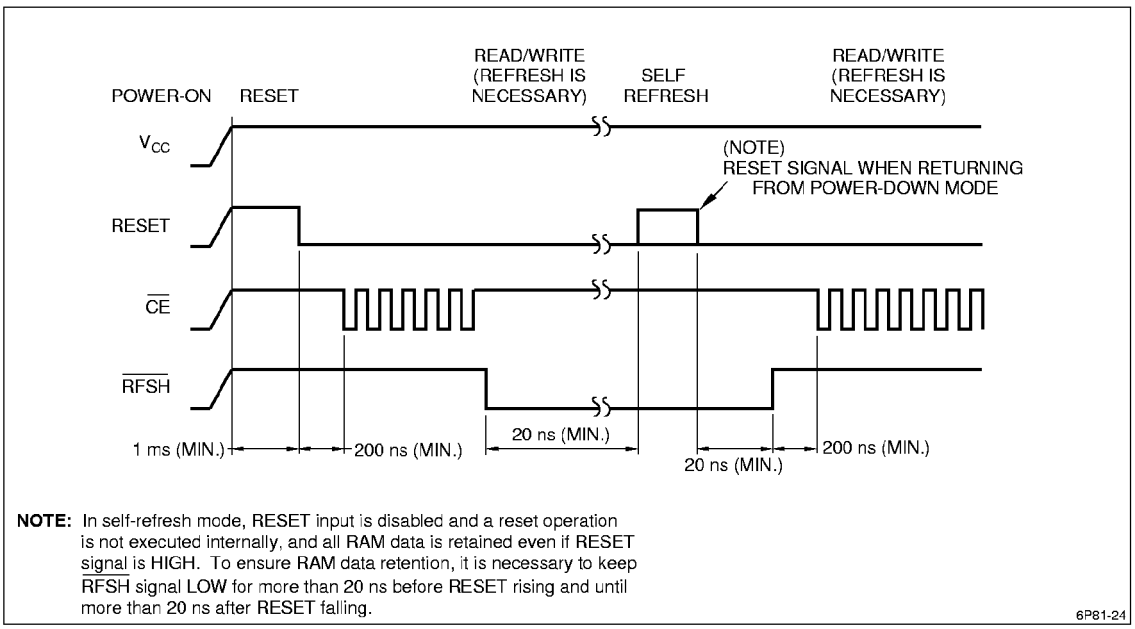


Figure 7. Return From Self-Refresh Mode

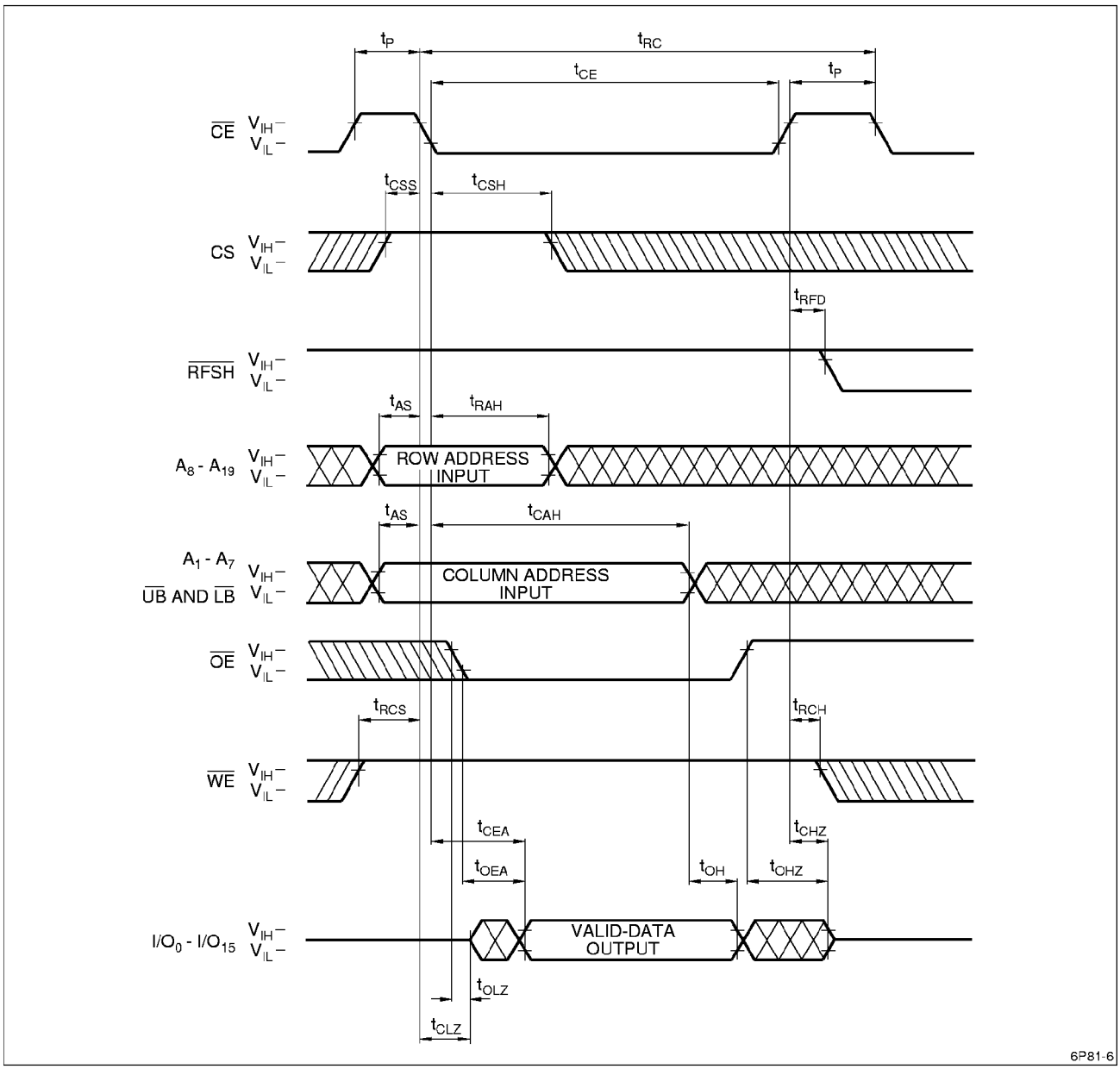


Figure 8. Read Cycle

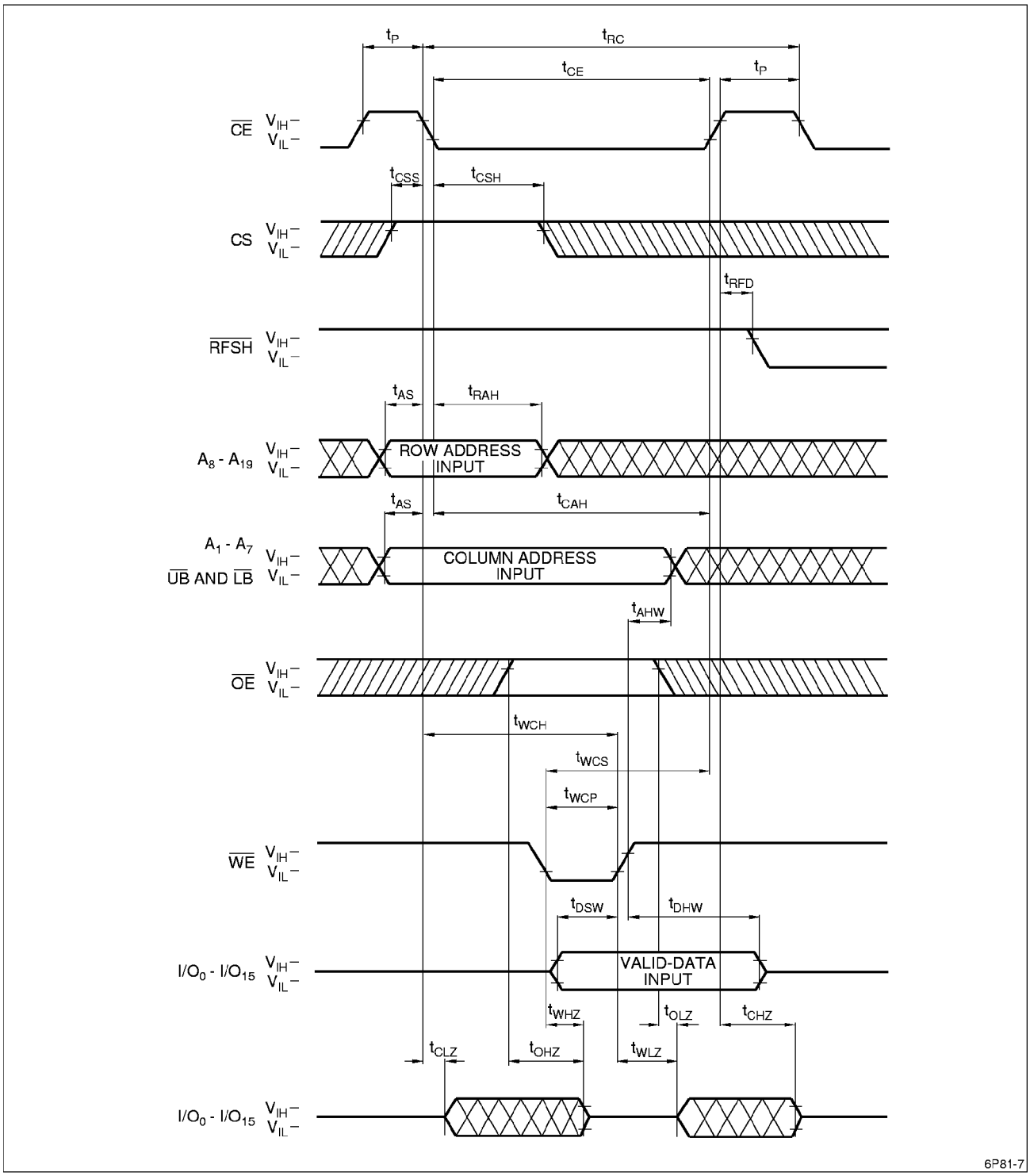


Figure 9. Write Cycle (1)
($\overline{OE}$ CLOCK)

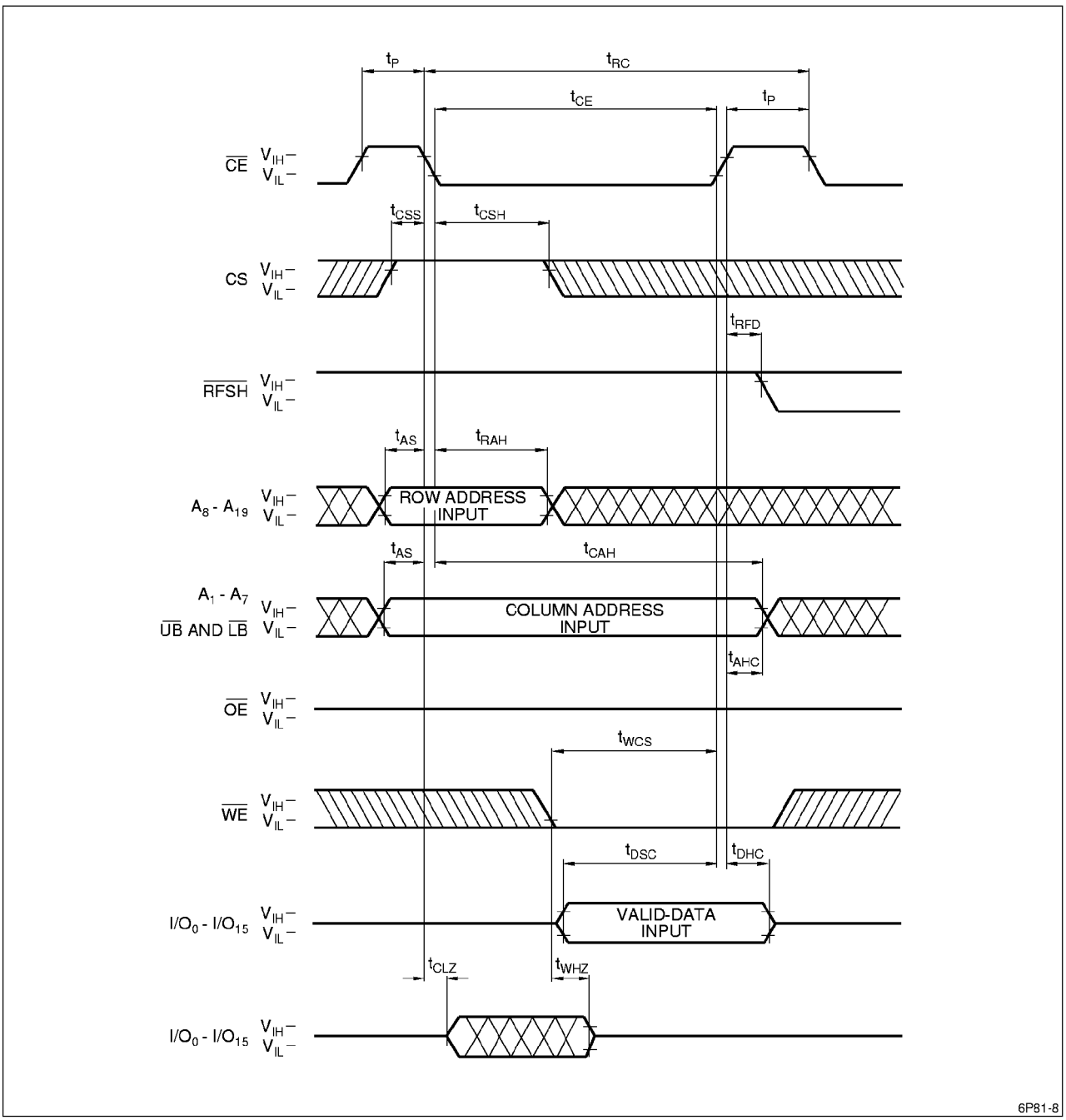


Figure 10. Write Cycle (2)
(OE = LOW, CE Control)

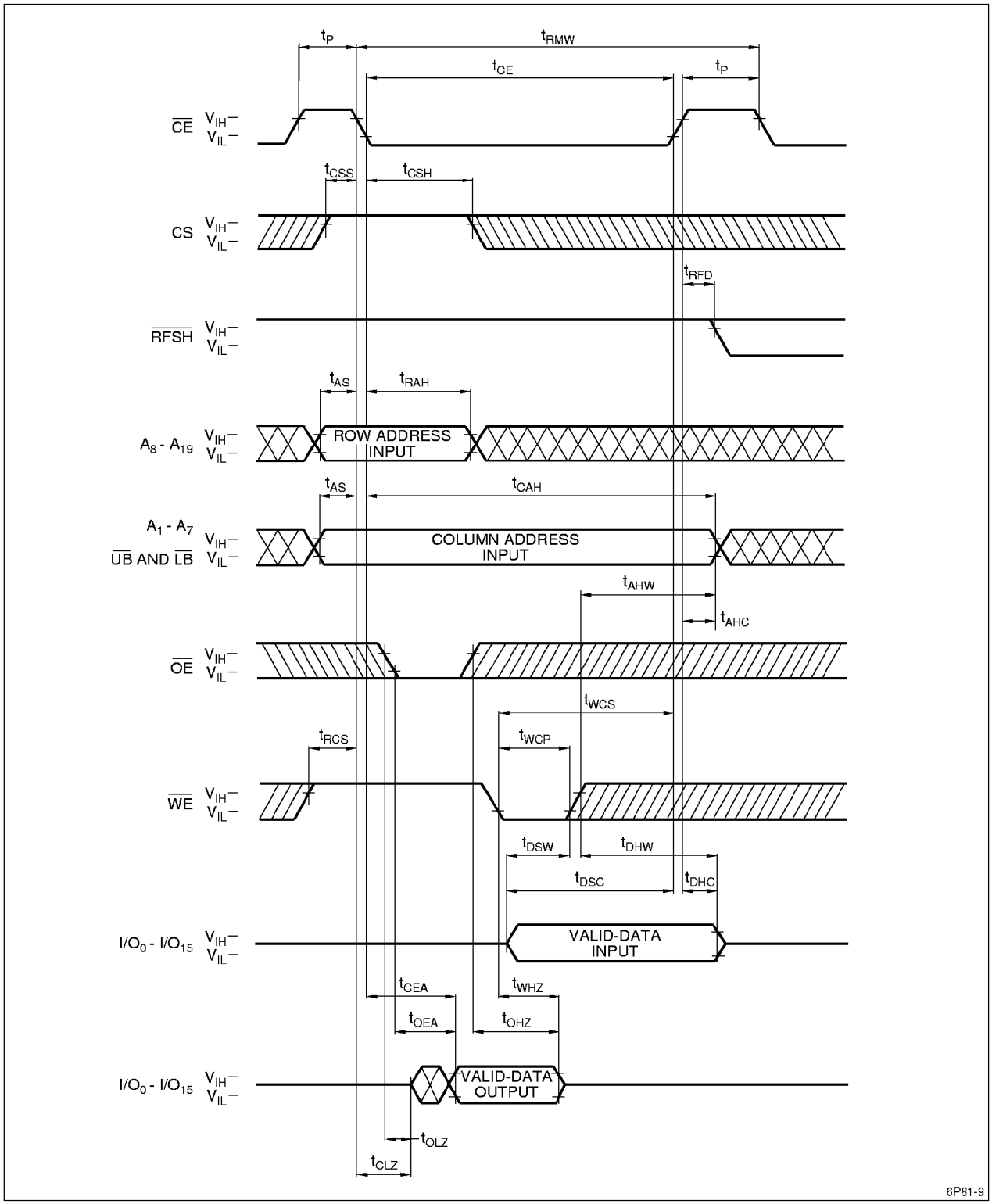


Figure 11. Read Write/Read Modify Write Cycle

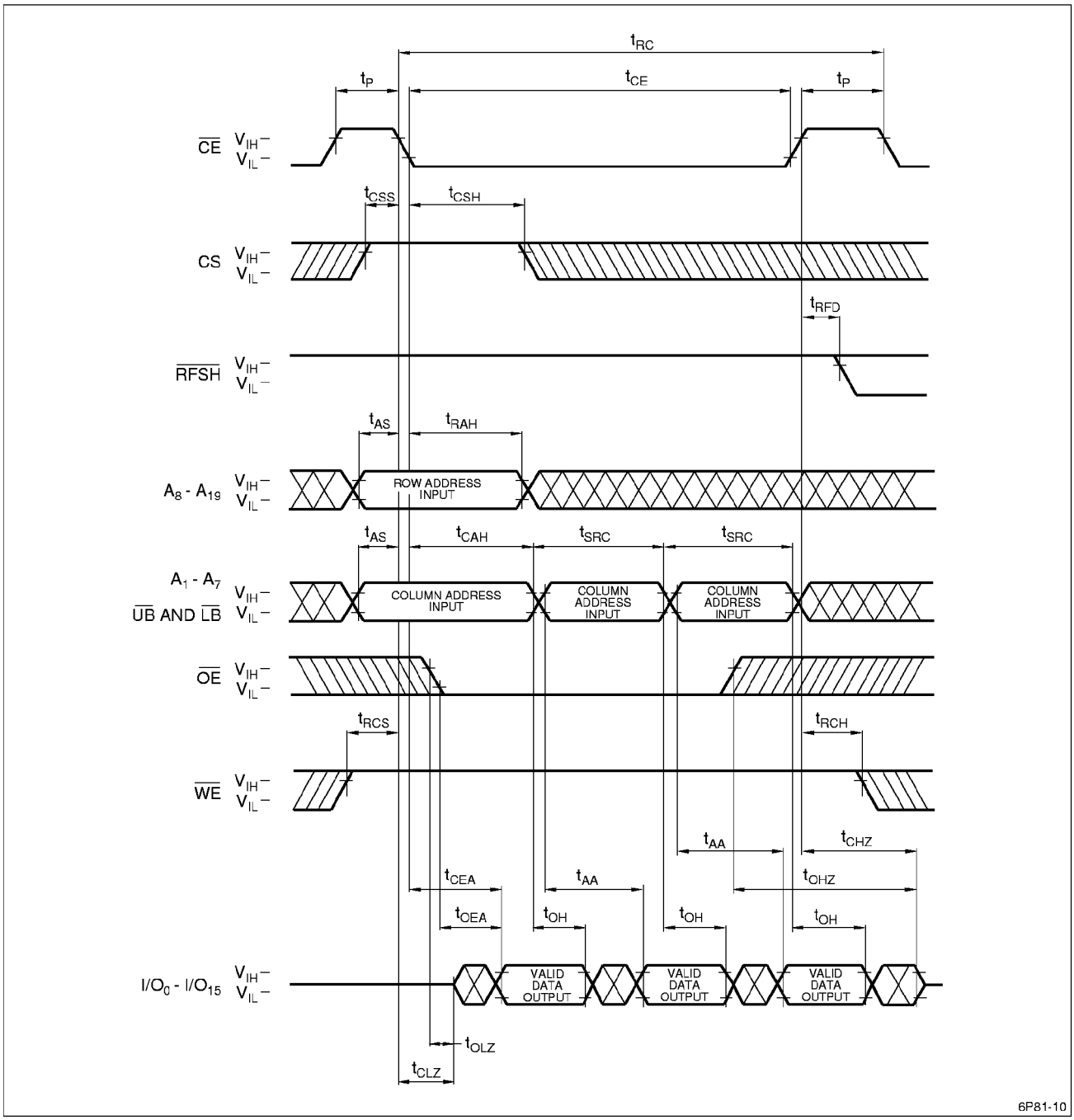


Figure 12. Static Column Mode Read Cycle

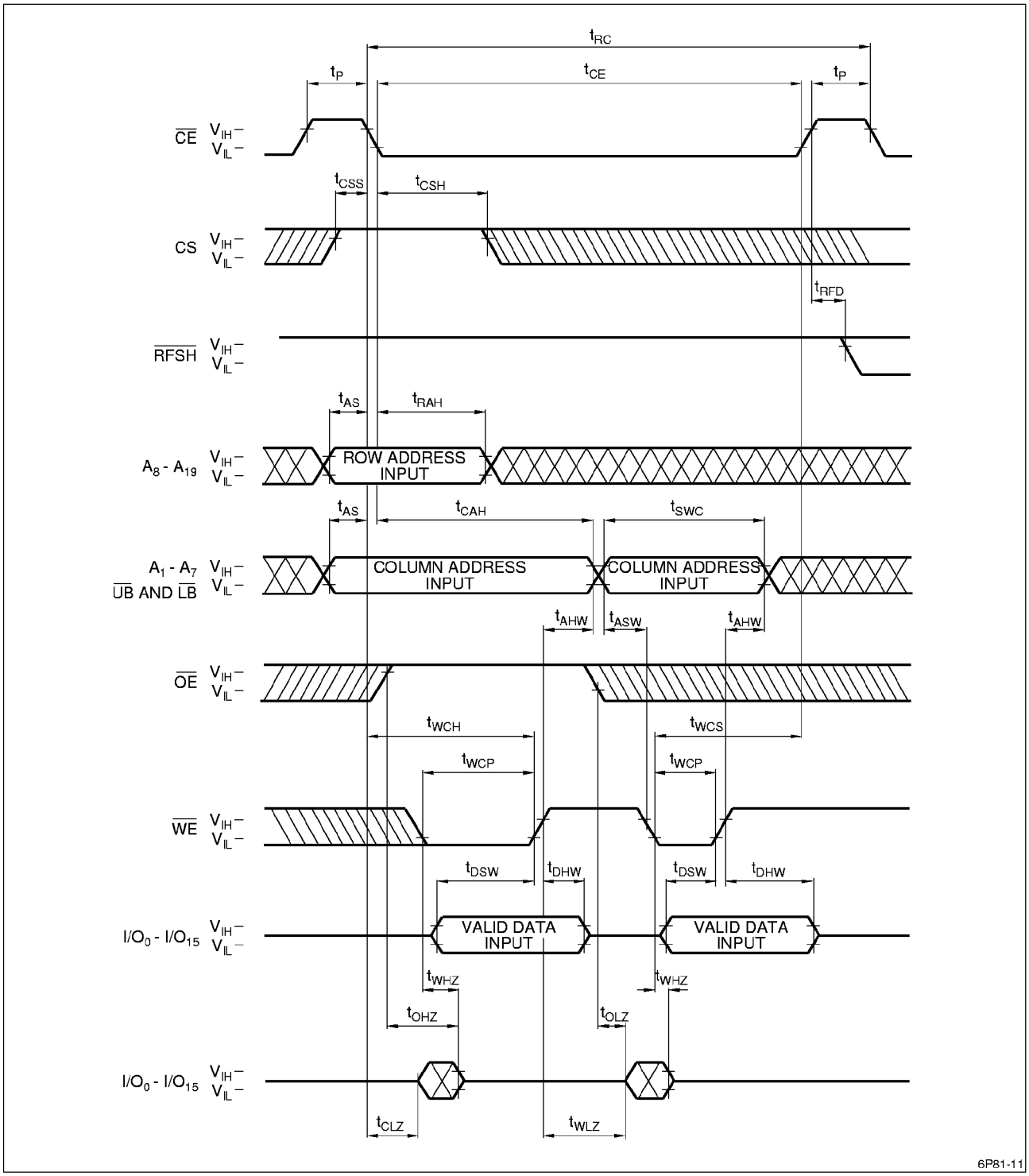


Figure 13. Static Column Mode Write Cycle

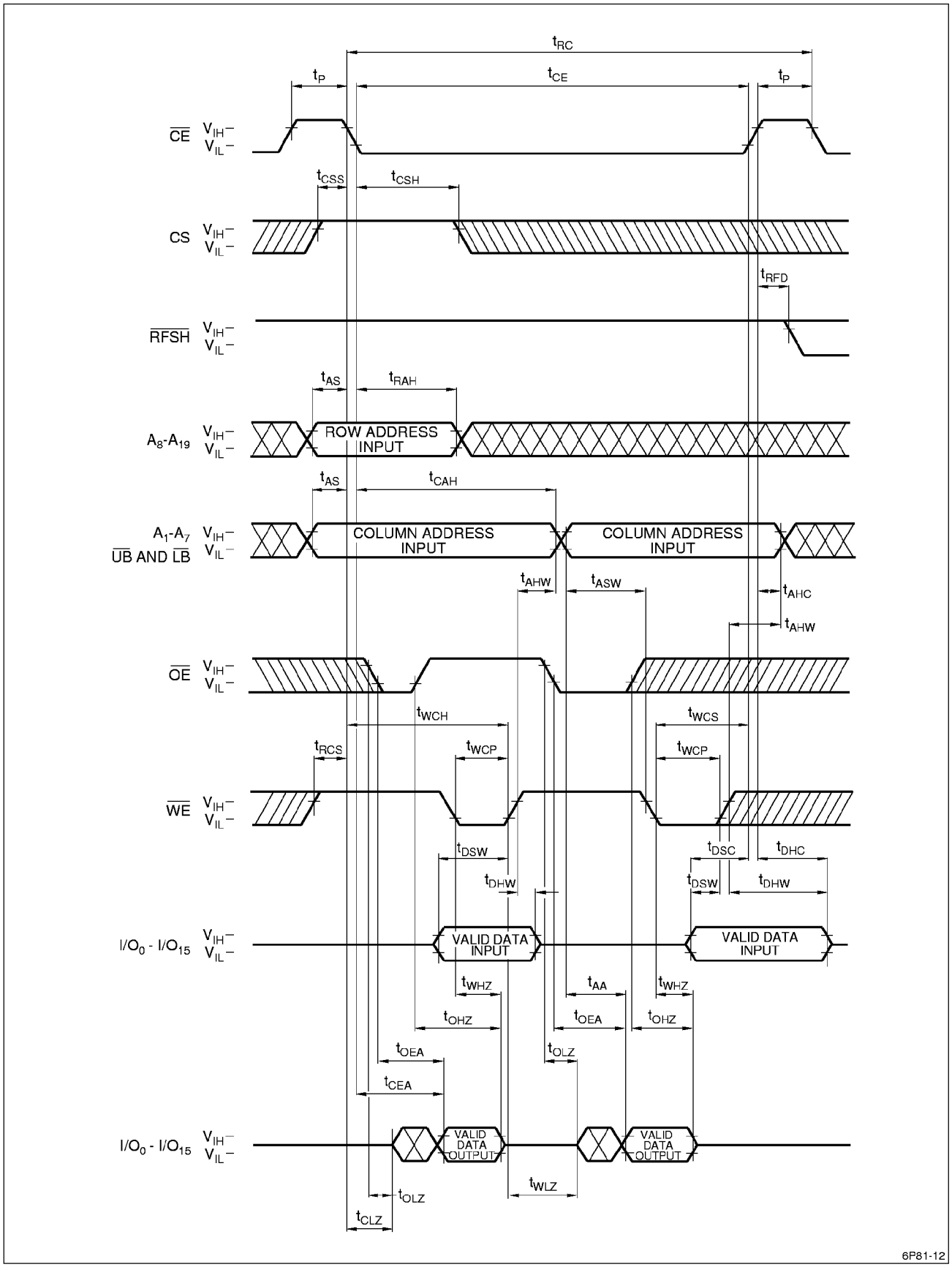
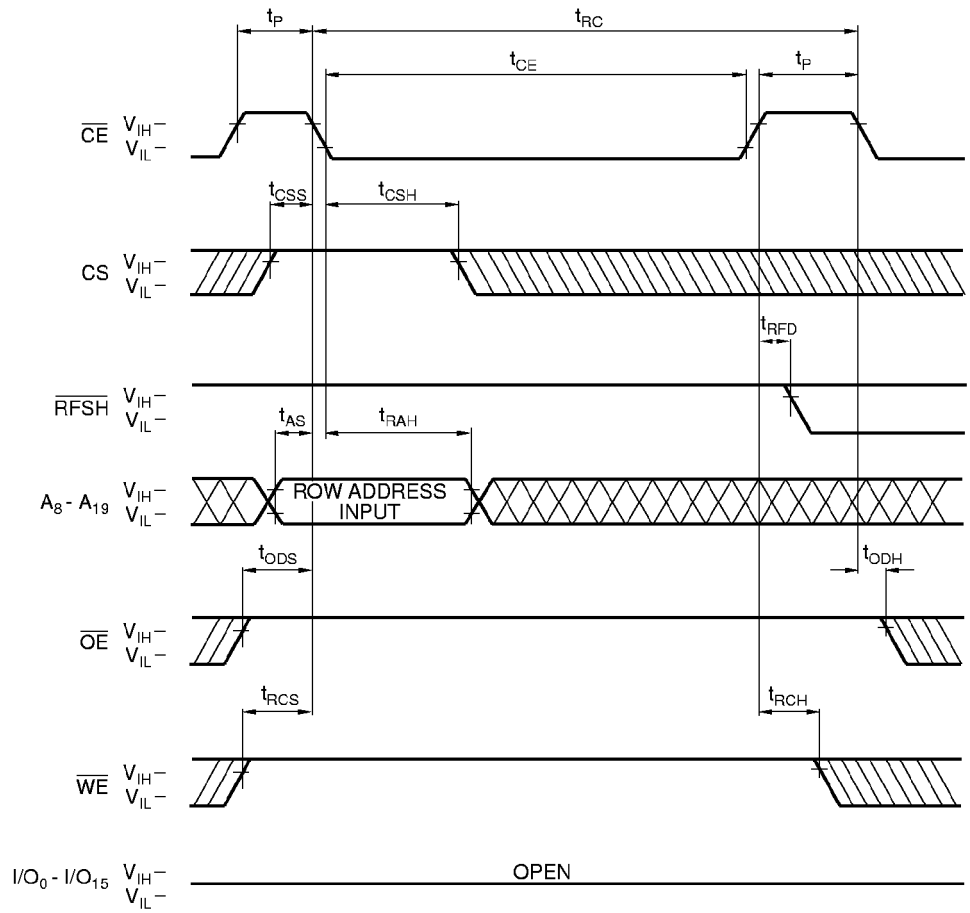


Figure 14. Static Column Mode Read Modify Write Cycle



NOTES:

1. A_1 - A_7, $\overline{UB}$, and $\overline{LB}$ = Don't Care.
2. Address refresh or auto-refresh needs to be executed 4,096 times within 64 ms.
3. Regardless of the memory type (ROM or RAM), it is necessary to refresh all row addresses every 64 ms (MAX.) interval.

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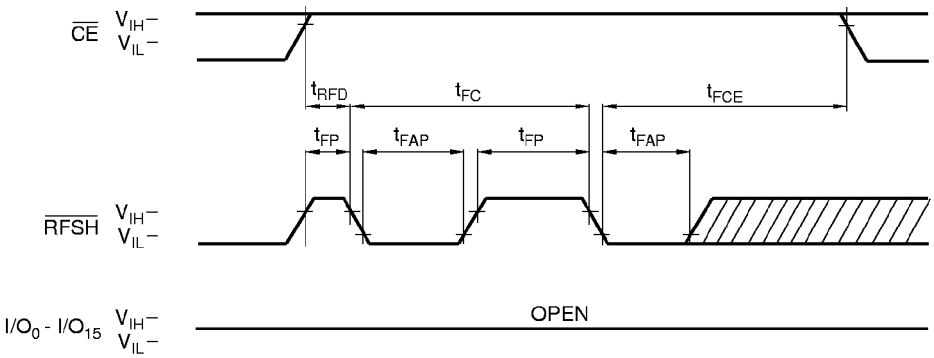
Figure 15. Address Refesh Cycle



NOTES:
1. CS, A_1 - A_{19}, $\overline{UB}$, $\overline{LB}$, $\overline{WE}$, and $\overline{OE}$ = Don't Care.
2. Address refresh or auto-refresh needs to be executed 4,096 times within 64 ms.
3. Regardless of the memory type (ROM or RAM), it is necessary to refresh all row addresses every 64 ms (MAX.) interval.

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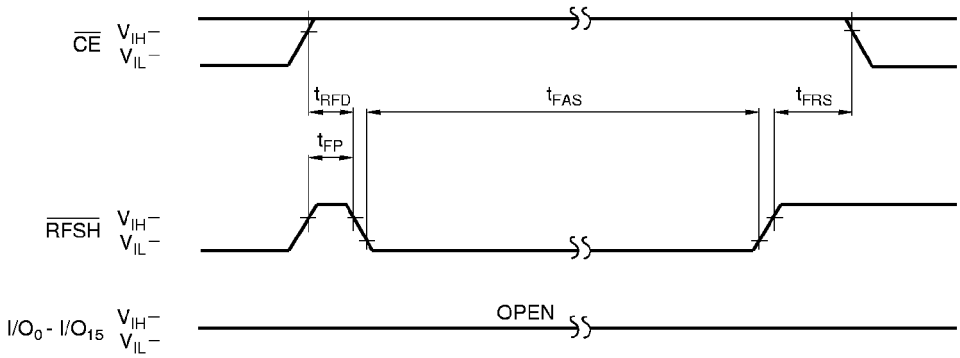
Figure 16. Auto Refresh Cycle



NOTE: CS, A_1 - A_{19}, $\overline{UB}$, $\overline{LB}$, $\overline{WE}$, and $\overline{OE}$ = Don't Care.

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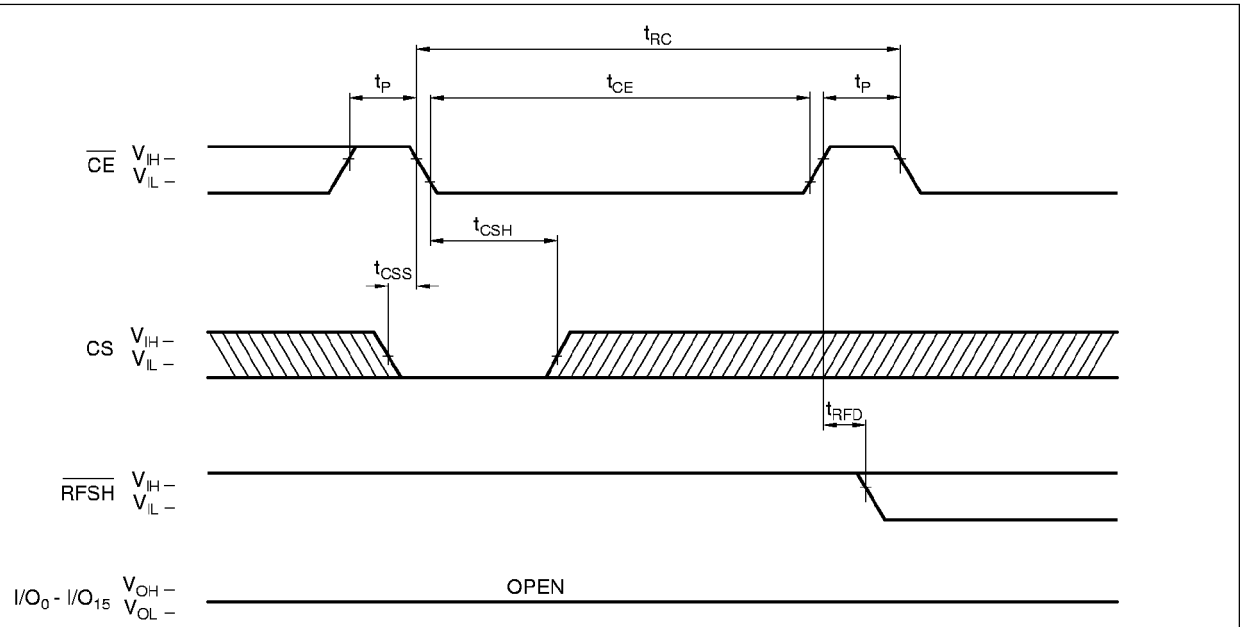
Figure 17. Self Refresh Cycle



NOTE: A_1 - A_{19}, $\overline{UB}$, $\overline{LB}$, $\overline{WE}$, and $\overline{OE}$ = Don't Care.

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Figure 18. CS Standby Mode