Integrated Device Technology, Inc.

16-BIT CMOS MULTILEVEL PIPELINE REGISTERS

PRELIMINARY
IDT 7320
IDT 7321

T-46-09-09

FEATURES:

- IDT7320: Eight 16-bit high-speed pipeline registers
- IDT7321: Seven 16-bit high-speed pipeline registers plus a direct feed-through path
- 12ns to 20ns access time
- Programmable multilevel register configurations
- Powerful instruction set: transfer, hold, load directly
- Functionally replaces four Am29520s
- Applications as temporary address storage or programmable pipeline registers for DSP products
- Coefficient storage for FIR filters
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 48-pin plastic and ceramic DIP and 52-pin surface mount PLCC and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT7320 and IDT7321 are multilevel pipeline registers. With IDT's high-performance CEMOS technology, the IDT7320 and IDT7321 have access times of 12ns.

The IDT7320 contains eight 16-bit registers which can be configured as one 8-level, two 4-level, four 2-level or eight 1-level pipeline registers.

The IDT7321 contains seven 16-bit registers and a direct feed-through path. The seven registers can be configured as one 7-level, a 4-level plus a 3-level, three 2-level or seven 1-level pipeline registers.

An eight-to-one output multiplexer allows data to be read from any one of the registers or from the feed-through path on the IDT7321. Three input control pins (SEL_0 - SEL_2) select which of the multiplexer inputs are directed to the output (Y_0 - Y_{15}).

These pipeline registers are ideal for high throughput, vector-oriented operations such as those in digital signal processing (DSP). The IDT7320 and IDT7321 can also be used as quick access scratch pad registers for general purpose computing.

The two pipeline registers are packaged in 48-pin plastic and ceramic DIPs for through-hole designs as well as 52-pin PLCC and LCC for surface mount designs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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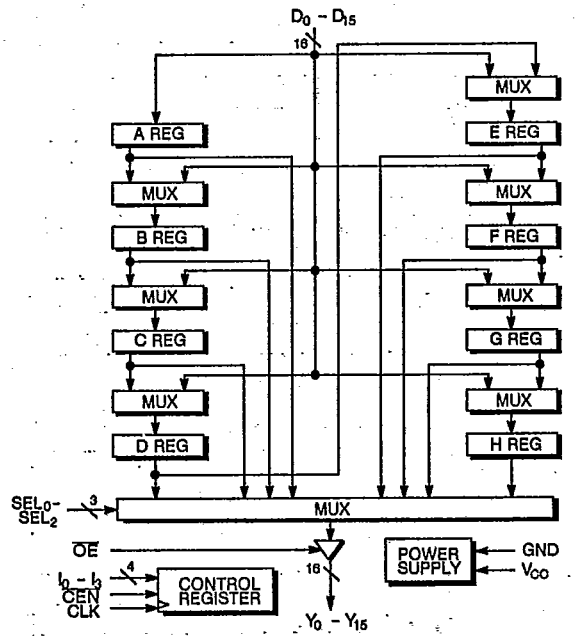
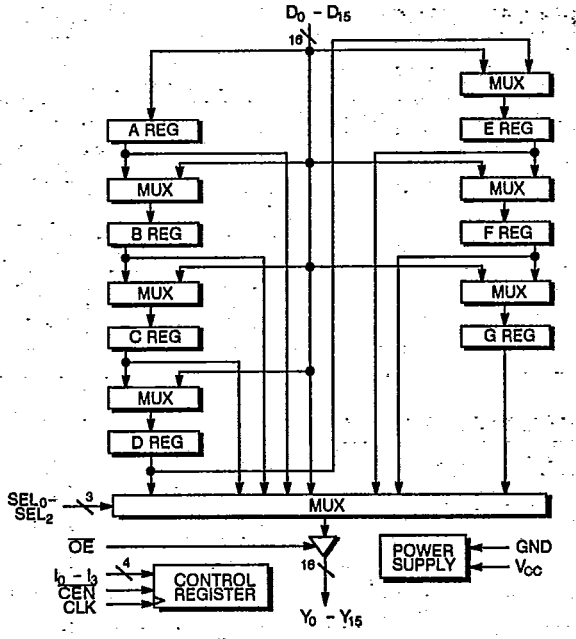
FUNCTIONAL BLOCK DIAGRAMS



IDT7320



IDT7321

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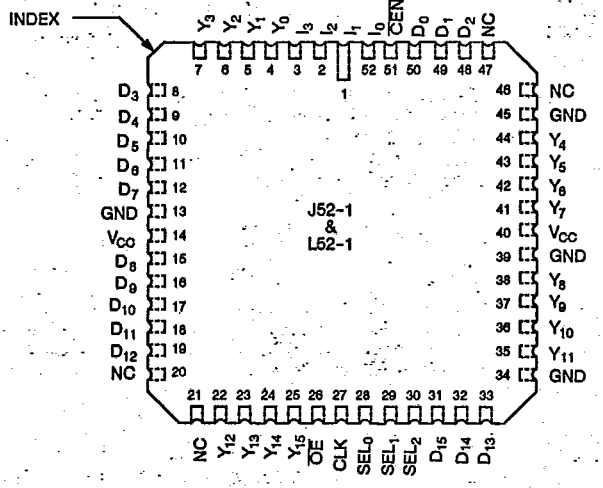
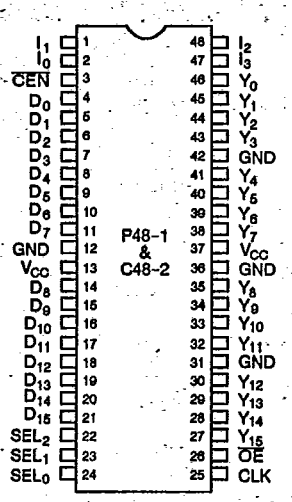
PIN CONFIGURATIONS



PLCC/LCC
TOP VIEW



DIP
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$D_0 - D_{15}$	I	Sixteen-bit data input port.
$Y_0 - Y_{15}$	O	Sixteen-bit data output port.
$I_0 - I_3$	I	Four control pins to select the register operation performed.
$SEL_0 - SEL_2$	I	Three control pins to select the register appearing at the output.
CLK	I	Clock input.
$\overline{CEN}$	I	Clock enable control pin. When this pin is low, the instruction $I_0 - I_3$ is performed on the registers. When high, no register operation occurs.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
V_{CC}		Power supply pin, 5V.
GND		Ground pins, 0V.

IDT7320 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y OUTPUT
0	0	0	A → $Y_0 - Y_{15}$
0	0	1	B → $Y_0 - Y_{15}$
0	1	0	C → $Y_0 - Y_{15}$
0	1	1	D → $Y_0 - Y_{15}$
1	0	0	E → $Y_0 - Y_{15}$
1	0	1	F → $Y_0 - Y_{15}$
1	1	0	G → $Y_0 - Y_{15}$
1	1	1	H → $Y_0 - Y_{15}$

IDT7321 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y OUTPUT
0	0	0	A → $Y_0 - Y_{15}$
0	0	1	B → $Y_0 - Y_{15}$
0	1	0	C → $Y_0 - Y_{15}$
0	1	1	D → $Y_0 - Y_{15}$
1	0	0	E → $Y_0 - Y_{15}$
1	0	1	F → $Y_0 - Y_{15}$
1	1	0	G → $Y_0 - Y_{15}$
1	1	1	$D_0 - D_{15} \rightarrow Y_0 - Y_{15}$

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IDT7320 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	MNEMONIC	FUNCTION	PIPELINE LEVELS
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	LDH	$D_0 - D_{15} \rightarrow H$	1
1	0	0	0	LSHAH	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	8
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEH	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	4
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LSHGH	$D_0 - D_{15} \rightarrow G \rightarrow H$	2
1	1	1	1	HOLD	Hold All Registers	–

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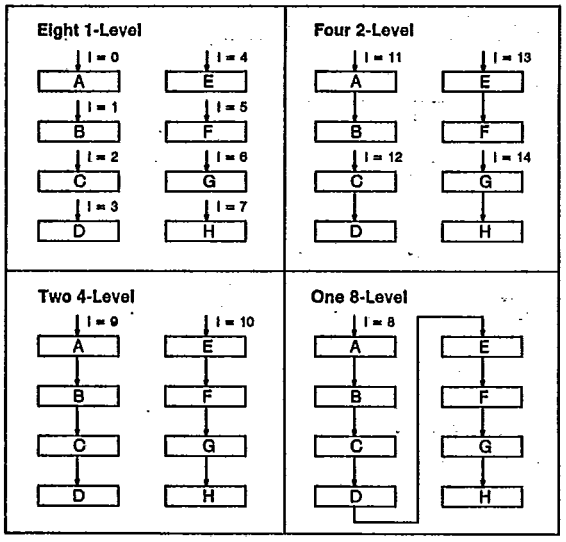
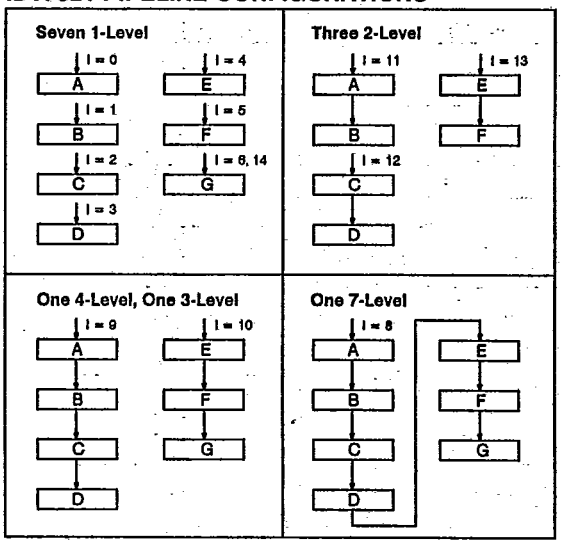
IDT7321 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	MNEMONIC	FUNCTION	PIPELINE LEVELS
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	HOLD	Hold All Registers	–
1	0	0	0	LSHAG	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G$	7
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEG	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G$	3
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
1	1	1	1	HOLD	Hold All Registers	–

IDT7320 PIPELINE CONFIGURATIONS



IDT7321 PIPELINE CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	–	–	V
V_{IL}	Input Low Voltage	–	–	0.8	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is sampled at initial characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
$\|I_{LO}\|$	Output Leakage Current	HI Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	–	0.1	5	–	0.1	10	µA
I_{CC}	Operating Power Supply Current	Outputs Open; f = 67MHz							
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$							
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq 0.2V$							
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -15.0mA (COM'L.), I_{OH} = -12.0mA (MIL.)	2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24.0mA (COM'L.), I_{OL} = 20.0mA (MIL.)		–	0.4	–	–	0.4	V

NOTE:

1. Typical implies V_{CC} = 5V and T_A = +25°C.

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AC ELECTRICAL CHARACTERISTICS – COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

PARAMETER	7320L10 7321L10		7320L12 7321L12		7320L15 7321L15		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
CLK to Y_0 – Y_{15} Propagation Delay	–	–	–	12	–	15	ns
SEL_0 – SEL_2 to Y_0 – Y_{15} Propagation Delay	–	–	–	12	–	15	ns
D_0 – D_{15} to CLK Setup Time	–	–	3	–	4	–	ns
D_0 – D_{15} to CLK Hold Time	–	–	1	–	2	–	ns
I_0 – I_3 to CLK Setup Time	–	–	4	–	5	–	ns
I_0 – I_3 to CLK Hold Time	–	–	2	–	2	–	ns
$\overline{OE}$ Enable Time	–	–	–	9	–	10	ns
$\overline{OE}$ Disable Time	–	–	–	8	–	9	ns
CLK Pulse Width HIGH	–	–	4	–	5	–	ns
CLK Pulse Width LOW	–	–	4	–	5	–	ns
CLK Period	–	–	–	12	–	15	ns

AC ELECTRICAL CHARACTERISTICS – MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to 125°C)

PARAMETER	7320L12 7321L12		7320L15 7321L15		7320L20 7321L20		UNITS
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
CLK to Y_0 – Y_{15} Propagation Delay	–	–	–	15	–	20	ns
SEL_0 – SEL_2 to Y_0 – Y_{15} Propagation Delay	–	–	–	15	–	20	ns
D_0 – D_{15} to CLK Setup Time	–	–	4	–	5	–	ns
D_0 – D_{15} to CLK Hold Time	–	–	2	–	3	–	ns
I_0 – I_3 to CLK Setup Time	–	–	5	–	6	–	ns
I_0 – I_3 to CLK Hold Time	–	–	2	–	3	–	ns
$\overline{OE}$ Enable Time	–	–	–	10	–	13	ns
$\overline{OE}$ Disable Time	–	–	–	9	–	13	ns
CLK Pulse Width HIGH	–	–	5	–	6	–	ns
CLK Pulse Width LOW	–	–	5	–	6	–	ns
CLK Period	–	–	–	15	–	20	ns

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

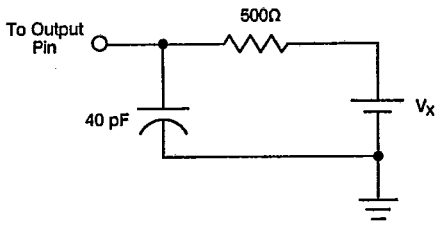

Figure 1. AC Output Test Load (V_X = 2.0V except for $\overline{OE}$ enable/disable)

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ORDERING INFORMATION