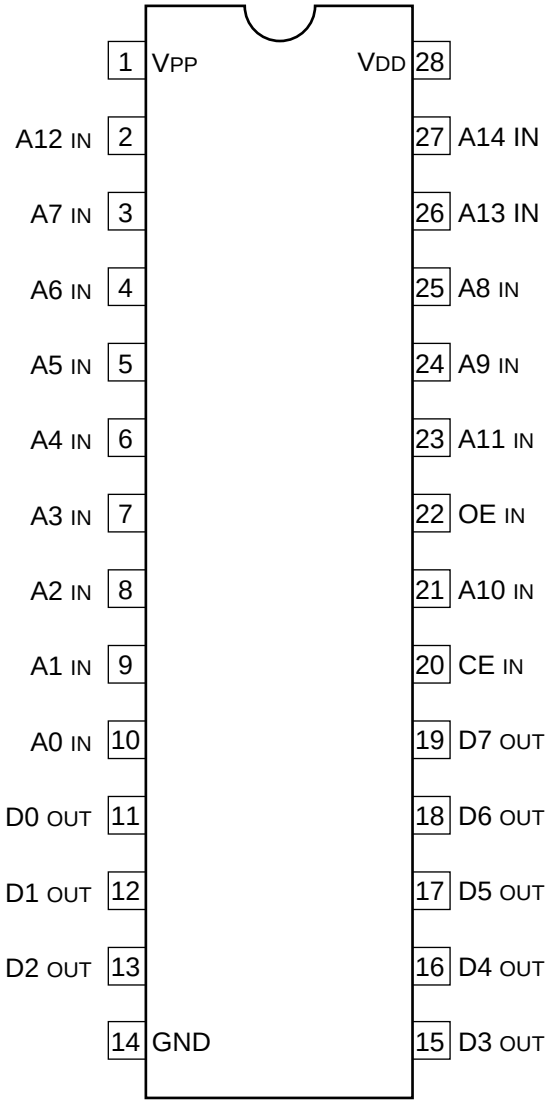
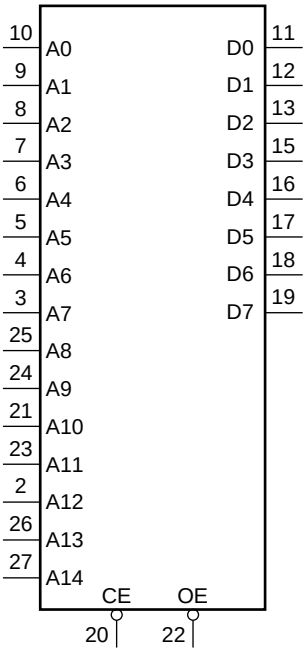
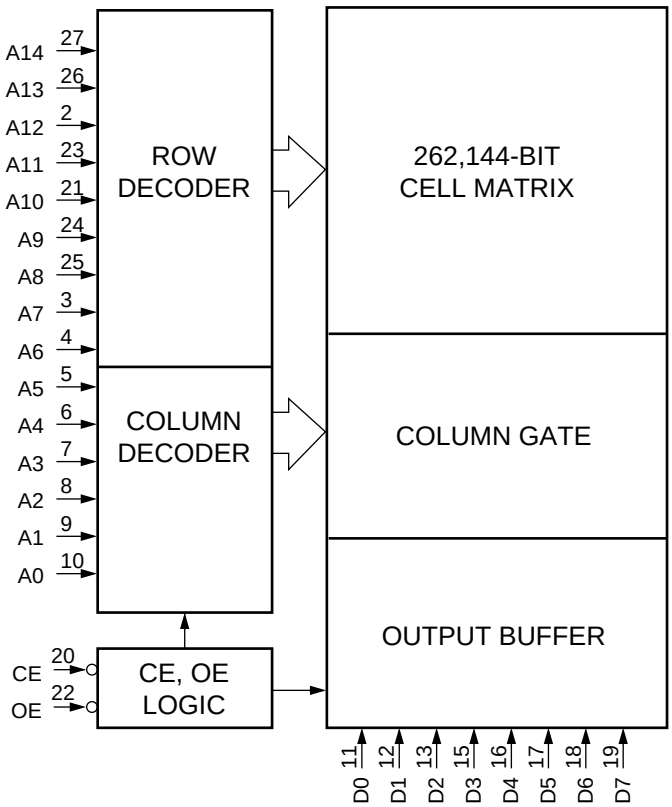
C-MOS 256 K (32 K × 8)-BIT UV ERASABLE PROM WITH 3-STATE OUTPUTS

—TOP VIEW—







A0 - A14	:	ADDRESS INPUTS
$\overline{CE}$	:	CHIP ENABLE INPUT
D0 - D7	:	DATA OUTPUTS
$\overline{OE}$	:	OUTPUT ENABLE INPUT
VPP	:	PROGRAM POWER SUPPLY

An	CE	OE	V_{DD}	V_{PP}	Dn	FUNCTION
An	0	0	+5 V	+5 V	D_{OUT}	READ
An	0	1	+5 V	+5 V	HI-Z	OUTPUT DISABLE
×	1	×	+5 V	+5 V	HI-Z	STANDBY
An	0	1	+6 V	+12.5 V	D_{IN}	PGM
An	1	0	+6 V	+12.5 V	D_{OUT}	PGM VERIFY (1)
An	0	0	+6 V	+12.5 V	D_{OUT}	PGM VERIFY (2)
×	1	1	+6 V	+12.5 V	HI-Z	PGM INH
AO	0	0	+5 V	+5 V	DEVICE CODE	ELECTRONIC SIGNATURE*

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE
HI-Z : HIGH IMPEDANCE

* SEE FOLLOWING DESCRIPTION

ELECTRONIC SIGNATURE FOR P ROM WRITER
ADDRESS SETTINGS IN READ MODE

A1 - A8	A9	A10 - A13	A14, Vpp
0	12 V	0	1

	AO	CODE DATA								
		D7	D6	D5	D4	D3	D2	D1	D0	
MAKER CODE	0	0	0	0	0	0	1	0	0	04H
DEVICE CODE	1	0	1	1	0	0	0	1	0	62H