



PRELIMINARY

**SOLID STATE DEVICES, INC.**

14830 Valley View Blvd \* La Mirada, Ca 90638  
 Phone: (562) 404-7855 \* Fax: (562) 404-1773

**SFF9130-28D**

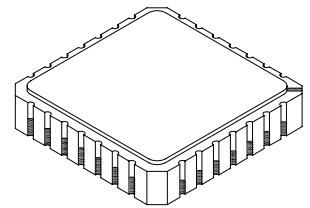
**-11 AMP  
 -100 VOLTS  
 0.30Ω  
 DUAL UNCOMMITTED  
 P-CHANNEL POWER MOSFET**

**DESIGNER'S DATA SHEET**

**FEATURES:**

- Rugged construction with poly silicon gate
- Low RDS (on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input transfer capacitance for easy paralleling
- Hermetically sealed surface mount package
- TX, TXV and Space Level screening available
- Replaces: 2x IRF9130 Types

**28 PIN CLCC**



**MAXIMUM RATINGS**

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V <sub>DS</sub>	-100	Volts
Gate to Source Voltage	V <sub>GS</sub>	±20	Volts
Continuous Drain Current T <sub>C</sub> = 25°C T <sub>C</sub> = 100°C	I <sub>D</sub>	-11 -7	Amps
Operating and Storage Temperature	T <sub>op</sub> & T <sub>stg</sub>	-55 to +150	°C
Thermal Resistance, Junction to Case (Both)	R <sub>θJC</sub>	3.5	°C/W
Total Device Dissipation T <sub>C</sub> = 25°C T <sub>C</sub> = 55°C	P <sub>D</sub>	36 37	Watts
Single Pulse Avalange Energy	E <sub>AS</sub>	84	mJ
Repetitive Avalange Energy	E <sub>AR</sub>	7.5	mJ

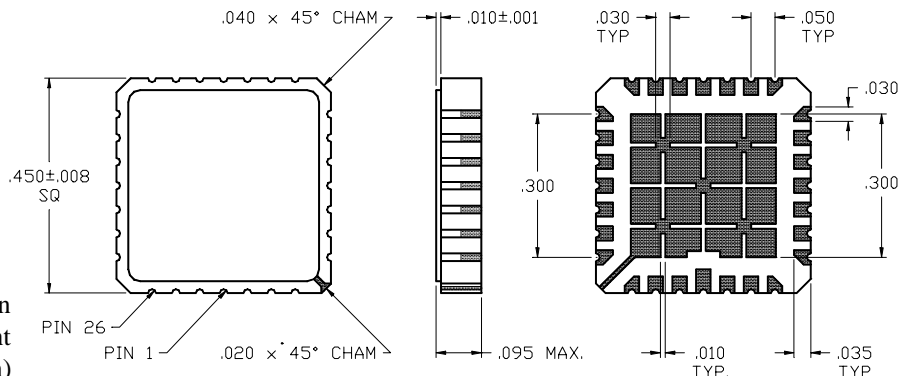
**PACKAGE OUTLINE: 28 PIN CLCC**

**PIN OUT:**

- SOURCE (1): 16 - 21
- DRAIN (1): 24 - 28
- GATE (1): 22
- SOURCE (2): 9 - 14
- DRAIN (2): 2 - 6
- GATE (2): 8

**NOTE:**

All drain/source pins must be connected on the PC board in order to maximize current carrying capability and to minimize RDS (on)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

**DATA SHEET #: FP0035D**

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## ELECTRICAL CHARACTERISTICS @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)

RATING		SYMBOL	MIN	TYP	MAX	UNIT
<b>Drain to Source Breakdown Voltage</b> (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1mA)		<b>BV<sub>DSS</sub></b>	-100	-	-	<b>V</b>
<b>Temperature Coefficient of Breakdown Voltage</b>		$\frac{\Delta BV_{DSS}}{\Delta T_J}$	-	0.87	-	<b>V</b>
<b>Drain to Source ON State Resistance<sup>1/</sup></b> (V <sub>GS</sub> = -10 V)	<b>I<sub>D</sub> = 7A</b> <b>I<sub>D</sub> = 11A</b>	<b>R<sub>DS(on)</sub></b>	-	-	0.30 0.35	<b>Ω</b>
<b>Gate Threshold Voltage</b> (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA)		<b>V<sub>GS(th)</sub></b>	-2.0	-	-4.0	<b>V</b>
<b>Forward Transconductance</b> (V <sub>DS</sub> > I <sub>D(on)</sub> x R <sub>DS(on)</sub> Max, I <sub>DS</sub> = 7A)		<b>g<sub>fs</sub></b>	3.0	5.0	-	<b>S(Ω)</b>
<b>Zero Gate Voltage Drain Current</b> (V <sub>DS</sub> = 80% rated V <sub>DS</sub> , V <sub>GS</sub> = 0 V, T <sub>A</sub> = 25°C ) (V <sub>DS</sub> = 80% rated V <sub>DS</sub> , V <sub>GS</sub> = 0 V, T <sub>A</sub> = 125°C )		<b>I<sub>DSS</sub></b>	-	-	-25 250	<b>μA</b>
<b>Gate to Source Leakage Forward</b> <b>Gate to Source Leakage Reverse</b>	At rated V <sub>GS</sub>	<b>I<sub>GSS</sub></b>	-	-	-100 100	<b>nA</b>
<b>Total Gate Charge</b> <b>Gate to Source Charge</b> <b>Gate to Drain Charge</b>	V <sub>GS</sub> = -10 Volts 50% rated V <sub>DS</sub> I <sub>D</sub> = -11A	<b>Q<sub>g</sub></b> <b>Q<sub>gs</sub></b> <b>Q<sub>gd</sub></b>	15 1 2	26 3 14	29 7.1 21	<b>nC</b>
<b>Turn on Delay Time</b> <b>Rise Time</b> <b>Turn off DELAY Time</b> <b>Fall Time</b>	V <sub>DD</sub> = 50% of rated V <sub>DS</sub> I <sub>D</sub> = 11A R <sub>G</sub> = 7.5Ω	<b>t<sub>d(on)</sub></b> <b>t<sub>r</sub></b> <b>t<sub>d(off)</sub></b> <b>t<sub>f</sub></b>	- - - -	15 10 30 12	60 140 140 140	<b>nsec</b>
<b>Diode Forward Voltage</b> (I <sub>S</sub> = rated I <sub>D</sub> , V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C)		<b>V<sub>SD</sub></b>	-	-	-4.7	<b>V</b>
<b>Diode Reverse Recovery Time</b> <b>Reverse Recovery Charge</b>	T <sub>J</sub> = 25°C I <sub>F</sub> = 10A di/dt = 100A/μsec	<b>t<sub>rr</sub></b> <b>Q<sub>RR</sub></b>	- -	125 -	250 3	<b>nsec</b> <b>μC</b>
<b>Input Capacitance</b> <b>Output Capacitance</b> <b>Reverse Transfer Capacitance</b>	V <sub>GS</sub> = 0 Volts V <sub>DS</sub> = -25 Volts f = 1 MHz	<b>C<sub>iss</sub></b> <b>C<sub>oss</sub></b> <b>C<sub>rss</sub></b>	- - -	860 350 125	- - -	<b>pF</b>

For thermal derating curves and other characteristic curves please contact SSDI Marketing Department.

### NOTES:

- <sup>1/</sup> All package pins of the same terminations (Drain/Source/Gate) must be connected together to minimize R<sub>DS(on)</sub> and maximize current carrying capability.