

## 3.3 V OPERATION 16M-WORD BY 72-BIT DYNAMIC RAM MODULE

### BUFFERED TYPE, EDO

#### Description

The MC-4216LFC72 is a 16,777,216 words by 72 bits dynamic RAM module on which 18 pieces of 64M DRAM :  $\mu$ PD4265405 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

#### Features

- Buffered type
- EDO (Hyper page mode)
- 16,777,216 words by 72 bits organization
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	EDO (Hyper page mode) cycle time (MIN.)	Power consumption (MAX.)	
				Active	Standby
MC-4216LFC72-A50	50 ns	84 ns	20 ns	8.65 W	262.8 mW
MC-4216LFC72-A60	60 ns	104 ns	25 ns	7.35 W	(CMOS level input)

- Refresh cycle

Family	Refresh cycle	Refresh
MC-4216LFC72-A50	4,096 cycles / 64 ms	/RAS only refresh, Normal read / write, /CAS before /RAS refresh,
MC-4216LFC72-A60		Hidden refresh

- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Single +3.3 V  $\pm$  0.3 V power supply

The information in this document is subject to change without notice.

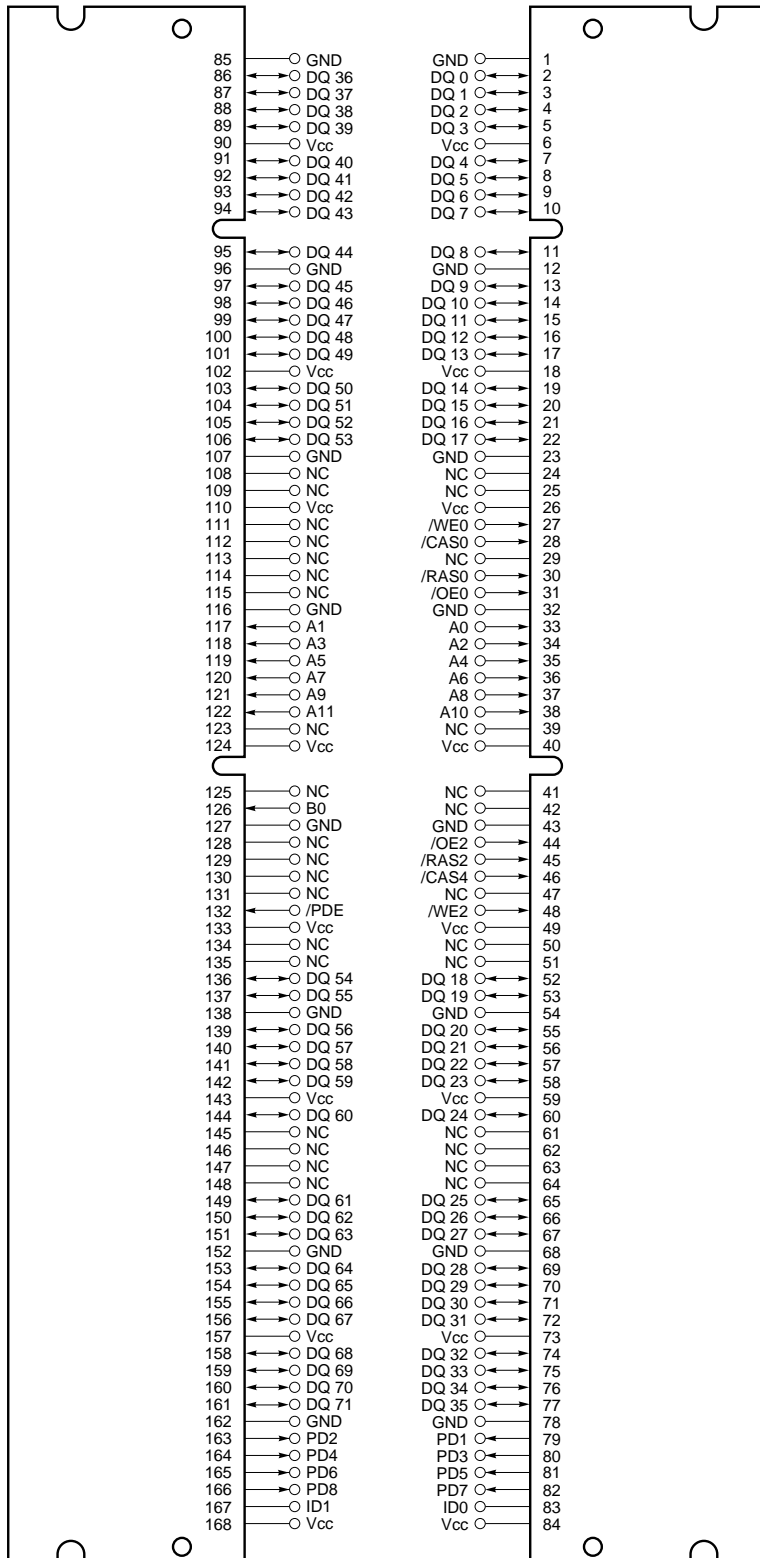
**Ordering Information**

Part number	Access time (MAX.)	Package	Mounted devices
MC-4216LFC72FH-A50	50 ns	168-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated	18 pieces of $\mu$ PD4265405G5 (400 mil TSOP(II))
MC-4216LFC72FH-A60	60 ns		[Double side]
MC-4216LFC72FB-A50	50 ns		18 pieces of $\mu$ PD4265405LE (400 mil SOJ)
MC-4216LFC72FB-A60	60 ns		[Double side]

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)

[MC-4216LFC72FH, 4216LFC72FB]



/XXX indicates active low signal.

PD and ID Table

Pin name	Pin No.	Access Time	
		50 ns	60 ns
PD1	79	H	H
PD2	163	H	H
PD3	80	H	H
PD4	164	H	H
PD5	81	H	H
PD6	165	L	H
PD7	82	L	H
PD8	166	L	L
ID0	83	GND	GND
ID1	167	GND	GND

Remark H : VOH L : VOL

A0 - A11, B0 : Address Inputs

[ Row : A0 - A11, B0, Column : A0 - A11, B0 ]

DQ0 - DQ71 : Data Inputs / Outputs

/RAS0, /RAS2 : Row Address Strobe

/CAS0, /CAS4 : Column Address Strobe

/WE0, /WE2 : Write Enable

/OE0, /OE2 : Output Enable

/PDE : Presence Detect Enable

PD1 - PD8 : Presence Detect Pins

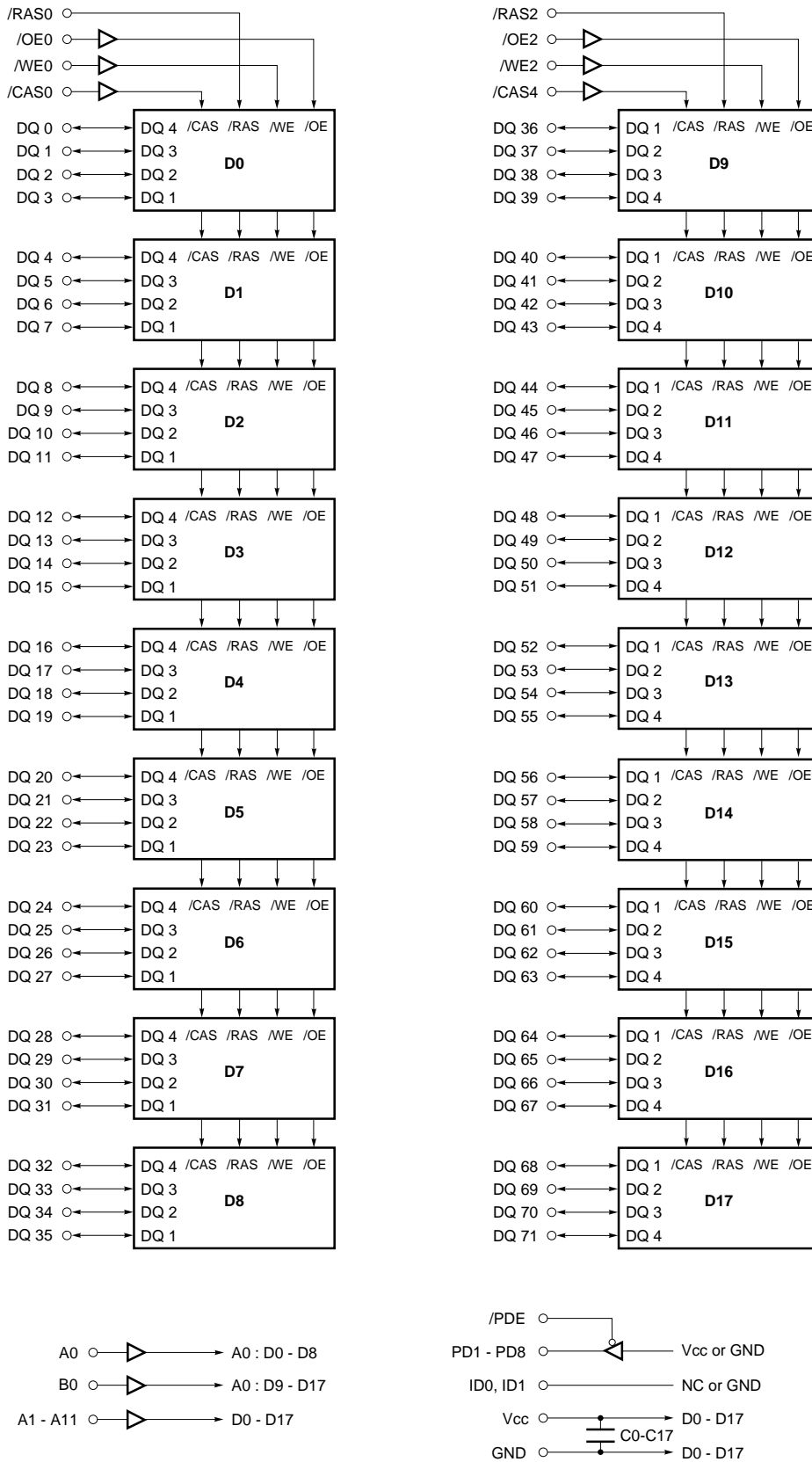
ID0, ID1 : Identity Pins

Vcc : Power Supply

GND : Ground

NC : No Connection

Block Diagram



Remark D0 - D17 :  $\mu$ PD4265405 (16M words by 4 bits organization)

**Electrical Specifications**

- All voltages are referenced to GND.
- After power up ( $V_{CC} \geq V_{CC(MIN.)}$ ), wait more than 100  $\mu s$  (/RAS, /CAS inactive) and then, execute eight /CAS before /RAS or /RAS only refresh cycles as dummy cycles to initialize internal circuit.

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	$V_T$		-0.5 to +4.6	V
Supply voltage	$V_{CC}$		-0.5 to +4.6	V
Output current	$I_o$		50	mA
Power dissipation	$P_D$		18	W
Operating ambient temperature	$T_A$		0 to +70	$^{\circ}C$
Storage temperature	$T_{stg}$		-55 to +125	$^{\circ}C$

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	$V_{CC}$		3.0	3.3	3.6	V
High level input voltage	$V_{IH}$		2.0		$V_{CC} + 0.3$	V
Low level input voltage	$V_{IL}$		-0.3		+0.8	V
Operating ambient temperature	$T_A$		0		70	$^{\circ}C$

**Capacitance ( $T_A = 25^{\circ}C$ ,  $f = 1$  MHz)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{I1}$	A0 - A11, B0			20	pF
	$C_{I2}$	/RAS0, /RAS2			88	
	$C_{I3}$	/CAS0, /CAS4			20	
	$C_{I4}$	/WE0, /WE2			20	
	$C_{I5}$	/OE0, /OE2			20	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ71			30	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current	I <sub>CC1</sub>	/RAS, /CAS cycling t <sub>RC</sub> = t <sub>RC (MIN.)</sub> , I <sub>O</sub> = 0 mA	t <sub>RAC</sub> = 50 ns	2,404	mA	1, 2, 3
			t <sub>RAC</sub> = 60 ns	2,044		
Standby current	I <sub>CC2</sub>	/RAS, /CAS ≥ V <sub>IH (MIN.)</sub> , I <sub>O</sub> = 0 mA		82	mA	
		/RAS, /CAS ≥ V <sub>CC</sub> -0.2 V, I <sub>O</sub> = 0 mA		73		
/RAS only refresh current	I <sub>CC3</sub>	/RAS cycling, /CAS ≥ V <sub>IH (MIN.)</sub> t <sub>RC</sub> = t <sub>RC (MIN.)</sub> , I <sub>O</sub> = 0 mA	t <sub>RAC</sub> = 50 ns	2,404	mA	1, 2, 3, 4
			t <sub>RAC</sub> = 60 ns	2,044		
Operating current (Hyper page mode (EDO))	I <sub>CC4</sub>	/RAS ≤ V <sub>IL (MAX.)</sub> , /CAS cycling t <sub>HPC</sub> = t <sub>HPC (MIN.)</sub> , I <sub>O</sub> = 0 mA	t <sub>RAC</sub> = 50 ns	1,864	mA	1, 2, 5
			t <sub>RAC</sub> = 60 ns	1,684		
/CAS before /RAS refresh current	I <sub>CC5</sub>	/RAS cycling t <sub>RC</sub> = t <sub>RC (MIN.)</sub> , I <sub>O</sub> = 0 mA	t <sub>RAC</sub> = 50 ns	2,404	mA	1, 2
			t <sub>RAC</sub> = 60 ns	2,044		
Input leakage current	I <sub>I (L)</sub>	V <sub>I</sub> = 0 to 3.6 V All other pins not under test = 0 V	/RAS	-45	μA	
			Others	-5		
Output leakage current	I <sub>O (L)</sub>	V <sub>O</sub> = 0 to 3.6 V Output is disabled (Hi-Z)	-5	+5	μA	
High level output voltage	V <sub>OH</sub>	I <sub>O</sub> = -2.0 mA	2.4		V	
Low level output voltage	V <sub>OL</sub>	I <sub>O</sub> = +2.0 mA		0.4	V	

**Notes** 1. I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC5</sub> depend on cycle rates (t<sub>RC</sub> and t<sub>HPC</sub>).

2. Specified values are obtained with outputs unloaded.

3. I<sub>CC1</sub> and I<sub>CC3</sub> are measured assuming that address can be changed once or less during /RAS ≤ V<sub>IL (MAX.)</sub> and /CAS ≥ V<sub>IH (MIN.)</sub>.

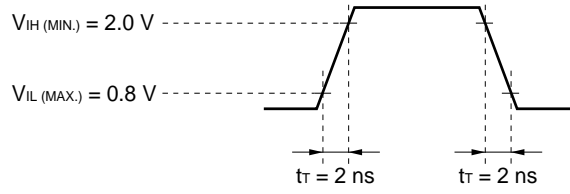
4. I<sub>CC3</sub> is measured assuming that all column address inputs are held at either high or low.

5. I<sub>CC4</sub> is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

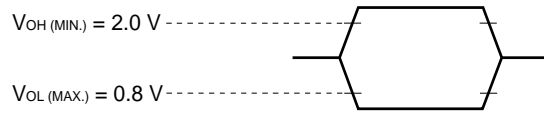
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

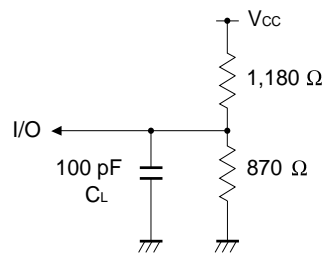
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



**Common to Read, Write, Read Modify Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t <sub>RC</sub>	84	–	104	–	ns	
/RAS precharge time	t <sub>RP</sub>	30	–	40	–	ns	
/CAS precharge time	t <sub>CPN</sub>	7	–	10	–	ns	
/RAS pulse width	t <sub>RAS</sub>	50	10,000	60	10,000	ns	
/CAS pulse width	t <sub>CAS</sub>	8	10,000	10	10,000	ns	
/RAS hold time	t <sub>RSH</sub>	18	–	20	–	ns	
/CAS hold time	t <sub>CSH</sub>	33	–	35	–	ns	
/RAS to /CAS delay time	t <sub>RCD</sub>	6	32	9	40	ns	1
/RAS to column address delay time	t <sub>RAD</sub>	4	20	7	25	ns	1
/CAS to /RAS precharge time	t <sub>CRP</sub>	10	–	10	–	ns	2
Row address setup time	t <sub>ASR</sub>	5	–	5	–	ns	
Row address hold time	t <sub>RAH</sub>	2	–	5	–	ns	
Column address setup time	t <sub>ASC</sub>	0	–	0	–	ns	
Column address hold time	t <sub>CAH</sub>	7	–	10	–	ns	
/OE lead time referenced to /RAS	t <sub>OES</sub>	5	–	5	–	ns	
/CAS to data setup time	t <sub>CLZ</sub>	5	–	5	–	ns	
/OE to data setup time	t <sub>OLZ</sub>	5	–	5	–	ns	
/OE to data delay time	t <sub>OED</sub>	15	–	18	–	ns	
Transition time (rise and fall)	t <sub>r</sub>	1	50	1	50	ns	
Refresh time	t <sub>REF</sub>	–	64	–	64	ms	

**Notes 1.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from /RAS
t <sub>RAD</sub> ≤ t <sub>RAD</sub> (MAX.) and t <sub>RCD</sub> ≤ t <sub>RCD</sub> (MAX.)	t <sub>RAC</sub> (MAX.)	t <sub>RAC</sub> (MAX.)
t <sub>RAD</sub> > t <sub>RAD</sub> (MAX.) and t <sub>RCD</sub> ≤ t <sub>RCD</sub> (MAX.)	t <sub>AA</sub> (MAX.)	t <sub>RAD</sub> + t <sub>AA</sub> (MAX.)
t <sub>RCD</sub> > t <sub>RCD</sub> (MAX.)	t <sub>CAC</sub> (MAX.)	t <sub>RCD</sub> + t <sub>CAC</sub> (MAX.)

t<sub>RAD</sub> (MAX.) and t<sub>RCD</sub> (MAX.) are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t<sub>RAC</sub>, t<sub>AA</sub> or t<sub>CAC</sub>) is to be used for finding out when output data will be available. Therefore, the input conditions t<sub>RAD</sub> ≥ t<sub>RAD</sub> (MAX.) and t<sub>RCD</sub> ≥ t<sub>RCD</sub> (MAX.) will not cause any operation problems.

**2.** t<sub>CRP</sub> (MIN.) requirement is applied to /RAS, /CAS cycles.



**Read Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Access time from /RAS	t <sub>RAC</sub>	–	50	–	60	ns	1
Access time from /CAS	t <sub>CAC</sub>	–	18	–	20	ns	1
Access time from column address	t <sub>AA</sub>	–	30	–	35	ns	1
Access time from /OE	t <sub>OE A</sub>	–	18	–	20	ns	
Column address lead time referenced to /RAS	t <sub>RAL</sub>	30	–	35	–	ns	
Read command setup time	t <sub>RCS</sub>	0	–	0	–	ns	
Read command hold time referenced to /RAS	t <sub>RRH</sub>	–5	–	–5	–	ns	2
Read command hold time referenced to /CAS	t <sub>RCH</sub>	0	–	0	–	ns	2
Output buffer turn-off delay time from /OE	t <sub>OEZ</sub>	5	15	5	18	ns	3
/CAS hold time to /OE	t <sub>CHO</sub>	5	–	5	–	ns	4

**Notes 1.** For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from /RAS
t <sub>RAD</sub> ≤ t <sub>RAD (MAX.)</sub> and t <sub>RCD</sub> ≤ t <sub>RCD (MAX.)</sub>	t <sub>RAC (MAX.)</sub>	t <sub>RAC (MAX.)</sub>
t <sub>RAD</sub> > t <sub>RAD (MAX.)</sub> and t <sub>RCD</sub> ≤ t <sub>RCD (MAX.)</sub>	t <sub>AA (MAX.)</sub>	t <sub>RAD</sub> + t <sub>AA (MAX.)</sub>
t <sub>RCD</sub> > t <sub>RCD (MAX.)</sub>	t <sub>CAC (MAX.)</sub>	t <sub>RCD</sub> + t <sub>CAC (MAX.)</sub>

t<sub>RAD (MAX.)</sub> and t<sub>RCD (MAX.)</sub> are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t<sub>RAC</sub>, t<sub>AA</sub> or t<sub>CAC</sub>) is to be used for finding out when output data will be available. Therefore, the input conditions t<sub>RAD</sub> ≥ t<sub>RAD (MAX.)</sub> and t<sub>RCD</sub> ≥ t<sub>RCD (MAX.)</sub> will not cause any operation problems.

2. Either t<sub>RCH (MIN.)</sub> or t<sub>RRH (MIN.)</sub> should be met in read cycles.
3. t<sub>OEZ (MAX.)</sub> defines the time when the output achieves the condition of Hi-Z and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
4. /WE : inactive (in read cycle)  
 /CAS : inactive, /OE : active ..... t<sub>CHO</sub> is effective.  
 /RAS, /OE : active ..... t<sub>CH</sub> is effective.

**Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
/WE hold time referenced to /CAS	t <sub>WCH</sub>	7	–	10	–	ns	1
/WE pulse width	t <sub>WP</sub>	7	–	10	–	ns	1
/WE lead time referenced to /RAS	t <sub>RWL</sub>	18	–	20	–	ns	
/WE lead time referenced to /CAS	t <sub>CWL</sub>	7	–	10	–	ns	
/WE setup time	t <sub>WCS</sub>	0	–	0	–	ns	2
/OE hold time	t <sub>OEH</sub>	0	–	0	–	ns	
Data-in setup time	t <sub>DS</sub>	–5	–	–5	–	ns	3
Data-in hold time	t <sub>DH</sub>	12	–	15	–	ns	3

- Notes**
1. t<sub>WP</sub> (MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t<sub>WCH</sub> (MIN.) should be met.
  2. If t<sub>WCS</sub> ≥ t<sub>WCS</sub> (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
  3. t<sub>DS</sub> (MIN.) and t<sub>DH</sub> (MIN.) are referenced to the /CAS falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the /WE falling edge.

**Read Modify Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t <sub>RWC</sub>	107	–	133	–	ns	
/RAS to /WE delay time	t <sub>RWD</sub>	59	–	72	–	ns	1
/CAS to /WE delay time	t <sub>CWD</sub>	27	–	32	–	ns	1
Column address to /WE delay time	t <sub>AWD</sub>	39	–	47	–	ns	1

- Note**
1. If t<sub>WCS</sub> ≥ t<sub>WCS</sub> (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.  
 If t<sub>RWD</sub> ≥ t<sub>RWD</sub> (MIN.), t<sub>CWD</sub> ≥ t<sub>CWD</sub> (MIN.), t<sub>AWD</sub> ≥ t<sub>AWD</sub> (MIN.) and t<sub>CPWD</sub> ≥ t<sub>CPWD</sub> (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

**Hyper Page Mode (EDO)**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Read / Write cycle time	t <sub>HPC</sub>	20	–	25	–	ns	1
/RAS pulse width	t <sub>RASP</sub>	50	125,000	60	125,000	ns	
/CAS pulse width	t <sub>HCAS</sub>	8	10,000	10	10,000	ns	
/CAS precharge time	t <sub>CP</sub>	7	–	10	–	ns	
Access time from /CAS precharge	t <sub>ACP</sub>	–	35	–	40	ns	
/CAS precharge to /WE delay time	t <sub>CPWD</sub>	41	–	52	–	ns	2
/RAS hold time from /CAS precharge	t <sub>RHCP</sub>	35	–	40	–	ns	
Read modify write cycle time	t <sub>HPRWC</sub>	52	–	66	–	ns	
Data output hold time	t <sub>DHC</sub>	10	–	10	–	ns	
/OE to /CAS hold time	t <sub>OCH</sub>	5	–	5	–	ns	3
/OE precharge time	t <sub>OEP</sub>	5	–	5	–	ns	
Output buffer turn-off delay from /WE	t <sub>WEZ</sub>	5	15	5	18	ns	4, 5
/WE pulse width	t <sub>WPZ</sub>	7	–	10	–	ns	5
Output buffer turn-off delay from /RAS	t <sub>OFR</sub>	0	10	0	13	ns	4, 5
Output buffer turn-off delay from /CAS	t <sub>OFC</sub>	5	15	5	18	ns	4, 5

**Notes 1.** t<sub>HPC</sub> (MIN.) is applied to /CAS access.

**2.** If t<sub>WCS</sub> ≥ t<sub>WCS</sub> (MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t<sub>TRWD</sub> ≥ t<sub>TRWD</sub> (MIN.), t<sub>TCWD</sub> ≥ t<sub>TCWD</sub> (MIN.), t<sub>AWD</sub> ≥ t<sub>AWD</sub> (MIN.) and t<sub>CPWD</sub> ≥ t<sub>CPWD</sub> (MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

**3.** /WE : inactive (in read cycle)

/CAS : inactive, /OE : active ..... t<sub>CHO</sub> is effective.

/CAS, /OE : active ..... t<sub>CH</sub> is effective.

**4.** t<sub>OFC</sub> (MAX.), t<sub>OFR</sub> (MAX.) and t<sub>WEZ</sub> (MAX.) define the time when the output achieves the conditions of Hi-Z and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.

**5.** To make DQs to Hi-Z in read cycle, it is necessary to control /RAS, /CAS, /WE, /OE as follows. The effective specification depends on state of each signal.

(1) Both /RAS and /CAS are inactive (at the end of the read cycle)

/WE : inactive, /OE : active

t<sub>OFC</sub> is effective when /RAS is inactivated before /CAS is inactivated.

t<sub>OFR</sub> is effective when /CAS is inactivated before /RAS is inactivated.

The slower of t<sub>OFC</sub> and t<sub>OFR</sub> becomes effective.

(2) Both /RAS and /CAS are active or either /RAS or /CAS is active (in read cycle)

/WE, /OE : inactive ..... t<sub>WEZ</sub> is effective.

Both /RAS and /CAS are inactive or /RAS is active and /CAS is inactive (at the end of read cycle)

/WE, /OE : active and either t<sub>RRH</sub> or t<sub>RCH</sub> must be met ..... t<sub>WEZ</sub> and t<sub>WPZ</sub> are effective.

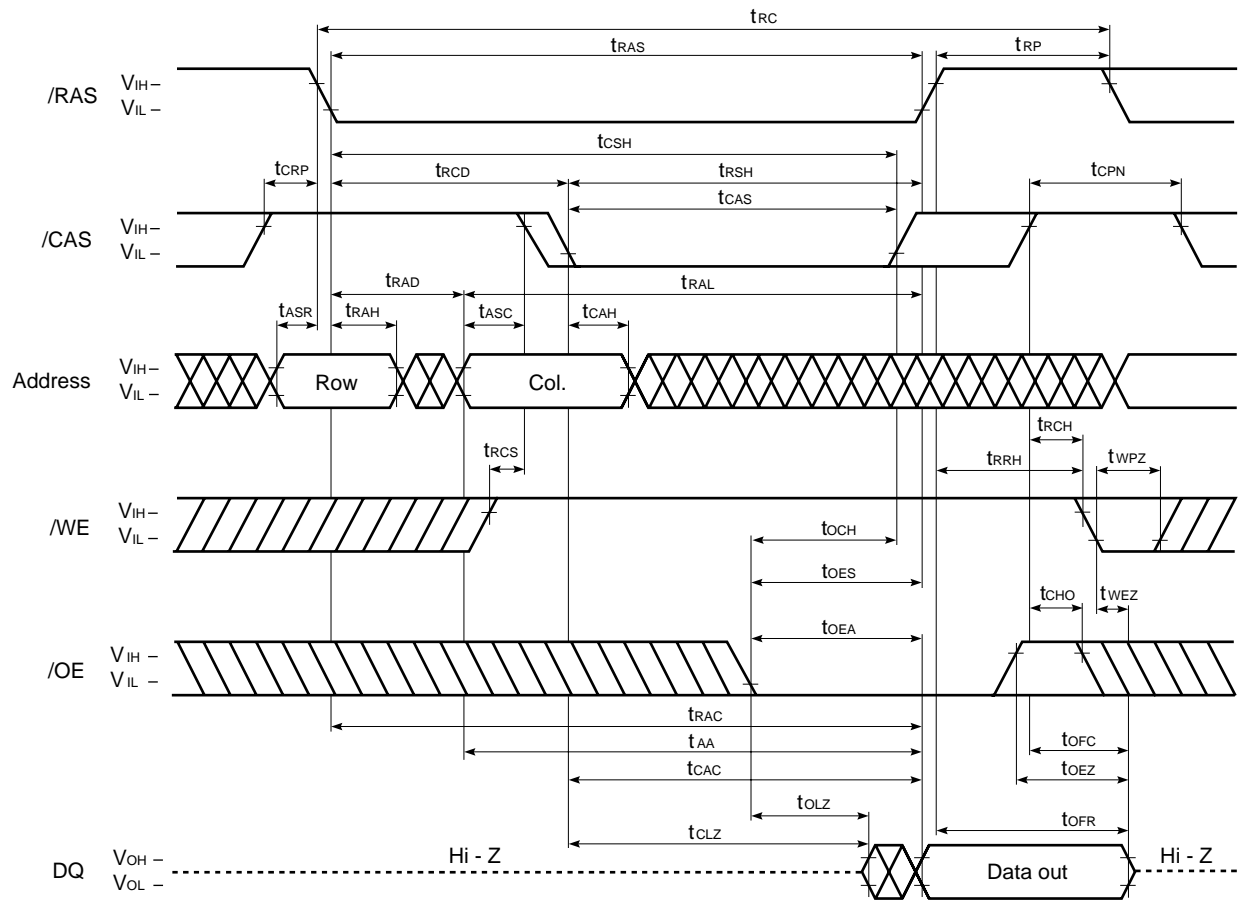
The faster of t<sub>WEZ</sub> and t<sub>WEZ</sub> becomes effective.

The faster of (1) and (2) becomes effective.

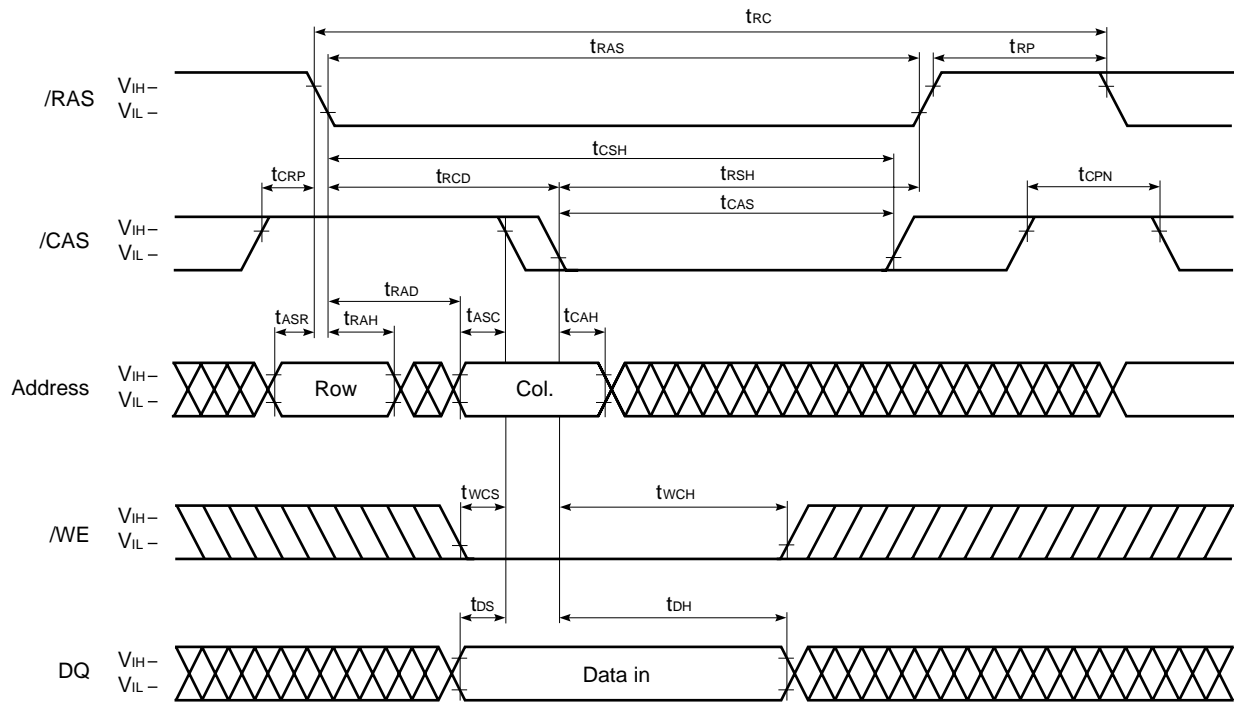
**Refresh Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.		
/CAS setup time	t <sub>CSR</sub>	10	–	10	–	ns	
/CAS hold time (/CAS before /RAS refresh)	t <sub>CHR</sub>	5	–	5	–	ns	
/RAS precharge /CAS hold time	t <sub>RPC</sub>	0	–	0	–	ns	
/WE setup time	t <sub>WSR</sub>	15	–	15	–	ns	
/WE hold time	t <sub>WHR</sub>	10	–	10	–	ns	

Read Cycle

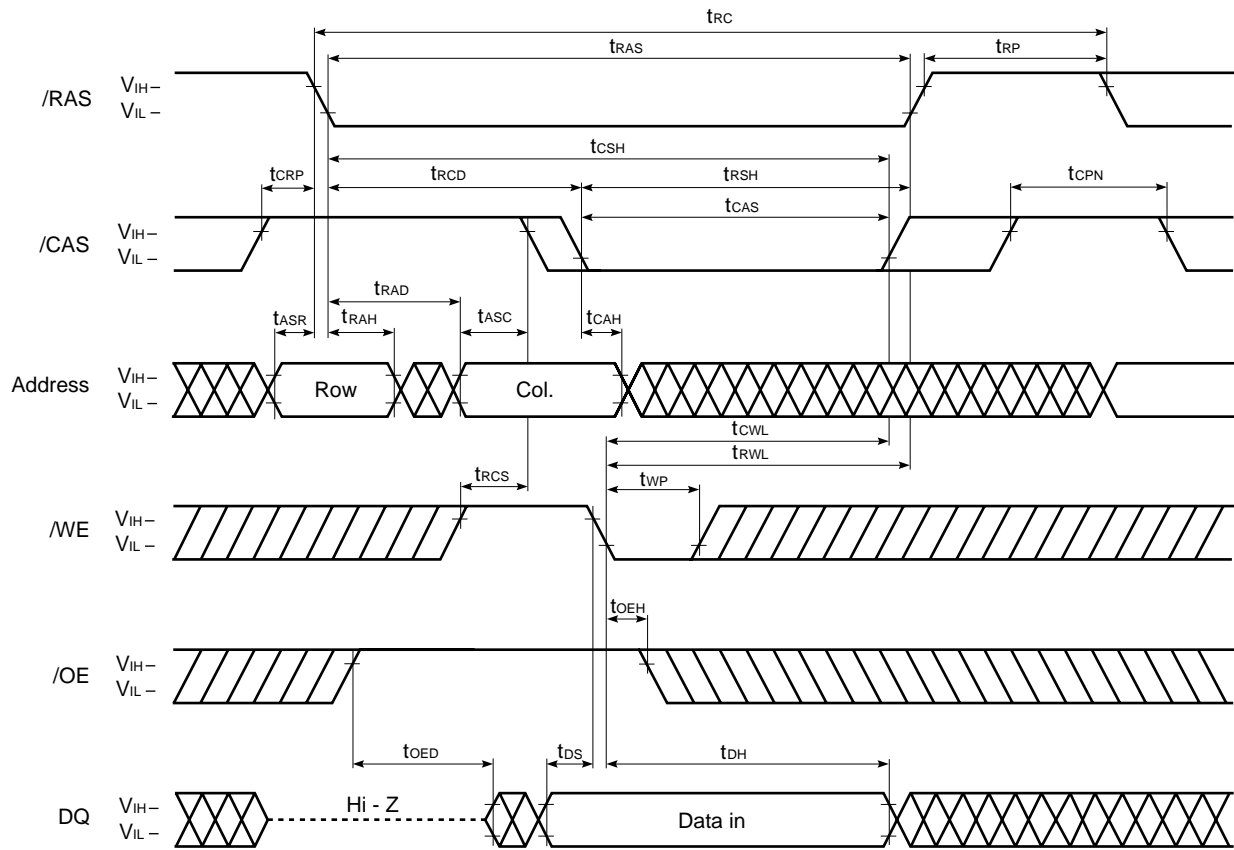


Early Write Cycle

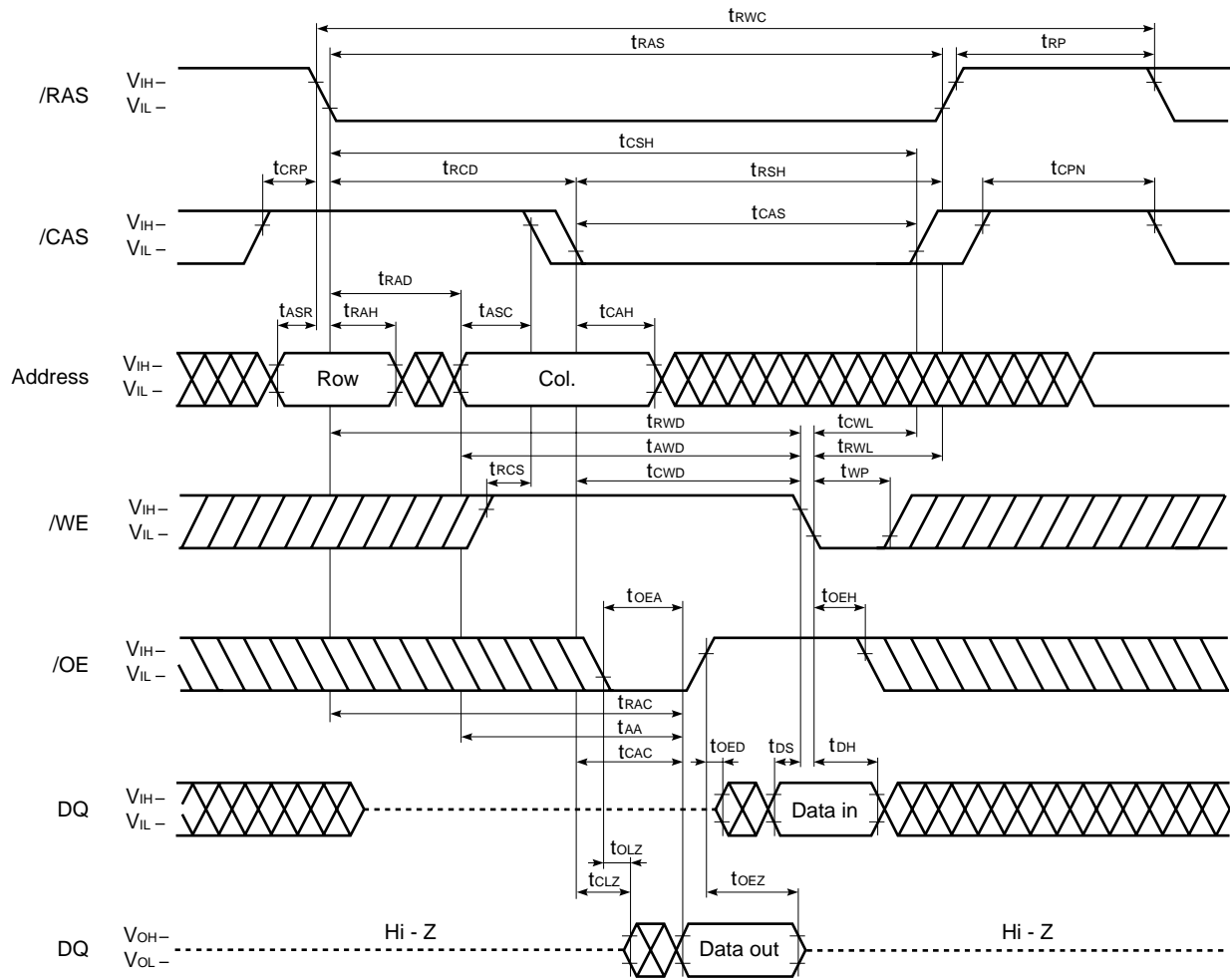


Remark /OE : Don't care

Late Write Cycle

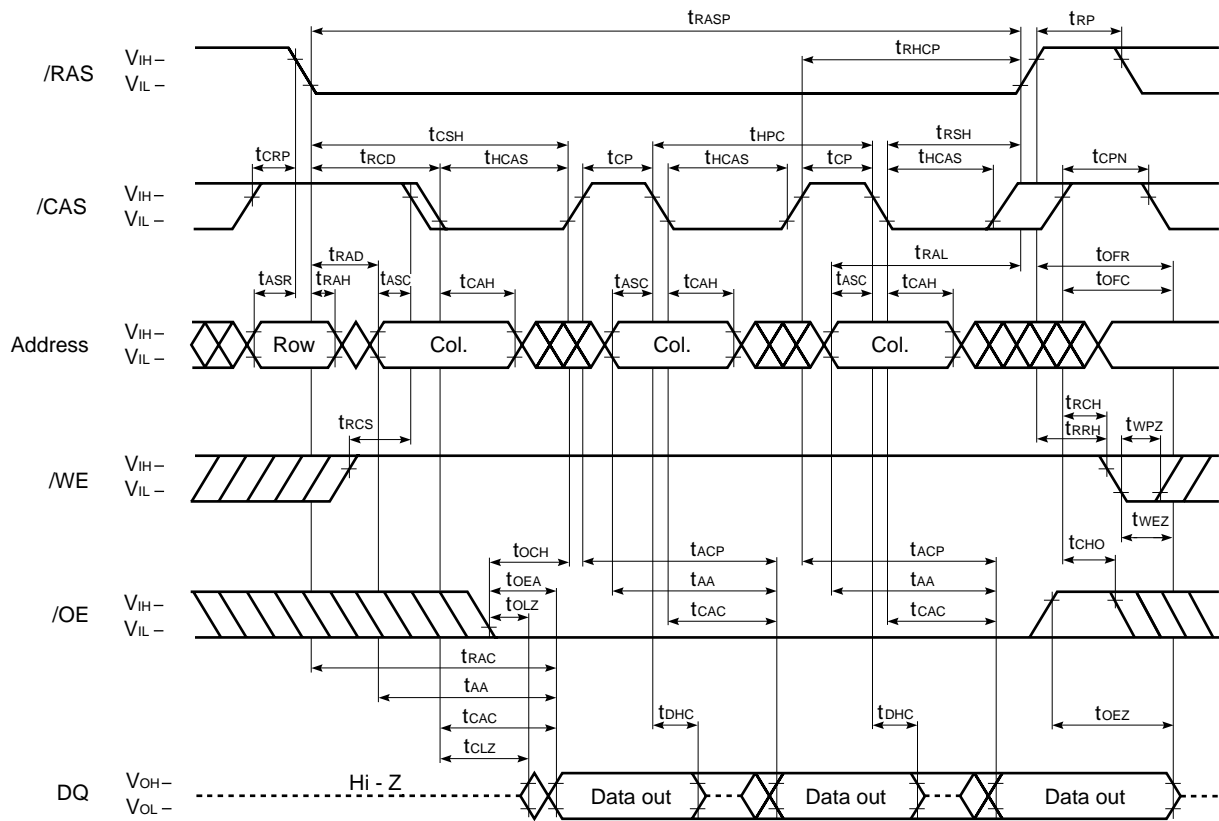


Read Modify Write Cycle



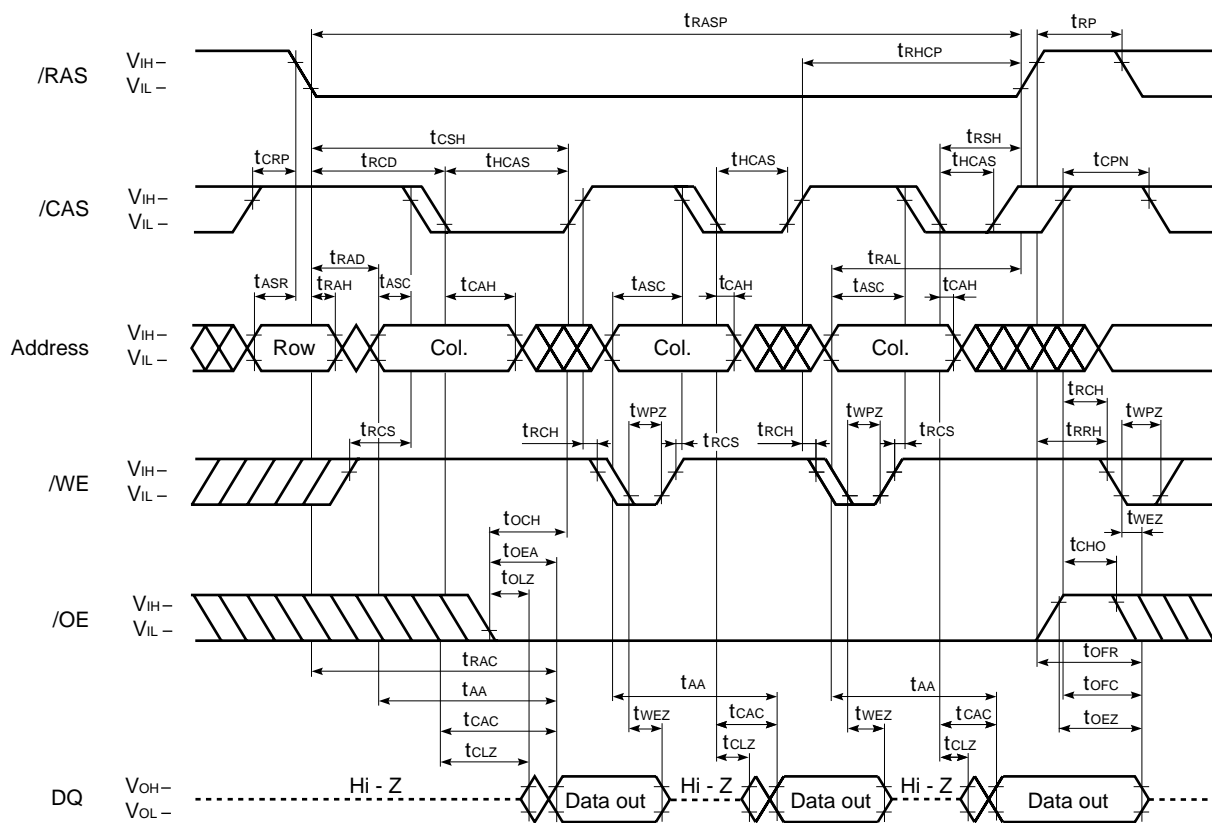


**Hyper Page Mode (EDO) Read Cycle**



**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

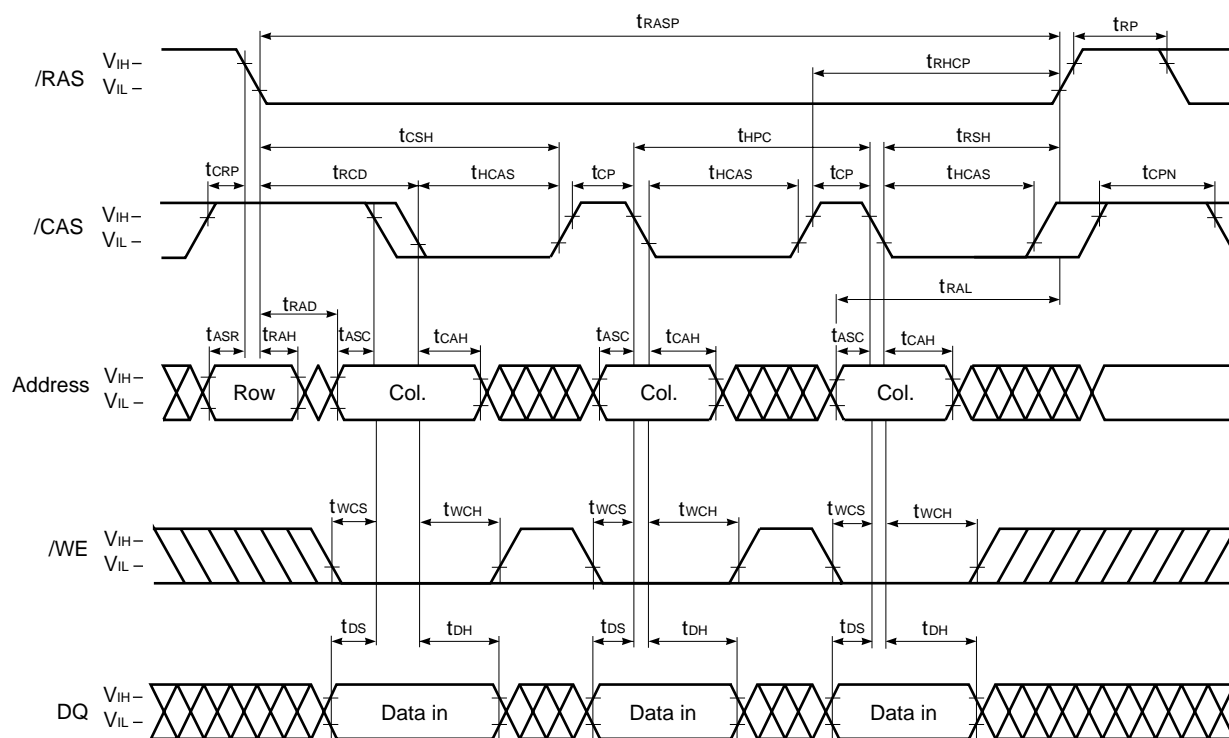
Hyper Page Mode (EDO) Read Cycle (/WE Control)



**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.



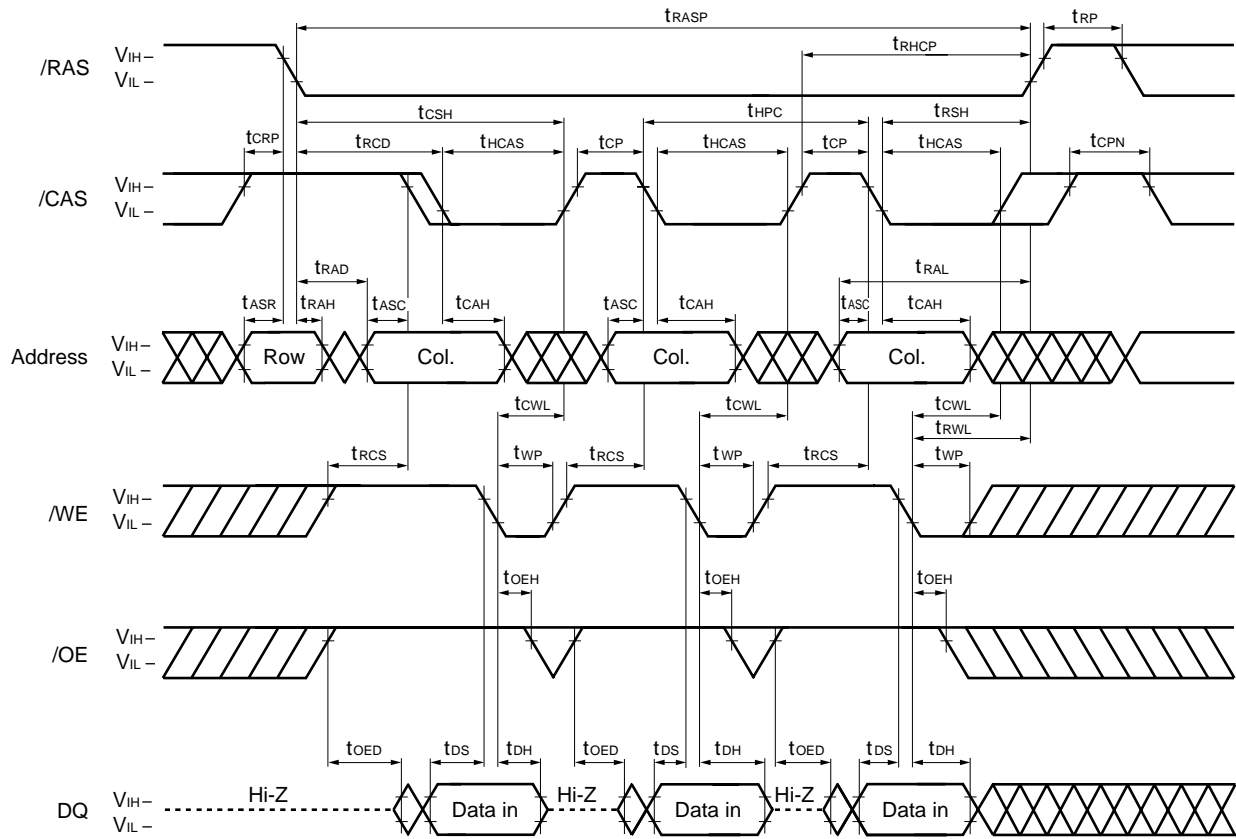
Hyper Page Mode (EDO) Early Write Cycle



Remarks 1. /OE : Don't care

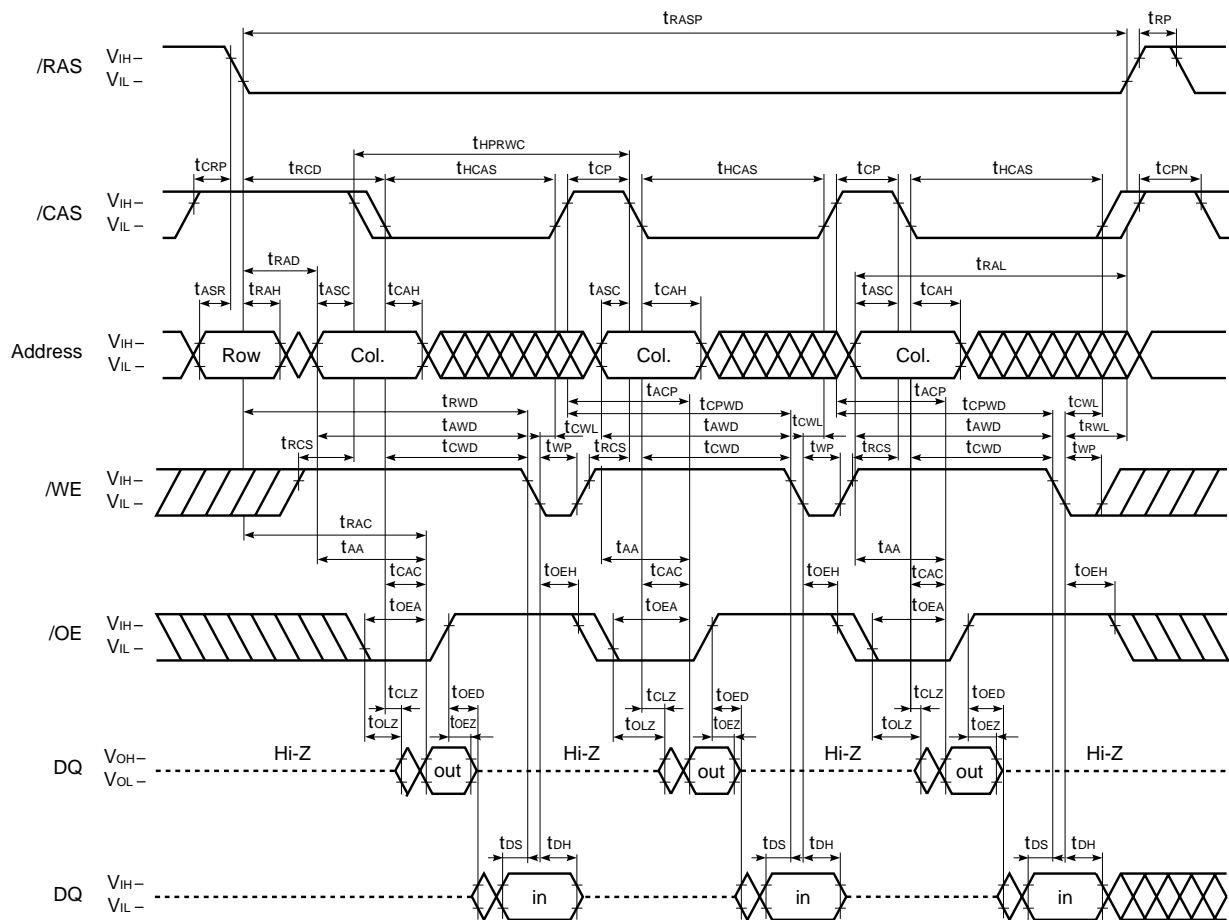
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

Hyper Page Mode (EDO) Late Write Cycle



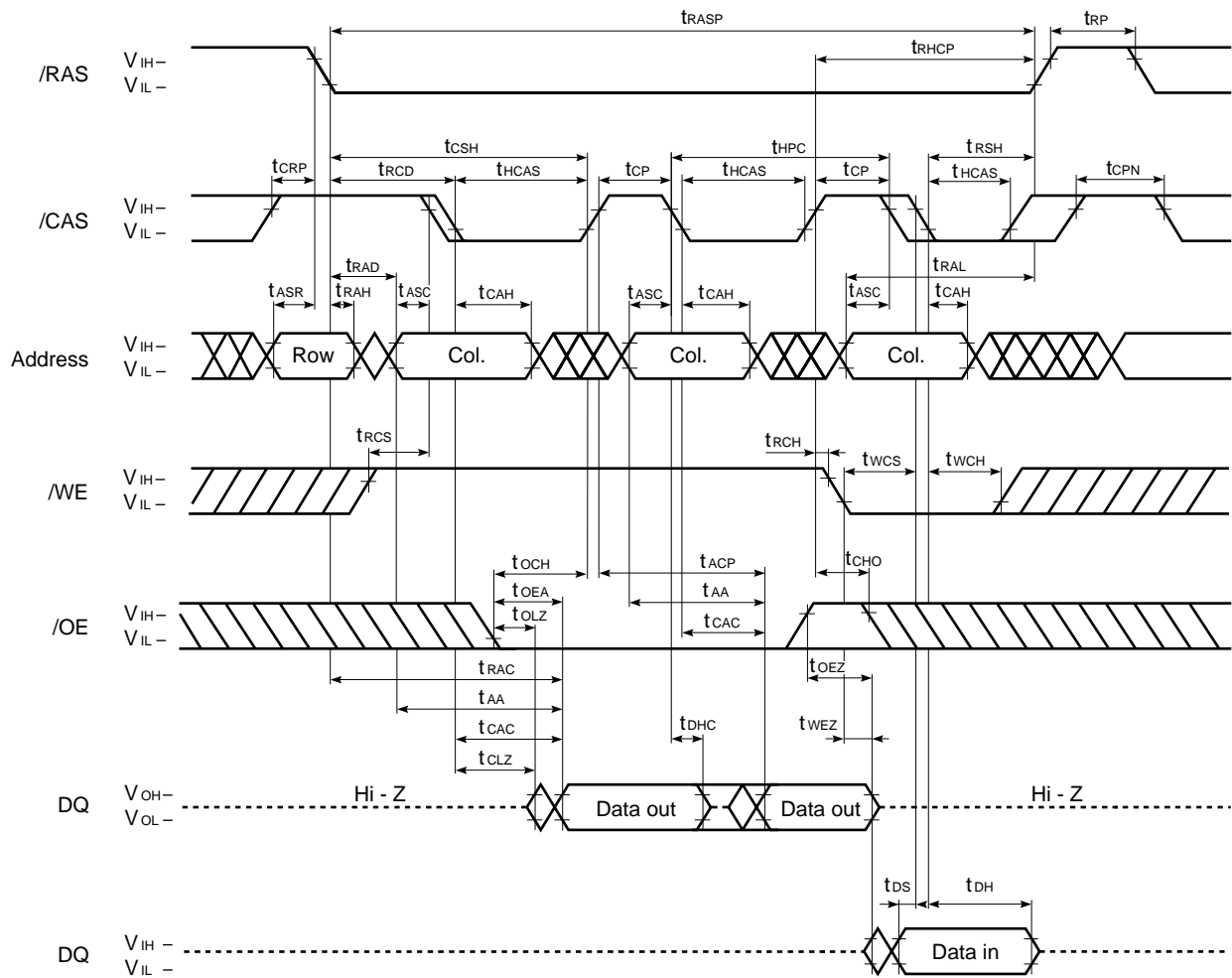
**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

Hyper Page Mode (EDO) Read Modify Write Cycle



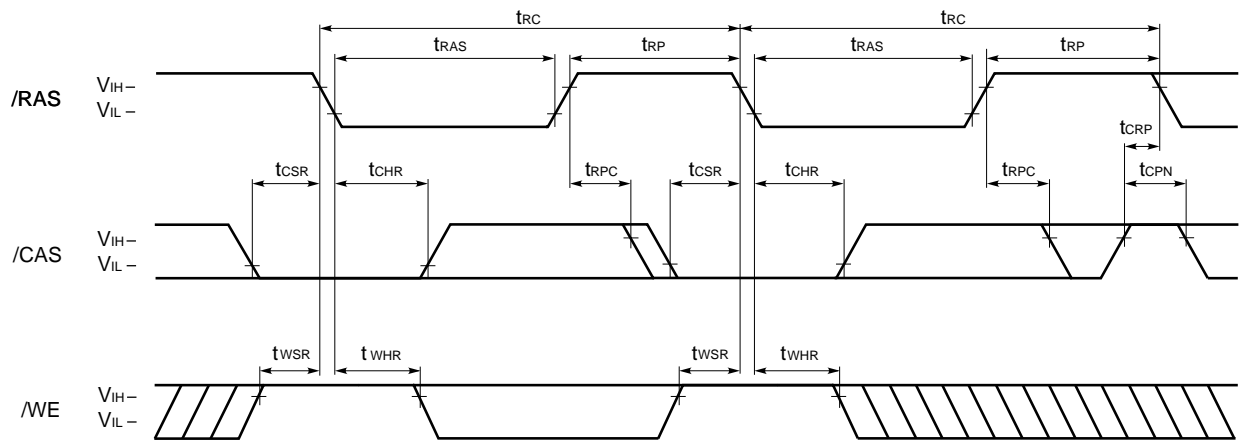
**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

Hyper Page Mode (EDO) Read and Write Cycle



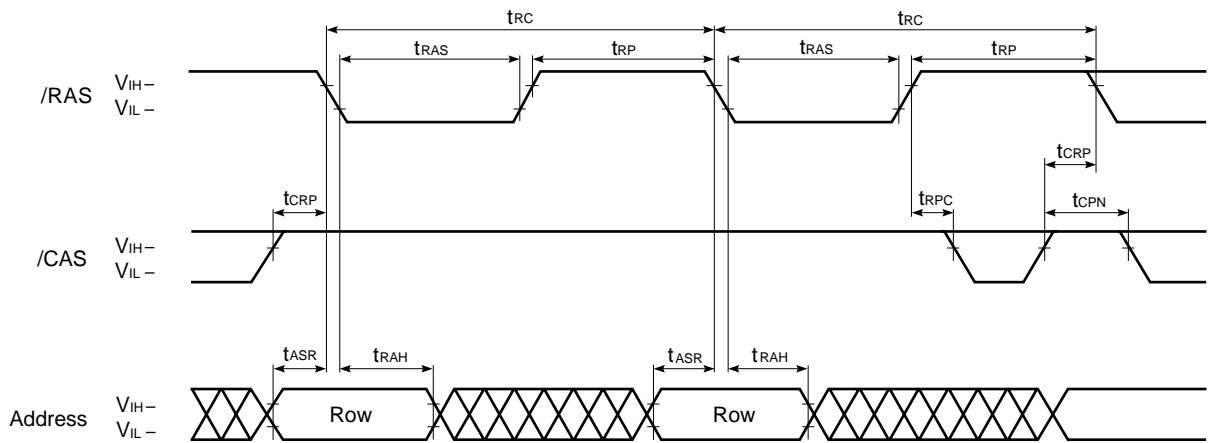
**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive /CAS cycles within the same /RAS cycle.

**/CAS Before /RAS Refresh Cycle**



**Remark** Address, /OE : Don't care DQ : Hi-Z

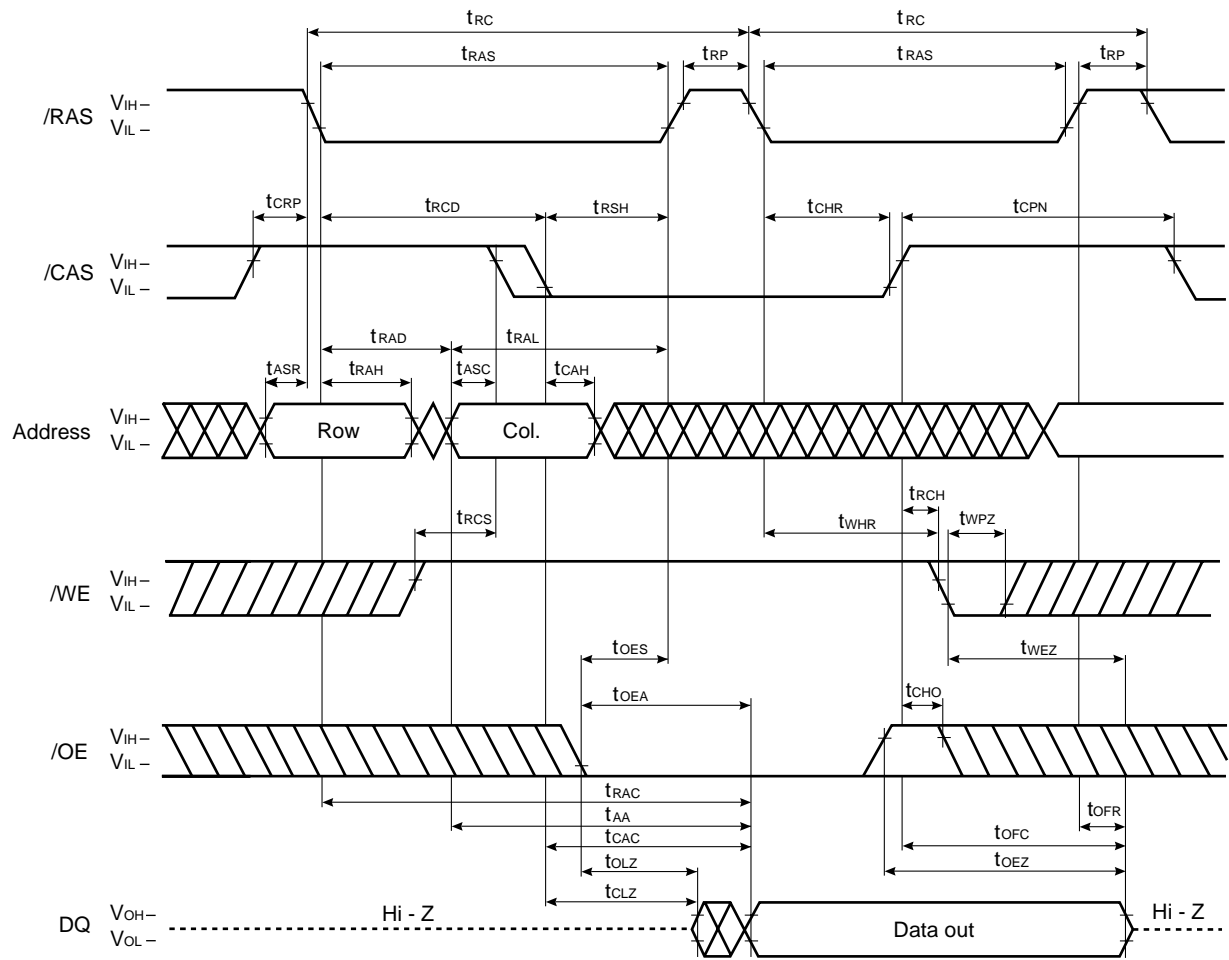
**/RAS Only Refresh Cycle**



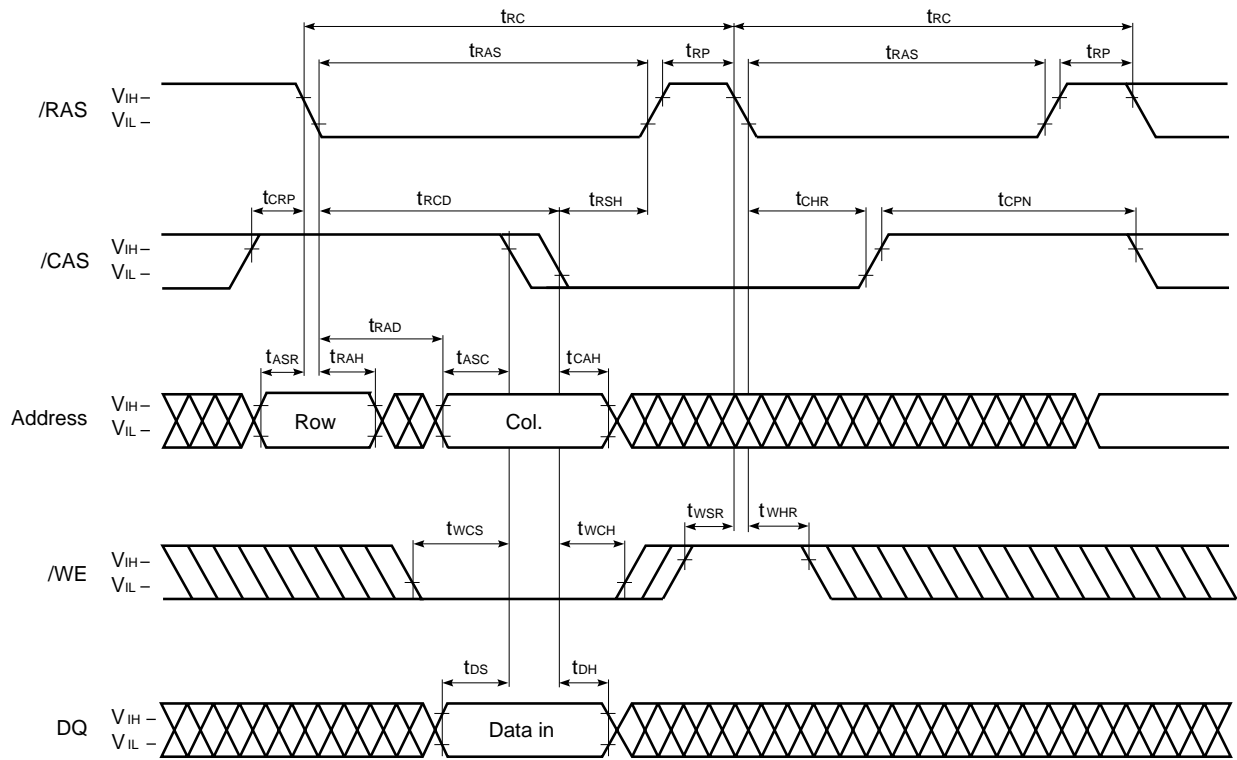
**Remark** /WE, /OE : Don't care DQ : Hi-Z



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)

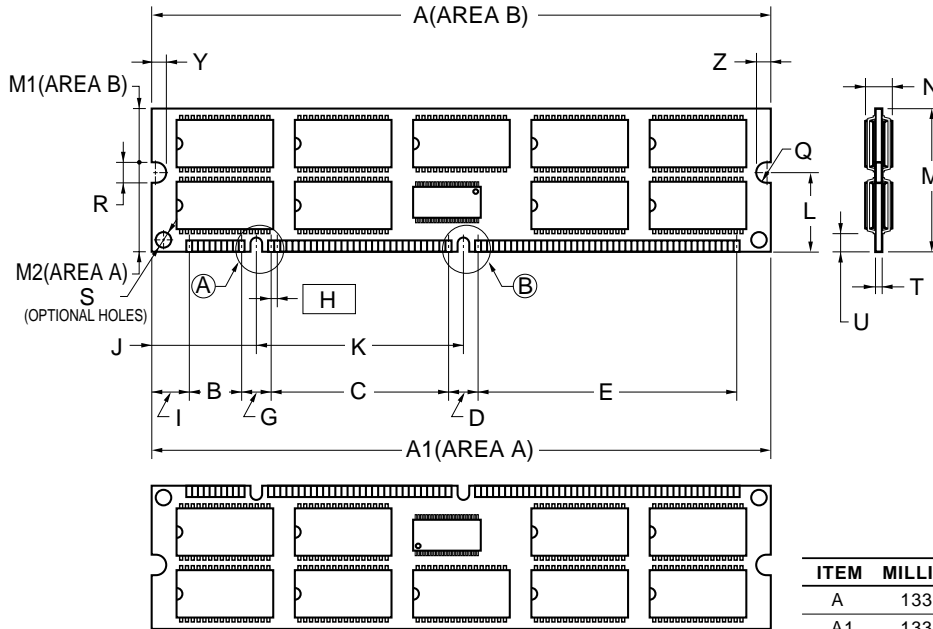


Remark /OE : Don't care

★ Package Drawings

[ MC-4216LFC72FH ]

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)

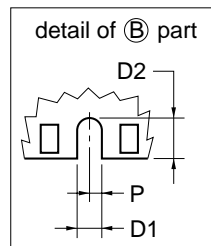
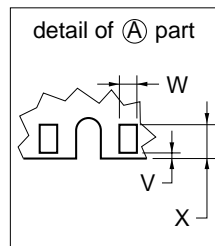
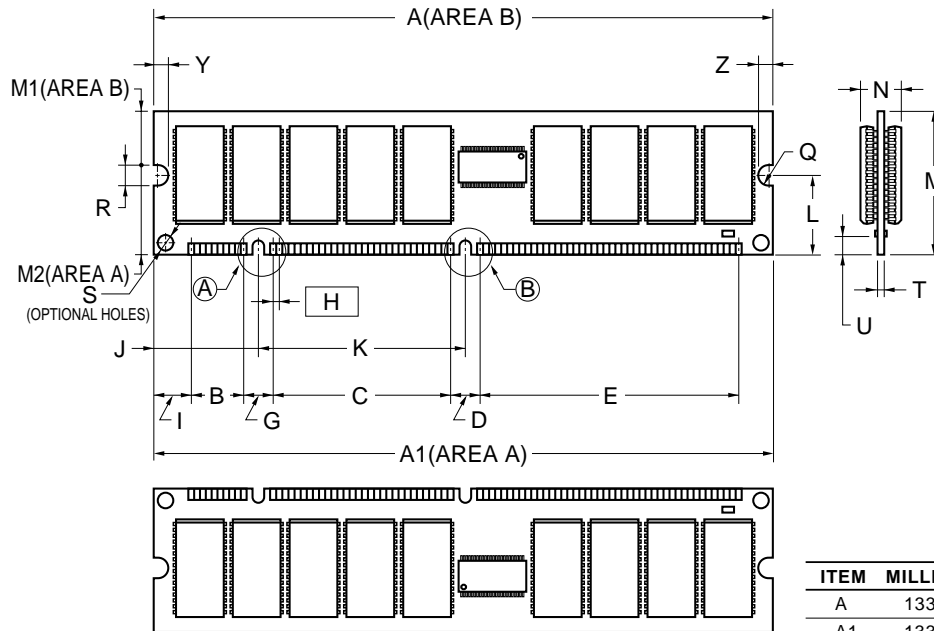


ITEM	MILLIMETERS	INCHES
A	133.35	5.250
A1	133.35±0.13	5.250±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
M	31.75±0.13	1.250±0.006
M1	11.97	0.471
M2	19.78	0.779
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.00±0.10	0.157 <sup>+0.005</sup> <sub>-0.004</sub>
S	∅3.0	∅0.118
T	1.27±0.1	0.050±0.004
U	4.00 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 <sup>+0.003</sup> <sub>-0.002</sub>
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A51

[ MC-4216LFC72FB ]

168 PIN DUAL IN-LINE MODULE (SOKET TYPE)



ITEM	MILLIMETERS	INCHES
A	133.35	5.250
A1	133.35±0.13	5.250±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	23.495	0.925
K	43.18	1.700
L	17.78	0.700
M	31.75±0.13	1.250±0.006
M1	11.97	0.471
M2	19.78	0.779
N	9.0 MAX.	0.355 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.00±0.10	0.157 <sup>+0.005</sup> <sub>-0.004</sub>
S	∅3.0	∅0.118
T	1.27±0.1	0.050±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	0.039 <sup>+0.003</sup> <sub>-0.002</sub>
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M168S-50A15-1

[ MEMO ]

[ MEMO ]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

**CAUTION FOR HANDLING MEMORY MODULES**

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.