MCD212 Video Decoder and System Controller

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Advance Information

MCD212

Video Decoder and System Controller (with JTAG)

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MCD212/D

MCD212: Video Decoder and System Controller
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1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Video Decoder and System Controller with JTAG (VDSC/JTAG) is a CMOS device integrating a 680X0 family system controller and video graphics decoder, see Figure 1–1 below.

The MCD212 is a programmable, multi–scan video device that can function as either a master or a slave. It is functionally equivalent to the MCD211 with the addition of JTAG testing. The MCD212 is a drop–in replacement for the MCD211 if the JTAG functionality is not required. It can directly drive up to 5M bytes[1] of memory and provides chip–select signals for system ROM and peripherals. The on–chip DRAM controller can support up to 4M bytes DRAM and controls access to the unspecialized System or Video DRAM. The CPU can access any memory location, even during active video display lines, thereby boosting system performance.

The video image is made up of four separate video planes: the cursor, two graphics planes (A and B), and one background plane. The video decoder receives two independent video channels from the Video DRAM. Each channel has a real–time file decoder permitting the display of normal, run–length, and mosaic compressed files. The resulting files can contain DYUV, CLUT, or direct RGB data. After decoding the resulting planes, A and B can be combined with a cursor and background allowing for visual effects like dissolves, mosaics, partial updates, etc., under software control. The resulting display is available in Red, Green, and Blue components, each being eight bits in length. The display resolution is programmable up to 768 x 560.

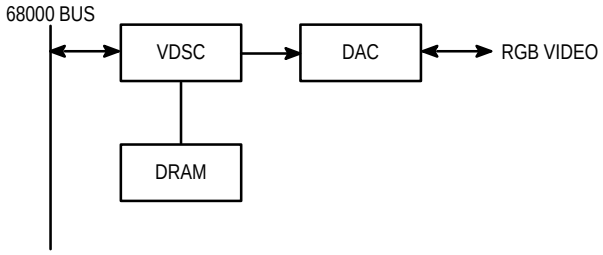


Figure 1–1. System Block Diagram

1. In this document a word is defined as 16 bits and a long–word as 32 bits.
Hexadecimal figures are indicated by an h in front.

1.2 FEATURES

System Interface:

- Direct Interface for 680X0 Bus Compatible Devices
- 1M Byte ROM Control
- 1K Byte I/O Control
- Reset Sequencer, Including ROM Shadowing
- Watchdog Timer

DRAM Interface:

- 4M Byte DRAM Direct Drive
- 256K x 4, 1M x 4, and 256K x 16 DRAM Types Can be Used

Video Interface:

- Up to 768 x 560 Screen Resolution
- Capability to Display Run–length Coded Files
- Mosaic Effect
- 256–entry Color Look Up Table (CLUT)
- Two Delta YUV Decoders
- Cursor Shape, Color, and Blink Control
- Overlaying of Four Video Planes
- Special Effects via Weight Control, Priority Control, etc.
- Dynamic Programmable Registers and CLUT Reload in Retrace Period
- Digital RGB Output (8 Bits per Component)
- Synchro Generator for 50 and 60 Hz Scan
- Synchronization with External Video

General:

- CMOS Technology
- 160–pin Quad Flat Pack Plastic Package

1.3 BLOCK DIAGRAM

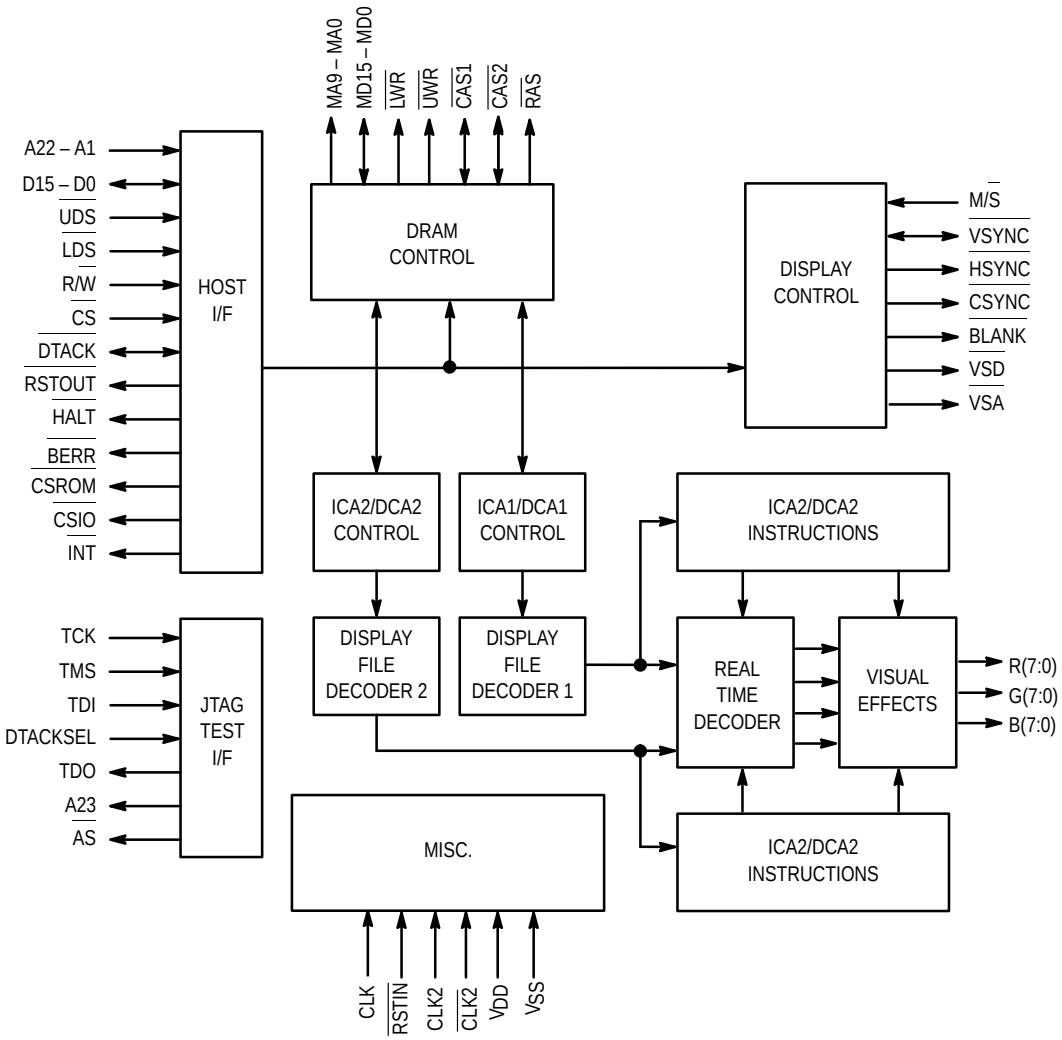


Figure 1–2. Internal Block Diagram

1.4 DIFFERENCES BETWEEN THE MCD211 AND THE MCD212

There are two differences between the parts:

1. JTAG testing has been added for automated board testing. The additional pins required to do this were V_{SS} pins on the MCD211. Hence, the MCD212 can be put in place of an MCD211 and will function identically. The functionality of the R/W, LDS, UDS, A1 – A22, RAS pins have been enhanced. (See Chapter 2 for the names of the new pins and the changes in functionality.)
2. Also, the processor interface timing has been improved to allow operation with higher speed processors. This is detailed in Section 11.3.

2
PIN DESCRIPTION

2.1 INTRODUCTION

“Active” and “inactive” or “asserted” and “negated” are referred to in this user manual independent of whether the signal is active in the high (logic 1) state or the low (logic 0) state. The definition of the active level of each signal may be found in the individual pin descriptions.

2.2 PIN FUNCTION DESCRIPTION

2.2.1 System Interface

Mnemonic	Type	Name and Function
A1 – A22	I	System address lines. Provides address for access from the system bus. Must be stable when UDS and/or LDS are asserted.
D0 – D15	I/O	Bidirectional data bus, three–state. Used to transfer DATA between system bus and VDSC. Must be stable when UDS or LDS is asserted during write access. Driven by VDSC during read cycles. D0 is the least significant bit.
$\overline{\text{UDS}}$	I	Upper Data Strobe. Active low. When asserted, $\overline{\text{UDS}}$ indicates that data is being addressed on D8 to D15.
$\overline{\text{LDS}}$	I	Lower Data Strobe. Active low. When asserted, $\overline{\text{LDS}}$ indicates that data is being addressed on D0 to D7.
R/$\overline{\text{W}}$	I	Read/Write. This input indicates transfer on the system bus. When low, indicates data is to be written into VDSC controlled resources or internal registers. When high, indicates a read is taking place.
$\overline{\text{CS}}$	I	Chip Select. Active low. When asserted, indicates data transfer between system bus and VDSC controlled resources is enabled. Validates address decode for system access.
$\overline{\text{DTACK}}$	I/O	Data Transfer Acknowledge signal. Active low, three–state. Asserted by VDSC when the system bus cycle, concerning VDSC controlled resources, can be continued. This pin must be pulled up externally.
$\overline{\text{RSTOUT}}$	O	Reset output. Active low, open drain. Asserted by the VDSC reset sequencer during the reset procedure. This pin must be pulled up externally.
$\overline{\text{HALT}}$	O	Halt line output. Active low, open drain. Asserted by the VDSC reset sequencer during the reset procedure. This pin must be pulled up externally.
$\overline{\text{BERR}}$	O	Bus Error output. Active low, three–state. Asserted, when enabled, by the VDSC watchdog timer circuit if UDS or LDS is still asserted at the end of the time–out period. This pin must be pulled up externally.

$\overline{\text{CSROM}}$	O	Chip Select ROM output. Active low. Asserted by an access on the system bus in the ROM address area, and when UDS and/or LDS are asserted.
$\overline{\text{CSIO}}$	O	Chip Select I/O output. Active low. Asserted by an access on the system bus in the I/O area, and when UDS and/or LDS are asserted.
$\overline{\text{INT}}$	O	Interrupt request output. Active low, three–state. Used to generate interrupts to the CPU. This pin must be pulled up externally.

2.2.2 Dynamic RAM Interface

Mnemonic	Type	Name and Function
MA0 – MA9	O	Memory Address lines. Multiplexed row/column address line outputs for DRAM control.
MD0 – MD15	I/O	Bidirectional Memory Data bus, three–state. Used to transfer data between DRAM bus and VDSC. Stable when LWR and/or UWR is asserted during a write cycle. Driven by VDSC during read cycles. MD0 is the least significant bit.
$\overline{\text{RAS}}$	O	Row Address Strobe. Active low. Validates the DRAM row address on the falling edge.
$\overline{\text{CAS1}}$	I/O	Column Address Strobe for memory bank 1. Active low, three–state. Validates the DRAM column address on the falling edge. Input during reset sequence to select/deselect memory bank 1. Active high validates bank inputs.
$\overline{\text{CAS2}}$	I/O	Column Address Strobe for memory bank 2. Active low, three–state. Validates the DRAM column address on the falling edge. Input during reset sequence to select/deselect memory bank 2. Active high validates bank inputs.
$\overline{\text{UWR}}$	O	Write signal for DRAM. Active low. It is asserted when writing MD8 – MD15 to the DRAM.
$\overline{\text{LWR}}$	O	Write signal for DRAM. Active low. It is asserted when writing MD0 – MD7 to the DRAM.

2.2.3 Video Interface

Mnemonic	Type	Name and Function
R0 – R7	O	Red color output (R7 = MSB, R0 = LSB). Three–state.
G0 – G7	O	Green color output (G7 = MSB, G0 = LSB). Three–state.
B0 – B7	O	Blue color output (B7 = MSB, B0 = LSB). Three–state.
OE	I	Output Enable. Active high. It disables three–state of RGB output.
$\overline{\text{VSYNC}}$	I/O	Vertical Synchronization. Active low. In master mode, this output is used as vertical synchronization signal for monitor. In slave TV mode it becomes a vertical synchronization input.
$\overline{\text{HSYNC}}$	O	Horizontal Synchronization. Active low. This output is used as a horizontal synchronization signal.
$\overline{\text{CSYNC}}$	O	Composite synchronization. Active low. This output is used as a composite synchronization signal.

$\overline{\text{BLANK}}$	O	Blanking output. Active low. It is asserted during vertical and horizontal blanking periods and high the rest of the time.
$\overline{\text{VSD}}$	O	Video Select for digital video. Active low. This signal is synchronous to the digital video output.
$\overline{\text{VSA}}$	O	Video Select for analog video. Active low. This signal is a CLK2 clock cycle delayed version of VSD and synchronous to analog video after clocked D/A conversion.
M/$\overline{\text{S}}$	I	Master/Slave TV mode selection. When high, the VDSC generates the video timing. When low the vertical synchronization can be slaved to an external video timing.

2.2.4 JTAG Test Signals

Mnemonic	Type	Name and Function
TCK	I	JTAG Test Clock input. Provides the clock for the test logic defined by IEEE Std. 1149.1–1990. 100 kΩ internal pull–up.
TMS	I	JTAG Test Mode Select input. The signal decoded by the TAP controller to control test operations, defined by IEEE Std. 1149.1–1990. 100 kΩ internal pull–up.
TDI	I	JTAG Test Data input. Pin at which serial test instructions and data are received by the test logic, defined by IEEE Std. 1149.1–1990. 100 kΩ internal pull–up.
TDO	OT	JTAG Test Data output. Three–state. Serial output for test instructions and data from the test logic defined by IEEE Std. 1149.1–1990.
A23	OT	System Address line (three–stated in functional mode). During JTAG EXTEST, A23 may drive system address line A23 off–chip.
$\overline{\text{AS}}$	OT	System Address strobe (three–stated in functional mode). During JTAG EXTEST, AS may drive the system address strobe line AS off–chip.
DTACKSEL	I	Selects advance time of the falling edge of DTACK before data (read) is valid on pins D0 – D15. For designs using 68000/68070–16 or 68340/341–16 series processors, tie DTACKSEL low; for 68340/341–25 designs, tie DTACKSEL high.

2.2.5 Miscellaneous Signals

Mnemonic	Type	Name and Function
CLK	I	External clock input.
$\overline{\text{RSTIN}}$	I	Reset input. Active low. Schmitt trigger. Initiates a reset sequence.
CLK2	O	CLK/2 clock output. Frequency is CLK frequency divided by 2.
$\overline{\text{CLK2}}$	O	CLK/2 clock output. Frequency is CLK frequency divided by 2. Inverse of CLK2.
V_{DD}	I	Power supply pins (5 V).
V_{SS}	I	Power and signal ground pins.

NOTE: All the pins are TTL compatible, except for CLK and $\overline{\text{RSTIN}}$, which use CMOS levels.

2.3 PIN TYPES

CMOS input	:CLK
CMOS Schmitt input	:$\overline{\text{RSTIN}}$
TTL input	:all inputs except CLK, $\overline{\text{RSTIN}}$
6 mA output	:D0 – D15, $\overline{\text{RSTOUT}}$, $\overline{\text{HALT}}$, $\overline{\text{BERR}}$, $\overline{\text{INT}}$, MD0 – MD15, MA0 – MA9, $\overline{\text{LWR}}$, $\overline{\text{UWR}}$, R0 – R7, G0 – G7, B0 – B7, $\overline{\text{BLANK}}$, CSYNC, HSYNC, VSYNC, VSD, CLK2, $\overline{\text{CLK2}}$
12 mA output	:$\overline{\text{CSIO}}$, $\overline{\text{CSROM}}$
16 mA output	:$\overline{\text{RAS}}$, $\overline{\text{CAS1}}$, $\overline{\text{CAS2}}$

3
SYSTEM CONTROL

The VDSC performs several 680X0 system control functions.

3.1 RESET AND HALT GENERATION

When the $\overline{\text{RSTIN}}$ pin is released, the timing chain counts eight video frames (= 8 x 312 x 112 x 16 CLK cycles) in the default internal configuration at power on before the RSTOUT (reset output) pin is released, i.e., 160 ms with a 28 MHz crystal, 150 ms with a 30 MHz crystal, or 148 ms with a 30.2097 MHz crystal. The HALT pin is released one video line later. At RESET, VDSC registers are configured in the state indicated in Section 3.2.

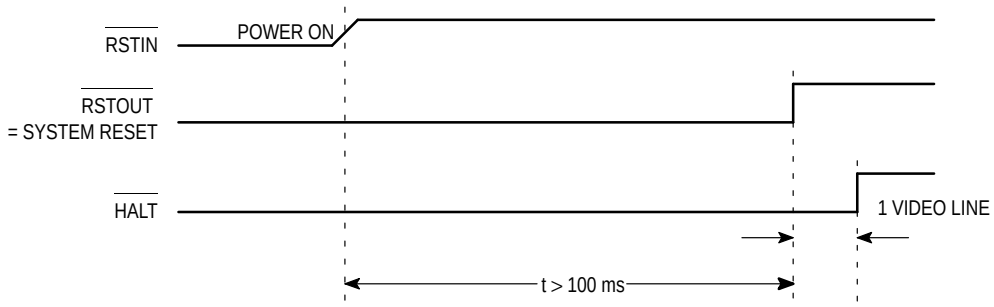


Figure 3–1. Reset and Halt Timing Chart

3.2 RESET MECHANISM

The following bits in these control registers are reset by the $\overline{\text{RESET}}$ input:

Image Coding Method Register: (hCO): bits 0, 1, 2, 3, 8, 9, 10, 11, 18 (plane A and B off, external video disabled)

Cursor Control Register: (hCE): bit 23 (cursor disabled)

Background Color Register: (hD8): bits 0, 1, 2, 3 (black backdrop)

The following bits in internal registers are reset by the $\overline{\text{RESET}}$ input:

CSR1W: DI1, DD1, DD2, TD, DD, ST, BE

CSR2W: DI2

DCR1: DE, CF, FD, SM, CM1, IC1, DC1

DCR2: CM2, IC2, DC2

DDR1: MF1, MF2, FT1, FT2

DDR2: MF1, MF2, FT1, FT2

The result of a reset will be a constant black level at the RGB outputs and no video synchronization output.

The active low reset pin must be connected to the system reset signal. The $\overline{\text{RSTIN}}$ also has an effect on the clock output CLK2 (see Figure 3–2). Two different waveforms for CLK2 are possible. It can be seen that CLK2 is present during and after reset.

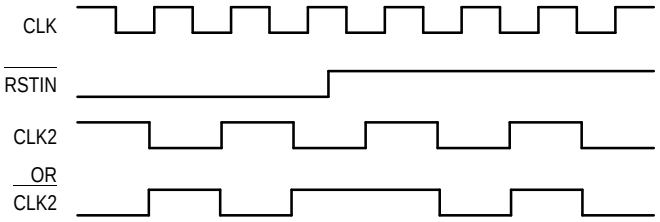


Figure 3–2. CLK2 Clocking and Resetting

CLK2 is clocked by the positive edge of CLK. Its phase after reset is related to the rising edge of RSTIN. CLK2 is always the inverse of CLK2.

3.3 VDSC INITIALIZATION SEQUENCE

In order to have a proper start–up, register CSR1W must be initialized to the DRAM used. Display and control data must be loaded in DRAM.

Register DCR1 must be initialized to the required display mode at a rising edge of the DA–bit (CSR1R register). At a falling edge of the DA–bit (CSR1R register), the DE–bit (DCR1 register) must be set. Now video synchronization is generated. On the next rising edge of the DA–bit, the IC1 bit (DCR1 register) and IC2–bit (DCR2 register) must be set and on the next falling edge of the DA–bit the DC1–bit (DCR1 register) and DC2–bit (DCR2 register) must be set. Now the RGB outputs will generate a picture.

3.4 MEMORY SWAPPING

After $\overline{\text{RSTIN}}$ is released the first four 680X0 word accesses are counted. If $\overline{\text{CS}}$ is asserted at such a word access, a chip select to the ROM is given.

The 680X0 first four accesses correspond to the SSP (System Stack Pointer) and the PC (Program Counter). The SSP and PC must be located at address h400000 and h400004 which are decoded during the swapping. Address h0 to h7 are normally decoded afterwards.

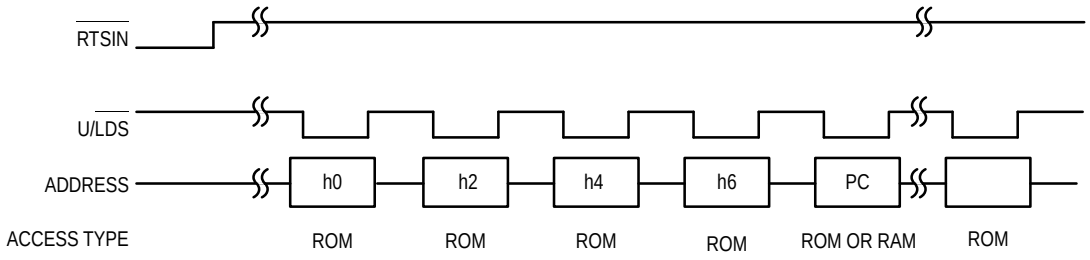


Figure 3–3. Memory Swapping Timing Chart

3.5 ADDRESS DECODING

The VDSC is connected to the system bus via 22 address lines and upper and lower data strobes. The address decoding is validated by CS.

Table 3–1. Address Map

h000000 – h3FFFFF	DRAM (4M byte)
h400000 – h4FFBFF	System ROM (1M byte)
h4FFC00 – h4FFFDF	System I/O (1K byte)
h4FFFE0 – h4FFFEF	Channel 2 internal registers
h4FFFF0 – h4FFFFF	Channel 1 internal registers

NOTE: The system ROM decoding asserts the $\overline{\text{CSROM}}$ pin that is not sensitive to the R/W signal. This allows the use of static RAM in the ROM mapping area. The system I/O decoding asserts the CSIO pin.

3.6 DATA ACKNOWLEDGE GENERATION

A data transfer is initiated by an upper and/or lower data strobe (U/$\overline{\text{LDS}}$) from the system. A data transfer is acknowledged by the VDSC via DTACK. A data transfer is terminated by U/LDS becoming inactive followed by DTACK becoming inactive.

The VDSC generates the data acknowledge ($\overline{\text{DTACK}}$) depending on the addressed area:

- Access to the DRAM is acknowledged as soon as it is certain that data can be read or written by the system.
- Access to the system ROM is acknowledged after a programmable number of clock or CLK cycles. The DTACK delay is controlled by Control Register CSR1W.

If U/$\overline{\text{LDS}}$ becomes inactive before $\overline{\text{DTACK}}$ is generated by the VDSC, $\overline{\text{DTACK}}$ will not be generated.

Table 3–2. $\overline{\text{DTACK}}$ Delay for ROM

DD	DD1	DD2	CLK Cycles
0	x	x	11 ≥ 12
1	0	0	3 ≥ 4
1	0	1	5 ≥ 6
1	1	0	7 ≥ 8
1	1	1	9 ≥ 10

NOTE: Access to the SYSTEM I/O device (CSIO pin) is not acknowledged by the VDSC but by the addressed device.

3.7 BUS ERROR GENERATION

The $\overline{\text{BERR}}$ signal is asserted if enabled by writing a 1 in the BE (bus error) bit of the control register CSR1W and if a data transfer is not acknowledged for at least one entire video line (approximately 64 μs) after selection. The BE flag bit is then set in the CSR2R register. The $\overline{\text{BERR}}$ pin is released as soon as the CPU releases UDS and LDS. The BE flag is reset when the CPU reads the CSR2R status register.

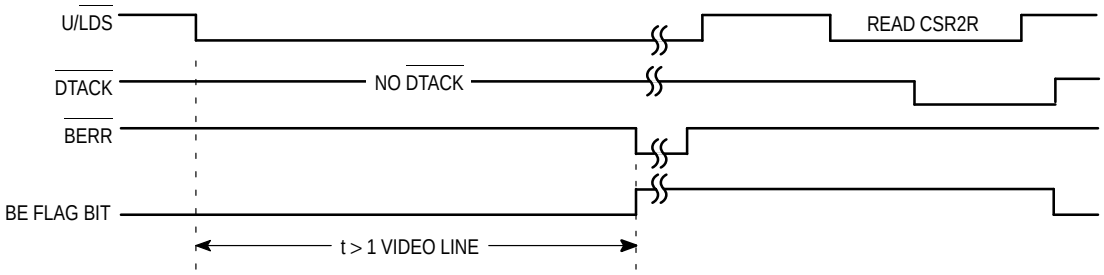


Figure 3–4. Bus Error Timing

3.8 INTERRUPT GENERATION

The VDSC can generate interrupts to the CPU by asserting its $\overline{\text{INT}}$ pin. The following conditions can generate an interrupt:

- The ICA1/DCA1 controller fetches an interrupt instruction. Then, the IT1 bit of the CSR2R register is set. If the DI1 bit in the CSR1W register is reset to 0, the IT1 bit of the CSR2R register can generate an interrupt on the $\overline{\text{INT}}$ pin.
- The ICA2/DCA2 controller fetches an interrupt instruction. Then, the IT2 bit of the CSR2R register is set. If the DI2 bit in the CSR2W register is reset to 0, the IT2 bit of the CSR2R register can generate an interrupt on the $\overline{\text{INT}}$ pin.

$$\overline{\text{INT}} = \text{not}((\text{not}(DI1) \text{ and } IT1) \text{ or } (\text{not}(DI2) \text{ and } IT2))$$

The IT1 bit and IT2 bit are reset after the CPU reads the CSR2R register. The $\overline{\text{INT}}$ pin is inactive when both IT1 and IT2 are reset (see equation above).

4
DRAM CONTROL

The VDSC has an on–chip dynamic RAM (DRAM) controller. It supports several DRAM configurations and performs DRAM arbitration, address multiplexing, timing generation, and refresh.

4.1 DRAM CONFIGURATION

The DRAM types the VDSC can drive are 256K x 4, 1M x 4 and 256K x 16. They always form a 16–bit data bus. The devices can be configured in one or two banks. Six configurations are possible:

- 4 Devices 256K x 4 (512K byte)
- 8 Devices 256K x 4 (1M byte)
- 4 Devices 1M x 4 (2M byte)
- 8 Devices 1M x 4 (4M byte)
- 1 Device 256K x16 (512K byte)
- 2 Devices 256K x16 (1M byte)

The TD (type of device) bit of the CSR1W register selects either 256K x 4, 256K x 16 (TD = 0), or 1M x 4 (TD = 1) DRAM type.

The selection between one or two banks is done by fixing the $\overline{\text{CAS1}}$ and $\overline{\text{CAS2}}$ pins to a logical level during reset. $\overline{\text{CAS1}}$ corresponds to bank 1 and $\overline{\text{CAS2}}$ corresponds to bank 2. See Table 4–1 for the address map of the DRAM banks. No DTACK is generated for addresses outside a certain configuration.

Table 4–1. Address Map of the DRAM Banks

Address Range	A22	A21	A20	A19	A18	TD = 0	TD = 1
h000000 – h03FFFF	0	0	0	0	0	bank 1	bank 1
h040000 – h07FFFF	0	0	0	0	1	bank 2	bank 1
h080000 – h0BFFFF	0	0	0	1	0		bank 1
h0C0000 – h0FFFFF	0	0	0	1	1		bank 1
h100000 – h13FFFF	0	0	1	0	0		bank 2
h140000 – h17FFFF	0	0	1	0	1		bank 2
h180000 – h1BFFFF	0	0	1	1	0		bank 2
h1C0000 – h1FFFFF	0	0	1	1	1		bank 2
h200000 – h23FFFF	0	1	0	0	0	bank 1	bank 1
h240000 – h27FFFF	0	1	0	0	1	bank 2	bank 1
h280000 – h2BFFFF	0	1	0	1	0		bank 1
h2C0000 – h2FFFFF	0	1	0	1	1		bank 1
h300000 – h33FFFF	0	1	1	0	0		bank 2
h340000 – h37FFFF	0	1	1	0	1		bank 2
h380000 – h3bFFFF	0	1	1	1	0		bank 2
h3c0000 – h3FFFFF	0	1	1	1	1		bank 2

4.2 DRAM ACCESS AND ARBITRATION

The VDSC allows the DRAM to be used simultaneously as both video and system memory so that a CPU can access any location of the entire memory space even during active video display time. Additionally, the DRAM bus can be accessed by several masters and an arbitration scheme is implemented to provide each master with a guaranteed access time.

The various masters are:

- The System Bus (CPU or DMA cycles)
- Display Decoder 1
- Display Decoder 2
- ICA/DCA Controller 1
- ICA/DCA Controller 2
- The DRAM Refresh Controller

The DRAM access consists of consecutive display periods of 32 CLK cycles, which are subdivided into four slots (see Figure 4–1). The CH#1 slot is used by a video related function of channel 1 (display decoder 1 or ICA/DCA controller 1). The CH#2 slot is used by a video related function of channel 2 (display decoder 2 or ICA/DCA decoder 2). The DRAM refresh controller uses the CH#1 and CH#2 slots for RAS only refresh with two DRAM rows per slot. The system slots are available for a DRAM access from the system bus (e.g., CPU or DMA cycles) once every 16 CLK periods.

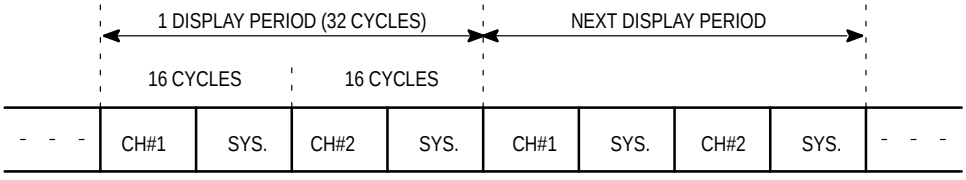
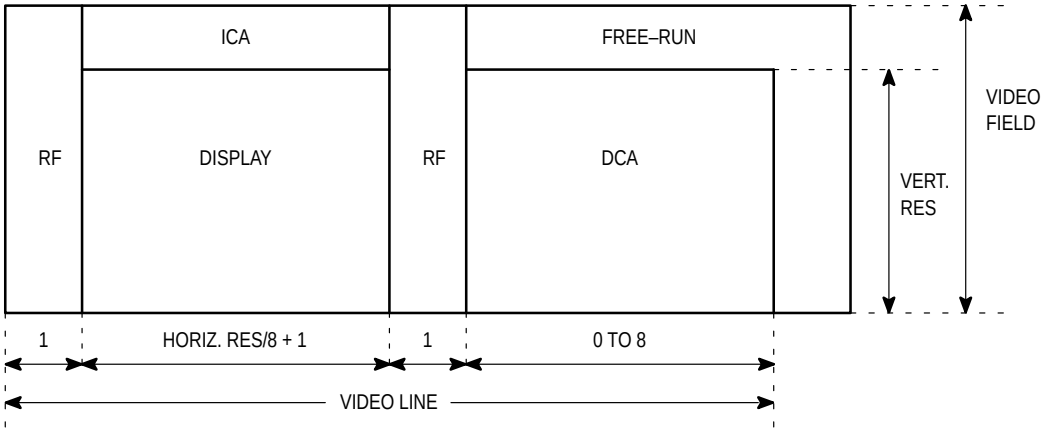


Figure 4–1. DRAM Access

Eleven CLK periods are used for accessing CH#1 or CH#2 data, as shown in Figure 4–3. This represents four DRAM accesses for data. These four 16–bit words can represent varying amounts of pixel data in plane #1 or plane #2. For example, when using RGB555 data type, the four accesses represent color information for four pixels. (NOTE: Only plane 2 is available with RGB555 data; therefore, one complete display period contains color information for eight pixels.) The remaining five CLK periods are used for one DRAM access for system data.

When no video or refresh functions are required, the access to DRAM is free–running with no display periods, so that a system bus access can be accepted at any time. Examples of this are after a stop instruction in ICA/DCA or during run–length files.

The selection between display, ICA, DCA, and refresh is done according to Figure 4–2, the time domain of a video frame.



NOTES:
1. RF is the refresh time area. Eight DRAM rows are refreshed per video line.
2. ICA and DCA only exist if enabled.
3. The free–run area starts when the ICA/DCA is completed or when an ICA/DCA stop instruction is encountered.
4. If the display is not enabled, the entire area is free–run except the refresh areas.
5. Each number is the number of display periods (32 CLK cycles).
6. Horizontal resolution is the number of pixels in normal resolution.

Figure 4–2. DRAM Cycles

Example:

The ICA time is at the beginning of each vertical field as shown in Figure 4–2. If there are no ICA instructions to execute, then this is free–run time. There is one display period when eight row addresses can be refreshed. Then, to calculate the maximum number of display periods in the display area, divide the normal resolution by 8 and add 1 (i.e., 384/8 = 48). Then there is one display period for refresh. Next is the DCA time if it has been enabled. The number of pixel periods of the DCA is programmed in the DCR register, with 8 (= 64 bytes) being the maximum. The rest of the video line time is then available as free–run time.

4.3 DRAM TIMING

The DRAM timing is based on the CLK clock (see Figure 4–3).

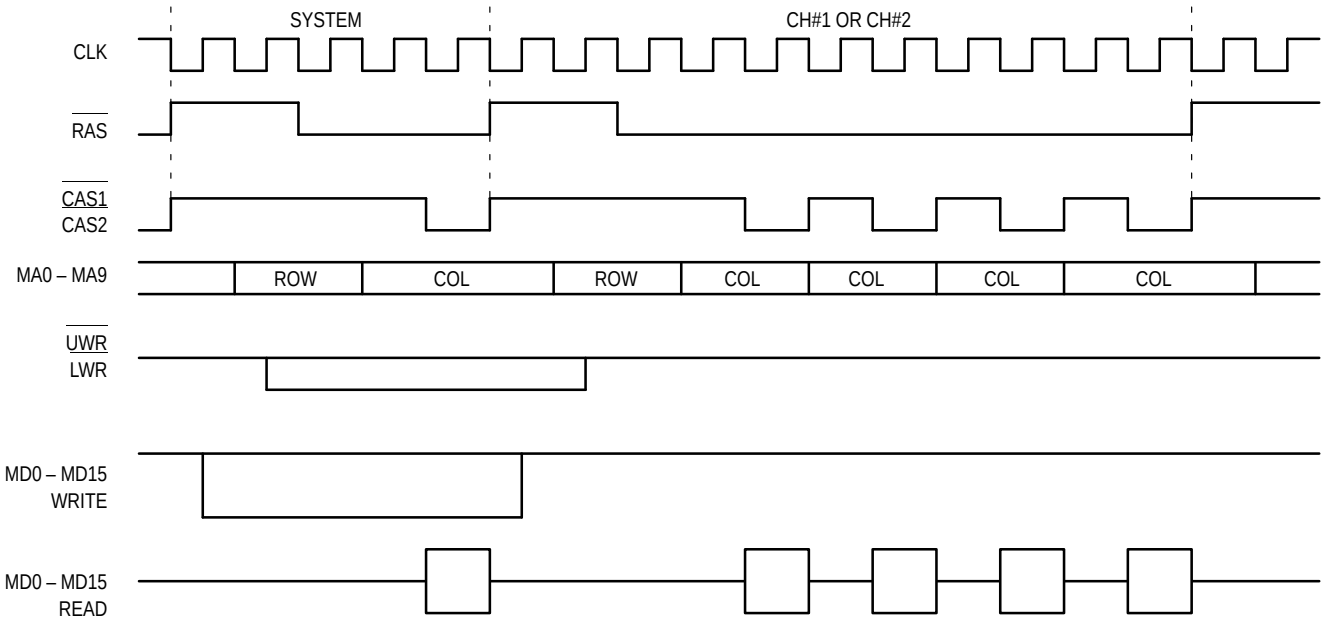


Figure 4–3. DRAM Timing

In the CH#1/CH#2 slot a burst of four words are read in fast page mode. If a page break occurs, the burst is incomplete. In the system slot a random read or write is possible.

The memory address bus (MA) is multiplexed in order to present the row address on RAS falling edge and the column address on CAS1 or CAS2 falling edge. The correspondence between memory address bus, MA0 – MA9 and system address A1 – A22 is indicated in Table 4–2. CAS1 and CAS2 function as bank select signals (see Table 4–3).

Table 4–2. Memory Address Distribution

	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9
RAS	A11	A12	A13	A14	A15	A16	A17	A18	Ax	A19
CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10

Ax = A10 for TD = 0 (256K x 4, 256K x 16)
Ax = A18 for TD = 1 (1M x 4)

Table 4–3. CAS1 and CAS2 Assertion

TD = 0	CAS1 asserted if validated and A18 = 0, A19 = 0, A20 = 0, A22 = 0 CAS2 asserted if validated and A18 = 1, A19 = 0, A20 = 0, A22 = 0
TD = 1	CAS1 asserted if validated and A20 = 0, A22 = 0 CAS2 asserted if validated and A20 = 1, A22 = 0

4.4 DRAM DESELECT

During the reset period, banks can be devalidated if their corresponding $\overline{CAS}$ pin is grounded. No DTACK is generated for devalidated banks. A pull–up is needed to validate banks.

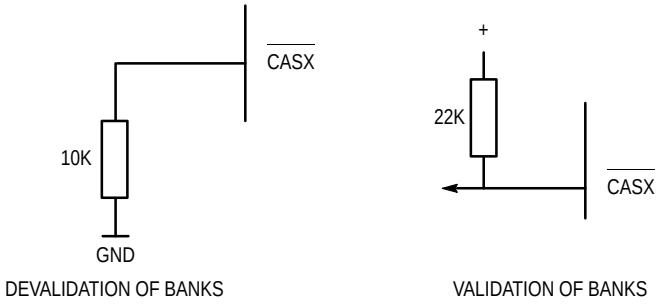


Figure 4–4. DRAM Banks Validation/Devalidation

4.5 DRAM IMPLEMENTATION

Tables 4–4 thru 4–6 show how the 256K x 4, 1M x 4, and 256K x 16 type DRAMs are connected to the VDSC.

Table 4–4. Implementing 256K x 4 DRAM

	Bank 1				Bank 2			
	DRAM 1	**DRAM 2**	**DRAM 3**	**DRAM 4**	**DRAM 5**	**DRAM 6**	**DRAM 7**	**DRAM 8**
MD0 – MD3	D0 – D3				D0 – D3			
MD4 – MD7		D0 – D3				D0 – D3		
MD8 – MD11			D0 – D3				D0 – D3	
MD12 – MD15				D0 – D3				D0 – D3
MA0 – MA8	A0 – A8	A0 – A8	A0 – A8	A0 – A8	A0 – A8	A0 – A8	A0 – A8	A0 – A8
$\overline{LWR}$	$\overline{W}$	$\overline{W}$			$\overline{W}$	$\overline{W}$		
$\overline{UWR}$			$\overline{W}$	$\overline{W}$			$\overline{W}$	$\overline{W}$
RAS	RAS	RAS	RAS	RAS	RAS	RAS	RAS	RAS
CAS1	CAS/OE	CAS/OE	CAS/OE	CAS/OE				
CAS2					CAS/OE	CAS/OE	CAS/OE	CAS/OE

Table 4–5. Implementing 1M x 4 DRAM

	Bank 1				Bank 2			
	DRAM 1	**DRAM 2**	**DRAM 3**	**DRAM 4**	**DRAM 5**	**DRAM 6**	**DRAM 7**	**DRAM 8**
MD0 – MD3	D0 – D3				D0 – D3			
MD4 – MD7		D0 – D3				D0 – D3		
MD8 – MD11			D0 – D3				D0 – D3	
MD12 – MD15				D0 – D3				D0 – D3
MA0 – MA9	A0 – A9	A0 – A9	A0 – A9	A0 – A9	A0 – A9	A0 – A9	A0 – A9	A0 – A9
LWR	W	W			W	W		
UWR			W	W			W	W
RAS	RAS	RAS	RAS	RAS	RAS	RAS	RAS	RAS
CAS1	CAS/OE	CAS/OE	CAS/OE	CAS/OE				
CAS2					CAS/OE	CAS/OE	CAS/OE	CAS/OE

Table 4–6. Implementing 256K x 16 DRAM

	Bank 1 DRAM 1	**Bank 2 DRAM 2**
MD0 – MD15	D0 – D15	D0 – D15
MA0 – MA8	A0 – A8	A0 – A8
LWR	LW	LW
UWR	UW	UW
RAS	RAS	RAS
CAS1	CAS/OE	
CAS2		CAS/OE

5
IMAGE DISPLAY CONTROL

The VDSC is programmable on a line–by–line (DCA) and/or field–by–field (ICA) basis. The image displayed by the VDSC is made up of four distinct, programmable graphics planes, as indicated in Figure 5–1. The foremost is the cursor plane, behind which are two video planes (A and B), and behind them is a background plane. The data for plane A is handled by CH#1, while CH#2 handles the B plane data. The order in which graphics planes A and B are displayed is controllable via the plane order register (hC2) through CH#1.

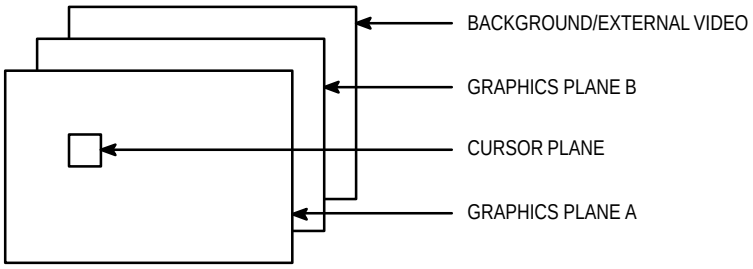


Figure 5–1. Four Video Planes of the Displayed Image

The VDSC is programmable for several pre–defined modes of display and contains two video start address registers (VSR1 and VSR2) to locate the video displays within the DRAM address space. The display logic reads words from the video display area and sends them to the display file decoder which serializes the data, either nibble per nibble or byte per byte. This programmability and flexibility allows the VDSC to do various special effects such as subscreens, windowing, mosaics, overlay and mixing, and transparency, among others.

5.1 IMAGE FORMATS

The VDSC supports NTSC monitor, NTSC TV, and PAL TV formats as well as providing a means to display images in one format that were created in the other. This compatibility feature allows this part to be used throughout the world. Also, interlace and non–interlace displays are supported.

5.1.1 NTSC/PAL

NTSC is the North American and Japanese standard for broadcast TV. The display is made up of 525 horizontal lines, counted in the vertical direction, displayed 30 times in one second. NTSC Monitor is a little–used standard in North America for in–studio use on monitors. It is also made up of 525 horizontal lines.

PAL is the European standard for broadcast TV. Its display is made up of 625 horizontal lines, counted in the vertical direction, but only displayed 25 times each second. Both systems allow for an image (or frame) to be made up of two fields, an odd and an even field. The field rate is twice the frame rate (60 Hz for NTSC and 50 Hz for PAL). Although each frame is made up of 525/625 lines, only 480/560 are visible on the screen.

5.2 RESOLUTION

The normal full–screen resolution of the VDSC is shown in Table 5–1.

Table 5–1. Normal Full–Screen Display Resolution

Display	Number of Pixels Horizontally	Number of Pixels Vertically
NTSC Monitors	360	240
NTSC TVs	384	240
PAL TVs	384	280

In addition to normal resolution, the VDSC provides both double resolution and high resolution modes. Double resolution is defined as twice the normal resolution in the horizontal direction, whereas high resolution is defined as twice the resolution in both horizontal and vertical directions. Although most TVs are not capable of clearly displaying single pixels in double resolution mode, this mode is useful in two areas:

- Where double resolution pixel pairs can give increased positional accuracy.
- Where a single pixel's reduced display quality does not reduce the identifiability of the graphic object or character (i.e., Kanji characters).

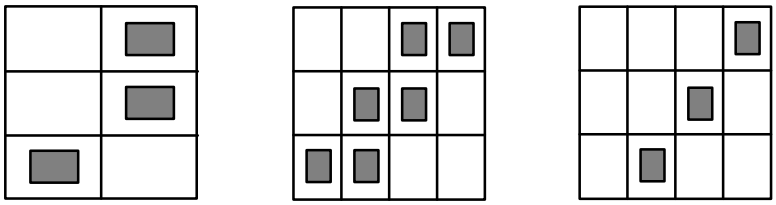


Figure 5–2. Example of Normal and Double Resolution Pixels

5.2.1 Horizontal Resolution

The horizontal resolution can be different between the two graphics planes (A and B) but both are controlled by various factors; the CF (Crystal Frequency) bit in the DCR1 register, the ST (Standard) bit in the CSR1W register, the CM1(Color Mode 1) bit in the DCR1 register, the CM2 (Color Mode 2) bit in the DCR2 register, and the frequency of the crystal. The effects of the various bits on the resolution are shown in Table 5–2.

Table 5–2. Horizontal Resolution

CF	ST	Frequency (MHz)	Pixels/Line		Active Line (μs)	Display System
			CM = 0	CM = 1		
0	x	28	360	720	51.4	NTSC Monitor
1	0	30/30.2097	384	768	51.2/50.84	PAL/NTSC TV
1	1	30/30.2097	360	720	48/47.67	PAL/NTSC TV

5.2.2 Vertical Resolution

The vertical resolution is dependent on the SM (Scan Mode) bit of the DCR1 register, the FD (Frame Duration) bit which is also in the DCR1 register, and the ST (Standard) bit which is in the CSR1W register.

The SM bit controls the scan mode of the VDSC by selecting between the interlace mode and the non–interlace mode as described in Table 5–3 and shown in Figure 5–3.

Table 5–3. Scan Modes

SM	SCAN Mode Description
0	Non–interlace mode. One image is composed of one field.
1	Interlace mode. One image is composed of two fields.

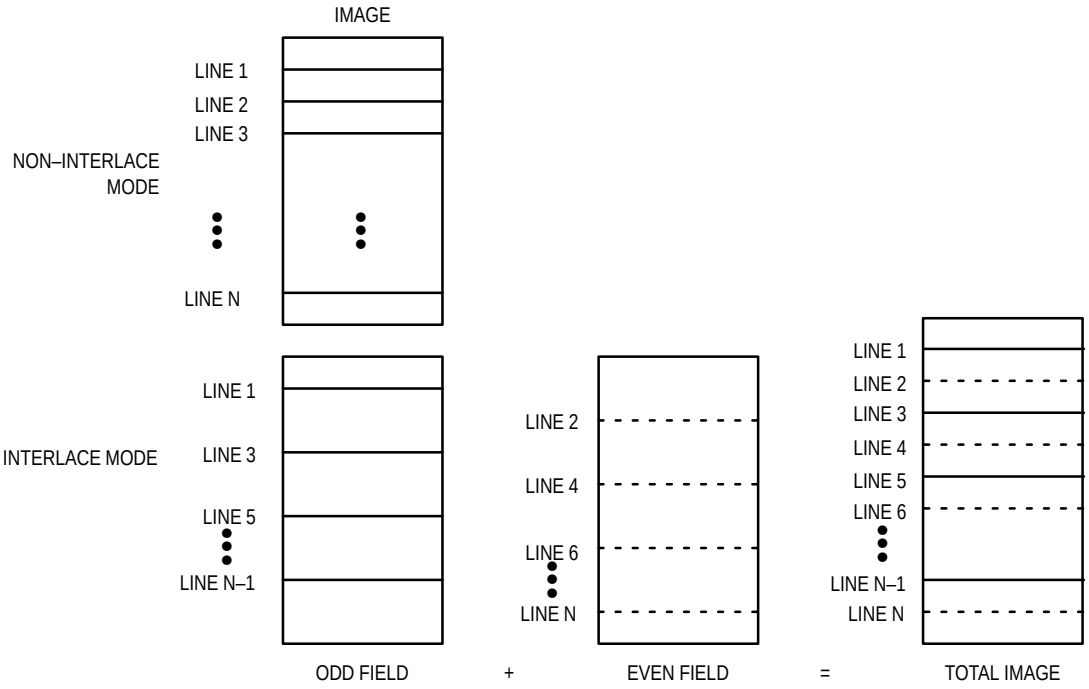


Figure 5–3. Line Display of Interlace versus Non–interlace Modes

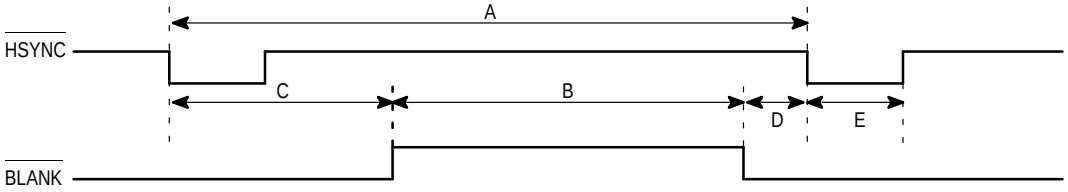
The FD bit and the ST bit only affect the display in the non–interlace mode. They are shown in Table 5–4.

Table 5–4. Vertical Resolution in the Non–interlace Mode

FD	ST	# of Video Lines	Frame Duration (ms)	Image Frequency (Hz)	Display Type
0	0	280	18	50	PAL
1	1	240	15.3	50	PAL
1	x	240	15.3	60	NTSC

5.3 TIMING

The following tables and figures depict the horizontal and vertical timing for the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, CSYNC, and BLANK signals in the master mode.

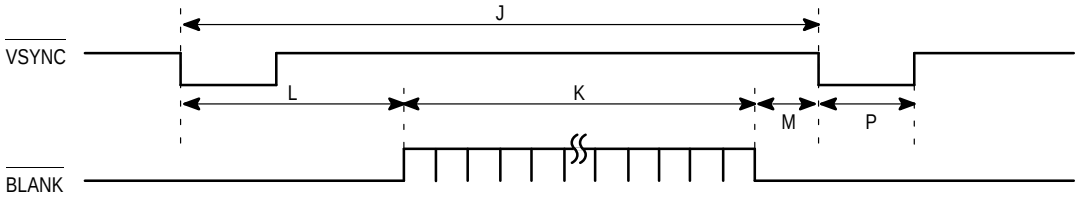


NOTES:
A: total horizontal line duration
B: active horizontal line duration
1 cycle = 16 CLK periods
1 cycle = 571.43 ns (CLK = 28 MHz – NTSC monitor)
1 cycle = 533.33 ns (CLK = 30 MHz – PAL TV)
1 cycle 529.63 ns (CLK = 30.2097 MHz – NTSC TV)

Figure 5–4. $\overline{\text{HSYNC}}$ and $\overline{\text{BLANK}}$ Timing

Table 5–5. Horizontal Synchronization Timing

	CF = 0 (Cycles)	CLK= 28 MHz (µs)	CF = 1 ST = 0 (Cycles)	CLK = 30 MHz (µs)	CLK = 30.2097 MHz (µs)	CF = 1 ST = 1 (Cycles)	CLK = 30 MHz (µs)	CLK = 30.2097 MHz (µs)
A	112	64.0	120	64.0	63.56	120	64.0	63.56
B	90	51.43	96	51.2	50.84	90	48.0	47.67
C	19	10.9	20	10.7	10.59	23	12.3	12.18
D	3	1.71	4	2.13	2.12	7	3.7	4.77
E	8	4.57	9	4.8	4.77	9	4.8	4.77
G	4	2.29	4	2.13	2.12	4	2.13	2.12
H	8	4.57	9	4.8	4.77	9	4.8	4.77



NOTES:
J = Total Vertical Display Period
K = Active Vertical Display
P = Vertical Sync Width

Figure 5–5. $\overline{\text{VSYNC}}$ and $\overline{\text{BLANK}}$ Timing

Table 5–6. Vertical Synchronization Timing (in lines)*

	50 Hz (FD = 0)		
	ST = 0	ST = 1	60 Hz (FD = 1)
J	312	312	262
K	280	240	240
L	26	46	18
M	6	26	4
P	2.5	2.5	3

* Non–interlace mode (SM = 0)

Table 5–7. Vertical Synchronization Timing (in lines)

	50 Hz (FD = 0)				60 Hz (FD = 1)	
	Odd Field (PA = 1)		Even Field (PA = 0)		Odd Field (PA = 1)	Even Field (PA = 0)
	ST = 0	ST = 1	ST = 0	ST =1		
J	312.5	312.5	312.5	312.5	262.5	262.5
K	280	240	280	240	240	240
L	26	46	26.5	46.5	18	18.5
M	6.5	26.5	6	26.5	4.5	4
P	2.5	2.5	2.5	2.5	3	3

* Interlace Mode (SM = 1)

NOTES:

To determine the time from the number of display lines, simply multiply the number of lines by the total line width (not the active display width). For instance, in an NTSC system with a 63.56 µs (from Table 5–5) line width, the total vertical display time for an interlace display is:

63.56 µs x 262.5 lines = 16.6845 ms

or the display rate is: 59.94 Hz.

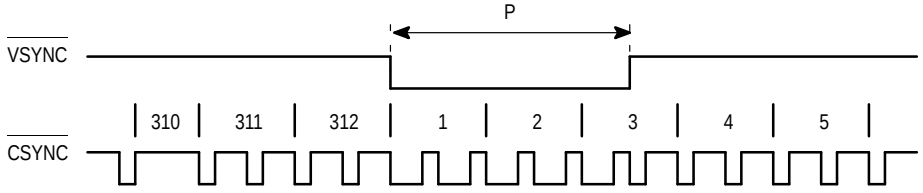


Figure 5–6. $\overline{\text{CSYNC}}$ Timing in the 50 Hz (FD = 0), Non–interlace Mode (SM = 0)

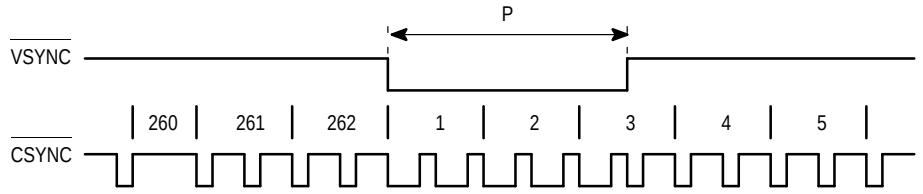


Figure 5–7. $\overline{\text{CSYNC}}$ Timing in the 60 Hz (FD = 1), Non–interlace Mode (SM = 0)

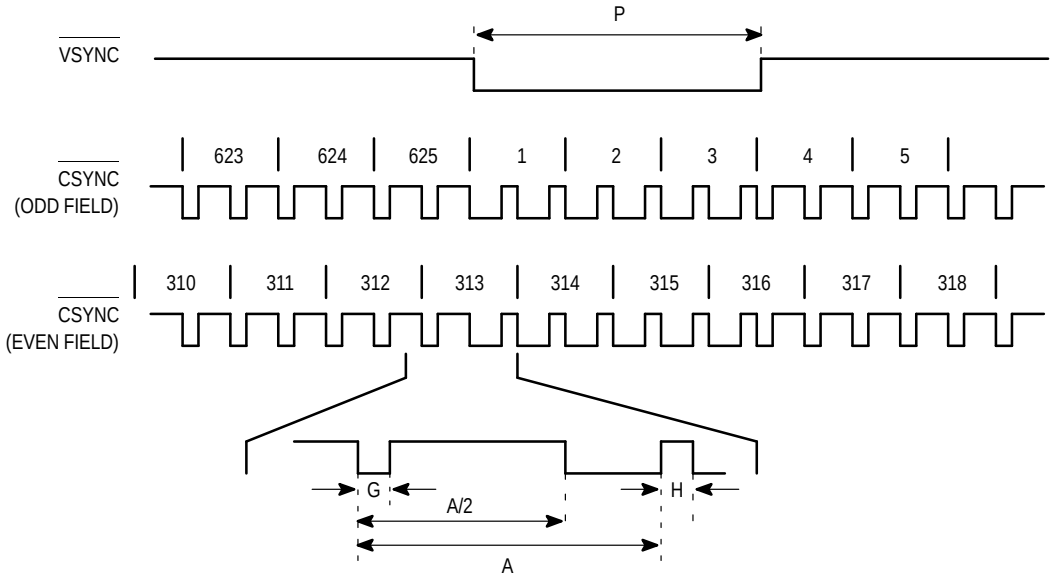


Figure 5–8. $\overline{\text{CSYNC}}$ Timing in the 50 Hz (FD = 0), Interlace Mode (SM = 1)

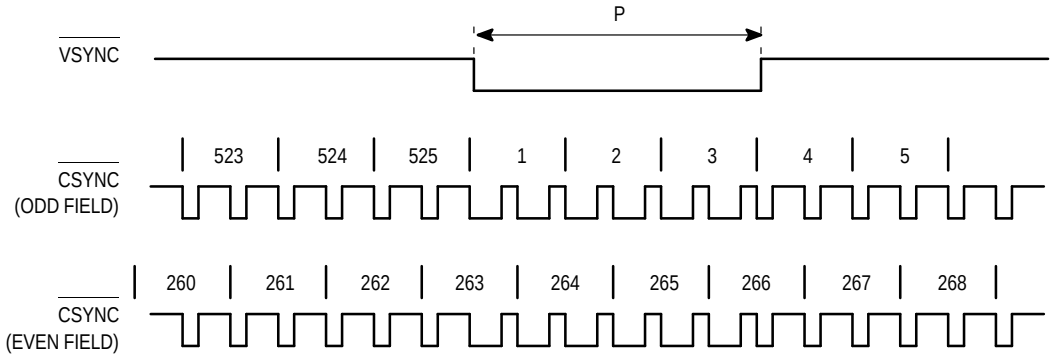


Figure 5–9. $\overline{\text{CSYNC}}$ Timing in the 60 Hz (FD = 1), Interlace Mode (SM = 1)

5.4 SOFTWARE

The VDSC offers the possibility to fetch control information during vertical and horizontal retrace periods from the Image Control Area (ICA) and Dynamic Control Area (DCA), respectively. Each video channel has its associated ICA and DCA. For channel 1 this is ICA1 and DCA1, and for channel 2 this is ICA2 and DCA2. ICA/DCA control is identical and independent for both channels.

5.4.1 ICA Control

ICA control consists of fetching long–word instructions during the vertical retrace period. The ICA pointers are indicated in Table 5–8.

Table 5–8. ICA Pointer Addresses

		Interlace	
	Non–Interlace	**Odd Field (PA = 1)**	**Even Field (PA = 0)**
Channel 1 (ICA1)	h400	h400	h404
Channel 2 (ICA2)	h200400	h200400	h200404

NOTE: Odd and even fields are indicated by the PA bit in the CSR1R register.

The possible number of ICA fetches is equal to the lines during vertical retrace times the display line width expressed in long words.

Example:

The number of crystal periods needed for a long–word access depends on the type of data being fetched. However, for example, if each access required five crystal periods then the following numbers would apply.

From Table 5–5: the total number of (16 CLK period) cycles = 120 per line. So, there are 120 x 16 = 1920 crystal periods.

From Table 5–6: the number of lines in vertical blanking is 262 – 240 = 22 lines for the non–interlace mode.

Therefore, there are: 22 x 1920 = 42,240 crystal periods during vertical blanking and 42,240/16 = 2640 memory fetches.

The video start register is also used as an ICA pointer after a “reload VSR” instruction to perform indirect ICA addressing during ICA instruction fetches to allow for linking blocks of instructions. All “reload VSR” instructions must contain an address with A0 = 0, A1 = 0, and A2 = 0. Each block ending with a “reload VSR” instruction must contain an even number of instructions including the “reload VSR” instruction, except for the first block.

5.4.2 DCA Control

The instruction fetch takes place in the horizontal retrace period. The DCA size is 64 bytes/line.

The DCA is completely independent of the bit map or display file areas. The DCA pointer (DCP) points to the first line of the DCA. The second DCA line is pointed to automatically by DCP + 64 bytes. The DCP can be changed at any time by the “reload DCP and stop” instruction. This allows for linking blocks of instructions on a line–by–line basis.

5.4.3 ICA/DCA Initialization

The ICA and DCA are enabled by the DE bit in the DCR1 register. The IC and DC bits of the DCR register control three possible ICA/DCA modes.

Table 5–9. ICA1/DCA1 and ICA2/DCA2 Modes

ICA1/DCA1 Modes					ICA2/DCA2 Modes				
DE	**IC1**	**DC1**	**ICA1**	**DCA1**	**DE**	**IC2**	**DC2**	**ICA2**	**DCA2**
1	0	x	No	No	1	0	x	No	No
1	1	0	Yes	No	1	1	0	Yes	No
1	1	1	Yes	Yes	1	1	1	Yes	Yes
0	x	x	No	No	0	x	x	No	No

When IC and DC are set to 1, the number of possible DCA fetches can be limited by the line retrace duration as indicated in the following tables.

Table 5–10. Possible DCA1/DCA2 Fetches per Line

Possible DCA1 Fetches Per Line				Possible DCA2 Fetches Per Line			
IC1	DC1	CF	DCA1 (in bytes)	IC2	DC2	CF	DCA2 (in bytes)
0	x	x	0	0	x	x	0
1	0	x	0	1	0	x	0
1	1	0	32	1	1	0	32
1	1	1	64	1	1	1	64

NOTE: An automatic stop instruction is performed at the end of the available area (when the effective DCA is larger than indicated). The allocated memory size is always 64 bytes even if the possible number of fetches is lower.

5.4.4 ICA/DCA Instructions

ICA/DCA instructions are contained in the system RAM. They are long–word aligned and long–word wide. The most significant byte indicates which register or registers are updated by the information contained in the other bytes. The instructions can be divided into two groups. The instructions from the first group affect the control of the instruction fetches, the display parameters, and interrupt generation (see Table 5–11). The instructions from the second group affect the video decoder and visual effects part (see Chapter 11). The control of the instructions fetches and display parameters can also be affected by the system (CPU). None of the registers can be read by the system.

Table 5–11. ICA Control Instructions

Instruction (Bit 31 – 0)	Acronym	Action
0000 ——— ——— ——— ——— ——— ——— ——— ———	STOP	Stop the control sequence. The instruction fetches are stopped until the next field.
0001 ——— ——— ——— ——— ——— ——— ——— ———	NOP	No operation.
0010 ——— —— pp pppp pppp pppp pppp pp ——	RELOAD DCP	Reload the DCP register and its associated address counter with the specified pointer (p).
0011 ——— —— pp pppp pppp pppp pppp pp ——	RELOAD DCP and STOP	Reload the DCP register and its associated address counter with the specified pointer (p) and stop control fetches as STOP instruction.
0100 ——— —— pp pppp pppp pppp pppp pppp	RELOAD VSR	Reload ICA pointer. It functions as a jump instruction. It does not affect the VSR pointer.
0101 ——— —— pp pppp pppp pppp pppp pppp	RELOAD VSR and STOP	Reload the VSR register and the video address counter with the specified pointer and stop the control fetches as STOP instruction.
0110 ——— ——— ——— ——— ——— ——— ——— ———	INTERRUPT	Set IT bit in CSR register.
0111 1 ——— ——— ——— ——— ——— ——0b cdef	RELOAD DISPLAY PARAMETERS	b = CM c = MF1 d = MF2 e = FT1 f = FT2

Table 5–12. DCA Control Instructions

Instruction (Bit 31 – 0)	Acronym	Action
0000 ——— ——— ——— ——— ——— ——— ——— ———	STOP	Stop the control sequence. The instruction fetches are stopped until the next field.
0001 ——— ——— ——— ——— ——— ——— ——— ———	NOP	No operation.
0010 ——— ——— pp pppp pppp pppp pppp pppp pp ———	RELOAD DCP	No operation.
0011 ——— ——— pp pppp pppp pppp pppp pppp pp ———	RELOAD DCP and STOP	Reload the DCP register and its associated address counter with the specified pointer (p) and stop control fetches as STOP instruction.
0100 ——— ——— pp pppp pppp pppp pppp pppp pppp	RELOAD VSR	Reload the VSR register and the video address counter with the specified pointer.
0101 ——— ——— pp pppp pppp pppp pppp pppp pppp	RELOAD VSR and STOP	Reload the VSR register and the video address counter with the specified pointer and stop the control fetches as STOP instruction.
0110 ——— ——— ——— ——— ——— ——— ——— ———	INTERRUPT	Set IT bit in CSR register.
0111 1 ——— ——— ——— ——— ——— ——— ———0b cdef	RELOAD DISPLAY PARAMETERS	b = CM c = MF1 d = MF2 e = FT1 f = FT2

Via several internal registers, the CLUT and the cursor–RAM, it is possible to program the real–time decoder of the VDSC and to perform visual effects. During the vertical and horizontal retrace periods, the VDSC can load above–mentioned registers/RAMs.

Each instruction consists of a long–word. The most significant byte indicates the register involved; the remaining three bytes contain control data. The instructions are transferred via CH#1 or CH#2, which are byte wide with the most significant byte first.

Table 5–13. Register Map

Channel No.	Address (h)	Register Name
1+2	80 to BF	CLUT Color 0 – 63
1	C0	Image Coding Method
1	C1	Transparency Control
1	C2	Plane Order
1+2	C3	CLUT Bank
1	C4	Transparent Color for Plane A
—	C5	Reserved
2	C6	Transparent Color for Plane B
1	C7	Mask Color for Plane A
—	C8	Reserved
2	C9	Mask Color for Plane B
1	CA	DYUV Abs. Start Value for Plane A
2	CB	DYUV Abs. Start Value for Plane B
—	CC	Reserved
1	CD	Cursor Position
1	CE	Cursor Control
1	CF	Cursor Pattern
1+2	D0 to D7	Region Control 0 – 7
1	D8	Backdrop Color
1	D9	Mosaic Pixel Hold for Plane A
2	DA	Mosaic Pixel Hold for Plane B
1	DB	Weight Factor for Plane A
2	DC	Weight Factor for Plane B
—	DD to FF	Reserved

5.4.4.1 CLUT Color Register 0 - 63 (h80 - hBF)

Programmable via CH#1 and CH#2.

Table 5–14. CLUT Color Register 0 – 63 — Address h80 – hBF

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	—	—	G7	G6	G5	G4	G3	G2	—	—	B7	B6	B5	B4	B3	B2	—	—

R7 – R2, G7 – G2, and B7 – B2 contain the color–data of one pixel. Only the 6 MSBs per byte are implemented.

The CLUT RAM is addressable in two steps.

First, one of the four CLUT banks must be selected via the CLUT bank register (address A7, A6).

Second, the address within the bank is given by selecting a CLUT register h80 – hBF.

Table 5–15. CLUT RAM Addresses

CLUT Bank	CLUT 0 – 63	CLUT Address (h)
0	00 (Reg. 80) – 3F (Reg. BF)	00 – 3F
1	00 (Reg. 80) – 3F (Reg. BF)	40 – 7F
2	00 (Reg. 80) – 3F (Reg. BF)	80 – BF
3	00 (Reg. 80) – 3F (Reg. BF)	C0 – FF

5.4.4.2 Image Coding Method Register (hC0)

Programmable via CH#1.

Table 5–16. Image Coding Method Register — Address hC0

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	CS	—	—	NR	EV	—	—	—	—	—	—	CM23	CM22	CM21	CM20	—	—	—	—	CM13	CM12	CM11	CM10

CS: CLUT select for dual 7–bit CLUTs:

0 = CLUT bank 0 and 1
1 = CLUT bank 2 and 3

NR: number of region flags:

0 = one region flag is used
1 = two region flags are used

EV: external video enable:

0 = disabled
1 = enabled

Table 5–17. CM1x, CM2x: Coding Method for Plane A, B

Input Channel	Mode	Resolution	CM 23	CM 22	CM 21	CM 20	CM 13	CM 12	CM 11	CM 10
CH#1	OFF	—	—	—	—	—	0	0	0	0
CH#2	OFF	—	0	0	0	0	—	—	—	—
CH#1	CLUT8	Normal	—	—	—	—	0	0	0	1
CH#1	CLUT7	Normal	—	—	—	—	0	0	1	1
CH#1	CLUT7+7	Normal	—	—	—	—	0	1	0	0
CH#1	DYUV	Normal	—	—	—	—	0	1	0	1
CH#1	CLUT4	Double	—	—	—	—	1	0	1	1
CH#1 + CH#2	RGB555	Normal	0	0	0	1	—	—	—	—
CH#2	CLUT7	Normal	0	0	1	1	—	—	—	—
CH#2	DYUV	Normal	0	1	0	1	—	—	—	—
CH#2	CLUT4	Double	1	0	1	1	—	—	—	—

5.4.4.3 Transparency Control Register (hC1)

Programmable via CH#1.

Table 5–18. Transparency Control Register — Address hC1

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MX	—	—	—	—	—	—	—	—	—	—	—	TB3	TB2	TB1	TB0	—	—	—	—	TA3	TA2	TA1	TA0

MX: disable mixing:

0 = mix
1 = no mix

Table 5–19. Transparency Control Register — Address hC1

TA3 TB3	TA2 TB2	TA1 TB1	TA0 TB0	Pixel is Transparent if:
0	0	0	0	Always (Plane Disabled)
0	0	0	1	Color Key = True
0	0	1	0	Transparency Bit = 1
0	0	1	1	Region Flag 0 = True
0	1	0	0	Region Flag 1 = True
0	1	0	1	Region Flag 0 or Color Key = True
0	1	1	0	Region Flag 1 or Color Key = True
0	1	1	1	N.U.
1	0	0	0	Never (No Transparent Area)
1	0	0	1	Color Key = False
1	0	1	0	Transparency Bit = 0
1	0	1	1	Region Flag 0 = False
1	1	0	0	Region Flag 1 = False
1	1	0	1	Region Flag 0 or Color Key = False
1	1	1	0	Region Flag 1 or Color Key = False
1	1	1	1	N.U.

NOTE: TA, TB = select transparency mechanism for plane A, B individually.

5.4.4.4 Plane Order Register (hC2)

Programmable via CH#1.

Table 5–20. Plane Order Register — Address hC2

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	O3	O2	O1

Table 5–21. Plane Order

O3	O2	O1	Plane Order
0	0	0	Plane A in front of Plane B
0	0	1	Plane B in front of Plane A

NOTE: All other values are not used.

5.4.4.5 CLUT Bank Register (hC3)

Programmable via CH#1 and CH#2 independently.

Table 5–22. CLUT Bank Register — Address hC3

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	A7	A6

Table 5–23. Bank Select

A7	A6	Bank Select
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

NOTE: Only banks 2 and 3 are programmable (A7 = 1) via CH#2.

5.4.4.6 Transparent Color Register (hC4 - hC6)

hC4: programmable via CH#1 for plane A.
hC5: reserved.
hC6: programmable via CH#2 for plane B.

Table 5–24. Transparent Color Register — Address hC4 – hC6

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	—	—	G7	G6	G5	G4	G3	G2	—	—	B7	B6	B5	B4	B3	B2	—	—

Transparent color is only defined for the CLUT mode: CLUT8, CLUT7, CLUT7 + 7, and CLUT4.

5.4.4.7 Mask Color Register (hC7 - hC9)

hC7: programmable via CH#1 for plane A.
hC8: reserved.
hC9: programmable via CH#2 for plane B.

Table 5–25. Mask Color Register — Address hC7 – hC9

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	—	—	G7	G6	G5	G4	G3	G2	—	—	B7	B6	B5	B4	B3	B2	—	—

Mask color is only defined for the CLUT mode: CLUT8, CLUT7, CLUT7 + 7, and CLUT4.

5.4.4.8 Delta YUV Absolute Start Value Register (hCA, hCB)

hCA: programmable via CH#1 for plane A.
hCB: programmable via CH#2 for plane B.

Table 5–26. Delta YUV Absolute Start Value Register — Address hCA – hCB

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	U7	U6	U5	U4	U3	U2	U1	U0	V7	V6	V5	V4	V3	V2	V1	V0

hCA: YUV start value for plane A.
hCB: YUV start value for plane B.

Y,U,V = absolute Y,U,V start value.

5.4.4.9 Cursor Position Register (hCD)

Programmable via CH#1.

Table 5–27. Cursor Position Register — Address hCD

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	—	—	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

Y9 – Y0: Cursor Y–position:

Y9 = MSB
Y0 = LSB

X9 – X0: Cursor X–position in double resolution:

X9 = MSB
X0 = LSB

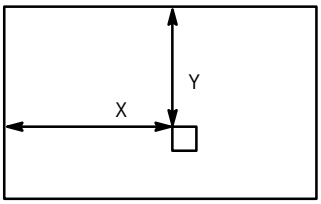


Figure 5–10. Cursor Position

The cursor origin is always the top lefthand corner of the full–screen display.

5.4.4.10 Cursor Control Register (hCE)

Programmable via CH#1.

Table 5–28. Cursor Control Register — Address hCE

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	BLKC	CON2	CON1	CON0	COF2	COF1	COF0	CUW	—	—	—	—	—	—	—	—	—	—	—	Y	R	G	B

EN: Cursor enable:

0 = cursor disable (transparent)
1 = cursor enabled

BLKC: blink type:

0 = on/off
1 = on/complement

CON2 – CON0: period of the cursor on:

Period = 12 * (CON–value) * (field–period)

COF2 – COF0: period of the cursor off:

Period = 12 * (COF–value) * (field–period)
If COF = 0 the cursor is on indefinitely.

Table 5–29. Cursor Color

Y	R	G	B	Cursor Color
0	0	0	0	Black
0	0	0	1	Half–brightness blue
0	0	1	0	Half–brightness green
0	0	1	1	Half–brightness cyan
0	1	0	0	Half–brightness red
0	1	0	1	Half–brightness magenta
0	1	1	0	Half–brightness yellow
0	1	1	1	Half–brightness white
1	0	0	0	Black
1	0	0	1	Blue
1	0	1	0	Green
1	0	1	1	Cyan
1	1	0	0	Red
1	1	0	1	Magenta
1	1	1	0	Yellow
1	1	1	1	White

CUW: cursor resolution:

0 = normal resolution for horizontal direction
1 = double resolution for horizontal direction

5.4.4.11 Cursor Pattern Register (hCF)

Programmable via CH#1.

Table 5–30. Cursor Pattern Register — Address hCF

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	AD 3	AD 2	AD 1	AD 0	CP 15	CP 14	CP 13	CP 12	CP 11	CP 10	CP 9	CP 8	CP 7	CP 6	CP 5	CP 4	CP 3	CP 2	CP 1	CP 0

AD3 – AD0: Y address register

CP15 – CP0: line pattern register:

CP15 is the left–most pixel.
CP0 is the right–most pixel.

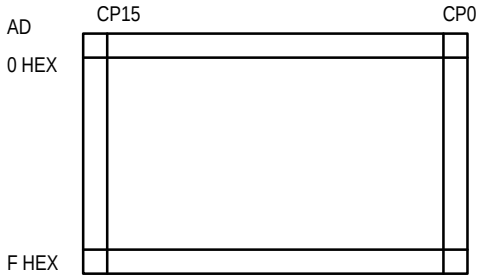


Figure 5–11. Cursor Pattern Diagram

5.4.4.12 Region Control Register 0 - 7 (hD0 - hD7)

Programmable via CH#1 and CH#2.

In case the registers are loaded simultaneously from both channels, then CH#1 has the first priority. At that moment CH#2 will be ignored.

If the region control is not used, then the operation code OP3 – OP0 of the region control register D0 and D4 must be 0000. This means the end of the region control for the line.

Table 5–31. Region Control Register — Address hD0 – hD7

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OP 3	OP 2	OP 1	OP 0	—	—	—	RF	WF 5	WF 4	WF 3	WF 2	WF 1	WF 0	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

OP3 OP2 OP1 OP0: operation control

Table 5–32. Operation Control Codes

OP3	OP2	OP1	OP0	Operation Control
0	0	0	0	End of Region Control for the Line
0	0	0	1	N.U.
0	0	1	0	N.U.
0	0	1	1	N.U.
0	1	0	0	Change Weight of Plane A. New Weight–Value is WF5–0
0	1	0	1	N.U.
0	1	1	0	Change Weight of Plane B. New Weight–Value is WF5 –WF0
0	1	1	1	N.U.
1	0	0	0	Reset Region Flag
1	0	0	1	Set Region Flag
1	0	1	0	N.U.
1	0	1	1	N.U.
1	1	0	0	Reset Region Flag and Change Weight of Plane A
1	1	0	1	Set Region Flag and Change Weight of Plane A
1	1	1	0	Reset Region Flag and Change Weight of Plane B
1	1	1	1	Set Region Flag and Change Weight of Plane B

RF: region flag to be changed:

0 = region flag 0
1 = region flag 1

The RF bit is only valid if the NR bit in register COH is 0.

WF5 – WF0: next new weight factor value

X9 – X0: X–position:

Distance from the lefthand edge of display, in double resolution.

5.4.4.13 Backdrop Color Register (hD8)

Programmable via CH#1.

Table 5–33. Background Color Register — Address hD8

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Y	R	G	B

Y R G B: Color of backdrop plane

Table 5–34. Color of Background Plane

Y	R	G	B	Color of Background
0	0	0	0	Black
0	0	0	1	Half–Brightness Blue
0	0	1	0	Half–Brightness Green
0	0	1	1	Half–Brightness Cyan
0	1	0	0	Half–Brightness Red
0	1	0	1	Half–Brightness Magenta
0	1	1	0	Half–Brightness Yellow
0	1	1	1	Half–Brightness White
1	0	0	0	Black
1	0	0	1	Blue
1	0	1	0	Green
1	0	1	1	Cyan
1	1	0	0	Red
1	1	0	1	Magenta
1	1	1	0	Yellow
1	1	1	1	White

5.4.4.14 Mosaic Pixel Hold Factor Register (hD9, hDA)

hD9: programmable via CH#1 for plane A.
hDA: programmable via CH#2 for plane B.

Table 5–35. Mosaic Pixel Hold Factor Register — Address hD9, hDA

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Z7	Z6	Z5	Z4	Z3	Z2	Z1	Z0

EN: pixel hold enable:

0 = mosaic off
1 = mosaic on

Z7 – Z0: number of pixels to be held:

0 = reserved
1 = normal usage
2–255 = mosaic effect

The pixel hold factor is effective at both normal and double resolution.

5.4.4.15 Weight Factor Register (hDB - hDC)

hDB: programmable via CH#1 for plane A.
hDC: programmable via CH#2 for plane B.

Table 5–36. Weight Factor Register — Address hDB – hDC

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	W5	W4	W3	W2	W1	W0

W5 – W0: weight factor value:

W5 = MSB
W0 = LSB

5.5 BITMAP

For bitmap files, the width of the bitmap is related to that of the display line, but not necessarily the same (see Table 5–37). For mosaic files, the width of the bitmap is divided by the mosaic factor. For run–length files, the bitmap width is not related to the display width.

The Video Start Pointer (VSR) points to the first pixel in a bitmap. In case of interlace mode this is the first pixel of the odd field. The bitmap of the even field follows the one of the odd field.

If no reload of the VSR is performed the first pixel of a line is consecutive to the last pixel of the previous line for all file types.

If in the DCA, a reload of the VSR is performed, the VSR will point to the first pixel of the following line. In the next frame, the reloaded VSR points to the first pixel of the (odd) frame.

Table 5–37. Bitmap Width for Bitmap Files

CF	ST	CM	Horizontal Resolution (pixels)	Bitmap Width (bytes)
0	0	0	360	360
0	0	1	720	360
0	1	0	360	384
0	1	1	720	384
1	0	0	384	384
1	0	1	768	384
1	1	0	360	360
1	1	1	720	360

5.6 EFFECT OF STANDARD BIT

5.6.1 Effect on Vertical Timing

The vertical action of the ST bit is to display images created with a 60 Hz system in a 50 Hz system and is possible only in 50 Hz mode (FD = 0).

If ST is set to 1, the vertical display area and blanking area have 40 lines less, 20 less at the top and 20 less at the bottom.

The vertical resolution becomes 240 lines.

5.6.2 Effect on Horizontal Timing

The action is to display images created with a 28 MHz system in a 30 MHz system and vice versa.

In the 28 MHz mode, if ST = 1, the horizontal resolution is unchanged (360 pixels) but the number of pixel fetches continue to 384. This allows the use of a 384 pixels bitmap file or the detection of the zero code (end of line) in a run–length line (see Section 6.2). If ST = 0, the resolution and the width of the bitmap are 360 pixels.

In the 30 MHz mode, if ST = 1, the horizontal resolution and the width of the bitmap are decreased from 384 to 360 pixels. Twelve pixels are masked on either side of the screen, giving a centered image. The horizontal display area is reduced by 24 pixels. This allows for the display of a 360–pixel bitmap. The BLANK pin now has a zero state during the masking area of 2 x 12 pixels.

N.B.: The explanation above concerns normal resolution display. With double resolution display all the widths must be doubled.

5.7 VIDEO SYNCHRONIZATION

If the DE (Display Enable) bit in the DCR1 register is set, the VDSC generates video synchronization at outputs HSYNC, VSYNC, CSYNC and BLANK. If DE is reset, the HSYNC, VSYNC, and CSYNC outputs are high and the BLANK output is low.

The VDSC may work in master or in slave TV mode. Selection of the mode is done with the M/S pin. If the M/S (Master/Slave) pin is pulled up, then the master mode is selected. If this pin is pulled down then the slave TV mode is selected.

Table 5–38. Synchronization Modes

$\overline{\text{M/S}}$	Synchro Mode	$\overline{\text{HSYNC}}$	$\overline{\text{CSYNC}}$	$\overline{\text{VSYNC}}$
1	Master	Out	Out	Out
0	Slave TV	Out	Out	In

In the master mode, the $\overline{\text{HSYNC}}$, $\overline{\text{CSYNC}}$, and $\overline{\text{VSYNC}}$ signals are generated as output.

In the slave TV mode, $\overline{\text{HSYNC}}$ and $\overline{\text{CSYNC}}$ are generated as output, the $\overline{\text{VSYNC}}$ pin is in the input mode and must receive an external VSYNC signal. An even frame is displayed if the falling edge of the VSYNC input falls in the range from 1/4 to 3/4 between two successive falling edges of the HSYNC output. An odd frame is displayed if the falling edge of VSYNC falls outside this range. HSYNC is input to the phase comperator of an external phase–lock loop oscillator supplying CLK. The other input of the phase comparator is an external HSYNC signal.

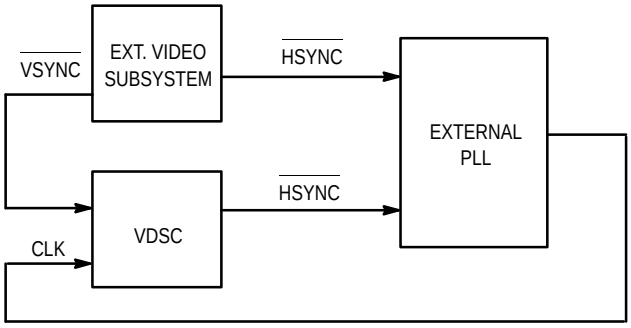


Figure 5–12. VDSC in Slave Mode with an External PLL for Clock Generation

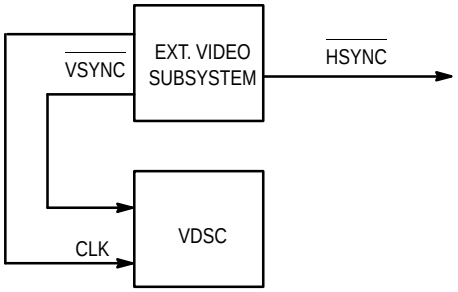


Figure 5–13. VDSC in Slave Mode with an External Clock

6
DISPLAY FILE DECODER

The VDSC contains two identical and independent display file decoders, one for channel 1 (plane A) and one for channel 2 (plane B). Each can handle three types of files:

- Normal file or bitmap file: each pixel has its own address.
- Run–length file: consecutive identical pixels (bytes or associated nibbles) are grouped in the same block of information.
- Mosaic file: as with a normal file but with resolution divided by a mosaic factor. The VDSC is in charge of duplicating each pixel according to the mosaic factor (2, 4, 8, or 16).

The initialization of the file type is made with the FT1 – FT2 bits of the DDR1 and DDR2 register:

Table 6–1. File Type of Display 1

FT 1	FT 2	Display 1 File Type
0	x	Bitmap
1	0	Run–length
1	1	Mosaic

NOTE: File type of display 1 is indicated in DDR1 register.

Table 6–2. File Type of Display 2

FT 1	FT 2	Display 1 File Type
0	x	Bitmap
1	0	Run–length
1	1	Mosaic

NOTE: File type of display 2 is indicated in DDR2 register.

6.1 BITMAP FILE

The pixel data are packed in the memory. Four words are fetched per memory access. These words are always page aligned in the DRAM. The first pixel of a line can be any of the eight bytes in the first access. Each word that the VDSC fetches in the memory for display is serialized according to Figures 6–1 and 6–2.

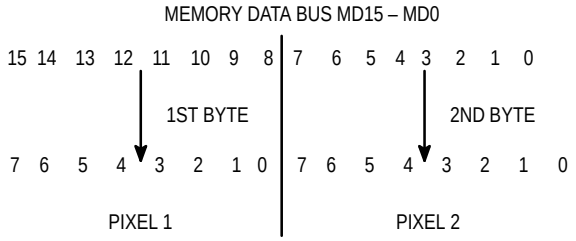


Figure 6–1. Bitmap Serialization in 8 Bits/Pixel

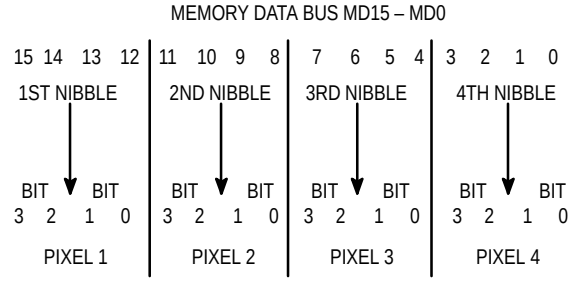


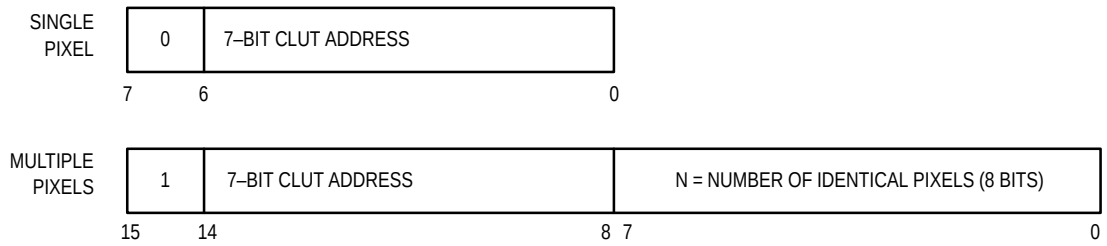
Figure 6–2. Bitmap Serialization in 4 Bits/Pixel

6.2 RUN-LENGTH FILE

The run–length coding technique permits file compression by grouping into one block consecutive pixels that have the same color. The VDSC uses either a 7– or a 3–bit color look up table (CLUT) to provide either 1 out of 128 colors or 1 out of 8 different colors. The run–length compression is applied to each video line independently of the others. The run–length file is organized as a list of information about pixels without any notion of width or height as in bitmap files. (Refer to Section 7.2, CLUT Decoder.)

6.2.1 Run-length 7-Bit CLUT Files

Run–length 7–bit CLUT files are either a single byte (for a single pixel) or two bytes (for a run of pixels on a single line) in length. A 0 in the first bit indicates a single pixel CLUT address whereas a 1 in the first bit indicates a run of pixels on the present line. The run only extends to the end of the line and does not continue to the next line. The second byte indicates the number of identical pixels to be reproduced on the current line. A 0 in the second byte indicates that this color is to be repeated to the end of the line. A 1 is forbidden in the second byte. The eight bits allowed for 2 to 255 identical bits to be repeated or with a 0, the rest of the line will have the same pixel repeated. Every line must finish with a “zero–length” run (N = 0), which means that at a minimum, the last two pixels of the line are identical. Figure 6–3 shows the format for both.

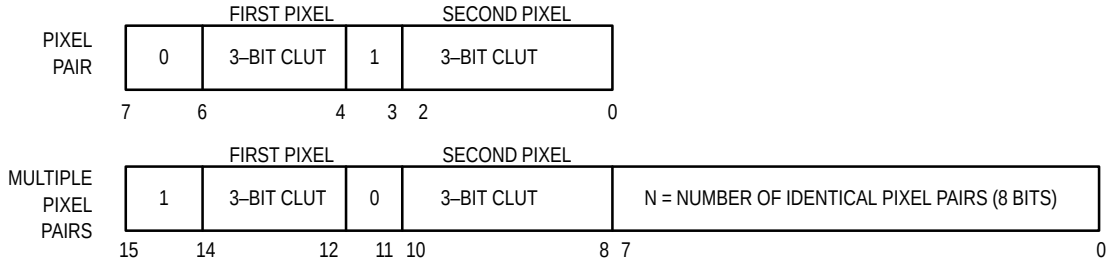


NOTE: N = 0 means “duplicate this pixel to the end of the line”.
N = 1 is forbidden.

Figure 6–3. Run–length Format in 7 Bits/Pixel

6.2.2 Run-length 3-Bit CLUT Files

The run–length 3–bit CLUT files are similar to the 7–bit files except that instead of a single pixel, this format specifies pixel pairs. Also, instead of 7–bit CLUT addresses only 3 bits plus a 0 in the MSB are used to generate a 4–bit CLUT.



NOTE: N = 0 means “duplicate this pixel to the end of the line”.
N = 1 is forbidden.

Figure 6–4. Run–length Format in 3 Bits/Pixel

If the number of pixel pairs indicated is greater than the number of remaining pixels in the line, then only the number of pixels necessary to complete the line is displayed.

6.3 MOSAIC FILE

The mosaic technique consists of changing the resolution of the screen by duplicating pixels by a mosaic factor, n. The mosaic file is then effectively compressed by the factor n. The VDSC automatically duplicates the pixels. The mosaic factor is indicated in the DDR1 and DDR2 register.

Table 6–3. Mosaic Factor of Display 1

MF1	MF2	Mosaic Factor
0	0	2
0	1	4
1	0	8
1	1	16

NOTE: Bits indicated in DDR1 register.

Table 6–4. Mosaic Factor of Display 2

MF 1	MF 2	Mosaic Factor
0	0	2
0	1	4
1	0	8
1	1	16

NOTE: Bits indicated in DDR2 register.

The mosaic file works at the byte level. In 4 bits/pixel mode, the pixels are duplicated by groups of two.

6.4 PIXEL OUTPUT

The video channels 1 and 2 are enabled by the DE–bit in the DCR1 register. The video channels can be in different modes (see Tables 6–5 and 6–6).

Table 6–5. Output Modes of Channel 1

DE	CM 1	Bits/Pixel	Frequency	Resolution
1	1	4	CLK/2	Double

NOTE: Bits indicated in DCR1 register.

Table 6–6. Output Modes of Channel 2

DE	CM 2	Bits/Pixel	Frequency	Resolution
1	1	4	CLK/2	Double

NOTE: Bits indicated in DCR1 register.

7
REAL-TIME DECODER

To decode the pixel streams entering via channel 1 and channel 2, several decoders are available: one delta YUV decoder per channel, one color look up table (CLUT) to be shared by both channels, and direct RGB to be generated via both channels. The decoded pixel streams represent the two graphics planes: A and B. The cursor and backdrop are programmed via channel 1.

7.1 DELTA YUV DECODER

YUV stands for luminance (Y) and color difference (U and V). The U and V components are horizontally subsampled by a factor of two and transmitted alternatively every other pixel. The missing U and V components are interpolated using linear interpolation. The human eye is much less sensitive to color variation than variations in luminance, therefore any error due to interpolation will not be detected. The last missing U or V component of a line is found by repeating the last U or V component.

The Y component ranges from 0 to 255. The U and V components are signed but are given an offset of 128 to make them positive. The U and V components then range from 1 to 255. The expected ranges for R, G, and B are from 0 to 255. To avoid wrap–around for values outside this range, output limiters are implemented.

The absolute Y, U, and V components are decoded to R, G, and B using the following equations:

$$R = \text{lim}[\ \text{trunc}\{\ (\ Y*256 + 351*(V - 128)\ )\ /\ 256\ \}\ ]$$

$$G = \text{lim}[\ \text{trunc}\{\ (\ Y*256)(86*(U - 128) + 179*(V - 128))\ )\ /\ 256\ \}\ ]$$

$$B = \text{lim}[\ \text{trunc}\{\ (\ Y*256 + 444*(U - 128)\ )\ /\ 256\ \}\ ]$$

trunc{x} = greatest integer less than or equal to x

lim[x] = 0 if x < 0

= 255 if x > 255

= x else

Delta YUV (DYUV) coding is particularly useful for the reproduction of high quality natural images. These images typically have a high degree of correlation between adjacent pixels. This correlation is used in delta YUV decoding by only coding the difference between adjacent pixels rather than their absolute value; this is the delta. This difference is coded in 4 bits, using a non–uniform 16–level fixed quantizer. The VDSC executes the opposite operation, using the values in Table 7–1.

Table 7–1. Dequantizer

Input	Output
0	0
1	1
2	4
3	9
4	16
5	27
6	44
7	79
8	128
9	177
10	212
11	229
12	240
13	247
14	252
15	255

The output of the dequantizer is added to the previous absolute value to obtain a new absolute value. The operation mentioned above applies for Y, U, and V. Decoding delta YUV comprises DYUV to YUV decoding and YUV to RGB decoding (matrixing). (For an explanation of delta YUV encoding, see Appendix A.)

Delta decoding is initialized before the beginning of each display line by using programmable absolute start values for Y, U, and V. These initial values for each line are loaded via the display control program. (See Section 5.4.5.8.)

Since the human eye is less sensitive to variations in color than to changes in intensity, the color data is subsampled by a factor of two. This means that for each pixel there is a Y value, but a U and V value for every other pixel. This allows for a certain amount of data compression with no perceived loss of image quality. The data is stored as the YUV for the first pixel and then the Y data for the second pixel and the UV data for the third pixel. The U and V data for the second pixel is interpolated from the first and third. The data structure of the input and output of the DYUV decoder is given in Figure 7–1. All calculations are performed using 8 bits, however only the most significant 7 bits of R, G, and B are given as output.

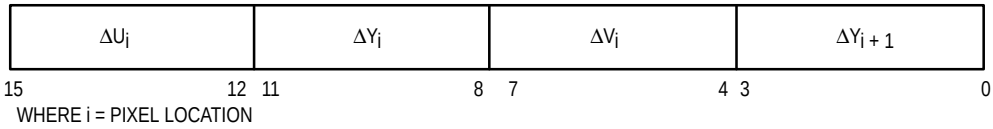


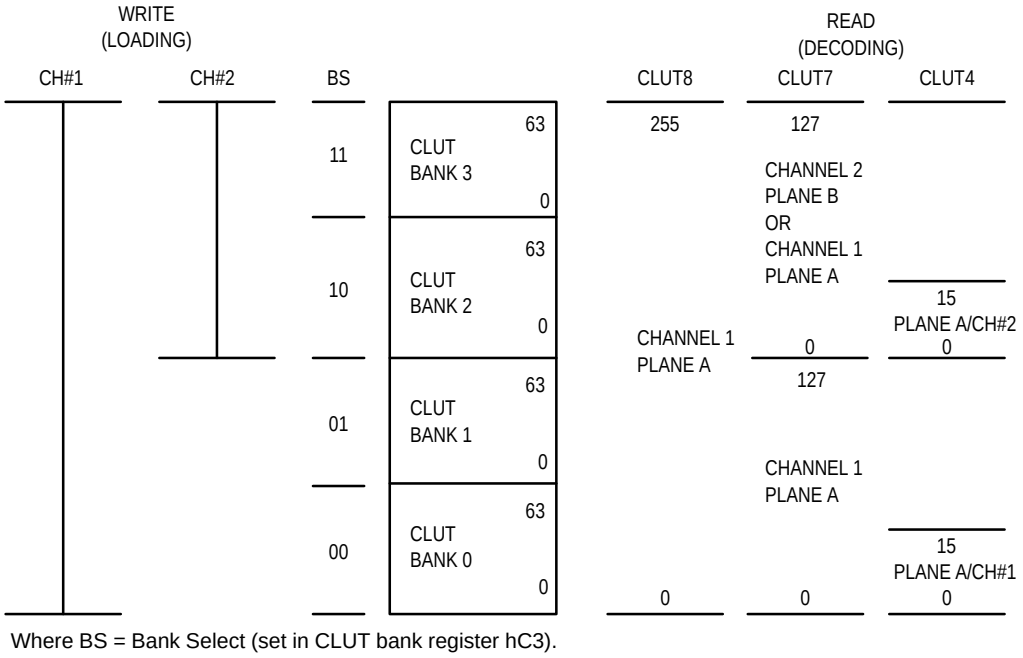
Figure 7–1. Data Structure of DYUV Decoder Input and Output Pixel–pair

DYUV decoding of coded pixel–data entering via channel 1 results in plane A and DYUV decoding of coded pixel–data entering via channel 2 results in plane B.

7.2 CLUT DECODER

Color look up table (CLUT) decoding is a method of compressing display files. Instead of using 24 bits of storage for each pixel, a table of colors is set up. Then, the pixel data that is stored in memory is not the actual color values, but rather a pointer to a specific color in the look up table.

The VDSC supports CLUT8 (256 colors), CLUT7 (128 colors), CLUT7+7 (2 x 128 colors), CLUT4 (16 colors), and CLUT3 (8 colors — used for run–length files). Pixel–decoding via a CLUT is useful for applications in which a limited number of different colors is required (e.g., computer graphics and bit–mapped text). The CLUT technique allows storing a maximum of 256 different colors in RGB, where each component has 6–bit accuracy (RGB666). This gives a total of 2**18 (262144) possible colors. To comply with RGB777, one LSB of 0 is added. The CLUT is divided into four banks (banks 0 to 3), see Figure 7–2, with each bank having 64 entries. The colors for the CLUT are loaded via the CLUT color registers (h80 – hBF) after the appropriate bank has been selected via the CLUT bank register (hC3). After the colors have been stored, using the control mechanism, the required color can be obtained by addressing it.



Where BS = Bank Select (set in CLUT bank register hC3).

Figure 7–2. CLUT Organization

Control–data entered via channel 1 can load banks 0 to 3. Control–data entered via channel 2 can load banks 2 and 3. The address is always in the range 0 – 63: CLUT 0 – 63. To be able to address all 256 entries, a CLUT bank selection is used. This CLUT bank selection is independent for both channels; so it is possible to simultaneously (i.e., in the same line) load colors to banks 0 and 1 via channel 1 and to load colors to banks 2 and 3 via channel 2. It is not possible to simultaneously load colors to banks 2 and 3 via both channels.

Pixel–data entering via channel 1 can address all banks. Pixel–data entering via channel 2 can address banks 2 and 3 only. Depending on the number of bits that can be used to address colors, different coding methods are distinguished: CLUT8 (256 colors), CLUT7 (128 colors), CLUT7+7 (2 x 128 colors), CLUT4 (16 colors). See Figure 7–3 for the pixel representation. CLUT7+7 means that 7 address bits are available to address either banks 0 and 1 or banks 2 and 3, depending on what banks are selected. CLUT8 and CLUT7+7 are not available for channel 2. When channel 1 uses CLUT8 or CLUT7+7, channel 2 has no CLUT mode.

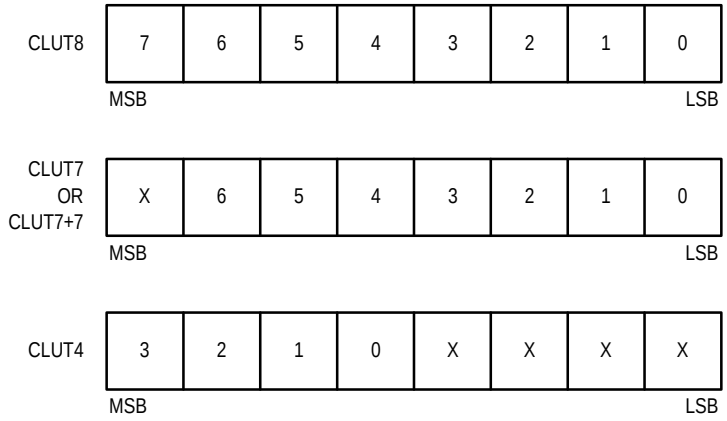


Figure 7–3. Data Structure of Input CLUT Pixel

CLUT4 can only be used in double resolution mode (768 pixels/line).

7.3 DIRECT RGB555

Direct RGB555 (R, G, and B in 5 bits each) is intended mainly for computer graphic images. It passes the pixel data of both channels directly to plane B. To comply with RGB777, two LSBs of 0 are added. To control RGB555 pixel transparency, a transparency bit (T) is used. Figure 7–4 shows the data structure of an RGB555 pixel.

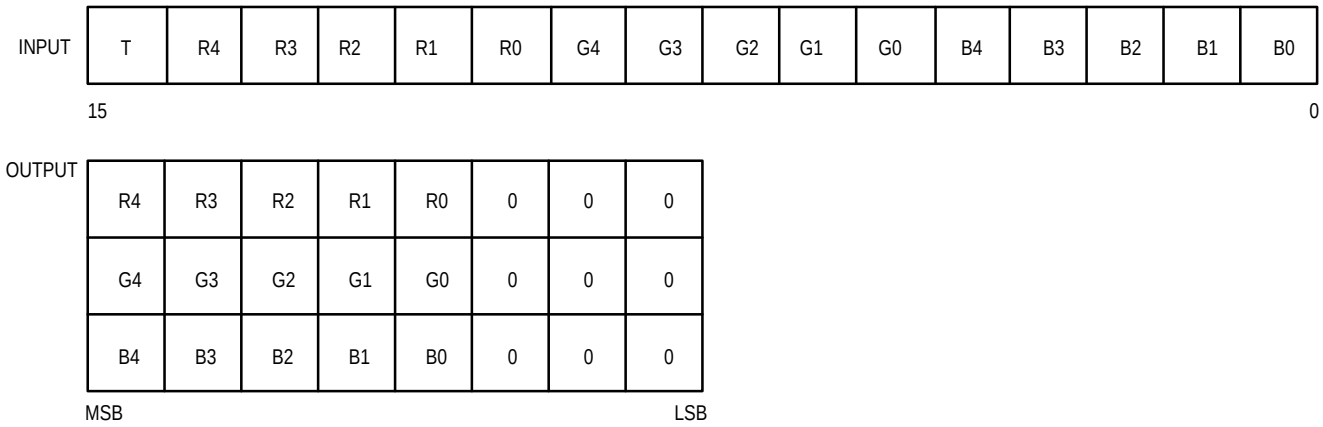


Figure 7–4. Data Structure of RGB555 Input and Output Pixel

7.4 DECODING COMBINATIONS

The available display modes for planes A and B are not identical, see Tables 7–2 and 7–3. Not every combination of display modes of plane A and plane B is possible. The combination of coding methods is restricted according to Table 7–4.

Table 7–2. Display Modes for Plane A

Channel	Coding Method	CM1	Resolution
CH1	OFF	x	x
CH1	CLUT8	0	Normal
CH1	CLUT7+7	0	Normal
CH1	CLUT7	0	Normal
CH1	CLUT4	1	Double
CH1	DYUV	0	Normal

Table 7–3. Display Modes for Plane B

Channel	Coding Method	CM1	Resolution
CH2	OFF	x	x
CH2	CLUT7	0	Normal
CH2	CLUT4	1	Double
CH2	DYUV	0	Normal
CH1 + 2	RGB555	0	Normal

Table 7–4. Possible Combinations of Display Modes

	Plane A					
Plane B	**Off**	**CLUT8**	**CLUT7+7**	**CLUT7**	**CLUT4**	**DYUV**
OFF	Y	Y	Y	Y	Y	Y
CLUT7	Y	N	N	Y	Y	Y
CLUT4	Y	N	N	Y	Y	Y
DYUV	Y	Y	Y	Y	Y	Y
RGB555	Y	N	N	N	N	N

Y = Possible Combination N = Not Possible

7.5 BACKDROP

The backdrop plane can have 16 different colors, see Table 7–5. This BD plane is positioned behind the cursor and planes A and B. The color is programmed by writing via CH1 to register hD8. The possible colors are listed in Table 7–5 along with the complimentary colors which can be used for the cursor.

Table 7–5. Possible Cursor and Background Colors

Cursor		Background	
Y R G B	**Color**	**Complementary Color**	**Y R G B**
0 0 0 0	Black	Grey	0 1 1 1
0 0 0 1	hb – Blue	hb – Yellow	0 1 1 0
0 0 1 0	hb – Green	hb – Magenta	0 1 0 1
0 0 1 1	hb – Cyan	hb – Red	0 1 0 0
0 1 0 0	hb – Red	hb – Cyan	0 0 1 1
0 1 0 1	hb – Magenta	hb – Green	0 0 1 0
0 1 1 0	hb – Yellow	hb – Blue	0 0 0 1
0 1 1 1	Grey	Black	0 0 0 0
1 0 0 0	Black	White	1 1 1 1
1 0 0 1	Blue	Yellow	1 1 1 0
1 0 1 0	Green	Magenta	1 1 0 1
1 0 1 1	Cyan	Red	1 1 0 0
1 1 0 0	Red	Cyan	1 0 1 1
1 1 0 1	Magenta	Green	1 0 1 0
1 1 1 0	Yellow	Blue	1 0 0 1
1 1 1 1	White	Black	1 0 0 0

NOTE: hb = Half Brightness.
Full Brightness = level 230, Half = level 122, Black = level 16.

7.6 CURSOR

The cursor is shown in the cursor plane. The dimension of the cursor plane is 16 x 16 pixels. A 1 in the cursor plane activates the cursor color for that pixel, while a 0 sets it to transparency. The resolution of the cursor can be switched between normal resolution and double resolution. The cursor has one color. The cursor plane can be enabled or disabled.

The cursor color is set by programming the cursor control register via CH#1 at location hCE. Along with setting the color, the cursor enable, the on/off period, and cursor resolution can be programmed via this same register. The cursor can be set to blink with programmable on and off periods. Both periods can be specified by three bits. The on/off periods equal multiples of 12 times the TV field period (200 ms in 60 Hz system; 240 ms in 50 Hz system). If on and off periods are both set to 0, then the cursor is on indefinitely. The blink type may be “on/off” or “normal color/complementary color”.

The cursor position is related to the position of the upper–left pixel in the cursor plane and is programmed via CH#1 in the cursor position register at location hCD. The X–position of this pixel is specified by the number of double resolution pixels between this pixel and the left border of the full screen display. The Y–position is specified by the number of lines between this pixel and the upper part of the full screen display.

Cursor control and position can be programmed during horizontal and/or vertical retrace periods.

The cursor pattern is programmed via CH#1 at location hCF.

8
VISUAL EFFECTS

8.1 PLANES

The real–time decoder provides four planes, represented in RGB components. These planes are:

- Cursor
- Image Plane A
- Image Plane B
- Backdrop

The two image planes can originate from four types of coding:

- OFF
- Direct RGB555
- CLUT
- DYUV

Here OFF means a black image (level 16, where 235 is the nominal peak white level).

The cursor and backdrop each consist of one color, both of which are programmable.

The visual effects combine the separate planes into one final image.

8.2 PIXEL HOLD

The pixel hold allows plane A and/or plane B to be viewed at reduced resolution. The pixel hold function operates after the pixel codes have been decoded to RGB. Therefore, it can be used for all images, independent of their coding method, either by DYUV, CLUT, or RGB. Both image planes contain such a pixel–hold mechanism that can act independently of the other plane. Every Nth pixel RGB value is held for that pixel and the next N–1 pixels, where N is the pixel hold factor. This produces a mosaic–type effect on the image. See Figure 8–1 for an example.

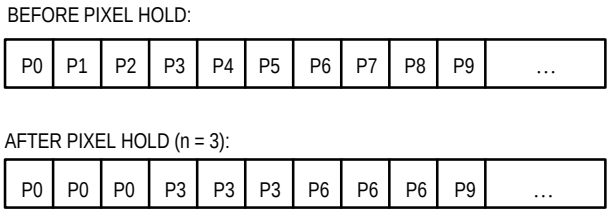


Figure 8–1. Pixel Hold Example for N = 3

The pixel hold function causes a “mosaic” or “granulation” effect in the horizontal direction (i.e., the resolution is lowered without the image size changing).

The pixel hold factor is programmed via the mosaic pixel hold factor register located at location hD9 for plane A and hDA for plane B. Plane A is programmed via CH#1 and Plane B is programmed via CH#2.

The pixel hold factor can be any value from 2 to 255. The pixel hold factor is effective at both normal resolution and double resolution according to the resolution.

8.3 REGIONS

Within the image planes, regions can be defined by means of two region flags, called flag RF0 and flag RF1. Two region flags allow regions to overlap (see Figure 8–2). These flags can be set and reset by eight region control registers. These registers are loaded during the horizontal and vertical retrace periods, using the control mechanism.

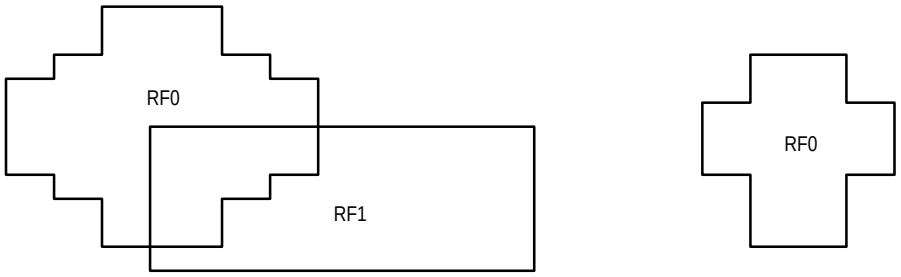


Figure 8–2. Example Showing Overlapping and Non–overlapping Regions

The region control registers 0 – 7 can control the two region flags in two modes. In the first mode, registers 0 – 3 are linked to region flag 0 and registers 4 – 7 are linked to region flag 1 (see Figure 8–3). In the second mode, the eight registers are explicitly linked to a region flag (see Figure 8–4). The first mode allows the two region flags to be changed at the same position. The selection of the mode used is done in the “image coding method register” by the NR bit.

RF0:

REGION CONTROL REGISTER	0	1	2	3
HORIZONTAL POSITION	X0	X1	X2	X3

CONSTRAINT: X0 < X1 < X2 < X3

RF1:

REGION CONTROL REGISTER	4	5	6	7
HORIZONTAL POSITION	X4	X5	X6	X7

CONSTRAINT: X4 < X5 < X6 < X7

Figure 8–3. Implicit Control of Region Flags (NR = 1)

REGION CONTROL REGISTER	0	1	2	3	4	5	6	7
REGION FLAG	RF0/ RF1	RF0/ RF1	RF0/ RF1	RF0/ RF1	RF0/ RF1	RF0/ RF1	RF0/ RF1	RF0/ RF1
HORIZONTAL POSITION	X0	X1	X2	X3	X4	X5	X6	X7

CONSTRAINT: X0 < X1 < X2 < X3 < X4 < X5 < X6 < X7

Figure 8–4. Explicit Control of Region Flags (NR = 0)

The region control registers are examined on their specified horizontal position sequentially. Depending on the mode, this sequence ranges from 0 to 7 or from 0 to 3 and from 4 to 7. When a match between the specified horizontal position and the actual horizontal pixel count is found, the corresponding command is executed. This command can set/reset the corresponding or specified region flag, change one of the two weight factors, or end the region control for the line (no further registers are examined). So for all registers to be noticed, the position sequence stored in the region control registers has to be ascending (see Figures 8–3 and 8–4). The horizontal position is specified with respect to the double rate clock (maximally 768 pixels per line). The region flags are automatically reset before the start of each line.

8.4 TRANSPARENCY

Transparency of planes can be obtained by:

- Disabling
- Regions
- Color Key
- Transparency Bit

The image planes (A/B) and the cursor can be made transparent by disabling them.

Parts of both image planes can be made transparent depending on the state of one of the two region flags.

For both image planes a color key is available for CLUT decoded images. The state of the color key is determined on a pixel basis. Every CLUT decoded pixel is compared to an in RGB666 specified color; the so–called transparent color. If all bits match or if the corresponding mask bit is true, the color key is true.

A transparency bit is available from every direct RGB555 coded pixel.

8.5 OVERLAY AND MIXING

The four planes must be combined into one image. This is achieved by overlay and mixing. Overlay means that only one plane at a time is shown. This is done by giving the planes an order and by using transparency, a plane can only be seen if it is not transparent and all higher order planes are transparent. The order is from high to low cursor, plane A/plane B, backdrop. The order of A and B can be selected A in front of B or B in front of A (see Figure 8–5).

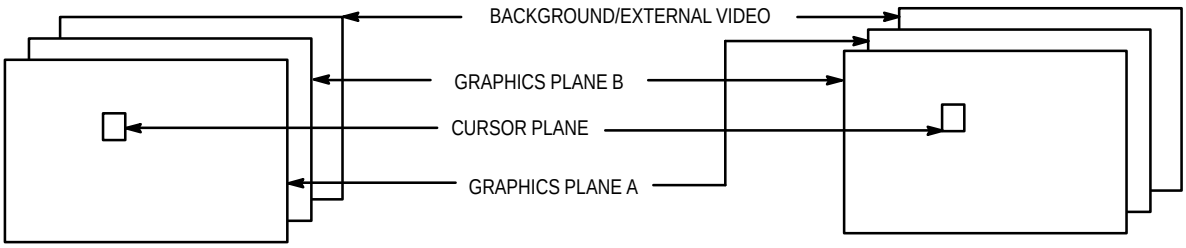


Figure 8–5. Plane Order

It is also possible to overlay external video as an alternative for backdrop. This is done by using an external switch operated by the VDSC pin VSD or VSA. The VSD signal is synchronous to the digital output, whereas VSA is delayed one CLK2 clock cycle to counteract for a delay caused by a clocked DAC. VSD and VSA are active if enabled by the EV–bit of the “image coding method register” and when the backdrop is shown.

Mixing is applied to image planes A and B. They are weighted and added (see Figure 8–6). The weighting and adding is done preserving the black level (level 16):

$$AB = lim[(A) 16) * WEIGHT\_A/64 + (B) 16) * WEIGHT\_B/64 + 16]$$

When the result exceeds level 255, the result is fixed at 255. When the result is less than level 0, the result is fixed at 0. Planes A and B are made transparent for overlay by making them black.

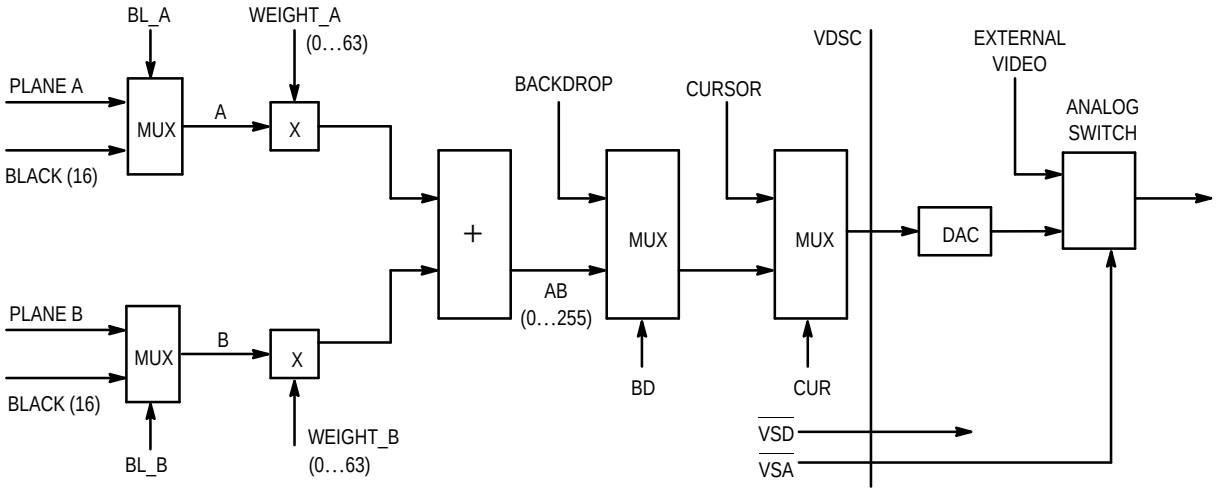


Figure 8–6. Overlay and Mixing — One Color Component

Weight factors are programmed via the weight registers. The weight factors can be dynamically changed by the region control registers at the position they indicate.

Backdrop and cursor can be overlaid on the combined planes A and B.

During horizontal and vertical blanking of the video a constant level is set on each component.

For 50 Hz display this level is 16 and for 60 Hz display 0.

9
REGISTER DESCRIPTION

This section describes the internal registers of the VDSC. Below is a chart that describes the registers that affect video plane 1 and plane 2. Table 9–1 shows the various registers and which bits in those registers can be read or written.

Table 9–1. Register Summary

Channel 1

CSR1R	Status Register 1	Read	h4FFFF1
CSR1W	Control Register 1	Write	h4FFFF0
DCR1	Display Command Register 1	Write	h4FFFF2
VSR1	Video Start Register 1	Write	h4FFFF4
DDR1	Display Decoder Register 1	Write	h4FFFF8
DCP1	DCA Pointer 1	Write	h4FFFFA

Channel 2

CSR2R	Status Register 2	Read	h4FFFE1
CSR2W	Control Register 2	Write	h4FFFE0
DCR2	Display Command Register 2	Write	h4FFFE2
VSR2	Video Start Register 2	Write	h4FFFE4
DDR2	Display Decoder Register 2	Write	h4FFFE8
DCP2	DCA Pointer 2	Write	h4FFFEA

9.1 REGISTER MAP

Table 9–2. Register Bitmap

Name	15	14	13	12	10	9	8	7	6	5	4	3	2	1	0
CSR1R	x	x	x	x	x	x	x	DA	x	PA	x	x	x	x	x
CSR2R	x	x	x	x	x	x	x	x	x	x	x	x	IT1	IT2	BE
CSR1W	DI1	x	x	x	x	DD1	DD2	x	x	TD	x	DD	x	ST	BE
CSR2W	DI2	x	x	x	x	x	x	x	x	x	x	x	x	x	x
DCR1	DE	CF	FD	SM	CM1	0	IC1	DC1	x	x	*	*	*	*	*
DCR2	x	x	x	x	CM2	0	IC2	DC2	x	x	*	*	*	*	*
DDR1	x	x	x	x	MF1	MF2	FT1	FT2	x	x	*	*	*	*	*
DDR2	x	x	x	x	MF1	MF2	FT1	FT2	x	x	*	*	*	*	*
VSR1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
VSR2	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
DCP1	*	*	*	*	*	*	*	*	*	*	*	*	*	x	x
DCP2	*	*	*	*	*	*	*	*	*	*	*	*	*	x	x

9.1.1 Control Registers CSR1W and CSR2W

These registers control the system related functions of the VDSC. They are reset to 0 during the initialization sequence. This is the default configuration.

CSR1W (write, 4FFFF0)

Table 9–3. Control Register 1 — Write, 4FFFF0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DI1	—	—	—	—	—	DD1	DD2	—	—	TD	—	DD	—	ST	BE

DI1 (Disable Interrupts) When set to 1, disables the propagation to the $\overline{\text{INT}}$ pin for the IT1 bit (see STATUS register). This bit does not disable the IT1 bit.

DD1 – DD2 ($\overline{\text{DTACK}}$ delay) Active when DD = 1. These two bits permit four different delays for the $\overline{\text{DTACK}}$ generation when the CPU accesses the system ROM.

Table 9–4. $\overline{\text{DTACK}}$ Delay

DD	DD1	DD2	CLK Cycles
0	x	x	11 ≥ 12
1	0	0	3 ≥ 4
1	0	1	5 ≥ 6
1	1	0	7 ≥ 8
1	1	1	9 ≥ 10

TD (Type of DRAM) to be 0 for 256K x 4 and 256K x 16 devices and 1 for 1M x 4 devices.

DD $\overline{\text{DTACK}}$ Delay for the ROM. See DD1 – DD2.

ST (Standard bit) When set to 1, this bit permits a resolution modification in order to display images which don't have the resolution indicated by the DCR1 register. When set to 1, the effect is:

Vertical resolution: In 50 Hz mode (FD = 0), the resolution is shortened by 20 lines at the top and 20 lines at the bottom. Images created in a 60 Hz system are then directly usable in a 50 Hz system.

Horizontal resolution:

- In 28 MHz, the bit map file is 384 pixels wide instead of 360 pixels. The horizontal resolution is unchanged, but it is possible to display bitmap, run–length or mosaic coded images created with a 30 MHz or 30.2097 MHz system.
- In 30 MHz or 30.2097 MHz, the horizontal resolution is decreased from 384 pixels to 360 pixels, 12 pixels are masked on either side of the screen.

BE (Bus Error) When set to 1, this bit activates the watchdog timer and enables the BERR generation.

CSR2W (write, 4FFFE0)

Table 9–5. Control Register 2 — Write, 4FFFE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DI2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

DI2 (Disable Interrupts) When set to 1, disables the propagation to the $\overline{\text{INT}}$ pin for the IT2 bit (see STATUS register). This bit does not disable the IT2 bit.

9.1.2 Status Registers CSR1R and CSR2R

These registers are read as a byte and contain the status of the VDSC.

CSR1R (read, 4FFFF1)

Table 9–6. Status Register CSR1R — Read, 4FFFF1

7	6	5	4	3	2	1	0
DA	—	PA	—	—	—	—	—

DA (Display Active) This bit is the vertical display active information. When high, it indicates that the display controller is fetching information from the video memory. It does not change on each horizontal retrace.

PA (Parity) This bit indicates the frame parity when the scan mode is in interlace or interlace field repeat mode. It is 1 for the odd frame and 0 for the even frame.

CSR2R (read, 4FFFE1)

Table 9–7. Status Register CSR2R — Read, 4FFFE1

7	6	5	4	3	2	1	0
—	—	—	—	—	IT1	IT2	BE

IT1 (Interrupt1) This bit can be set to 1 by the ICA/DCA mechanism to generate an interrupt to the CPU. At the same time, the INT pin goes low, if the DI1 bit is set to 1 in the CSR1 register. The IT1 bit and the INT pin will be reset automatically when the CPU reads the status register.

IT2 (Interrupt2) This bit can be set to 1 by the ICA/DCA mechanism to generate an interrupt to the CPU. At the same time, the INT pin goes low, if the DI2 bit is set to 1 in the CSR2 register. The IT2 bit and the INT pin will be reset automatically when the CPU reads the status register.

BE (Bus Error) This bit is set to 1 when a bus error condition has been generated by the watchdog timer. This bit is automatically reset after a status read operation.

9.1.3 Display Command Registers DCR1 and DCR2

The Display Command Registers group control bits for the display and six MSBs of the Video start address.

The eight MSBs are reset to 0 after the RESET sequence.

DCR1 (write, 4FFFF2)

Table 9–8. Display Command Register DCR1 — Write, 4FFFF2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DE	CF	FD	SM	CM1	0	IC1	DC1	—	—	A21	A20	A19	A18	A17	A16

DE (Display Enable) Enables display access to DRAM and enables synchronization outputs when set to 1.

CF (Crystal Frequency) Must be programmed as a function of the crystal oscillator frequency as follows.

Table 9–9. Crystal Frequency

CF	Frequency in MHz
0	28
1	30, 30.2097

FD (Frame Duration) When reset to 0, a 50 Hz scan is generated. When set to 1, a 60 Hz scan frequency is generated.

SM (Scan Mode) This bit is used to select the scan mode.

Table 9–10. Scan Mode

SM	Scan Mode
0	Non–interlace
1	Interlace

CM1 (Color Mode of channel 1) This bit controls the pixel output mode.

Table 9–11. Channel 1 Color Mode

CM1	Bits/Pixel	Pixel Frequency
1	4	CLK/2

IC1 – DC1 (ICA1 – DCA1) These two bits enable the ICA1 and DCA1 mechanisms.

Table 9–12. ICA1/DCA1 Enable

IC1	DC1	ICA1	DCA1
0	x	No	No
1	0	Yes	No
1	1	Yes	Yes

A21 – A16 Most significant bits of the video start address, acting in conjunction with the VSR.

DCR2 (write, 4FFFE2)

Table 9–13. Display Command Register DCR2 — Write, 4FFFE2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	CM2	0	IC2	DC2	—	—	A21	A20	A19	A18	A17	A16

CM2 (Color Mode of channel 2) This bit controls the pixel output mode.

Table 9–14. Channel 2 Color Mode

CM2	Bits/Pixel	Pixel Frequency
0	8	CLK/4
1	4	CLK/2

IC2 – DC2 (ICA2 – DCA2) These two bits enable the ICA2 and DCA2 mechanisms.

Table 9–15. ICA1/DCA1 Enable

IC2	DC2	ICA2	DCA2
0	x	No	No
1	0	Yes	No
1	1	Yes	Yes

A21 – A16 Most significant bits of the video start address, acting in conjunction with the VSR.

9.1.4 Display Decoder Registers DDR1 and DDR2

These registers contain control bits for the display, files to be displayed, and the six MSB bits of the DCA pointer. All the bits, except the six LSBs, are reset to 0 after the reset sequence.

DDR1 (write, 4FFFF8)

Table 9–16. Display Decoder Register 1 — Write, 4FFFF8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	MF1	MF2	FT1	FT2	—	—	A21	A20	A19	A18	A17	A16

MF1 – MF2 (Mosaic Factor) Set the horizontal mosaic factor:

Table 9–17. Channel 1 Mosiac Factor

MF1	MF2	Mosaic Factor
0	0	2
0	1	4
1	0	8
1	1	16

FT1 – FT2 (File type) Indicate the type of file to be displayed:

Table 9–18. Channel 1 Display File Type

FT1	FT2	Display File Type
0	x	Bitmap
1	0	Run–length
1	1	Mosaic

A21 – A16 Most significant bits of the DCA1 pointer.

DDR2 (write,4FFFE8)

Table 9–19. Display Decoder Register 2 — Write, 4FFFE8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	MF1	MF2	FT1	FT2	—	—	A21	A20	A19	A18	A17	A16

MF1 – MF2 (Mosaic Factor) Set the horizontal mosaic factor:

Table 9–20. Channel 2 Mosiac Factor

MF1	MF2	Mosaic Factor
0	0	2
0	1	4
1	0	8
1	1	16

FT1 – FT2 (File type) Indicate the type of file to be displayed:

Table 9–21. Channel 2 Display File Type

FT1	FT2	Display File Type
0	x	Bitmap
1	0	Run–length
1	1	Mosaic

A21 – A16 Most significant bits of the DCA2 pointer.

9.1.5 Video Start Registers VSR1 and VSR2

These 16–bit registers plus some bits in DCR1[5:0]/DCR2[5:0] give a 22–bit video start register address that points to the first byte of the display area that can be located anywhere in the DRAM. Horizontal or vertical rolling subscreens can be implemented anytime by the “reload VSR and stop” ICA or DCA instruction. The VSR is also used as an ICA pointer with the “reload VSR” instruction, which allows indirect addressing inside ICA.

VSR1 (write, 4FFFF4)

Table 9–22. Video Start Register 1 — Write, 4FFFF4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

VSR2 (write, 4FFFE4)

Table 9–23. Video Start Register 2 — Write, 4FFFE4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

9.1.6 DCA Pointers DCP1 and DCP2

These 14–bit registers plus some bits in DDR1[5:0]/DDR2[5:0] give a 20–bit DCA pointer that points to the first long–word of the DCA.

The DCA can thus be located anywhere in the DRAM and the DCA pointer is always long–word aligned.

DCP1 (write, 4FFFFA)

Table 9–24. Display Control Pointer 1 — Write, 4FFFFA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	—	—

DCP2 (write, 4FFFEA)

Table 9–25. Display Control Pointer 2 — Write, 4FFFEA

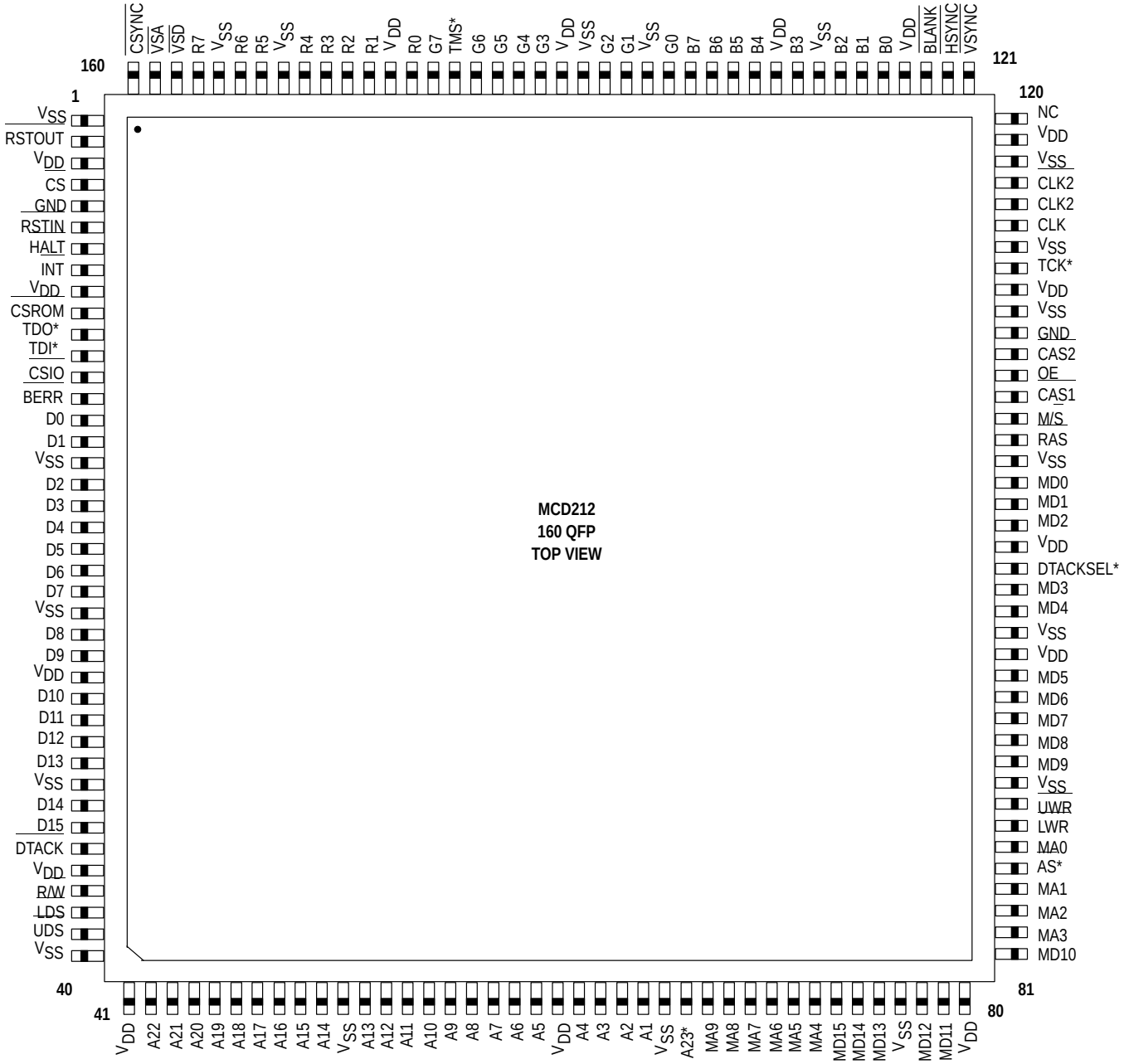
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	—	—

10
PIN LIST

10.1 PIN FUNCTION TABLE

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	V_{SS}	33	D14	65	A1	97	MD4	129	B3
2	$\overline{\text{RSTOUT}}$	34	D15	66	V_{SS}	98	MD3	130	V_{DD}
3	V_{DD}	35	$\overline{\text{DTACK}}$	67	A23	99	DTACKSEL	131	B4
4	$\overline{\text{CS}}$	36	V_{DD}	68	MA9	100	V_{DD}	132	B5
5	GND	37	R/$\overline{\text{W}}$	69	MA8	101	MD2	133	B6
6	$\overline{\text{RSTIN}}$	38	$\overline{\text{LDS}}$	70	MA7	102	MD1	134	B7
7	$\overline{\text{HALT}}$	39	$\overline{\text{UDS}}$	71	MA6	103	MD0	135	G0
8	$\overline{\text{INT}}$	40	V_{SS}	72	MA5	104	V_{SS}	136	V_{SS}
9	V_{DD}	41	V_{DD}	73	MA4	105	RAS	137	G1
10	CSROM	42	A22	74	MD15	106	M/$\overline{\text{S}}$	138	G2
11	TDO	43	A21	75	MD14	107	CAS1	139	V_{SS}
12	TDI	44	A20	76	MD13	108	$\overline{\text{OE}}$	140	V_{DD}
13	$\overline{\text{CSIO}}$	45	A19	77	V_{SS}	109	CAS2	141	G3
14	$\overline{\text{BERR}}$	46	A18	78	MD12	110	GND	142	G4
15	D0	47	A17	79	MD11	111	V_{SS}	143	G5
16	D1	48	A16	80	V_{DD}	112	V_{DD}	144	G6
17	V_{SS}	49	A15	81	MD10	113	TCK	145	TMS
18	D2	50	A14	82	MA3	114	V_{SS}	146	G7
19	D3	51	V_{SS}	83	MA2	115	CLK	147	R0
20	D4	52	A13	84	MA1	116	$\overline{\text{CLK2}}$	148	V_{DD}
21	D5	53	A12	85	$\overline{\text{AS}}$	117	CLK2	149	R1
22	D6	54	A11	86	MA0	118	V_{SS}	150	R2
23	D7	55	A10	87	LWR	119	V_{DD}	151	R3
24	V_{SS}	56	A9	88	UWR	120	NC	152	R4
25	D8	57	A8	89	V_{SS}	121	VSYNC	153	V_{SS}
26	D9	58	A7	90	MD9	122	HSYNC	154	R5
27	V_{DD}	59	A6	91	MD8	123	BLANK	155	R6
28	D10	60	A5	92	MD7	124	V_{DD}	156	V_{SS}
29	D11	61	V_{DD}	93	MD6	125	B0	157	R7
30	D12	62	A4	94	MD5	126	B1	158	$\overline{\text{VSD}}$
31	D13	63	A3	95	V_{DD}	127	B2	159	$\overline{\text{VSA}}$
32	V_{SS}	64	A2	96	V_{SS}	128	V_{SS}	160	$\overline{\text{CSYNC}}$

10.2 PIN CONFIGURATION



NOTE: Pin differences between the MCD211 and MCD212 are denoted with *.

11
ELECTRICAL SPECIFICATION

11.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	– 0.5	+ 7.0	V
Input Voltage	V_I	– 1.5	V_{DD} + 1.5	V
Output Voltage	V_O	– 0.5	V_{DD} + 0.5	V
Output Current	I_O	—	± 25	mA
Power Dissipation	P_D	—	1200	mW
Operating Temperature	T_{opr}	0	+ 70	°C
Storage Temperature	T_{stg}	– 65	+ 150	°C

Test Conditions: V_{SS} = 0 V, T_A = 70 °C.

11.2 DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0° – 70°C

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Supply Current	I_{DD}	$V_I = V_{DD}$ or V_{SS} CLK at 30.3 MHz	—	220	mA
Input Voltage (CMOS input)	V_{IH} V_{IL}		0.7 V_{DD} —	— 0.3 V_{DD}	V
Input Voltage (TTL input)	V_{IH} V_{IL}	V_{DD} = 4.5 V V_{DD} = 5.5 V V_{DD} = 5.5 V	2.0 2.2 —	— — 0.8	V
CMOS Schmitt Trigger Input Voltage	V_{T+} V_{T-}	V_{DD} = 4.5 V – 5.5 V	2.0 1.5	3.4 2.6	V
Hysteresis — Schmitt CMOS		V_{DD} = 4.5 V – 5.5 V	0.11 V_{DD}	0.18 V_{DD}	V
Input Leakage Current	I_{LI}	$V_I = V_{DD}$ or V_{SS}*	– 1	1	µA
Output Voltage (4 mA Output Type)	V_{OH} V_{OL}	I_O = – 4 mA, V_{DD} = 4.5 V I_O = 4 mA, V_{DD} = 4.5 V	3.7 —	— 0.4	V
Output Voltage (8 mA Output Type)	V_{OH} V_{OL}	I_O = – 8 mA, V_{DD} = 4.5 V I_O = 8 mA, V_{DD} = 4.5 V	3.7 —	— 0.4	V
Output Leakage Current	I_{OZ}		– 5	5	µA
Input Capacitance	C_{in}	$V_{DD} = V_I$ = 0 V	—	10	pF
Output Capacitance	C_{out}		—	12.5	pF

* Leakage current is in addition to input current generated in pull–up resistors when the input is held low. (TDI, TMS, TCK have 100 kΩ pull–ups).

11.3 AC CHARACTERISTICS

Conditions:

V_{DD} = 5 V (± 10%)

T_A = 0° – 70°C

V_{OL} = 0.8 V, V_{OH} = 2.2 V

C_{load} ($\overline{DTACK}$, $\overline{INT}$) =130 pF , R_{load} ($\overline{DTACK}$, $\overline{INT}$) = 1 kΩ

C_{load} (D0 – D15, $\overline{RSTOUT}$, $\overline{HALT}$, $\overline{BERR}$) = 130 pF

C_{load} (MA0 – MA9, $\overline{RAS}$, $\overline{CAS1}$, $\overline{CAS2}$) = 100 pF

C_{load} ($\overline{CSIO}$, $\overline{CSROM}$, MD0 – MD15) = 50 pF

C_{load} (CLK2, $\overline{CLK2}$, $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{CSYNC}$, $\overline{BLANK}$, $\overline{UWR}$, $\overline{LWR}$

RO – R7, G0 – G7, B0 – B7, $\overline{VSA}$, $\overline{VSD}$) = 75 pF

TIMING

No.	Parameter	Min	Max	Unit	Note
1	CLK Period	32	—	ns	
2	CLK High Time	13	—	ns	
3	CLK Low Time	13	—	ns	
4	CLK High to CLK2	0	25	ns	
5	CLK High to $\overline{CLK2}$	0	25	ns	
6	CLK2 Low to $\overline{CLK2}$ High	– 5	6	ns	
7	CLK2 Low to R0 – R7, G0 – G7, B0 – B7, $\overline{VSYNC}$, $\overline{HSYNC}$, $\overline{CSYNC}$, $\overline{BLANK}$5	4	26	ns	
8	$\overline{CLK2}$ High to R0 – R7, G0 – G7, B0 – B7	5	27	ns	
9	$\overline{CLK2}$ High to $\overline{VSYNC}$, $\overline{HSYNC}$, $\overline{CSYNC}$, $\overline{BLANK}$	5	26	ns	
10	CLK2 Low to $\overline{VSD}$, $\overline{VSA}$	5	25	ns	

TIMING (continued)

No.	Parameter	Min	Max	Unit	Note
11	CLK2 High to VSD, VSA	5	25	ns	
12	OE Low to R0 – R7, G0 – G7, B0 – B7 Three–State	5	23	ns	
13	OE High to R0 – R7, G0 – G7, B0 – B7 Active	5	23	ns	
14	Address to U/LDS Low (Read)	0	—	ns	
15	U/LDS High to Address Invalid (Read)	5	—	ns	
16	U/LDS Low to R/W High (Read)	—	25	ns	
17	U/LDS Low to CS Low (Read)	—	25	ns	
18	U/LDS High to R/W Hold (Read)	5	—	ns	
19	U/LDS Low to DTACK Low (DRAM Read)	235	320	ns	1
20	U/LDS Low to DTACK Low (Register Read)	75	135	ns	1
21 21a	U/LDS High to DTACK High (Three–State) DTACK Active High Time	0 TBD	43 TBD	ns	
22 22a	DTACK Low to Data Valid (Read) – Pin 99 Low DTACK Low to Data Valid (Read) – Pin 99 High	— —	40 32	ns	2
23 23a	U/LDS High to Data Invalid (Read) U/LDS High to Data Three–State (Read)	0 —	— 40	ns	
24	Address to U/LDS Low (Write)	0	—	ns	
25	U/LDS High to Address Invalid (Write)	0	—	ns	
26 26a	U/LDS Low to R/W Low (Write) U/LDS Low to CS Low (Write)	— —	25 25	ns	
27	U/LDS High to R/W High (Write)	0	—	ns	
28	Data Valid to U/LDS Low (Write)	0	—	ns	
29	U/LDS High to Data Invalid (Write)	0	—	ns	
30 30a	U/LDS Low to DTACK Low (DRAM Write) U/LDS Low to DTACK Low (Register Write)	45 75	105 135	ns	1 1
31	U/LDS High to DTACK Three–State (Write)	0	43	ns	
32	U/LDS Low to CSROM or CSIO Low	—	17	ns	
33	U/LDS High to CSROM or CSIO High	—	13	ns	
34	U/LDS Low to DTACK for ROM Low	11 + d	43 + d	ns	3
35	U/LDS High to DTACK for ROM High	0	50	ns	
36	RAS High Pulse Duration (t_{RP})	65	—	ns	
37	RAS Low Pulse Duration (t_{RAS})	90	—	ns	
38	CAS High Pulse Duration (t_{CP})	20	—	ns	
39	CAS Low Pulse Duration (t_{CAS})	30	—	ns	
40	CAS High to RAS Low Delay (t_{CRP})	50	—	ns	
41	RAS Low to CAS Low Delay (t_{RCD})	60	—	ns	

NOTES:

1. These figures are valid for free–run. If video is enabled the max delay increases with a maximum of 16 CLK periods.
2. This timing is switchable using Pin 99 and is valid for Video Channel and DRAM accesses
   Pin 99 – Low 40 ns (max) advance (68000/070/340/341–16)
   Pin 99 – High 32 ns (max) advance (68340/341–25)
   Timing of DTACK for ROM accesses is unchanged.
3. The delay d is the delay mentioned in the Delay Times Table and depends on the CLK frequency and the programmed value DD, DD1, DD2.

TIMING (continued)

No.	Parameter	Min	Max	Unit	Note
42	$\overline{CAS}$ Low to $\overline{RAS}$ High Delay (t_{RSH})	25	—	ns	
42	$\overline{CAS}$ Low to $\overline{RAS}$ High Delay (t_{RSH})	25	—	ns	
43	$\overline{RAS}$ Low to $\overline{CAS}$ High Delay (t_{CSH})	95	—	ns	
43	$\overline{RAS}$ Low to $\overline{CAS}$ High Delay (t_{CSH})	95	—	ns	
44	$\overline{RAS}$ Low to Column Address Delay (t_{RAD})	30	—	ns	
45	Row Address Set–Up Time (t_{ASR})	15	—	ns	
46	Row Address Hold Time (t_{RAH})	30	—	ns	
47	Column Address Set–Up Time (t_{ASC})	20	—	ns	
48	Column Address Hold Time (t_{CAH})	25	—	ns	
49	Data Set–Up Time to $\overline{CAS}$ Low (t_{DS})	100	—	ns	
50	Data Hold Time to $\overline{CAS}$ Low (t_{DH})	40	—	ns	
51	Read Set–Up Time to $\overline{CAS}$ Low (t_{RCS})	75	—	ns	
52	Read Hold Time to $\overline{CAS}$ High (t_{RCH})	35	—	ns	
53	Write Set–Up Time to $\overline{CAS}$ Low (t_{WCS})	70	—	ns	
54	Write Hold Time to $\overline{CAS}$ Low (t_{WCH})	75	—	ns	
55	$\overline{RAS}$ Low to Data Valid (t_{RAC})	—	90	ns	
56	$\overline{CAS}$ Low to Data Valid (t_{CAC})	—	21	ns	
57	Column Address to Data Valid (t_{AA}) RAS Cycle Time CAS Cycle Time	 150 50	 45 45	ns	
58	$\overline{CAS}$ High to Data Invalid (t_{OFF})	0	—	ns	
59	Refresh Period 1M (t_{RFSH})	9	—	ns	
60	Refresh Period 256K x 4 and 256K x 16 (t_{RFSH})	5	—	ns	
61	$\overline{RSTIN}$ Low to $\overline{RSTOUT}$/$\overline{HALT}$ Low	75	140	ns	
62	$\overline{RSTIN}$ Low Time	2	—	ns	
63	$\overline{RSTIN}$ High to $\overline{RSTOUT}$ High	150	160	ns	
64	$\overline{RSTOUT}$ High to $\overline{HALT}$ High	59	64	ns	
65	U/$\overline{LDS}$ High to $\overline{BERR}$ High	TBD	TBD	ns	
66	DTACKSEL to $\overline{DTACK}$ Delay Active	TBD	TBD	ns	
67	$\overline{DTACK}$ Low to Data Invalid (Write)	TBD	TBD	ns	

DELAY TIMES

			CLK = 28 MHz		CLK = 30 MHz		CLK = 30.2097 MHz		
DD0	DD1	DD2	Min	Max	Min	Max	Min	Max	Units
0	x	x	400	470	375	445	370	440	ns
1	0	0	115	185	110	175	105	170	ns
1	0	1	185	260	175	240	170	235	ns
1	1	0	260	330	240	310	235	305	ns
1	1	1	330	400	310	375	305	370	ns

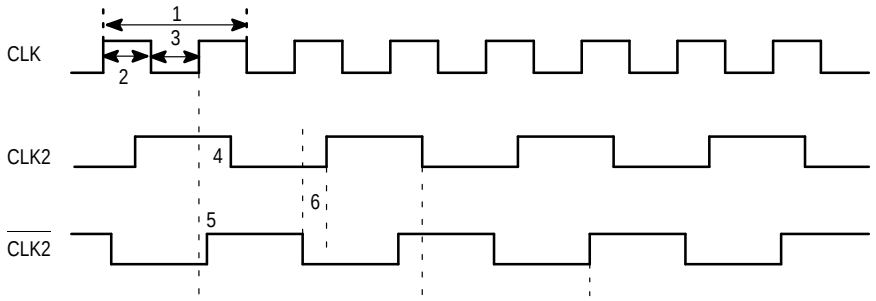
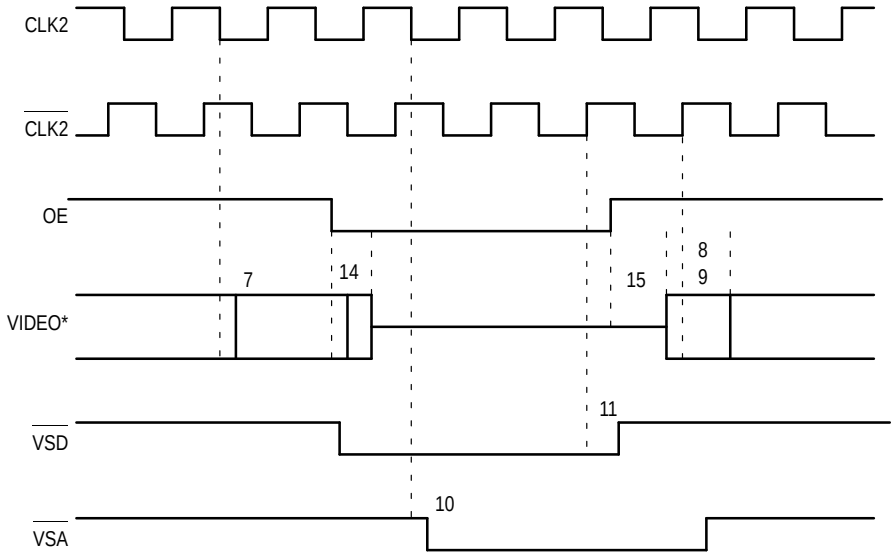


Figure 11–1. Clock Timing



* Video: R0 – R7, G0 – G7, B0 – B7, VSYNC, HSYNC, BLANK

Figure 11–2. Video Timing

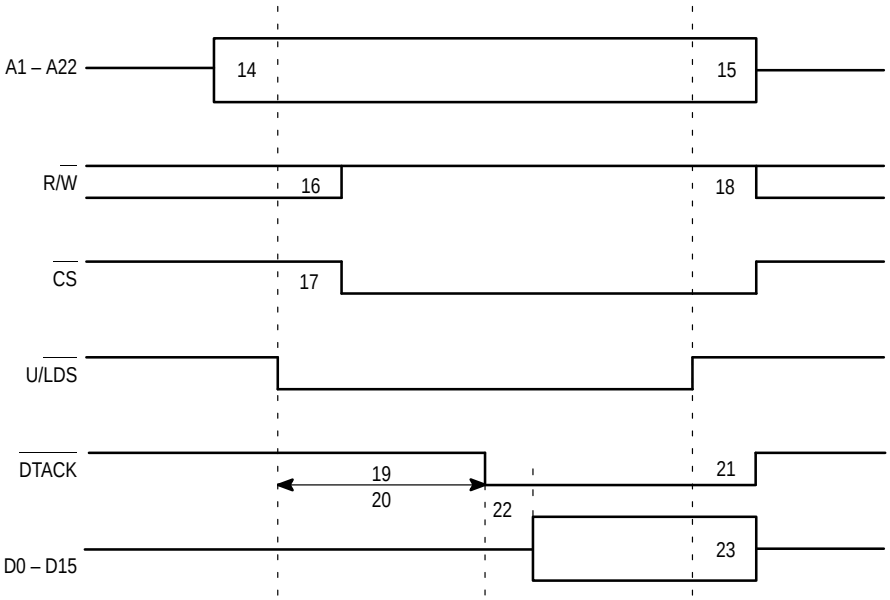


Figure 11–3. CPU Read Cycle Timing

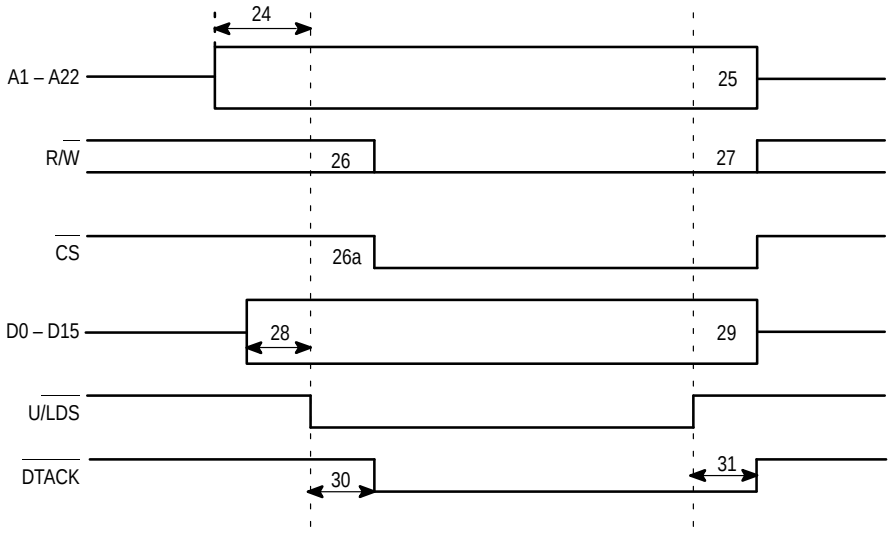


Figure 11–4. CPU Write Cycle Timing

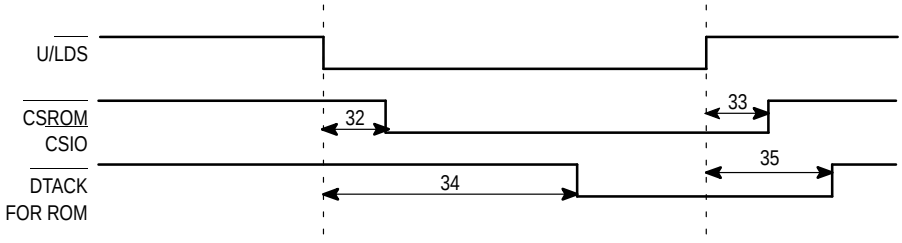


Figure 11–5. System Timing

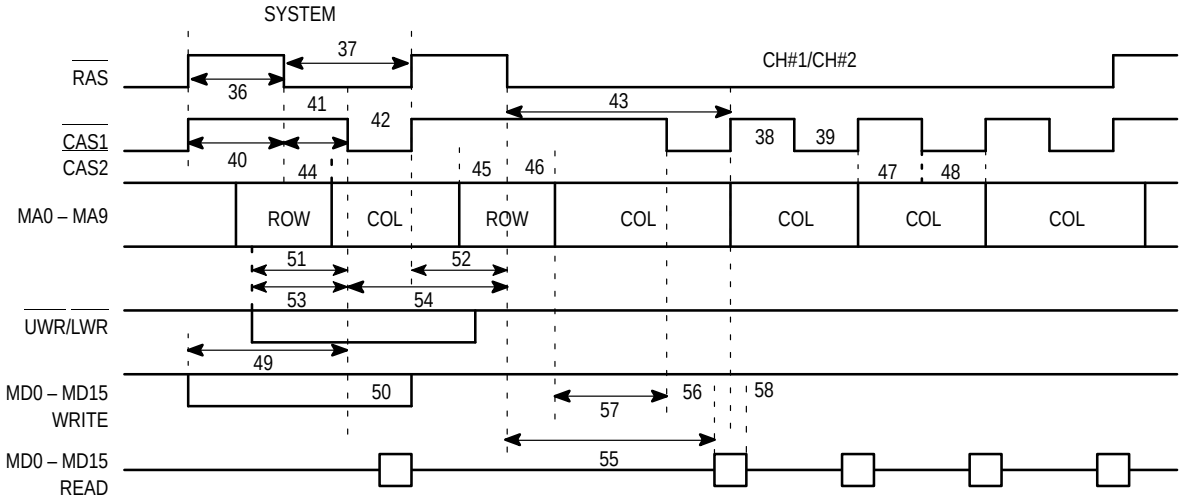


Figure 11–6. DRAM Timing

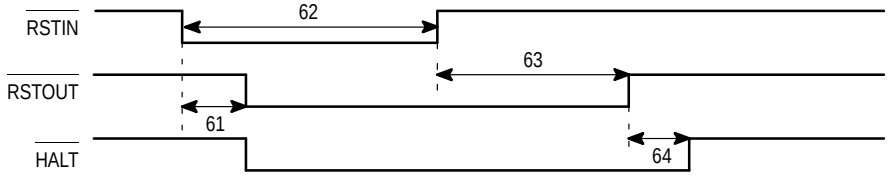
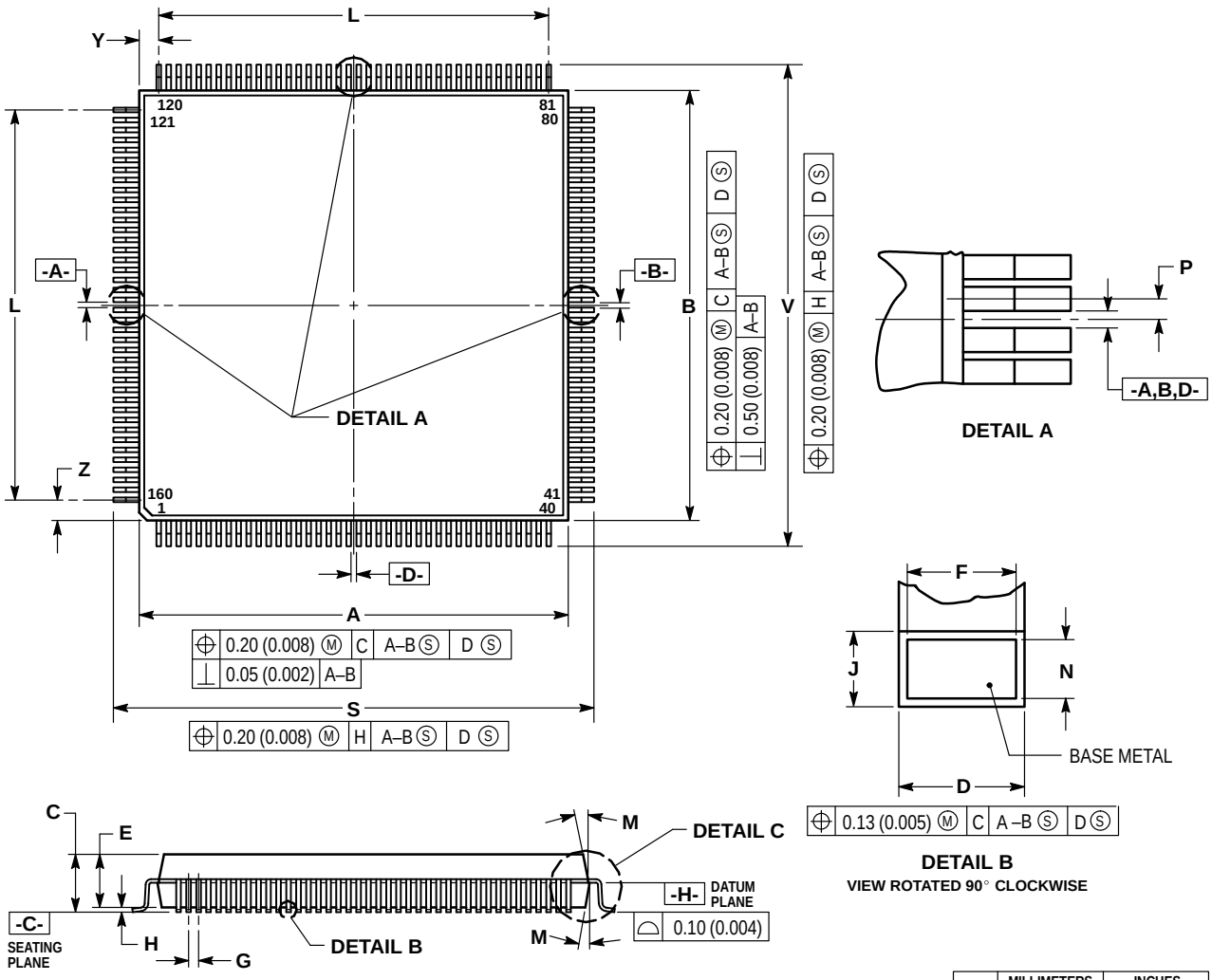


Figure 11–7. Reset and Halt Timing

12
PACKAGE DIMENSIONS

The VDSC is a surface mounting component and is housed in a 160–pin Plastic Quad Flat Package (QFP).

QUAD FLAT PACK (QFP)
CASE 1007–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, –B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	0.152
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.650 BSC		0.0256 BSC	
H	0.25	0.35	0.010	0.012
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 REF		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.0130 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.40	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

A
APPENDIX

A.1 DELTA YUV ENCODING

The MCD212 does not do the encoding of any image but this section is included as an informational reference to the process of image coding using the delta YUV (DYUV) process. Natural images are particularly well suited to DYUV encoding since there is usually little difference in the color or intensity of adjacent pixels. This makes for a very efficient coding of an image.

The process to produce a normal resolution DYUV image (384 x 240) begins with a high resolution RGB image (768 x 480). The process to change from RGB to YUV uses the equations below:

$$Y = 0.299 * R + 0.587 * G + 0.114 * B$$
$$U = 0.564 * (B - Y)$$
$$V = 0.713 * (R - Y)$$

The normalized, eight–bit values of the components are obtained from the following equations:

$$|Y| = 219 * Y + 16$$
$$|U| = 224 * U + 128$$
$$|V| = 224 * V + 128$$

In order to solve aliasing problems, the image is filtered, typically with a FIR filter to maintain the correct phase and then is subsampled by a factor of two in both the horizontal and vertical directions for the Y component. For the U and V components, the subsampling is by a factor of two in the vertical direction, but by a factor of four in the horizontal direction since the human eye is less sensitive to changes in color as opposed to changes in luminance.

A.2 DELTA CODING

The YUV components are now delta coded in the horizontal direction only. An initial 24–bit absolute value of the first pixel is used as the starting value (8 bits for each component). The YUV component of each sample for the rest of the line is coded using a 16–level quantizer (shown in Table A–1).

Table A–1. 16–Bit Quantization Table

Input Difference		Code	Output Difference
0		0	0
1 2	– (254 ... 255)	1	1
3 6	– (250 ... 253)	2	4
7 12	– (244 ... 249)	3	9
13 ... 21	– (235 ... 243)	4	16
22 ... 35	– (221 ... 234)	5	27
36 ... 61	– (195 ... 220)	6	44
62 ... 99	– (157 ... 194)	7	79
100 ... 156	– (100 ... 156)	8	128
157 ... 194	– (62 ... 99)	9	177
195 ... 220	– (36 ... 61)	10	212
221 ... 234	– (22 ... 35)	11	229
235 ... 243	– (13 ... 21)	12	240
244 ... 249	– (7 ... 12)	13	247
250 ... 253	– (3 ... 6)	14	252
254 ... 255	– (1 ... 2)	15	255

Example:

Assume that the first seven pixels of the line (expressed as RGB) are as follows:

0,0,0 16,0,0 0,128,255 128,64,68 232,240,12 0,255,0 0,0,255

Converting to YUV gives:

16,128,128 20,126,135 105,203,63 88,120,156 197,29,141 144,54,35 41,240,110

Then the absolute value of the first pixel (8 bits) is sent for each of the components (shown in hex):

h10,h80,h80

then the delta between the first and second pixels is calculated as 4–bit data from the table above (in hex):

h2,hF,h3

then the delta of the Y component is calculated based on the difference from the last calculated value and the desired value (the U and V are skipped):

h7

next the delta for all components is calculated:

hD,hD,h4

and so on for the rest of the pixels:

h8 h9,h9,h8 h9

In the MCD212, the data is reconstructed as follows:

The first pixel is given by the absolute value:

16,128,128

The second is calculated using the output difference column from the table above:

20,127,137

Then the rest are calculated in the same way:

99	90,118,153	218	139,39,25	60	

Therefore the data for the seven pixels would be stored on disk as follows (in hex):

h10,h80,h80,hF2,h37,hDD,h48,h99,h89