

Agilent ACPM-7831

CDMA 1900, PCS Power Amplifier Module

Data Sheet



Description

The ACPM-7831 is a fully matched CDMA Power Amplifier module. Designed around Agilent Technologies new Enhancement Mode pHEMT (E-pHEMT) process, the ACPM-7831 offers premium performance in a small, easy to use package. Fully matched to 50 Ohms on the input and output allows faster design, less overall system optimization and more reliable performance in production.

The amplifier has excellent ACPR and efficiency performance, at both high and medium

Pout levels, with a single bias control voltage. For lower quiescent current, a dynamic bias control circuit can be used; $V_{ctrl} = 1.2V$ to $2.7V$.

Designed in a surface mount RF package, the ACPM-7831 is cost and size competitive.

The ACPM-7831 is another key component of the Agilent CDMAAdvantage RF chipset.

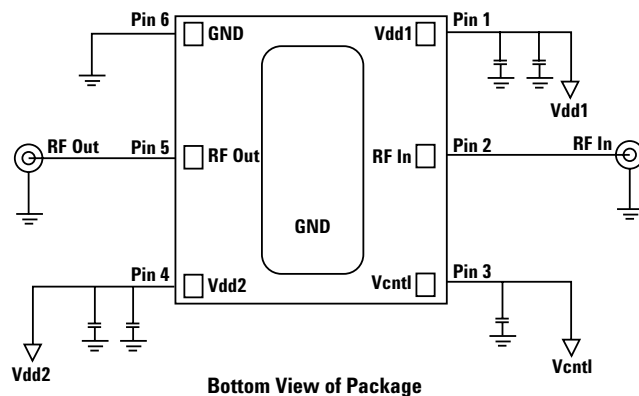
Features

- Operating frequency: 1850–1910 MHz
- 28.5 dBm linear output power @ 3.4 V
- High efficiency: 40% PAE
- Internal 50 ohm matching networks for both RF IN/OUT
- 3.2– 4.2 V linear operation
- cdma2000 1xRTT capable
- Excellent operation at $V_{dd} = 3.0V$
- Only 3 SMT parts needed
- Dynamic bias control or
- Very low quiescent current with single control voltage
- 6.0 x 6.0 x 1.8 mm SMT package

Applications

- 1900 MHz CDMA handsets
- Wireless data terminals

Package Circuit Diagram



Absolute Maximum Ratings^[1]

Parameter	Unit	Value
Vdd Supply Voltage	V	5.0
Power Dissipation ^[2]	W	2.5
Bias Current	A	1.5
Control Voltage (Vcntl)	V	3.0
Amplifier Input RF Power	dBm	10
Junction Temperature	°C	+150
Storage Temperature (case temperature)	°C	-30 to +100

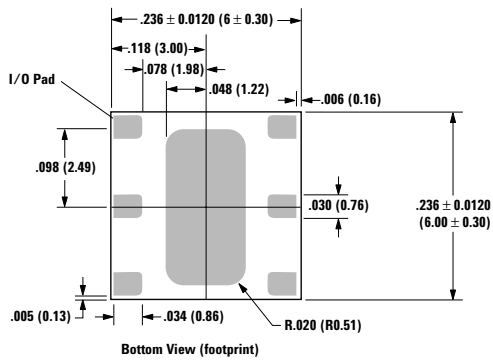
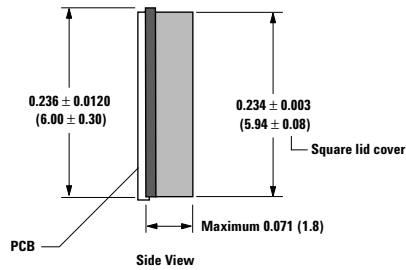
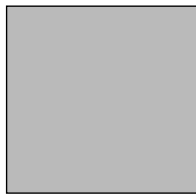
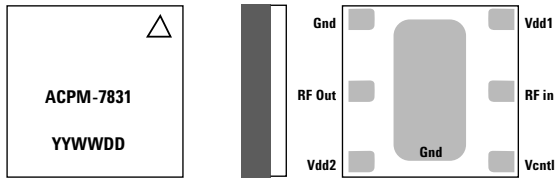
Thermal Resistance^[2] $\theta_{jc} = 28^{\circ}\text{C}/\text{W}$

Recommended operating range of Vdd = 3.2 to 4.2 V, Ta = -30 to +85°C

Notes:

1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Tcase = 25°C

Package Marking and Dimensions



Electrical Characterization Information

All tests are done in 50Ω system at $V_{dd} = 3.4V$, $25^{\circ}C$, unless noted otherwise.

Parameter	Units	Min	Typ	Max	Comments
PCS CDMA					
Frequency Range	MHz	1850		1910	
Gain (Fixed Cntl Voltage)					
($P_{out} = 28.5$ dBm)	dB	24	26		Vcntl= 2.2V
($P_{out} = 13$ dBm)	dB		25		Vcntl= 2.2V
($P_{out} = -5$ dBm)	dB		24		Vcntl= 2.2V
Gain (Dynamic Cntl Voltage)					
($P_{out} = 28.5$ dBm)	dB	24	26		Vcntl= 2.2V
($P_{out} = 13$ dBm)	dB		23		Vcntl= 1.6V
($P_{out} = -5$ dBm)	dB		17		Vcntl= 1.2V
Power Added Efficiency					
$P_{out} = 28.5$ dBm	%	36	40		Vcntl= 2.2V
$P_{out} = 16$ dBm	%		8.5		Vcntl= 1.6V
Total Supply Current	mA		575		$P_{out} = 28.5$ dBm, Vcntl= 2.2V
			100		$P_{out} = 13$ dBm, Vcntl= 1.6V
			30		$P_{out} = -5$ dBm, Vcntl= 1.2V
ACPR @ ± 1.25 MHz offset	dBc/30kHz	-45	-48		$P_{out} \leq 28.5$ dBm
ACPR @ ± 1.98 MHz offset	dBc/30kHz	-53	-55		$P_{out} \leq 28.5$ dBm
Quiescent Current	mA		60		$P_{out} \leq 28.5$ dBm, Vcntl= 2.2V
			40		$P_{out} \leq 13$ dBm, Vcntl= 1.6V
			30		$P_{out} \leq 0$ dBm, Vcntl= 1.2V
Input VSWR ($P_{out} = 28.5$ dBm)			2.0:1		
Input VSWR ($P_{out} = 16$ dBm)			2.5:1		
Noise Figure	dB		3.5		
Noise Power @ 80 MHz offset in 1930–1990 MHz	dBm/Hz		-138		
Stability (Spurious): Load VSWR 5:1	dBc		-50		All phases
Harmonic Suppression					
2Fo	dBc	-40	-30		
3Fo	dBc	-40	-30		

Typical Performance

Data measured in a 50Ω system, Vdd = 3.4V, Vcntl = 2.2V, T = 25°C, Freq = 1880 MHz.

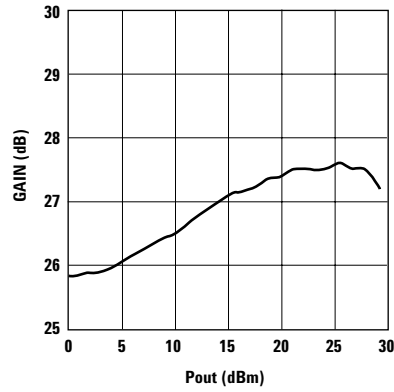


Figure 1. Gain vs. Pout.

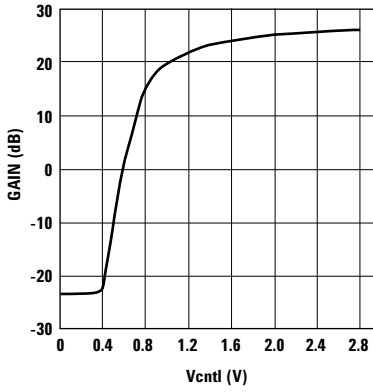


Figure 2. Gain vs. Vcntl.

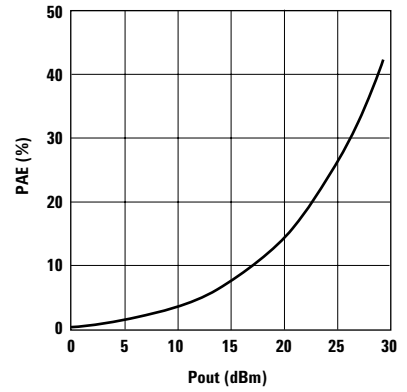


Figure 3. PAE vs. Pout.

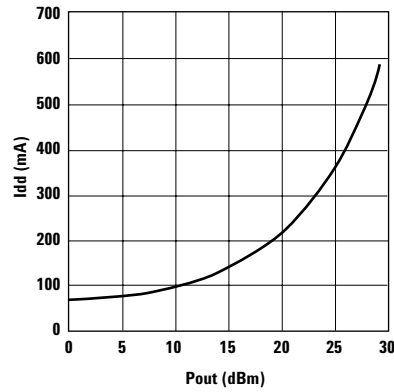


Figure 4. Idd vs. Output Power.

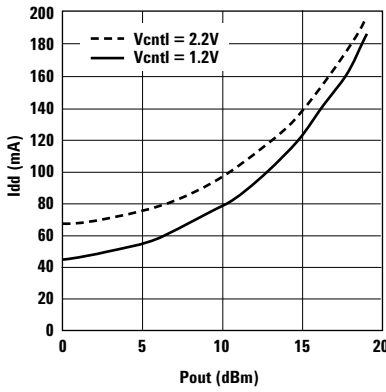


Figure 5. Idd vs. Low-Mid Output Power
Vdd = 3.4V, Vcntl = 2.2V and 1.2V.

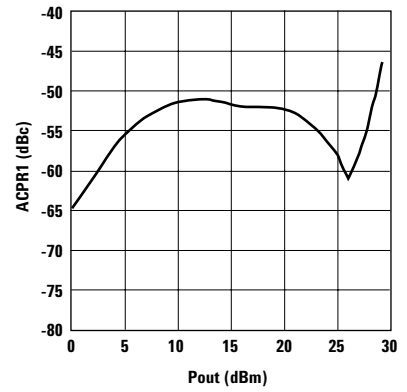


Figure 6. ACPR1 (1.25 MHz) vs. Pout.

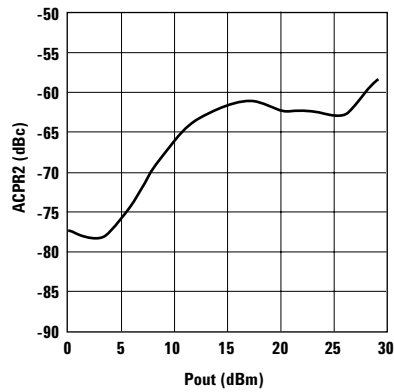


Figure 7. ACPR2 (1.98 MHz) vs. Pout.

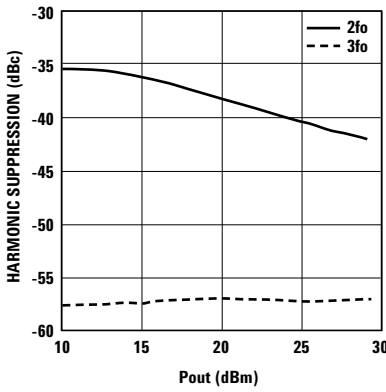
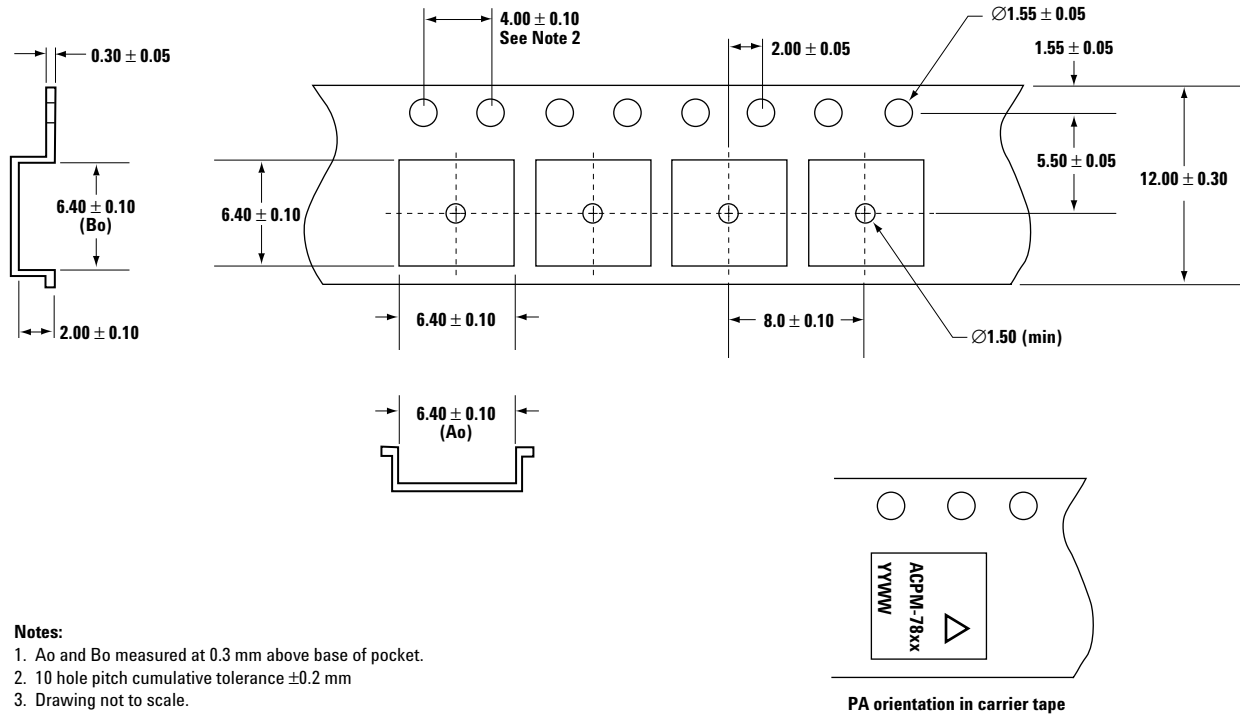


Figure 8. 2nd/3rd Harmonics vs. Pout.

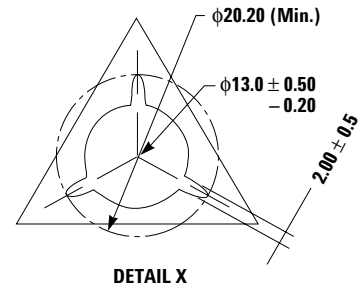
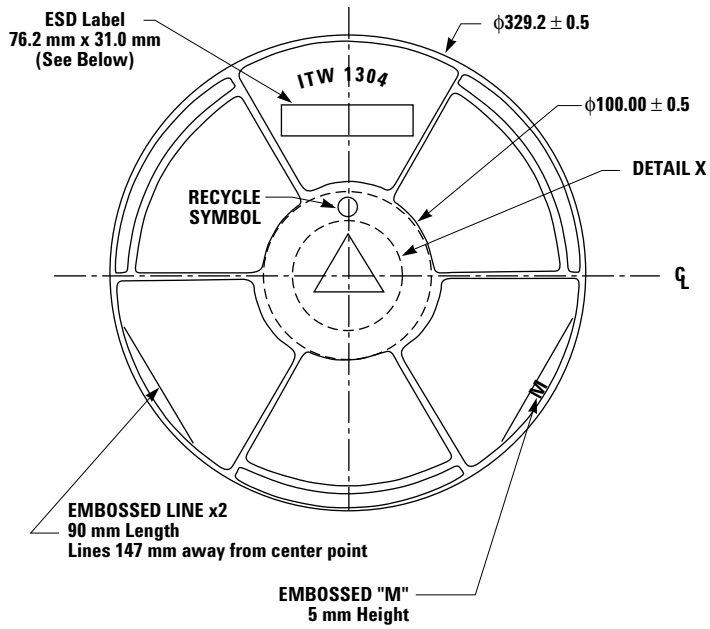
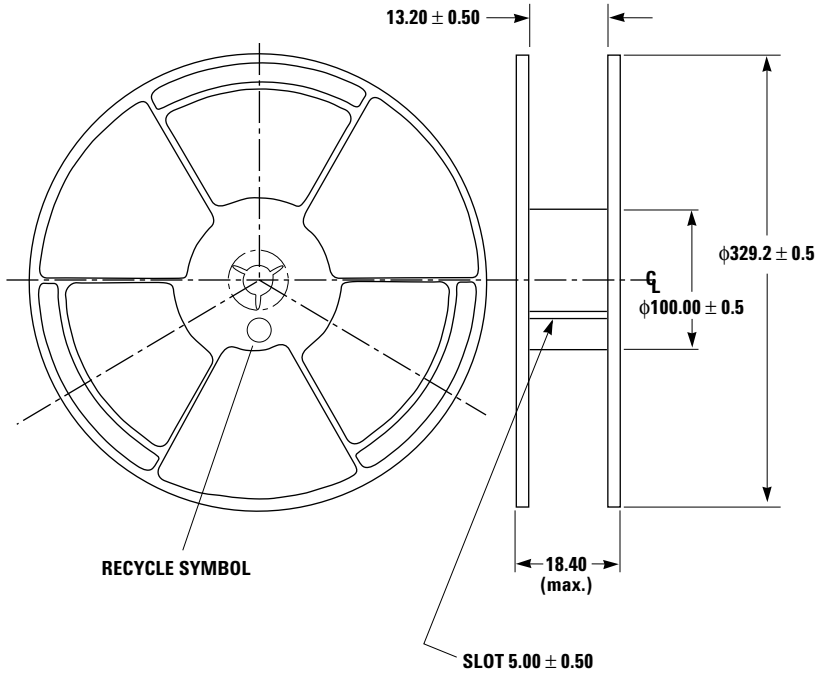
Ordering Information

Part Number	No. of Devices	Container
ACPM-7831-BLK	10	Bulk
ACPM-7831-TR1	2000	13" Tape and Reel

Tape Dimensions and Orientation



Reel Drawing



All dimensions in mm.

Application Information

The following material is presented to assist in general design and use of the APCM-7831.

- 3.0V Characterization, for use in Data Card Applications
- cdma2000 1XRTT Description and Characterization data
- Design tips on various methods to control the bias on Vcntl pin
- Description of ACPR measurement methods
- Description of Agilent evaluation demoboard for ACPM-7831
- IR Reflow Profile (applicable for all Agilent E-pHEMT PAs)

3.0 V Characterization, Data Card Applications

All tests are done in 50Ω system at $V_{dd} = 3.0V$, 25°C, unless noted otherwise.

Parameter	Units	Min	Typ	Max	Comments
PCS CDMA					
Frequency Range	MHz	1850		1910	
Gain (Fixed Cntl Voltage)					
(P _{out} = 28.5 dBm)	dB	24	26		Vcntl = 2.2V
(P _{out} = 13 dBm)	dB		25		Vcntl = 2.2V
(P _{out} = -5 dBm)	dB		24		Vcntl = 2.2V
Power Added Efficiency					
P _{out} = 28.5 dBm	%		44		Vcntl = 2.2V
P _{out} = 16 dBm	%		9		Vcntl = 2.2V
Total Supply Current	mA		575		P _{out} = 28.5 dBm, Vcntl = 2.2V
			100		P _{out} = 13 dBm, Vcntl = 1.6V
			30		P _{out} = -5 dBm, Vcntl = 1.2V
ACPR @ ± 1.25 MHz offset	dBc/30 kHz		-44		P _{out} ≤ 28.5 dBm
ACPR @ ± 1.98 MHz offset	dBc/30 kHz		-55		P _{out} ≤ 28.5 dBm
Quiescent Current	mA		60		P _{out} ≤ 28.5 dBm, Vcntl = 2.2V
Input VSWR					
(P _{out} = 28.5 dBm)			2.0:1		
(P _{out} = 16 dBm)			2.5:1		
Noise Figure	dB		3.5		
Noise Power @ 80 MHz offset in 1930–1990 MHz	dBm/Hz		-138		
Stability (Spurious): Load VSWR 5:1	dBc		-50		All phases
Harmonic Suppression					
2Fo	dBc		-40		
3Fo	dBc		-40		

Typical Performance

Vdd = 3.0V, Vcntl = 2.2V, Frequency = 1880 MHz

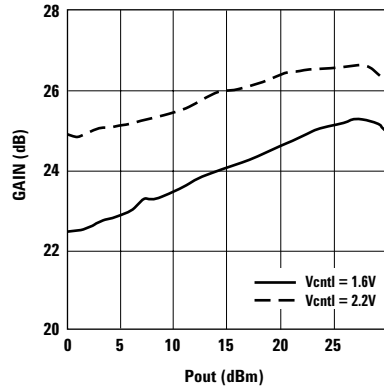


Figure 9. Gain vs. Pout.

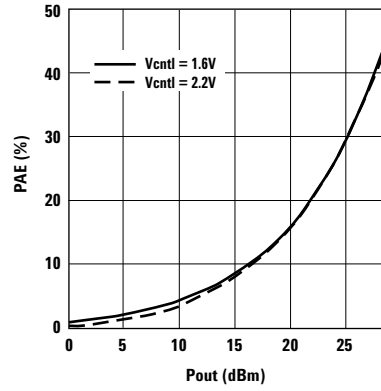


Figure 10. PAE vs. Pout.

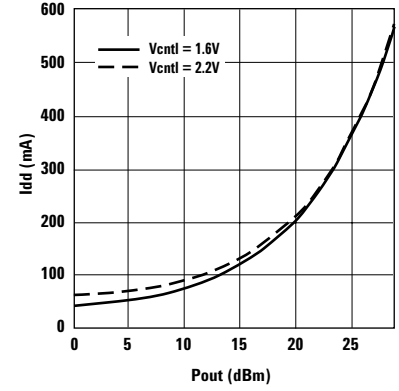


Figure 11. Idd vs. Pout.

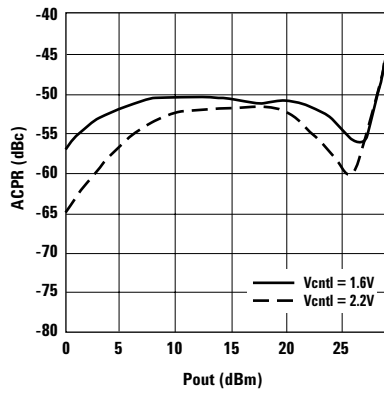


Figure 12. ACPR (1.25 MHz) vs. Pout.

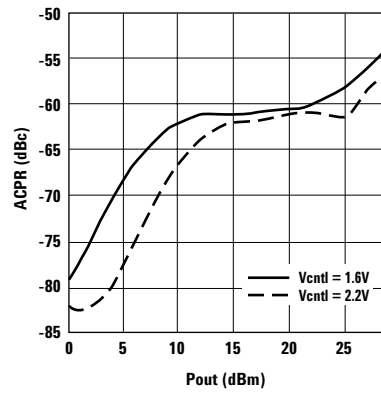


Figure 13. ACPR (1.98 MHz) vs. Pout.

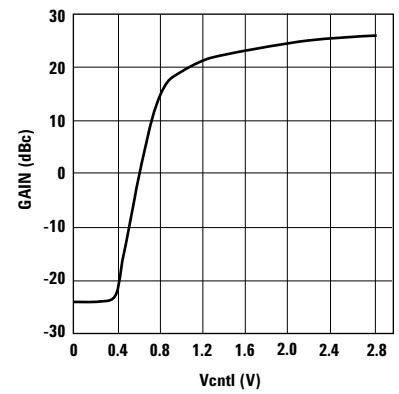


Figure 14. Gain vs. Vcntl.

cdma2000 1xRTT Characterization System Description

CDMA2000 is the TIA’s standard for third generation (3G) technology and is an evolution of the IS-95 CDMA format. CDMA2000 includes 1X RTT in the single-carrier mode and 3X RTT in the multi-carrier mode. CDMA2000 1X RTT, being an extension of the IS-95 standard, has a chip rate of

1.2288Mchip/s IS-95. However, in 1X RTT, the reverse link transmits more than one code channel to accommodate the high data rates. The minimum configuration consists of a reverse pilot (R-Pilot) channel for synchronous detection by the base transceiver stations (BTS) and a reverse fundamental channel (R-FCH) for voice. Additional

channels such as the reverse supplemental channels (R-SCHs) and the reverse dedicated channel (R-DCCH) are used to send data or signaling information. Channels can exist at different rates and power levels.

Table 1 shows the transmitter specification in CDMA2000 reverse link.

Specification	Spread Rate1	
ERP at Maximum	Lower limit +23 dBm	
Output Power	Upper limit +30 dBm	
Minimum Controlled Output Power	-50 dBm/1.23 MHz	
Waveform Quality Factor and Frequency Accuracy	>0.944	
Spurious Emission at Maximum RF output power offset frequency within the range	SR1, Band Class 0(Cellular band)	SR1, Band Class1(PCS band)
	885 kHz to 1.98 MHz Less stringent of -42 dBc/30 kHz or -54 dBm/1.23 MHz	885 kHz to 1.98 MHz Less stringent of -42 dBc/30 kHz or -54 dBm/1.23 MHz
	1.98 MHz to 3.125 MHz Less stringent of -54 dBc/30 kHz or -54 dBm/1.23 MHz	1.98 MHz to 2.25 MHz Less stringent of -50 dBc/30 kHz or -54 dBm/1.23 MHz
	3.125 MHz to 5.625 MHz -13 dBm/100 kHz	2.25 MHz to 6.25 MHz -13 dBm/1 MHz

Table 1. Transmitter Specification in Reverse Link.

Typical channel configurations below are based on the transmitter test condition in the reverse link.

1) “Basic” Voice only configuration

- R-PICH @ -5.3 dB
- R-FCH @ -1.5 dB 9.6 kbps

2) Voice and Data configuration

- R-PICH @ -5.3 dB
- R-FCH @ -4.54 dB 9.6 kbps
- R-SCH1 @ -4.54 dB 9.6 kbps

3) Voice and Control configuration

- R-PICH @ -5.3 dB
- R-FCH @ -3.85 dB 9.6 kbps
- R-DCCH @ -3.85 dB 9.6 kbps

4) Control channel only configuration

- R-PICH @ -5.3 dB
- R-DCCH @ -1.5 dB 9.6 kbps

Combinations of these channels will increase the peak to average power ratio for higher data rates. The complementary cumulative distribution function (CCDF) measurement characterizes the peak to average power statistics of CDMA2000 reverse link. For

reference, the system specifications of peak to average power ratio of IS-95 and CDMA2000 1X RTT are 3.9 dB and 5.4 dB at 1% CCDF respectively. Higher peak to average power ratio requires a higher margin, both in higher power gain and in

improved thermal stability for PA linearity to meet the minimum system specifications. Test results for the ACPM-7831 as tested under 4 cdma2000 channel configurations are shown in the table below.

Electrical Data

All tests are done in 50Ω system at $V_{dd} = 3.4V$, 25°C, unless noted otherwise.

Parameter	Units	Measured	Comments
PCS CDMA			
Frequency Range	MHz	1850–1910	
Gain (Fixed Control Voltage)			
($P_{out} = 28.5$ dBm)	dB	26	Vcntl = 2.2V
($P_{out} = 13$ dBm)	dB	25	Vcntl = 2.2V
($P_{out} = -5$ dBm)	dB	24	Vcntl = 2.2V
Gain (Dynamic Control Voltage)			
($P_{out} = 28.5$ dBm)	dB	26	Vcntl = 2.2V
($P_{out} = 13$ dBm)	dB	23	Vcntl = 1.6V
($P_{out} = -5$ dBm)	dB	17	Vcntl = 1.2V
Power Added Efficiency			
$P_{out} = 28.5$ dBm	%	40	
$P_{out} = 16$ dBm	%	8.5	
ACPR @ ± 1.25 MHz offset			
• Basic	dBc/30 kHz	-52	$P_{out} \leq 28.5$ dBm
• Voice + Data		-45	$P_{out} \leq 28.5$ dBm
• Voice + Control		-44	$P_{out} \leq 28.5$ dBm
• Control only		-52	$P_{out} \leq 26.0$ dBm
ACPR @ ± 1.98 MHz offset			
• Basic	dBc/30 kHz	-62	$P_{out} \leq 28.5$ dBm
• Voice + Data		-59	$P_{out} \leq 28.5$ dBm
• Voice + Control		-60	$P_{out} \leq 28.5$ dBm
• Control only		-60	$P_{out} \leq 26.0$ dBm

Typical Channel Configurations

(a) "Basic" Voice only configuration

- R-PICH @ -5.3 dB
- R-FCH @ -1.5 dB 9.6 kbps

(b) Voice and Data configuration

- R-PICH @ -5.3 dB
- R-FCH @ -4.54 dB 9.6 kbps
- R-SCH1 @ -4.54 dB 9.6 kbps

(c) Voice and Control configuration

- R-PICH @ -5.3 dB
- R-FCH @ -3.85 dB 9.6 kbps
- R-DCCH @ -3.85 dB 9.6 kbps

(d) Control channel only configuration

- R-PICH @ -5.3 dB
- R-DCCH @ -1.5 dB 9.6 kbps

Definitions:

- R-PICH Reverse Pilot Channel
- R-FCH Reverse fundamental channel
- R-SCH Reverse supplemental channel
- R-DCCH Reverse dedicated control channel

Peak to average power ration ($P_{out} = 16$ dBm)

CCDF(%)	Basic	Voice + Data	Voice + CNTL	CNTL only
10	1.98	3.20	3.26	3.87
1	3.48	4.48	4.94	5.50
0.1	4.35	5.32	5.89	6.47
0.01	4.82	5.81	6.42	6.91
0.001	5.01	6.17	6.64	7.12
0.0001	5.11	6.25	6.76	7.19

Design Tips to use Vcntl pin Power Amplifier Control Using Vcntl Pin on ACPM-7831

Power amplifier control scheme in CDMA systems is one of the important and challenging aspects of CDMA-based handset design. Handset designers must balance maintaining adequate linearity while optimizing efficiency at high, medium and low output power levels. The primary method to achieve these goals is to adjust the bias of the PA as a function of output power. Theoretically, the best efficiency would be achieved when the bias of the PA is continually adjusted based on the output power

requirement of the PA. However, implementing this type of circuit is complex and costly. Therefore several different approaches have been developed to provide an acceptable trade-off between optimum efficiency and optimum manufacturability. The following section reviews four methods of controlling the bias of a CDMA power amplifier: fixed, step, logical and dynamic.

1. Fixed Bias Control

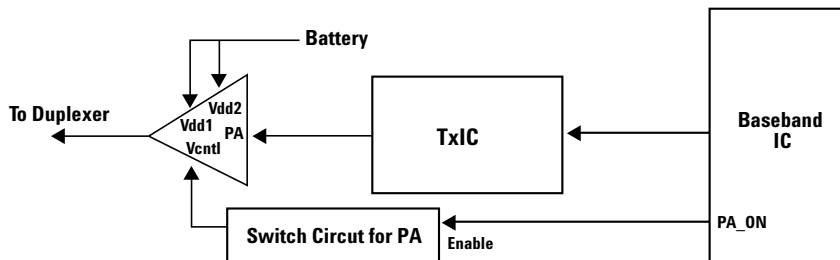
Using a fixed bias point on the PA is the traditional method, and it is the simplest. In fact, a fixed control voltage is recommended when using Agilent's Power

Amplifiers, Vcntl=2.2V for the ACPM-7831. The Vcntl pin on the PA is controlled by PA_ON pin of the baseband IC. When PA_ON is HIGH, the output RF signal of the PA is enabled, enabling the subscriber unit to transmit the required data. The switch circuit supplies the Vcntl with enable/disable (PA on/off mode).

Below is an example of how to control the PA_ON and Vcntl pin of the PA.

Power Mode	PA_ON	Vcntl	Power Range
Shut Down	LOW	0V	—
High Power	HIGH	2.2V*	≤ 28.5 dBm

Note: * Vcntl for PCS Band



2. Step Bias Control

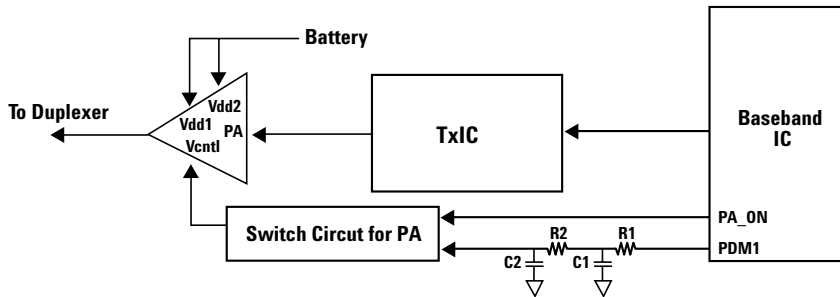
The PDM1 output from the baseband IC can be used to create a software-programmable voltage, to be used at the phone designer's discretion. The two-pole filter is used to improve RF performance in terms of fast response time. To get high efficiency and better ACPR, the phone designers can change control voltage of the PA by

adjusting PDM1 voltage according to output power of PA. A caution when using this approach—careful consideration must be made to avoid an abrupt discontinuity in the output signal when the step bias control voltage is applied.

Below shows the example how to control the PA_ON, PDM1 and Vcntl pin of PA.

Power Mode	PA_ON	Vcntl	Power Range
Shut Down	LOW	0V	—
Low Power	HIGH	1.2V	~ -5 dBm
Mid Power	HIGH	1.6V	-5 dBm ~ 13 dBm
High Power	HIGH	2.2V	13 dBm ~ 28.5 dBm

Note: Adjust PDM1 pulse waveform to set low/mid/high power mode



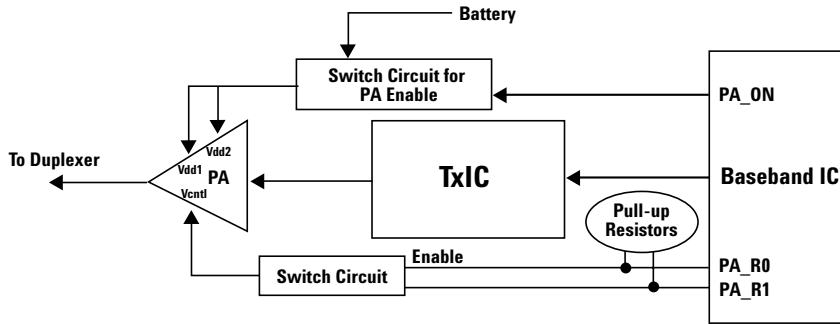
3. Logical Bias Control

This scheme is similar to step bias control circuit above but also uses the PA_R0 and PA_R1 pins on a typical baseband IC. PA_R[1:0] is an open-drain output, requiring an external pull-up resistor, and is used to step the gain of the Tx signal path by changing voltages on

Vcntl. As with the step bias control, there must be some consideration of the hysteresis step to avoid an abrupt discontinuity with logical bias control voltage.

Below shows the example how to control the PA_R[1:0] and Vcntl pin of PA.

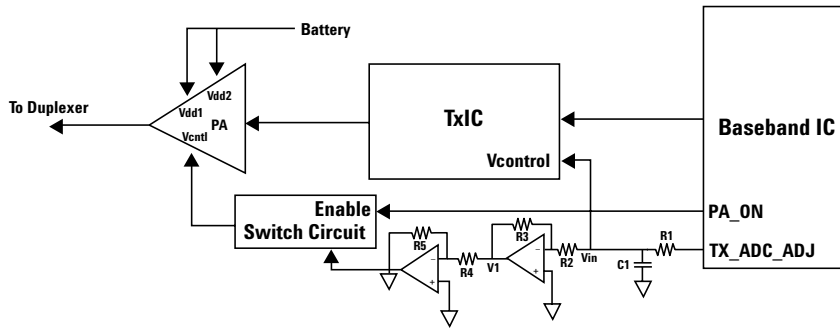
Power Mode	PA_R0	PA_R1	Vcntl	Power Range
Shut Down	0	0	0V	—
Low Power	0	1	1.2V	~ -5 dBm
Mid Power	1	0	1.6V	-5 dBm ~ 13 dBm
High Power	1	1	2.2V	13 dBm ~ 28.5 dBm



4. Dynamic Bias Control

Phone designers can use TX_ADC_ADJ pin of the baseband IC to get dynamic bias control with Vcntl pin of PA. TX_ADC_ADJ is a PDM output pin produced by the TX AGC subsystem and used to control

the gain of the Tx signal prior to the PA. The variable output levels from two inverting operational amplifiers, generated and compared by TX_ADC_ADJ, provide dynamic control voltages for the Vcntl of 1.0V ~ 2.7V with a 0.1V step.



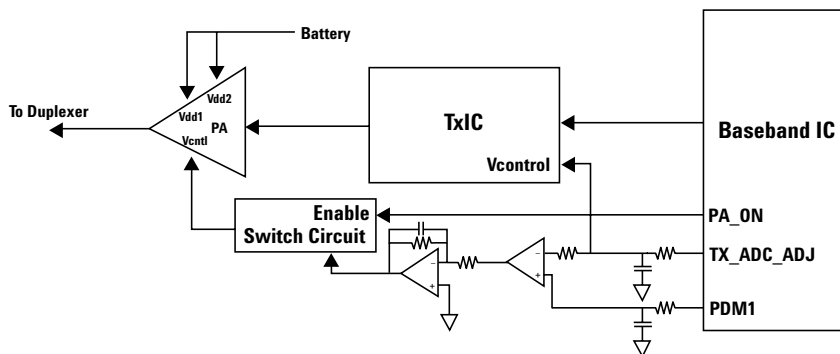
$$A_v = -(V_1/V_{in}) = -R_3/R_2,$$

$$V_1 = -(R_3/R_2)V_{in},$$

$$V_o = -(R_5/R_4)V_1 =$$

$$[(R_5 \cdot R_3)/(R_4 \cdot R_2)] \cdot V_{in}$$

The using of combination of two pins, PDM1 and TX_ADC_ADJ, is another method of realizing a dynamic bias control scheme. The two OP Amps control the Vcntl voltage levels with compared and integrated circuits.



ACPR Measurement Method

Adjacent-channel power ratio (ACPR) is used to characterize the distortion of power amplifiers and other subsystems for their tendency to cause interference with neighboring radio channels or systems. The ACPR measurement often is specified as the

ratio of the power spectral density (PSD) of the CDMA main channel to the PSD measured at several offset frequencies. For the Cellular band (824 ~ 849 MHz transmitter channel), the two offsets are at ± 885 kHz and ± 1.98 MHz and the measurement resolution bandwidth specified is

30 kHz. These offsets are at ± 1.25 MHz and ± 1.98 MHz for the PCS band (1850 ~ 1910 MHz Tx channel).

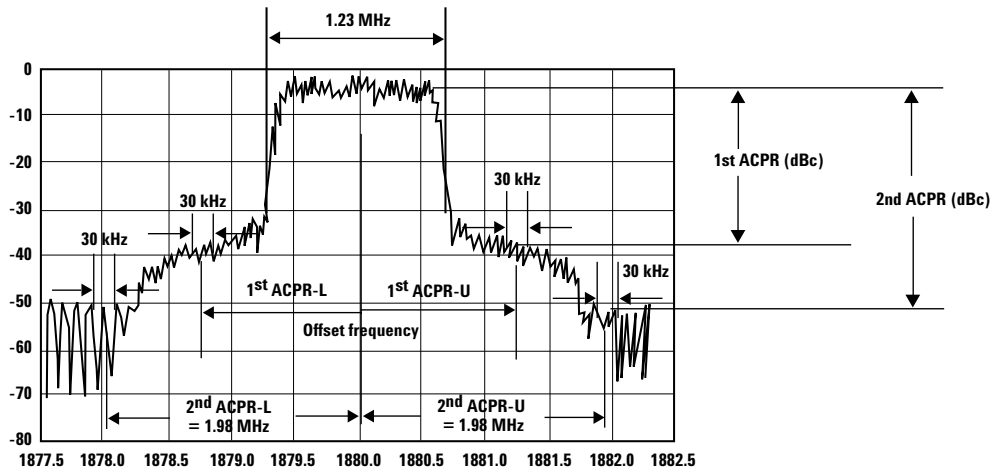


Figure 15. CDMA Adjacent-Channel Power Ratio Measurement.

Offset Frequencies	1st ACPR	2nd ACPR
Cellular Band	885 kHz	1.98 MHz
PCS Band	1.25 MHz	1.98 MHz

ACPR Testing Diagram Test

PA Test Setup

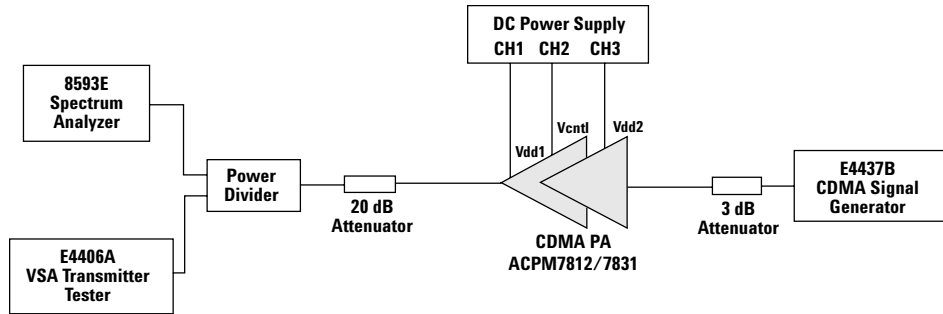


Figure 16. ACPR PA test equipment setup.

Test Result using VSA Transmitter Tester

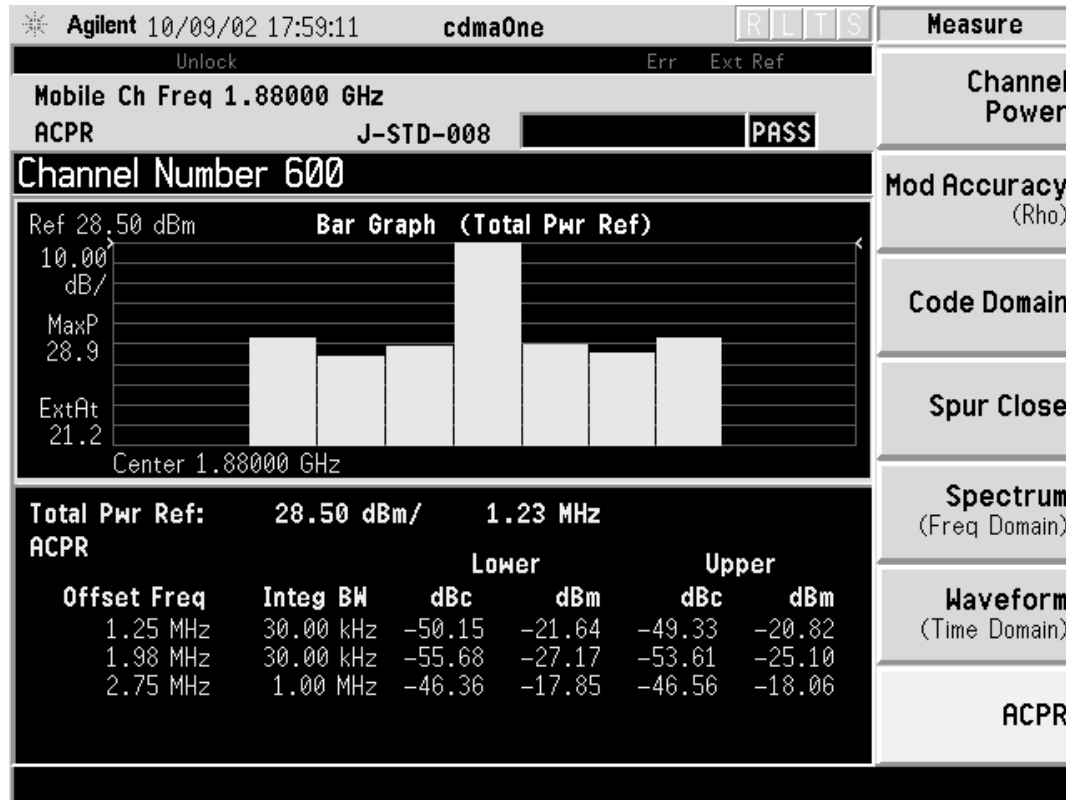


Figure 17. ACPR measurement using VSA Transmitter tester.

ACPR Test Results using Spectrum Analyzer

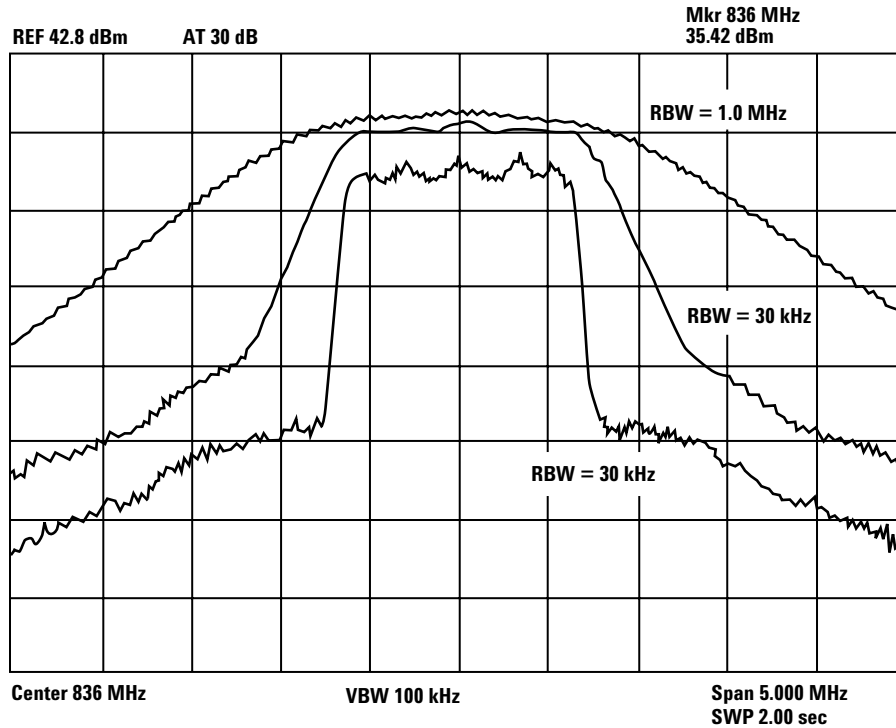


Figure 18. Example ACPR measurement using Spectrum Analyzer.

The meaning of 16 dB

The accurate ACPR measurement using Spectrum Analyzer needs to consider the normalization factor that is dependent on the Resolution Bandwidth, RBW, settings. The above figure (measurement shown at 836 MHz for general example) shows a comparison of the different ACPR measurement results as a function of various RBW values. As the RBW is reduced, less power is captured during the measurement and consequently the

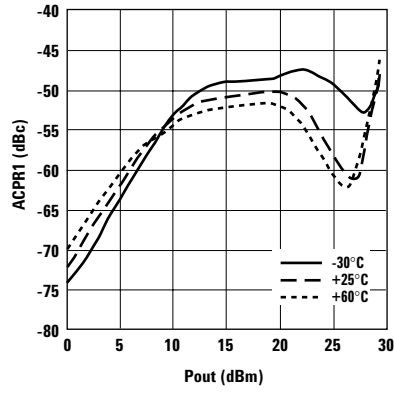
channel power is recorded as a smaller value. For example, if the main channel power is measured as 28 dBm in a 1.23 MHz bandwidth, its power spectral density is 28 dBm/1.23 MHz, which can be normalized to 11.87 dBm/30 kHz. The equation used to calculate the normalization factor of power spectral density is:

$$\begin{aligned} \text{Normalization Factor} &= \\ &= 10\log[\text{Normalization BW}/\text{Current BW} \\ &\quad (\text{Spectrum Analyzer RBW})] \\ &= 10\log[1.23 \times 10^6 / 30 \times 10^3] \\ &= 16.13 \text{ dB} \end{aligned}$$

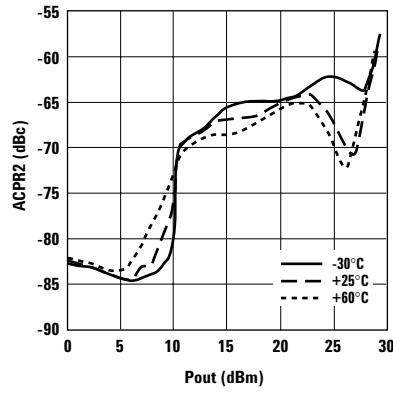
Since the ACPR in an IS95 system is specified in a 1.23 MHz bandwidth, a channel power that is measured using a different RBW, can be normalized to reflect the channel power as if it was measured in a 1.23 MHz bandwidth. The difference in channel power measured in 30 kHz bandwidth and the channel power measured in a 1.23 MHz bandwidth is 16 dB.

ACPR Test Results with Agilent ACPM-7831 CDMA PA

Test Condition: Vdd1 = Vdd2 = 3.4V typ., Vcntl = 2.2V, Frequency = 1880 MHz



1st ACPR Measurement



2nd ACPR Measurement

ACPM-7831 Demoboard Operation Instructions

1) Module Description

The ACPM-7831 is a fully matched Power Amplifier. The sample device is provided on a demonstration PC Board with SMA connectors for RF inputs and outputs, and a DC connector for all bias and control I/O's.

2) Circuit Operation

The design of the power module (PAM) provide bias control via Vref (Vcntl) to achieve optimal RF performance and power control. The control pin is labeled Vref (Vcntl). Please refer to Figure 3 for the block diagram of this PAM.

Typical Operation Conditions (Vdd = 3.4V)

Parameter	ACPM-7831
Frequency Range	1850 – 1910 MHz
Output Power	28.5 dBm
Vcntl (Vref)	2.2 V

3) Maximum Ratings

Vdd	5.0V
Drain Current	1.5A
Vref (Vcntl)	3V
RF input	10 dBm
Temperature	-30 to 80°C

Please Note: Avoid Electrostatic Discharge on all I/O's.

4) Heat Sinking

The demonstration PC Board provides an adequate heat sink. Maximum device dissipation should be kept below 2.5 Watts.

5) Testing

- Signal Source

The CDMA modulated signal for the test is generated using an Agilent ESG-D4000A (or ESG-D3000A) Digital Signal Generator with the following settings:

CDMA Setup : Reverse
Spreading: On
Bits/Symbol: 1
Data: PN15
Modulation: OQPSK
Chip Rate: 1.2288 Mcps
High Crest: On
Filter: Std
Phase Polarity: Invert

- ACPR Measurement

The ACPR (and channel power) is measured using an Agilent 4406 VSA with corresponding ACPR offsets for IS-98c and JSTD-8. Averaging of 10 is used for ACPR measurements.

- DC Connection

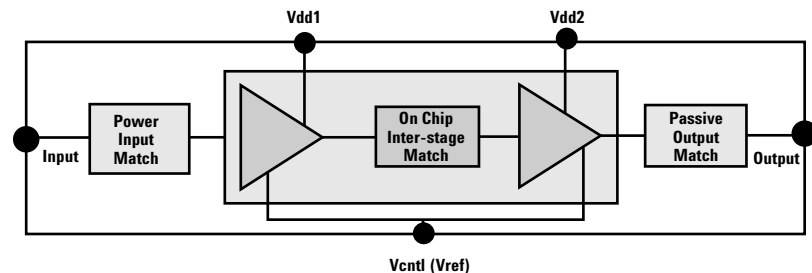
A DC connector is provided to allow ease of connection to the I/O's. Wires can be soldered to the connector pins, or the connector can be removed and I/O's contacted via clip leads or direct soldered connections. The wiring of I/O's are listed in Figure 1 through 3 and Pin

configuration table. The Vdd sense connections are provided to allow the use of remote-sensing power supplies for compensation for PCB traces and cable resistance.

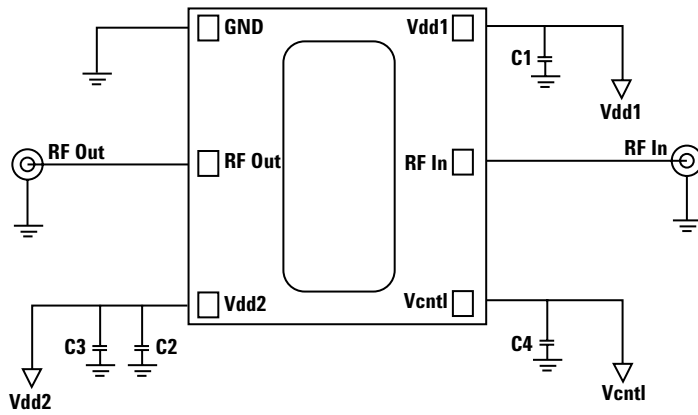
- Device Operation

- 1) Connect RF Input and Output for the band under test.
- 2) Terminate all unused RF ports into 50 Ohms.
- 3) Connect Vdd1 and Vdd2 supplies (including remote sensing labeled Vdd1 S and Vdd2 S on the board). Nominal voltage is 3.4V.
- 4) Apply RF input power according to the values listed in "Operation Data" in Data Packet.
- 5) Connect Vref (Vcntl) supply and set reference voltage to the voltage shown in the data packet. Note that the Vref (Vcntl) pin is on the back side of the demonstration board. Please limit Vref (Vcntl) to not exceed the corresponding listed "DC Biasing Condition" in the Data Packet. Note that increasing Vref (Vcntl) over the corresponding listed "DC Biasing Condition" can result in power decrease and current can exceed the rated limit.

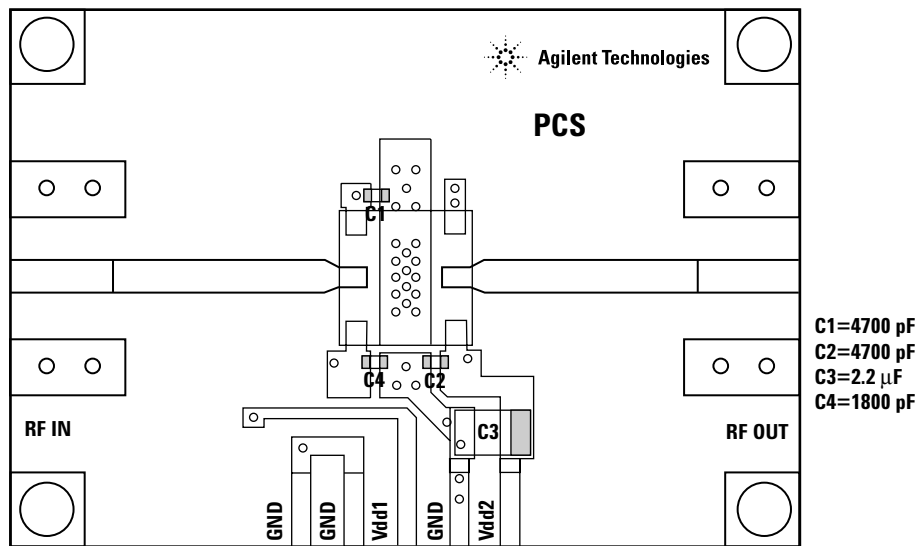
Power Module Block Diagram



ACPM-7831 Evaluation Board Schematic and Layout



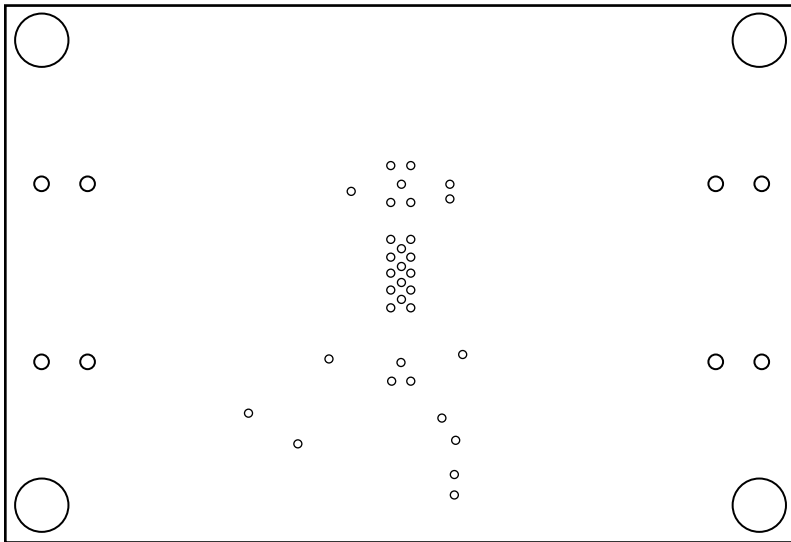
Layer 1 – Top Metal & Solder Mask (PCS)



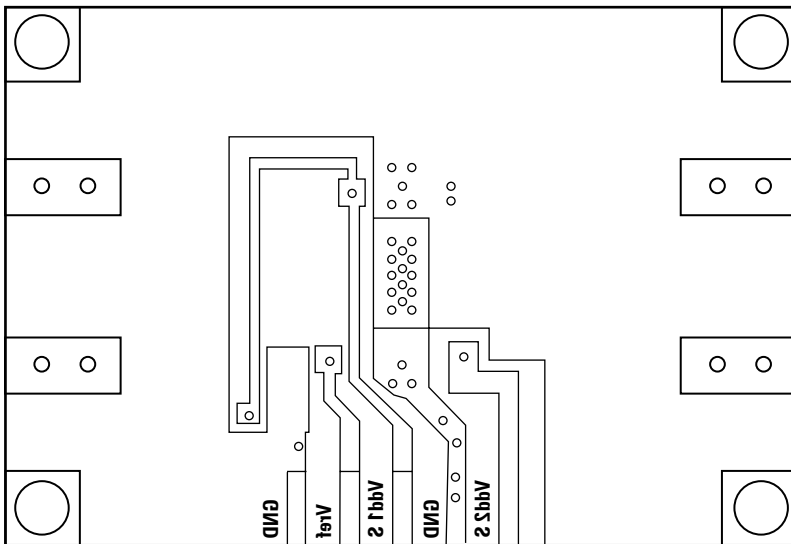
PIN Configuration Table

Top side	Back side
1 Ground	1b Vdd2 Sense
2 Ground	2b Ground
3 Vdd1	3b Vdd1 Sense
4 Ground	4b Vref (Vcntl)
5 Vdd2	5b Ground

Layer 2 – Ground



Layer 3 – Bottom Metal & Solder Mask



IR Reflow Soldering

Figure 19 is a straight-line representation of the recommended nominal time-temperature profile from JESD22-A113-B IR reflow.

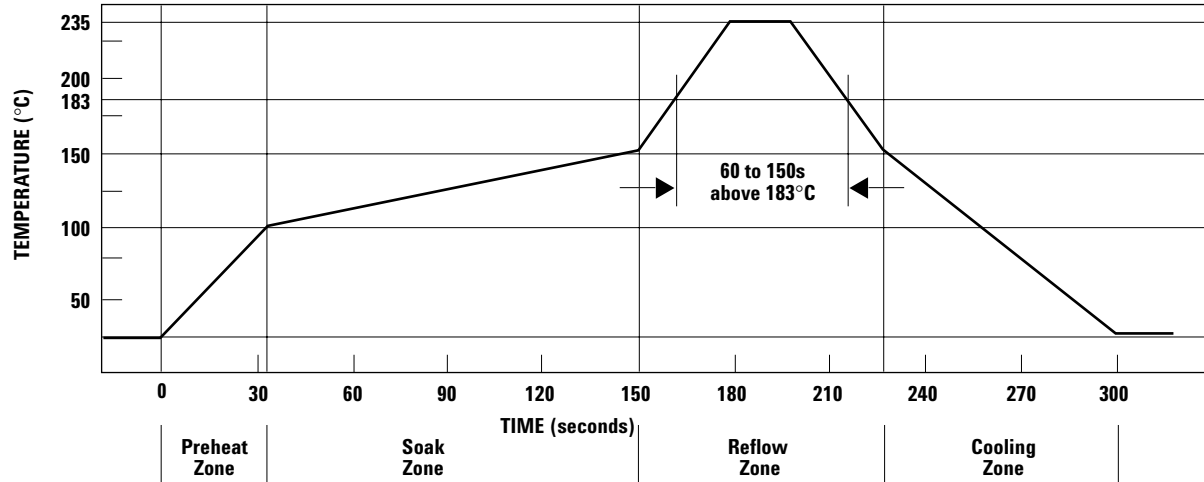


Figure 19. Time-temperature Profile for IR Reflow Soldering Process.

Table 1. IR Reflow Process Zone.

Process Zone	Δ Temperature	Δ Temperature/ Δ Time
Preheat Zone	25°C to 100°C	3°C/s MAX
Soak Zone	100°C to 150°C	0.5°C/s MAX (120s MAX)
Reflow Zone	150°C to 235°C (240°C MAX)	4.5°C/s TYP
	235°C to 150°C	-4.5°C/s TYP
Cooling Zone	150°C to 25°C	-6°C/s MAX

Table 2. Classification Reflow Profiles.

	Convection or IR/Convection
Average ramp-up rate (183°C to peak)	3°C/second max.
Preheat temperature 125 (\pm 25)°C	120 seconds max.
Temperature maintained above 183°C	60 – 150 seconds
Time within 5°C of actual peak temperature	10 – 20 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	6 minutes max.

Note: All temperatures measured refer to the package body surface.

Zone 1 – Preheat Zone

The average heat up rate for surface-mount component on PCB shall be less than 3°C/second to allow even heating for both the component and PCB. This ramp is maintained until it reaches 100°C where flux activation starts.

Zone 2 – Soak Zone

The flux is being activated here to prepare for even and smooth solder joint in subsequent zone. The temperature ramp is kept gradual to minimize thermal mismatch between solder, PC Board and components. Over-ramp rate here can cause solder splatter due to excessive oxidation of paste.

Zone 3 – Reflow Zone

The third process zone is the solder reflow zone. The temperature in this zone rises rapidly from 183°C to peak temperature of 235°C for the solder to transform its phase from solid to

liquids. The dwell time at melting point 183°C shall maintain at between 60 to 150 seconds. Upon the duration of 10–20 seconds at peak temperature, it is then cooled down rapidly to allow the solder to freeze and form solid.

Extended duration above the solder melting point can potentially damage temperature sensitive components and result in excessive inter-metallic growth that causes brittle solder joint, weak and unreliable connections. It can lead to unnecessary damage to the PC Board and discoloration to component's leads.

Zone 4 – Cooling Zone

The temperature ramp down rate is 6°C/second maximum. It is important to control the cooling rate as fast as possible in order to achieve the smaller grain size for solder and increase fatigue resistance of solder joint.

Solder Paste

The recommended solder paste is type Sn6337A or Sn60Pb40A of J-STD-006.

Note: Solder paste storage and shelf life shall be in accordance with manufacturer's specifications.

Stencil or Screen

The solder paste may be deposited onto PCB by either screen printing, using a stencil or syringe dispensing. The recommended stencil thickness is in accordance to JESD22-B102-C.

Nominal stencil thickness	Component lead pitch
0.102 mm (0.004 in)	Lead pitch less than 0.508 mm (0.020 in)
0.152 mm (0.006 in)	0.508 mm to 0.635 mm (0.02 in to 0.025 in)
0.203 mm (0.008 in)	Lead pitch greater than 0.635 mm (0.025 in)

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