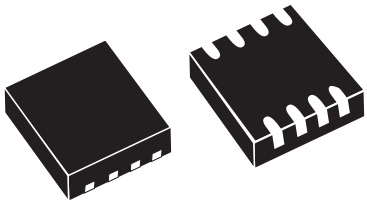
STM6513

Smart reset

Features

- Operating voltage 1.0 V (active-low output valid) to 5.5 V
- Low supply current 3 µA (typ.)
- Factory-programmable thresholds to monitor V_{CC} in the range of 1.575 to 4.625 V typ.
- Dual reset output
  - RST1 - active-high, push-pull
  - $\overline{RST2}$ - active-low, open-drain
- Two smart reset push-button inputs with user-programmable extended reset set up delay (by three-state input logic)
- User-programmable output reset pulse duration (t_{REC1}) by external capacitor C_{tREC}
- Power-on reset
- Operating temperature: industrial grade –40 °C to +85 °C
- Package: TDFN-8L 2 x 2 x 0.75 mm, 0.5 mm pitch
- RoHS compliant



TDFN-8L 2 x 2 mm

Applications

- MP3 players
- Portable navigation devices
- Mobile phones
- Any application that requires delayed reset push-button(s) response for improved system stability.

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1 Description

1.1 Smart reset devices

The smart reset device family STM65xx provides a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing extended smart reset input delay periods (t_{SRC}). Hence, when valid smart reset input conditions and set up periods are met, the reset outputs will generate a pulse with user-programmable timeout period (t_{REC}).

The typical application hookup shows that the dual smart reset inputs can be also connected to the applications interrupt to allow the control of both the interrupt pin and the hard reset functions. If the push-buttons are closed for a short time, the processor is only interrupted. If the system still does not respond properly, holding the push-buttons for the extended set up time (t_{SRC}) causes hard reset of the processor through the reset outputs. The smart reset feature helps significantly increase system stability.

The STM65xx family of smart reset devices consists of low current microprocessor reset circuits targeted e.g. at MP3 players, portable navigation or mobile phones; generally any application that requires delayed reset push-button(s) response for improved system stability. The STM65xx devices feature single or dual smart reset inputs (SRx). The delayed smart reset set up time (t_{SRC}) options of 0 s, 2 s, 6 s and 10 s (all min.) are adjustable by an external capacitor or resistor on the SRC pin or selectable by three-state logic. The delayed set up period ignores switch closures shorter than t_{SRC}, thus preventing unwanted resets.

The STM65xx devices have active-low (optionally active-high) open-drain reset ($\overline{RST}$) output(s) with or without internal pull-up resistor or push-pull as output options, with power-on reset function.

The reset output is also asserted when the monitored supply voltage V_{CC} drops below the specified threshold. The reset output remains asserted for the reset timeout period (t_{REC}) after the monitored supply voltage goes above the specified threshold.

1.2 STM6513

The STM6513 has two separate delayed smart reset inputs ($\overline{SR0}$, $\overline{SR1}$) which when taken low simultaneously provide three user-selectable delayed smart reset set up time (t_{SRC}) options of 2 s, 6 s and 10 s. These are selected through a three-state TSR input pin: when connected to ground, t_{SRC} = 2 s; when left open, t_{SRC} = 6 s; when connected to V_{CC}, t_{SRC} = 10 s (all the times are minimum). There are two reset outputs, both going active simultaneously after both the smart reset inputs were held active for the selected t_{SRC} delay time. The first reset output, RST1, is active-high, push-pull; the second reset output, $\overline{RST2}$, is active-low, open-drain requiring an external pull-up resistor to V_{CC}. The duration of the output reset pulses is independently programmable: t_{REC1} is user-programmable (by external capacitor C_{tREC}), t_{REC2} is factory-programmed to 210 ms (typ.), with the option of 360 ms typ. Additionally, the V_{CC} is monitored and if it drops below the selected V_{RST} threshold, both the reset outputs go active and remain so while V_{CC} is below the V_{RST} threshold, plus the defined duration of the reset pulse t_{REC} on each output.

Figure 1. Logic diagram

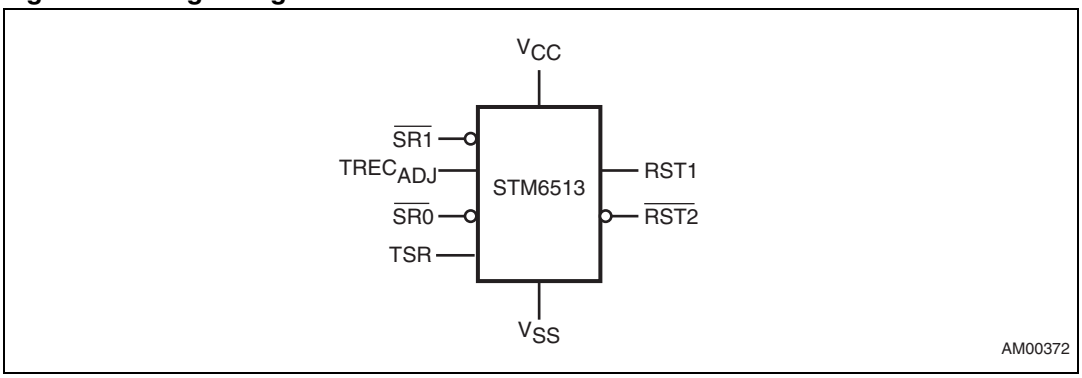
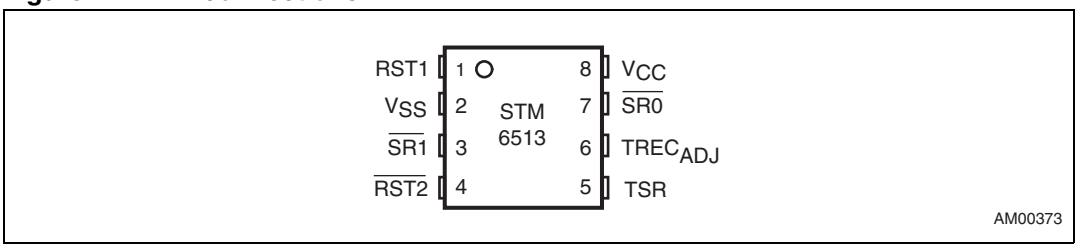


Figure 2. Pin connections



2 Device overview

Table 1. Signal names

Symbol	Input/output	Description
RST1	Output	First reset output, active-high, push-pull.
$\overline{RST2}$	Output	Second reset output, active-low, open-drain.
$\overline{SR0}$	Input	Primary push-button smart reset input. Active-low.
$\overline{SR1}$	Input	Secondary push-button smart reset input. Active-low.
TSR	Input	A Three-state smart reset input delay set up control. When connected to ground, t_{SRC} = 2 s; when left open, t_{SRC} = 6 s; when connected to V_{CC}, t_{SRC} = 10 s (all times are minimum). TSR is a DC-type input, intended to be either permanently grounded, permanently connected to V_{CC} or permanently left open.
$TREC_{ADJ}$	Input	Input pin for t_{REC1} reset pulse duration adjustment. Connect an external capacitor C_{tREC} to this pin to determine t_{REC1}; t_{REC2} is factory-programmed.
V_{CC}	Supply voltage	Positive supply voltage input. Power supply for the device and an input for the monitored supply voltage. A 0.1 µF decoupling ceramic capacitor is recommended to be connected between V_{CC} and V_{SS} pins.
V_{SS}	Supply ground	Ground

3 Pin descriptions

3.1 Power supply (V_{CC})

This pin is used to provide the power to the smart reset device and to monitor the power supply. A 0.1 µF decoupling ceramic capacitor is recommended to be connected between V_{CC} and V_{SS} pins.

3.2 Ground (V_{SS})

This is the ground for the device and all supplies.

3.3 Smart reset inputs ($\overline{SR0}$, $\overline{SR1}$)

Push-button smart reset inputs. Both inputs need to be held active at the same time for at least t_{SRC} to activate the reset outputs.

3.4 User-programmable smart reset delay (TSR pin)

Used to allow the user to program the set up time before the push-buttons action is validated by reset output. Controlled by different voltage levels on the TSR pin: when connected to ground, t_{SRC} = 2 s; when left open, t_{SRC} = 6 s; when connected to V_{CC}, t_{SRC} = 10 s (all times are minimum). TSR is a DC-type input, intended to be either permanently grounded, permanently connected to V_{CC} or permanently left open.

3.5 Reset outputs (RST1, $\overline{RST2}$)

Reset outputs, RST1 active-high, push-pull type, $\overline{RST2}$ active-low, open-drain.

3.6 Adjustable output reset timeout period input pin ($TREC_{ADJ}$)

The output reset timeout period (t_{REC1}) on RST1 is adjustable by connecting an external capacitor C_{tREC} to this pin. The relation between t_{REC1} and C_{tREC} is the following:

Device option with t_{REC1} programmed by external capacitor, most common t_{REC} values selected:

Table 2. t_{REC1} vs. C_{tREC} relation

C_{tREC} value (µF)	t_{REC1} (ms)			Closest common C_{tREC} value (µF)
	Min.	Typ.	Max.	
0	0.1	0.15	0.2	—
0.002	20	30	40	0.0022
0.01	100	150	200	0.01
0.014	140	210	280	0.015
0.028	280	420	560	0.027
0.056	560	840	1120	0.056
0.112	1120	1680	2240	0.12

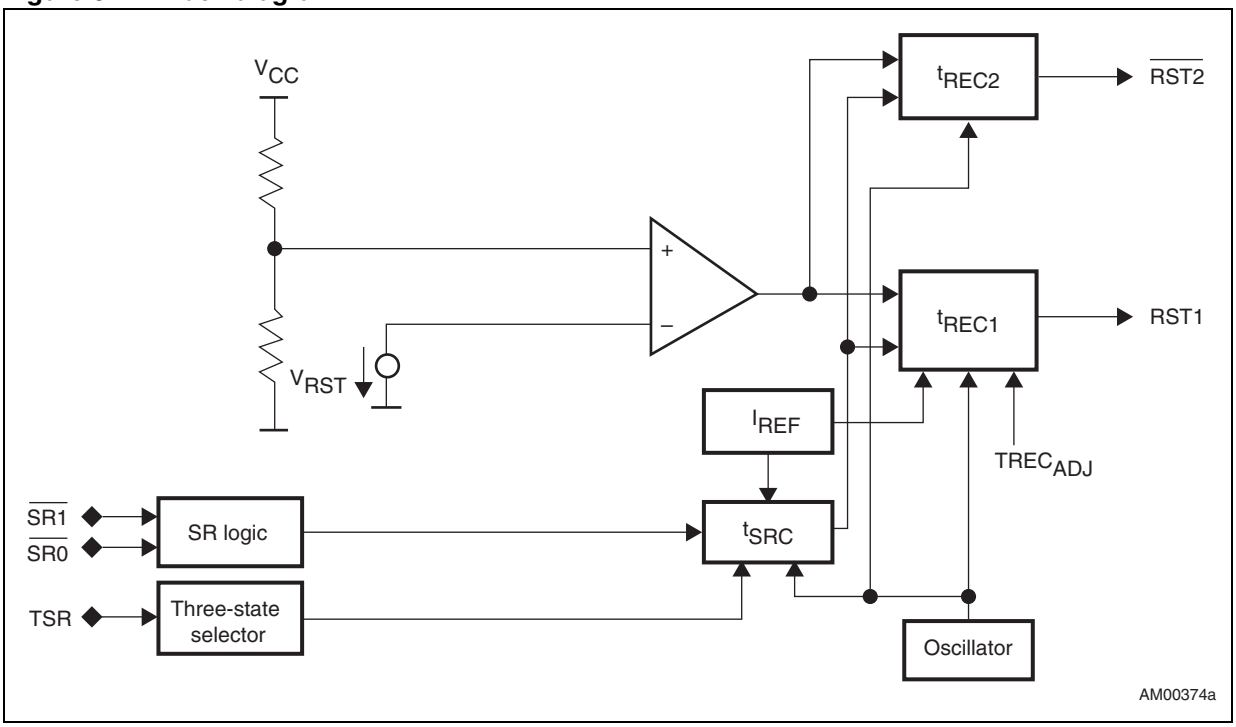
$t_{REC1\ min.} \approx$ 10 000 x C_{tREC} (ms, µF).

Note: 1 In case of quickly repeated activations of the internal t_{REC} counter, an interval of 10 ms min. is needed between t_{REC} intervals to fully discharge C_{tREC}, so that the next t_{REC1} is as specified.

2 It should be considered during application design and component selection that the current flowing into the external t_{REC} programming component (C_{tREC}) is in the order of 100 nA, therefore a low-leakage capacitor and PCB environment should be used to prevent t_{REC} accuracy from being affected.

4 Block diagram

Figure 3. Block diagram



STM6513 hookup with RST1 and $\overline{RST2}$, bridging the PS_hold reset pulse during the microprocessor reset initiated by the STM6513 smart reset device:

Figure 4. Typical application diagram

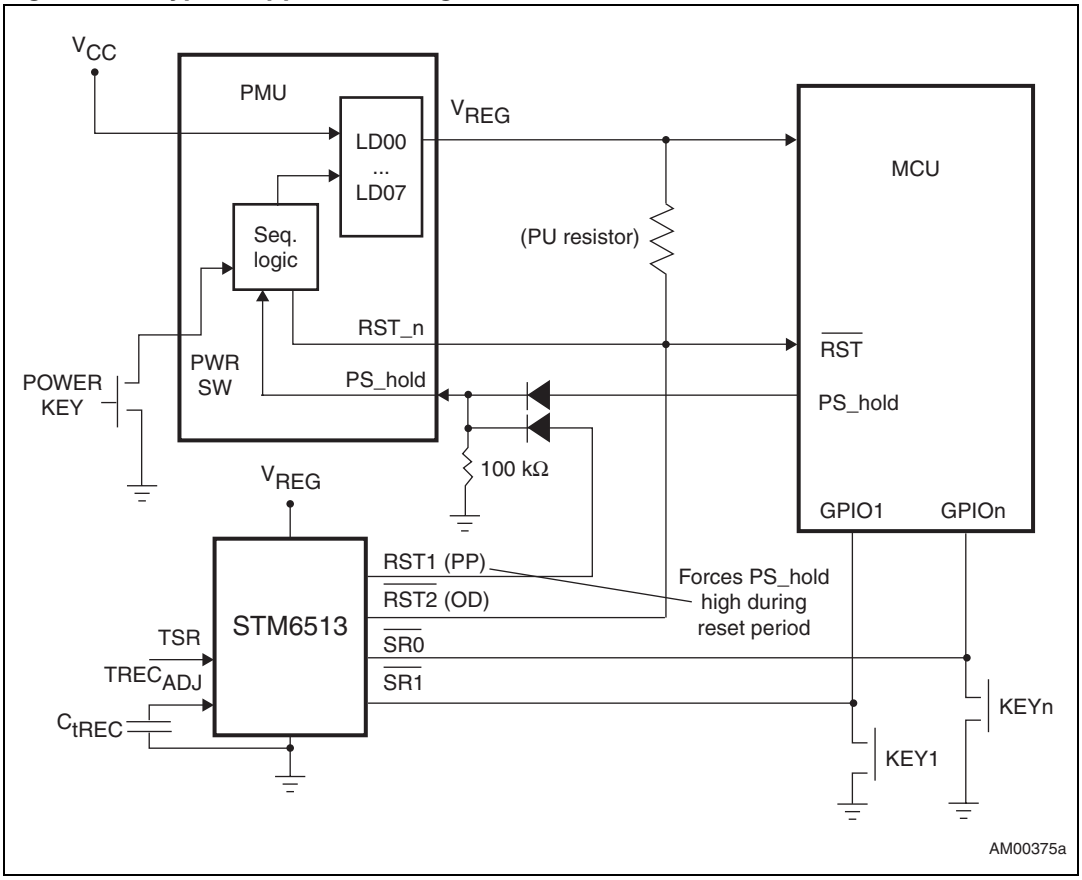
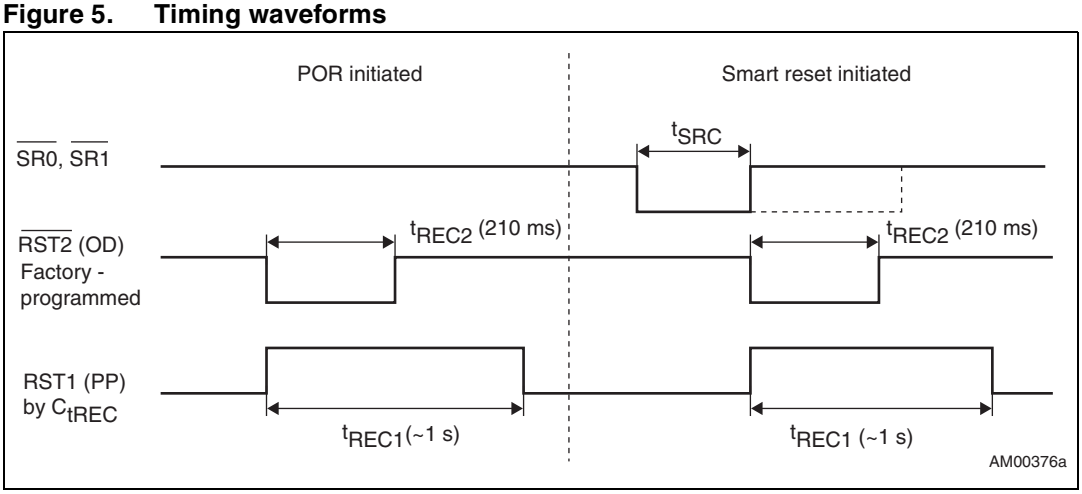


Figure 5. Timing waveforms



5 Typical operating characteristics

Figure 6. Smart reset delay t_{SRC} vs. temperature and supply voltage V_{CC}, TSR = V_{SS}

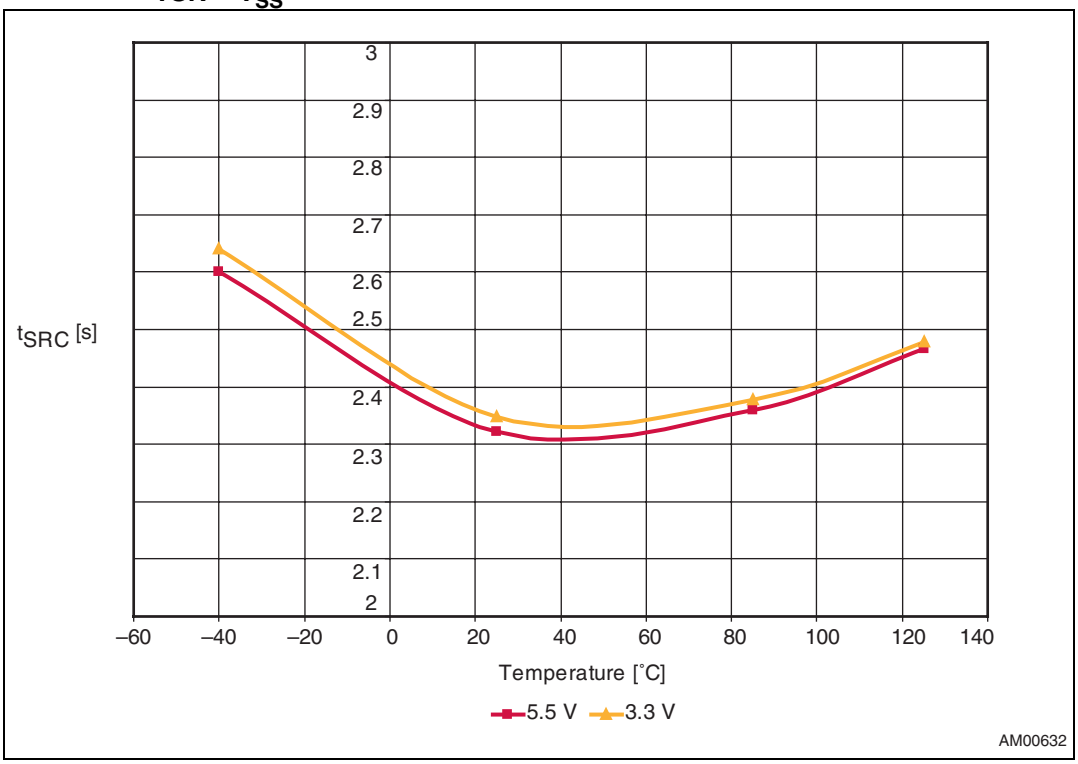


Figure 7. Output reset timeout period t_{REC2} vs. temperature and supply voltage V_{CC} (t_{REC} option E)

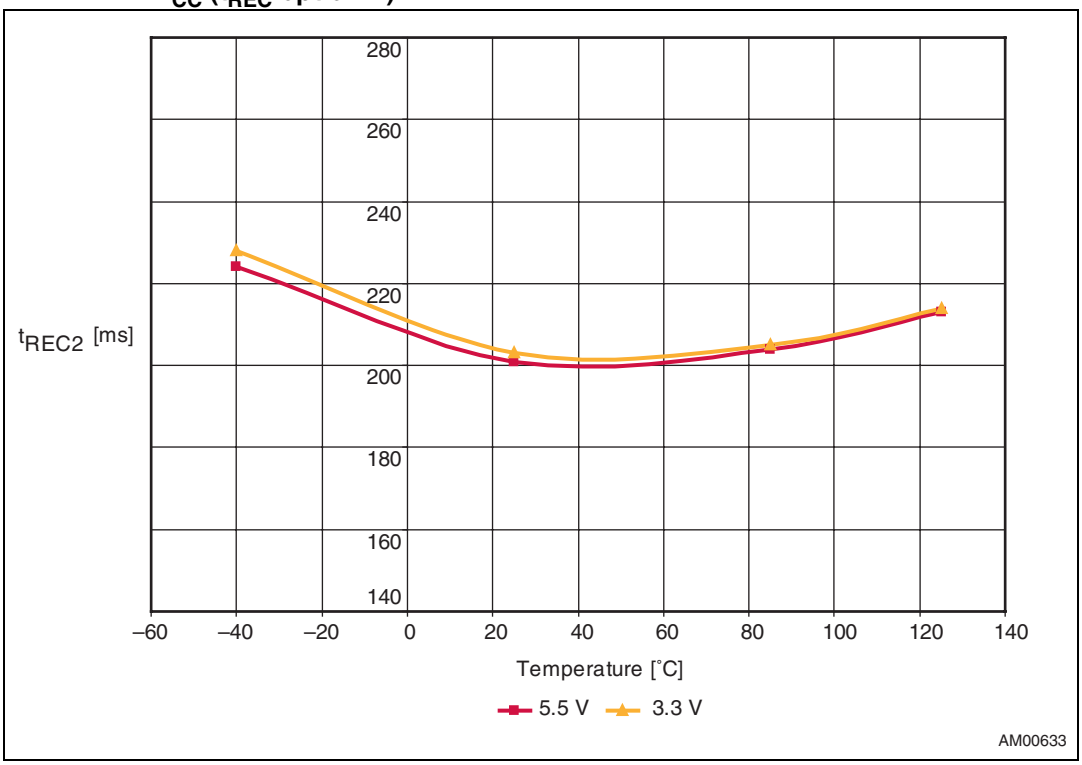


Figure 8. Supply current I_{CC} vs. temperature and supply voltage V_{CC}

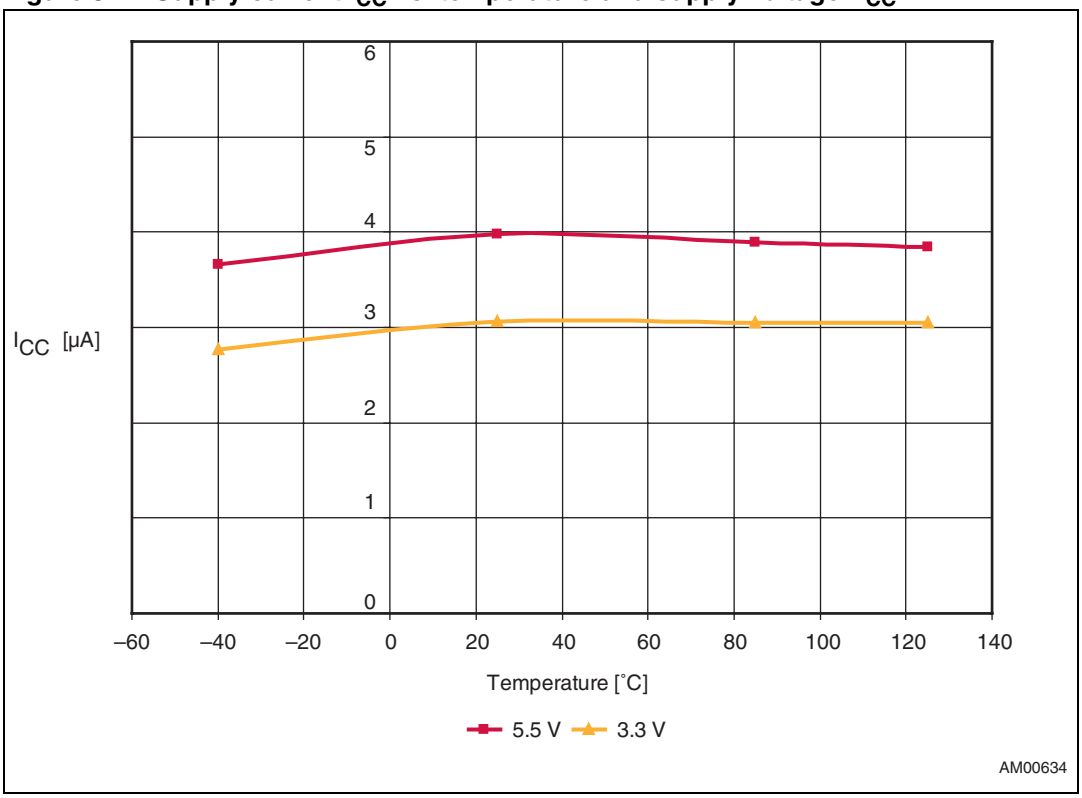


Figure 9. Reset voltage V_{RST} (falling) vs. temperature (threshold option S, 2.925 V typ.)

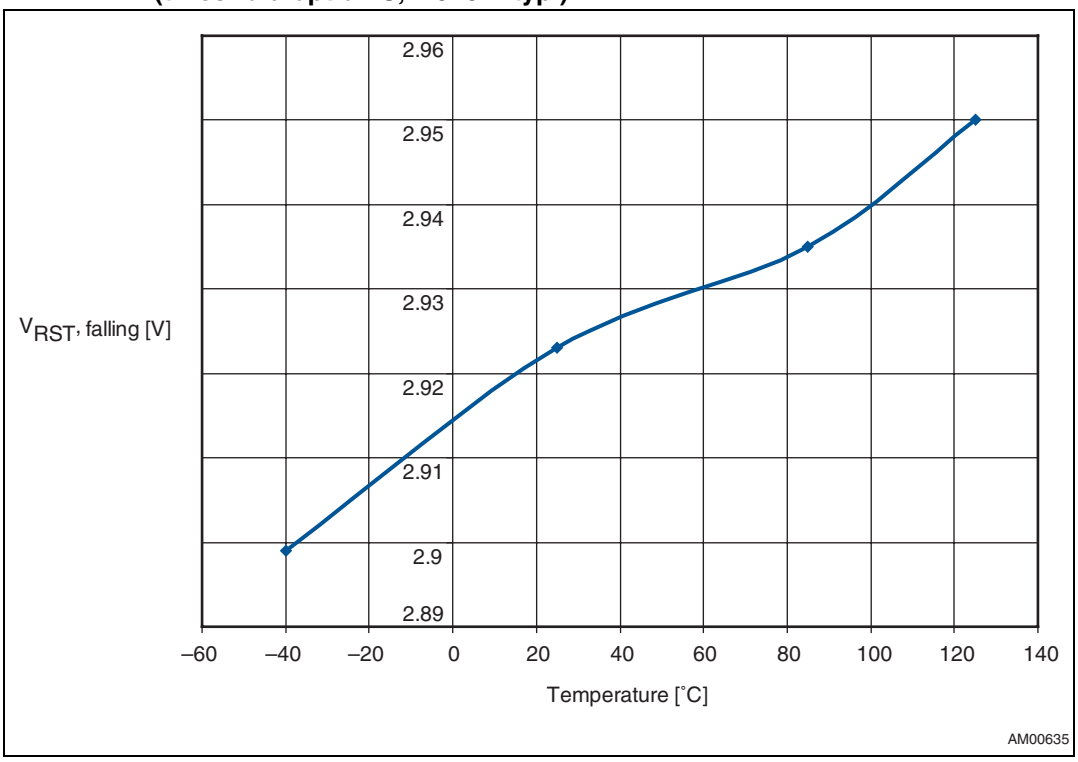


Figure 10. Input leakage current, TSR pin, logic low vs. temperature and supply voltage V_{CC}

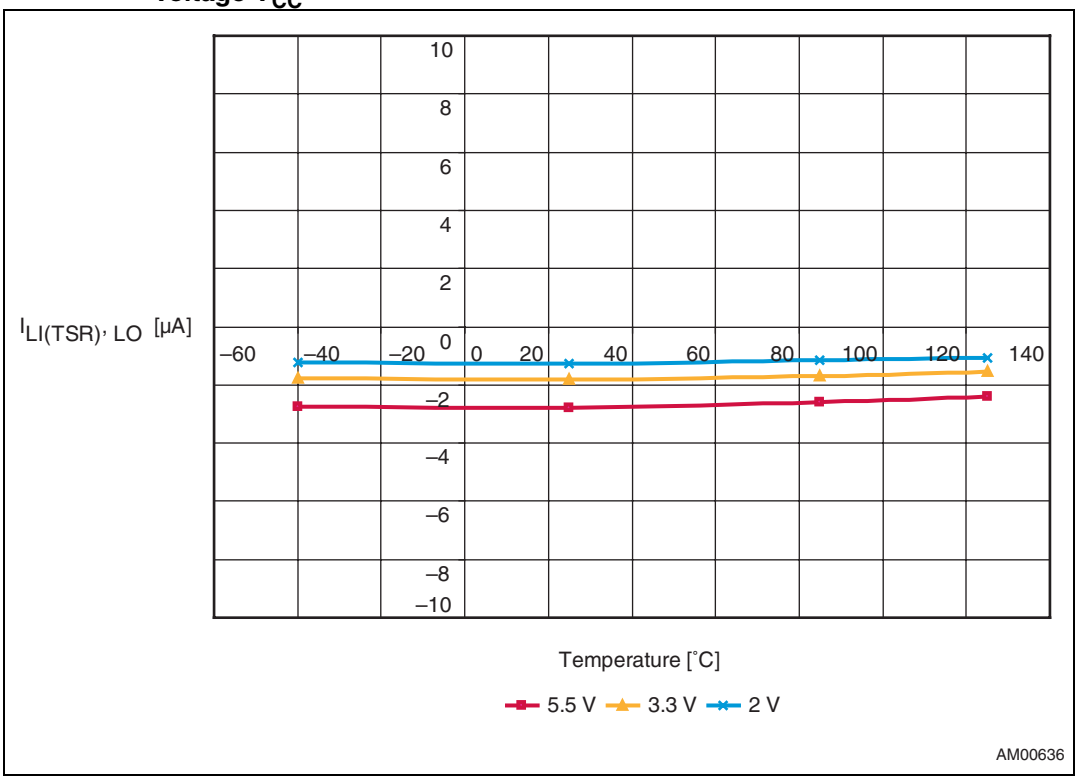
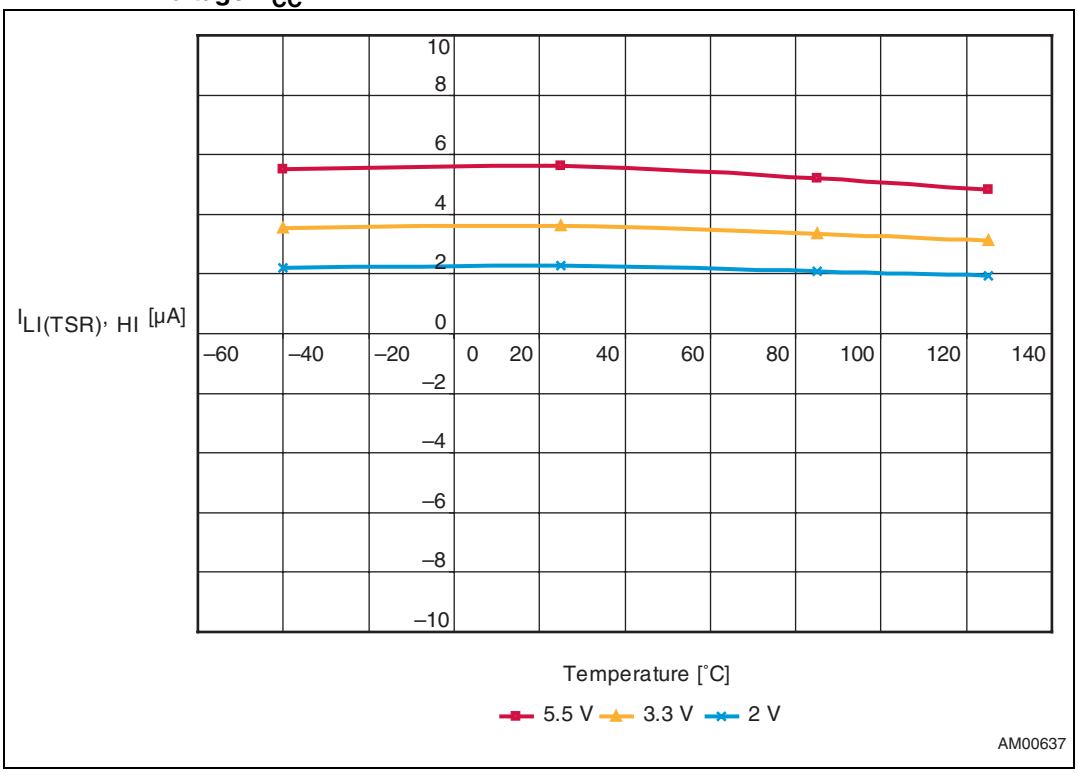


Figure 11. Input leakage current, TSR pin, logic high vs. temperature and supply voltage V_{CC}



6 Maximum rating

Stressing the device above the rating listed in the *Table 3: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_{STG}	Storage temperature (V_{CC} off)		–55 to +150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
θ_{JA}	Thermal resistance (junction to ambient)	TDFN8	149.0	°C/W
V_{IO}	Input or output voltage		–0.3 to V_{CC} +0.3	V
V_{CC}	Supply voltage		–0.3 to 7	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 s.

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the *Table 5: DC and AC characteristics* that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4.: Operating and measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and measurement conditions

Parameter	Value	Unit
V_{CC} supply voltage	1.0 to 5.5	V
Ambient operating temperature (T_A)	–40 to +85	°C
Input rise and fall times	≤ 5	ns
Input pulse voltages	0.2 to 0.8 V_{CC}	V
Input and output timing ref. voltages	0.3 to 0.7 V_{CC}	V

Figure 12. AC testing input/output waveforms

Table 5. DC and AC characteristics

Symbol	Parameter	Test conditions(1)	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage range	Reset output valid - active-low	1.0		5.5	V
		Reset output valid - active-high	1.2		5.5	V
I_{CC}	Supply current (V_{CC})	V_{CC} = 3.0 V		3	5	µA
		V_{CC} = 5.0 V		4	6	µA
V_{OL}	Reset output voltage low	V_{CC} ≥ 4.5 V, sinking 3.2 mA			0.3	V
		V_{CC} ≥ 3.3 V, sinking 2.5 mA			0.3	V
		V_{CC} ≥ 1.0 V, sinking 0.1 mA			0.3	V
V_{OH}	Reset output voltage high, RST1	V_{CC} ≥ 4.5 V, I_{SOURCE} = 0.8 mA	0.8 V_{CC}			V
		V_{CC} ≥ 2.7 V, I_{SOURCE} = 0.5 mA	0.8 V_{CC}			V
		V_{CC} ≥ 1.2 V, I_{SOURCE} = 0.05 mA	0.8 V_{CC}			V
V_{RST}	Fixed voltage trip point for V_{CC} (refer *Table 6*)	–40 to +85 °C	V_{RST} –2.5%	V_{RST}	V_{RST} +2.5%	V
		25 °C	V_{RST} –2.0%	V_{RST}	V_{RST} +2.0%	V
V_{HYST}	Hysteresis of V_{RST}	L, M		0.5%		
		T, S, R, Z, Y, W, V		1%		
	V_{CC} to reset delay	V_{CC} falling from (V_{RST} + 100 mV) to (V_{RST} - 100 mV) at 10 mV/µs		20		µs
t_{REC2}	Output reset timeout period on $\overline{RST2}$, factory-programmed	Option E	140	210	280	ms
		Option F	240	360	480	ms
t_{REC1}	User-programmable output reset timeout period on RST1			See *Table 2*		ms
Smart reset inputs ($\overline{SRx}$)						
t_{SRC}	Smart reset delay	TSR = V_{SS}	2	2.5	3	s
		TSR = floating	6	7.5	9	s
		TSR = V_{CC}	10	12.5	15	s
V_{IL}	$\overline{SR0}$, $\overline{SR1}$ input voltage low				0.3 V_{CC}	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$ input voltage high		0.7 V_{CC}			V
	Input glitch immunity	Corresponds to the actual t_{SRC}		t_{SRC}		s
$I_{LI(SR)}$	Input leakage current ($\overline{SR0}$, $\overline{SR1}$ pins)		–1		1	µA
$I_{LI(TSR)}$	Input leakage current (TSR pin)		–5		7	µA

1. Valid for ambient operating temperature: T_A = –40 to +85 °C; V_{CC} = 1.0 V to 5.5 V (except where noted).

Table 6. Possible V_{CC} voltage thresholds

V_{CC} voltage threshold V_{RST}	Typ.	±2.5% (–40 °C to +85 °C)		±2.0% (25 °C)		Unit
		Min.	Max.	Min.	Max.	
L (falling)	4.625	4.509	4.741	4.533	4.718	V
M (falling)	4.375	4.266	4.484	4.288	4.463	V
T (falling)	3.075	2.998	3.152	3.014	3.137	V
S (falling)	2.925	2.852	2.998	2.867	2.984	V
R (falling)	2.625	2.559	2.691	2.573	2.678	V
Z (falling)	2.313	2.255	2.371	2.267	2.359	V
Y (falling)	2.188	2.133	2.243	2.144	2.232	V
W (falling)	1.665	1.623	1.707	1.632	1.698	V
V (falling)	1.575	1.536	1.614	1.544	1.607	V

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 13. TDFN - 8-lead, 2 x 2 x 0.75 mm, 0.5 mm pitch

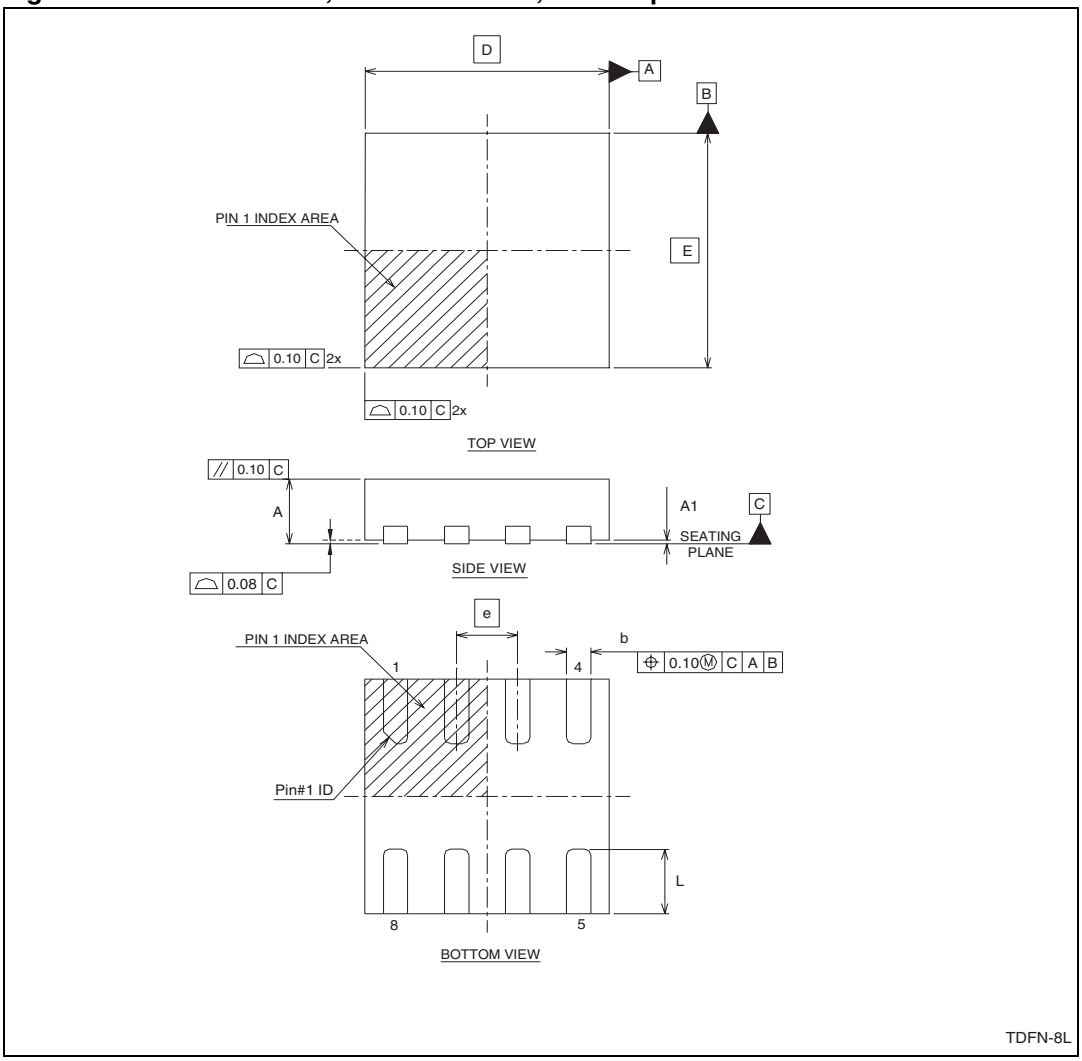


Table 7. TDFN – 8-lead 2 x 2 x 0.75 mm, 0.5 mm package mechanical data

Symbol	Dimension (mm)			Dimension (inches)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D BSC		2.00			0.079	
E BSC		2.00			0.079	
e		0.50			0.020	
L	0.45	0.55	0.65	0.018	0.022	0.026

9 Package footprint

Figure 14. Landing pattern - TDFN – 8-lead 2 x 2 mm without thermal pad

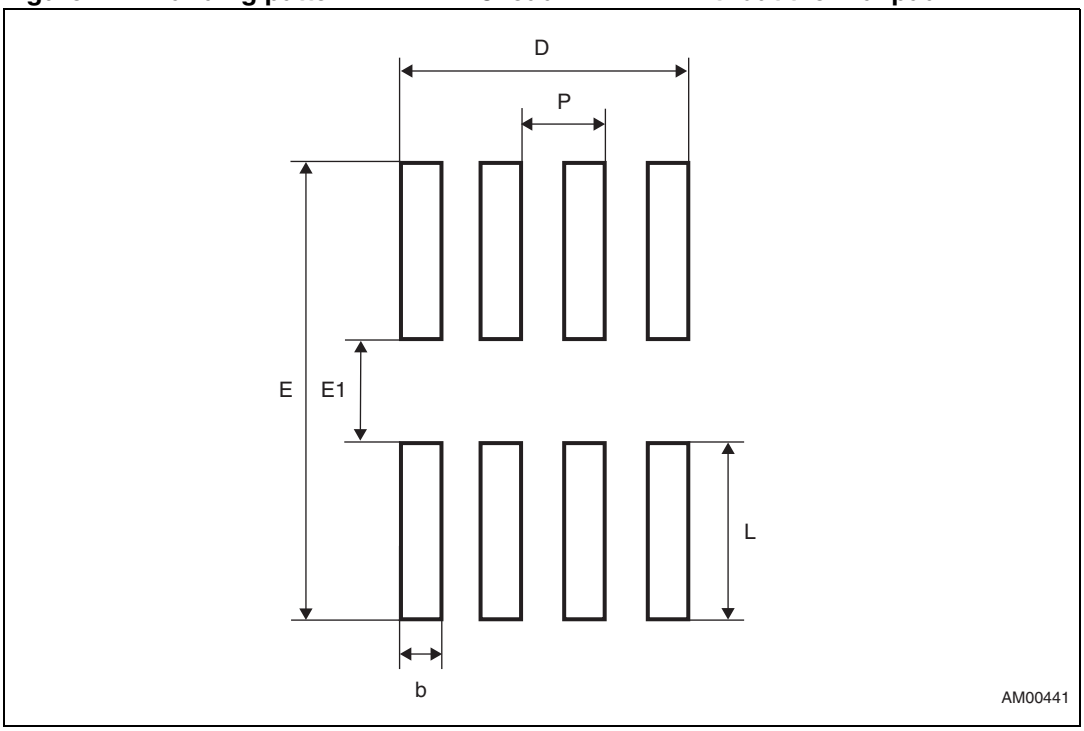


Table 8. Parameter for landing pattern - TDFN – 8-lead 2 x 2 mm package

Parameter	Description	Dimension (mm)		
		Min.	Nom.	Max.
L	Contact length	1.05	—	1.15
b	Contact width	0.25	—	0.30
E	Max. land pattern Y-direction	—	2.75	—
E1	Contact gap spacing	—	0.65	—
D	Max. land pattern X-direction	—	1.75	—
P	Contact pitch	—	0.5	—

10 Tape and reel information

Figure 15. Carrier tape

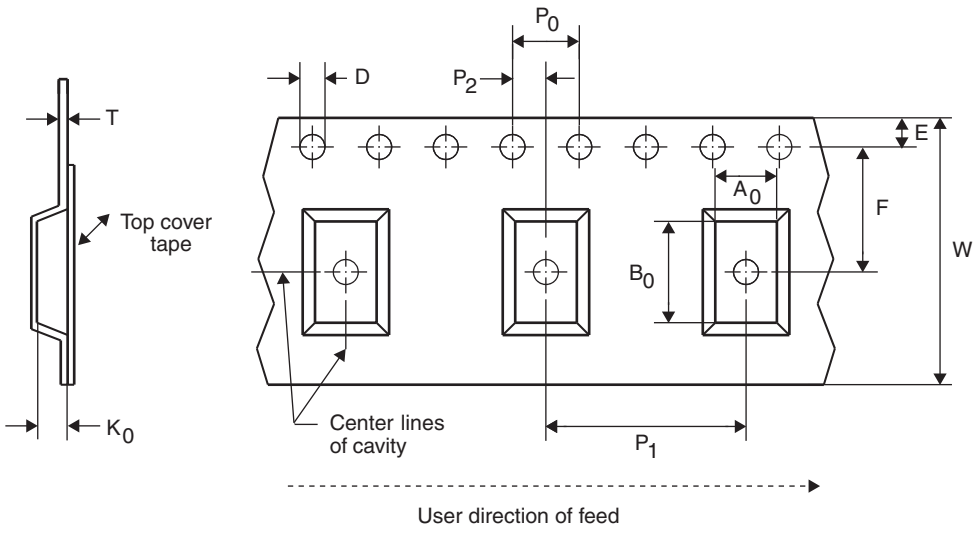


Table 9. Carrier tape dimensions

Package	W	D	E	P_0	P_2	F	A_0	B_0	K_0	P_1	T	Unit	Bulk Qty.
TDFN8	8.00 +0.30 −0.10	1.50 +0.10/ −0.00	1.75 ±0.10	4.00 ±0.10	2.00 ±0.10	3.50 ±0.05	2.30 ±0.05	2.30 ±0.05	1.00 ±0.05	4.00 ±0.10	0.250 ±0.05	mm	3000

Figure 16. Reel dimensions

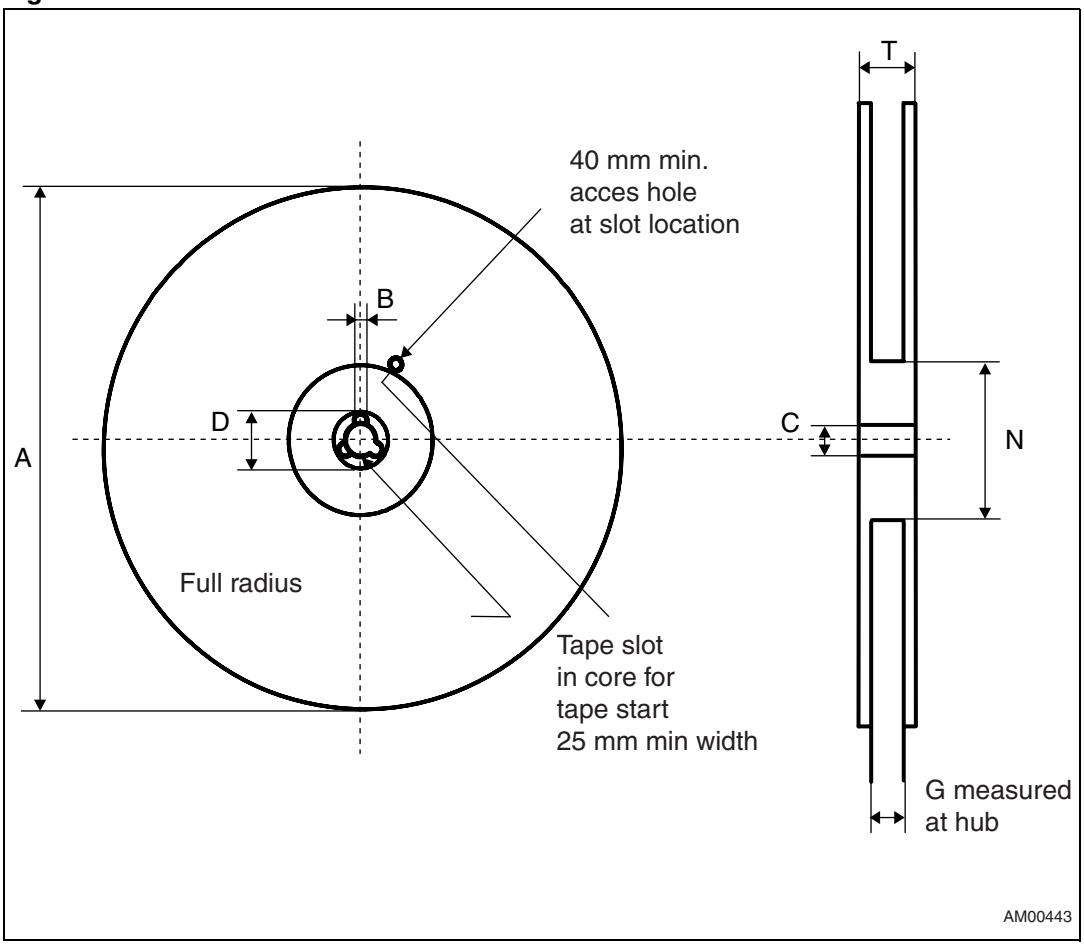


Table 10. Reel dimensions

Tape sizes	A max.	B min.	C	D min.	N min.	G	T max.
8 mm	180 (7 inches)	1.50	13.0 +/– 0.20	20.20	60	8.4 +2/–0	14.40

Figure 17. Tape trailer/leader

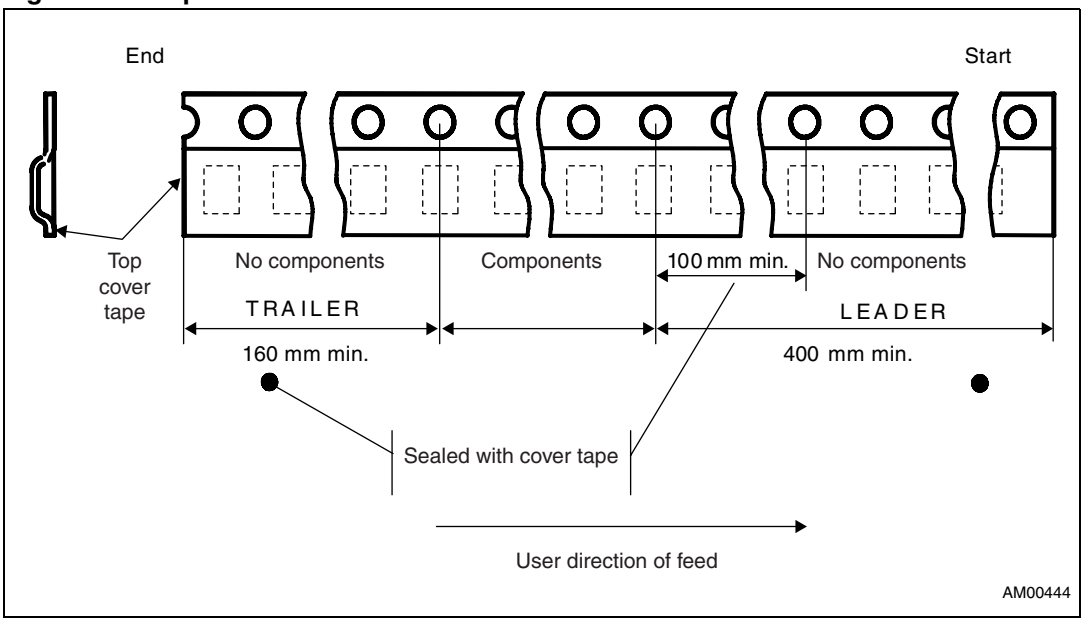
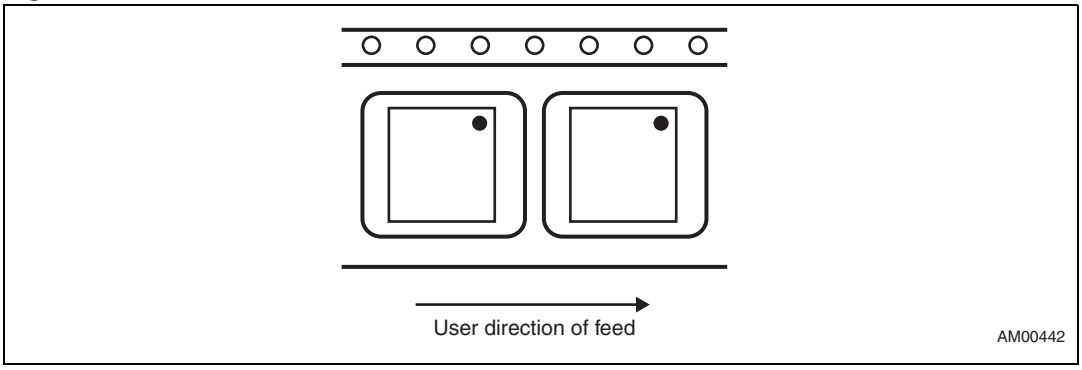


Figure 18. Pin 1 orientation



Note: 1 Drawings are not to scale.

2 All dimensions are in mm, unless otherwise noted.

11 Part numbering

Table 11. Ordering information scheme

Example: **STM6513 V E I E DG 6 F**

Device type

STM6513

Reset (V_{CC} monitoring threshold) voltage V_{RST}

L = 4.625 V (typ., falling)

M = 4.375 V

T = 3.075 V

S = 2.925 V

R = 2.625 V

Z = 2.313 V

Y = 2.188 V

W = 1.665 V

V = 1.575 V

Smart reset set up delay (t_{SRC}); presence of internal input pull-up on all smart reset inputs ($\overline{SR0}$, $\overline{SR1}$)

E = 2 or 6 or 10 s min., user-programmed (three-state); no input pull-up

Outputs type

I = RST1 active-high, push-pull, $\overline{RST2}$ active-low, open-drain, no pull-up

Reset timeout period (t_{REC})

E = t_{REC1} user-programmable (external capacitor), t_{REC2} factory-programmed (210 ms typ.)

F = t_{REC1} user-programmable (external capacitor), t_{REC2} factory-programmed (360 ms typ.)

Package

DG = TDFN8 - 2 x 2 x 0.75 mm, 0.5 mm pitch

Temperature range

6 = –40 °C to +85 °C

Shipping method

F = ECOPACK® package, tape and reel

For other options, voltage threshold values etc. or for more information on any aspect of this device, please contact the ST sales office nearest you.

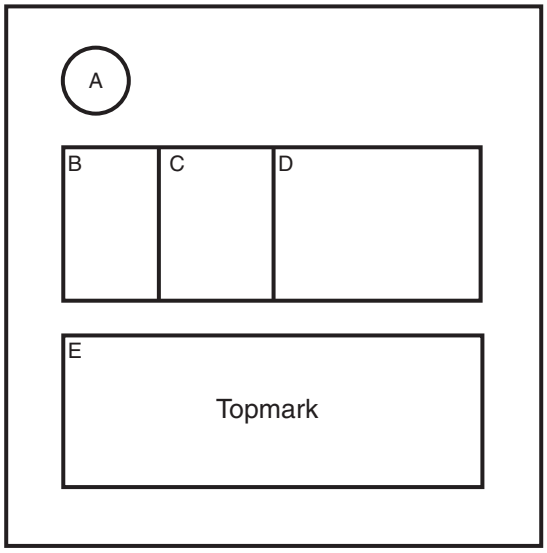
12 Package marking information

Table 12. Package marking(1)

Full part number	t_{SRC} delay control	Smart reset inputs type	V_{RST}	RST1 output type	t_{REC1} programming	RST2 output type	t_{REC2} option	Topmark
STM6513VEIEDG6F	TSR	AL	V	AH, PP	C_{tREC}	AL, OD	E	9AH
STM6513SEIEDG6F	TSR	AL	S	AH, PP	C_{tREC}	AL, OD	E	9SH
STM6513REIEDG6F	TSR	AL	R	AH, PP	C_{tREC}	AL, OD	E	9RH

1. AL = active-low, AH = active-high; PP = push-pull, OD = open-drain.

Figure 19. Package marking area, top view



A = dot (pin 1 reference)
B = assembly plant (P)
C = assembly year (Y, 0-9): 9 = 2009 etc.
D = assembly work week (WW, 01 to 52): 20 = WW20 etc.
E = marking area (topmark)

AM00479

13 Revision history

Table 13. Document revision history

Date	Revision	Changes
22-Oct-2009	1	Initial release.

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