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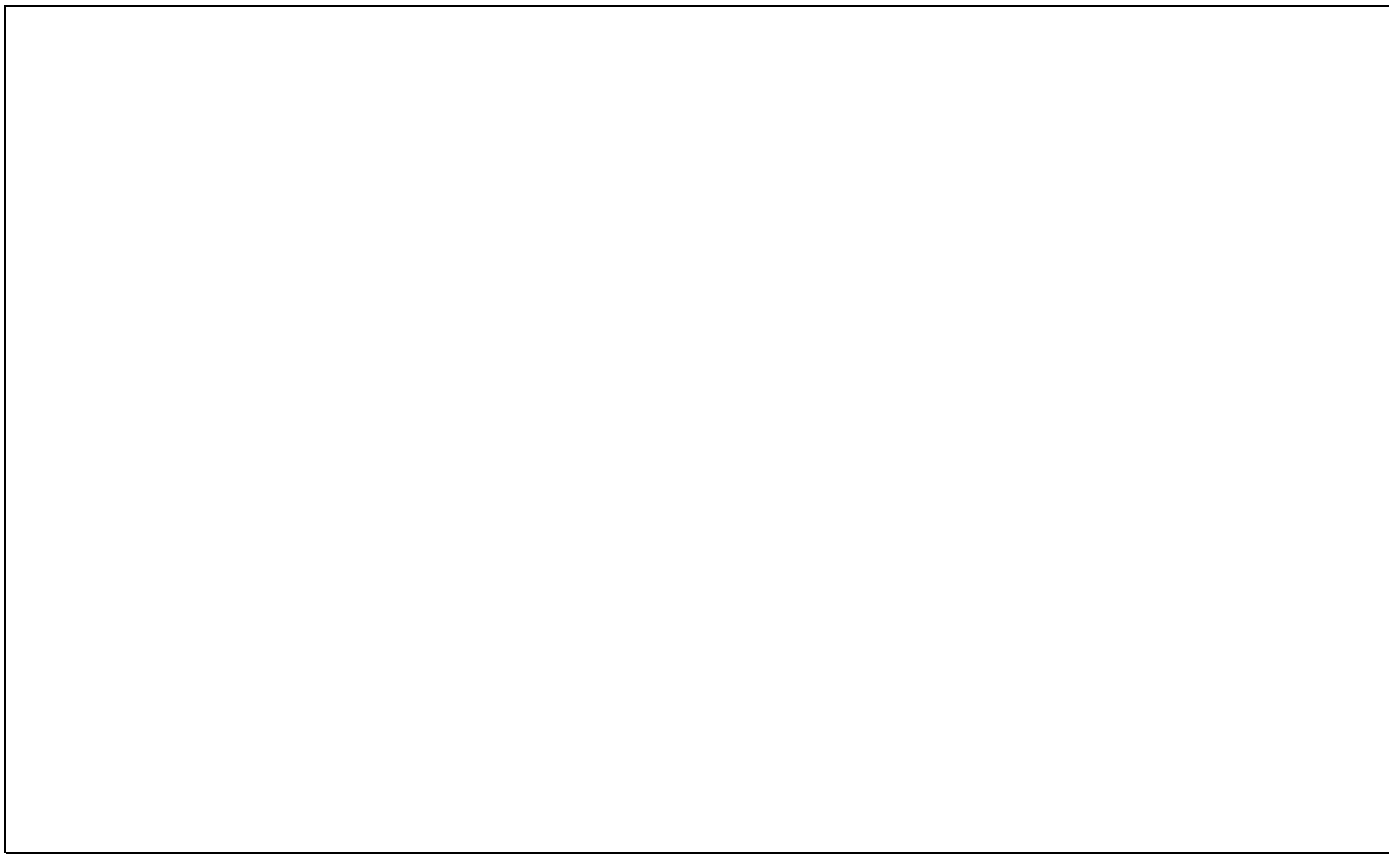

ICs for Consumer Electronics

DDC-PLUS-Deflection Controller
SDA 9361

Data Sheet 1998-02-01

Edition 1998-02-01

This edition was realized using the software system FrameMaker®

Published by Siemens AG, Bereich Halbleiter, Marketing-Kommunikation, Balanstraße 73, 81541 München

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SDA 9361 Revision History:		Current Version: 1998-02-01
Previous Version:		1997-04-07
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
33	35	Setup time of input HSYNC (CLEXT=1) changed from 6 ns to 4 ns
35	37	Nom. average and max. stand-by current specified
35	37	Specification of charge current pump of PLL pin LF is unnecessary

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Recommended Operating Conditions

Under this conditions the functions given in the circuit description are fulfilled. Nominal conditions specify mean values expected over the production spread and are the proposed values for interface and application. If not stated otherwise, nominal values will apply at T_A=25°C and the nominal supply voltage.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit.

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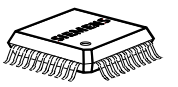
MOS

1 Overview



P-MQFP-44-2

1.1 Features

- Deflection - Protection - 16:9 / 4:3
- No external clock needed
- $\Phi 1$ PLL and $\Phi 2$ PLL on chip
- I^2C-Bus alignment of all deflection parameters
- All EW-, V- and H- functions
- PW EHT compensation
- PH EHT compensation
- Compensation of H-phase deviation (e.g. caused by white bar)
- Upper/lower EW-corner correction separately adjustable
- V-angle correction: Vertical frequent linear modulation of H-phase
- V-bow correction: Vertical frequent parabolic modulation of H-phase
- Three reduced V-scan modes (75 %, 66 %, 50 % V-size) adjustable by only 2 Bits
- H-frequent PWM output signal for general purpose
- H- and V-blanking time adjustable
- Partial overscan adjustable to hide the cut off control measuring lines in the reducedscan modes
- Stop/start of vertical deflection adjustable to fill out the 16/9 screen with different letterbox formats without annoying overscan
- Control signal SCAN as reference for vertical positioning of OSD, PIP etc.
- Vertical noise reduction with memory
- Standard and doubled line frequencies for NTSC and PAL, MUSE standard, ATV standard, HDTV standard
- Self adaptation of V-frequency/number of lines per field between 192 and 680 for each possible line frequency
- Protection against EHT run away (X-rays protection)

Type	Ordering Code	Package
SDA 9361	Q67107-H5167-A703	P-MQFP-44-2

- Protection against missing V-deflection (CRT-protection)
- Selectable softstart of the H-output stage
- Clock generation on chip
- P-MQFP-44-2 package
- 5 V supply voltage

1.2 General Description

The SDA 9361 is a highly integrated deflection controller for CTV receivers with standard or doubled line and field frequencies. It controls among others an horizontal driver circuit for a flyback line output stage, a DC coupled vertical saw-tooth output stage and an east/west raster correction circuit. All adjustable output parameters are I^2C Bus controlled. Inputs are HSYNC and VSYNC. The HSYNC signal is the reference for the internal clock system which includes the $\Phi 1$ and $\Phi 2$ control loops.

1.3 Pin Configuration

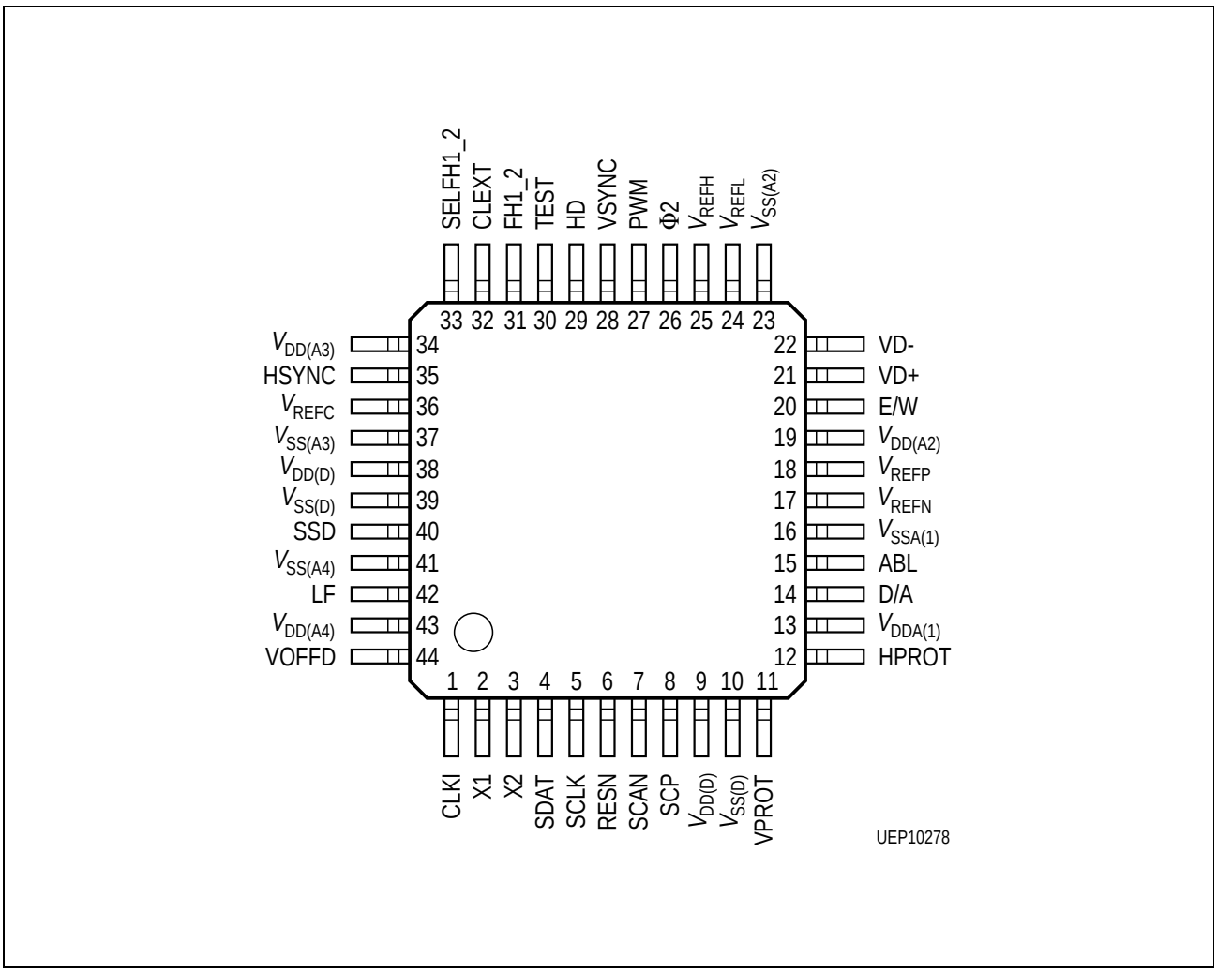


Figure 1

1.4 Pin Description

Pin No.	Symbol	Type	Description
1	CLKI	I/TTL	Input for external clock
2	X1	I	Reference oscillator input, crystal
3	X2	Q	Reference oscillator output, crystal
4	SDAT	IQ	I^2C-Bus data
5	SCLK	I	I^2C-Bus clock
6	RESN	I/TTL	Reset input, active low
7	SCAN	Q/TTL	Control signal for vertical positioning of OSD, PIP etc.
8	SCP	Q	Blanking signal with H- and color burst component (V-component selectable by I^2C Bus)
9	$V_{DD(D)}$	S	Digital supply
10	$V_{SS(D)}$	S	Digital ground
11	VPROT	I	Watching external V-output stage (input is the V-saw-tooth from feedback resistor)
12	HPROT	I	Watching EHT (input is e.g. H-flyback)
13	$V_{DD(A1)}$	S	Analog supply
14	D/A	Q	Output of an I^2C Bus controlled DC voltage
15	ABL	I	Input for a beam current dependent signal for stabilization of width, height and H-phase
16	$V_{SS(A1)}$	S	Analog ground
17	V_{REFN}	IQ	Ground for V_{REFP}, V_{REFH}, V_{REFL}
18	V_{REFP}	IQ	Reference voltage for IBEAM ADC, DAC, HPROT / VPROT thresholds
19	$V_{DD(A2)}$	S	Analog supply
20	E/W	Q	Control signal output for east/west raster correction
21	VD+	Q	Control signal output for DC coupled V-output stage
22	VD-	Q	Like VD+
23	$V_{SS(A2)}$	S	Analog ground
24	V_{REFL}	IQ	Reference voltages for E/W-DAC, V-DAC
25	V_{REFH}	IQ	Like V_{REFL}
26	$\Phi 2$	I	Line flyback for H-delay compensation
27	PWM	Q/TTL	Control signal output

1.4 Pin Description (cont'd)

Pin No.	Symbol	Type	Description
28	VSYNC	I/TTL	V-sync input
29	HD	Q	Control signal output for H driver stage
30	TEST	I/TTL	Switching normal operation (TEST = L) and test mode (TEST = H: pins 7, 27, 31, 32, 33, 40, 44 are additional test pins)
31	FH1_2	I/TTL	Switching between $1F_H$ mode (L) and $2F_H$ mode (H) (Pin SELFH1_2 = 0)
32	CLEXT	I/TTL	Switching between internal (L) and external clock (H)[1)]
33	SELFH1_2	I/TTL	Selection of switching between $1F_H$ mode and $2F_H$ mode SELFH1_2 = 0:$1F_H/2F_H$ selected via pin FH1_2 SELFH1_2 = 1:$1F_H/2F_H$ selected via I^2C-Bus register 00_H, Bit D5
34	$V_{DD(A3)}$	S	Analog supply
35	HSYNC	I	HSYNC input (CLEXT = 1: TTL; CLEXT = 0: analog)[1)]
36	V_{REFC}	I	Reference voltage for sync ADC
37	$V_{SS(A3)}$	S	Analog ground
38	$V_{DD(D)}$	S	Digital supply
39	$V_{SS(D)}$	S	Digital ground
40	SSD	I/TTL	Disables softstart
41	$V_{SS(A4)}$	S	Analog ground
42	LF	IQ	PLL loop filter
43	$V_{DD(A4)}$	S	Analog supply
44	VOFFD	I/TTL	Defines default value of VOFF-Bit (I^2C-Bus register 00_H, Bit D7)

1) The external clock mode can not be used with 33.75 kHz and 35 kHz line frequency.

1.5 Block Diagram

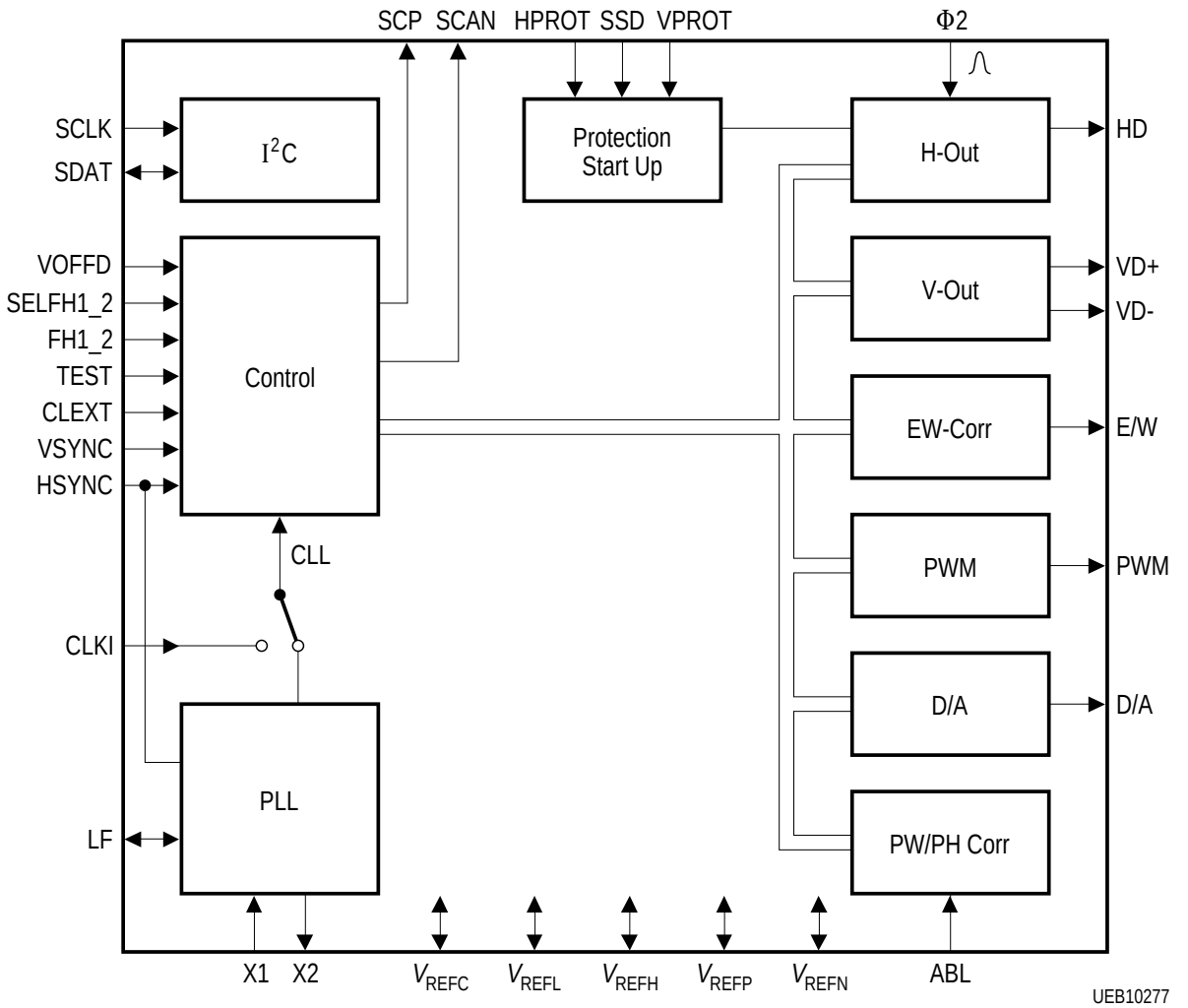


Figure 2

2 System Description

2.1 Functional Description

The main input signals are HSYNC with standard or doubled horizontal frequency and VSYNC with vertical frequencies of 50/100 Hz or 60/120 Hz.

The VSYNC is processed in a noise reduction circuit to enable synchronization by worse transmission too.

The output signals control the horizontal as well as the vertical deflection stages and the east/west raster correction circuit.

The H-output signal HD compensates the delays of the line output stage and its phase can be modulated vertical frequent to remove horizontal distortions of vertical raster lines (V-Bow, V-Angle). Time reference is the middle of the front and back edge of the line flyback pulse. A positive HD pulse switches off the line output transistor. Maximal H-shift is about 4.5 µs (for $1F_H$) or 2.25 µs (for $2F_H$).

Picture tubes with 4:3 or 16:9 aspect ratio can be used by adapting the raster to the aspect ratio of the source signal.

The V-output saw-tooth signals VD- and VD+ controls a DC coupled output stage and can be disabled. Suitable blanking signals are delivered by the IC.

The east/west output signal E/W is a vertical frequent parabola of 4th order, enabling an additional corner correction, separately for the upper and lower part.

The pulse width modulated horizontal frequent output signal PWM is for optional use. It can be modulated between 1 and 215 steps. The step width is $4*t_H/864$.

The output D/A delivers a variable DC signal for general purpose.

The picture width and picture height compensation (PW/PH Comp) processes the beam current dependent input signal ABL with effect to the outputs E/W and VD to keep width and height constant and independent of brightness.

The alignment parameter Horizontal Shift Compensation enables to adjust the influence of the input signal ABL on the horizontal phase.

The selectable start up circuit controls the energy supply of the H-output stage during the receiver's run up time by smooth decreasing the line output transistors switching frequency down to the normal operating value (softstart). HD starts with about double the line frequency and converges within 85 ms to its final value. The high time is kept constant.The normal operating pulse ratio H/L is 45/55.

The protection circuit watches an EHT reference and the saw-tooth of the vertical output stage. H-output stage is switched off if the EHT succeeds a defined threshold or if the V-deflection fails (**refer to page 46**).

HPROT:	Input	V_i < V2	Continuous blanking
		V_i > V1	HD disabled
		V2 ≤ V_i < V1	Operating range

VPROT: Vertical saw-tooth voltage
V_i < V1 in first half of V-period or
V_i > V2 in second half: HD disabled

The pin SCP delivers the composite blanking signal SCP. It contains burst (V_b), H-blanking HBL (V_{HBL}) and selectable V-blanking (control bit SSC). The phase and width of the H-blanking period can be varied by I^2C Bus. For the timing following settings are possible:

BD = 1	: t_{BL} = 0
BD = 0, BSE = 0 (default value)	: t_{HBL} = t_f (H-flyback time)
BD = 0, BSE = 1(alignment range)	: t_{HBL} = (4 ∗ H-blanking-time + 1) / CLL
	: t_{DBL} = (H-shift + 4 ∗ H-blanking-phase -2 ∗ H-blanking-time + 43) / CLL
SSC = 0	: t_{BL} = t_{VBL} during V-blanking period
SSC = 1	: t_{BL} is always t_{HBL}

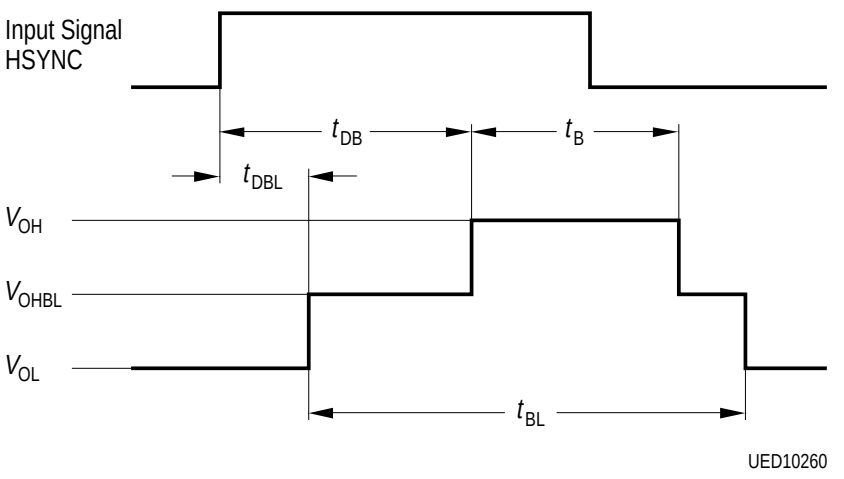


Figure 3

BG-pulse width t_B	54 / CLL	
Delay to HSYNC t_{DB}	if CLEXT = L-level:	(76-4 ∗ Internal-H-sync-phase) / CLL
	if CLEXT = H-level:	(38-4 ∗ Internal-H-sync-phase) / CLL

2.2 Circuit Description

The HSYNC is reference for a numeric PLL. This PLL generates a clock which is phase locked to the incoming horizontal sync pulse and exactly 864 times faster then the horizontal frequency. In order to lock the internal frequency to the external sync signal positive horizontal sync pulses are required (**see figure 4**).

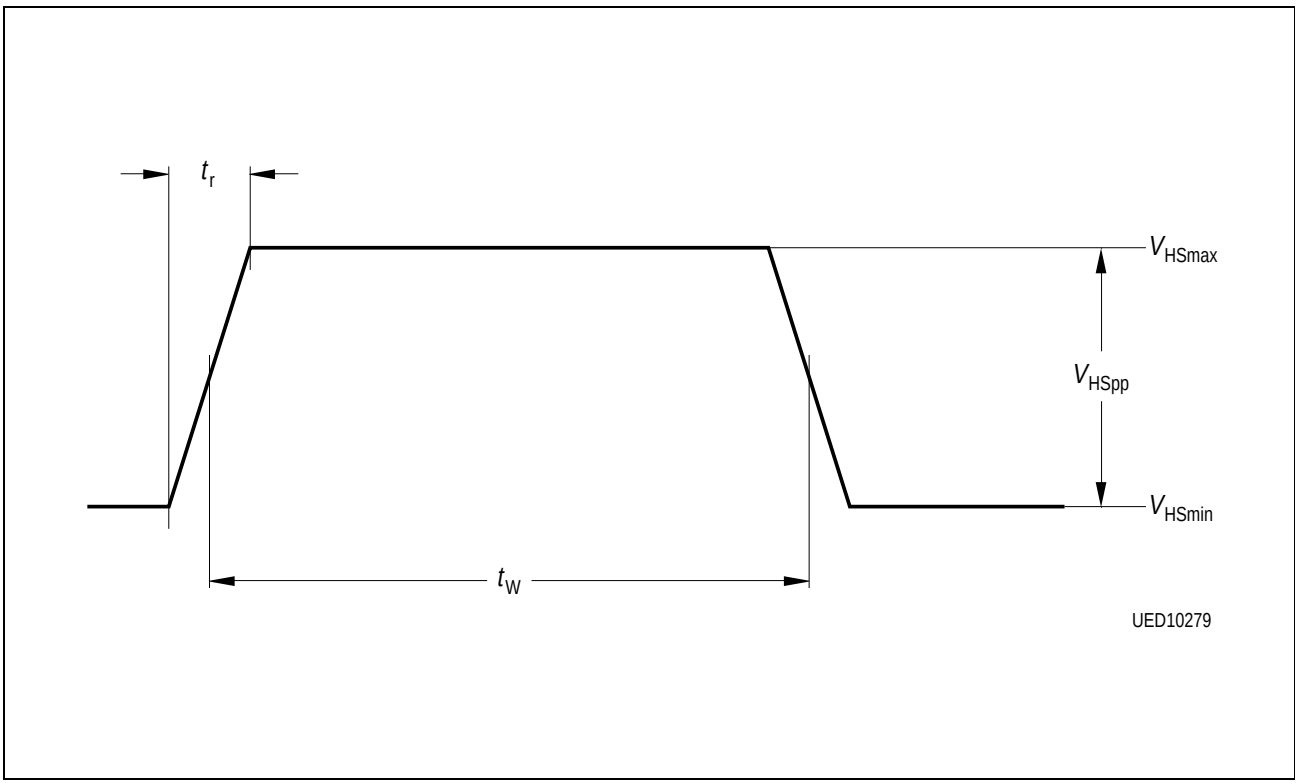


Figure 4
Incoming Signal HSYNC (CLEXT = 0)

Pulse width t_w for I^2C-Bus Bit 'HSWID' = 0:

3 µs ... 6.1 µs	low FH-range
1.5 µs ... 3.1 µs	high FH-range

Pulse width t_w for I^2C-Bus Bit 'HSWID' = 1:

3 µs ... 8.8 µs	low FH-range
1.5 µs ... 4.0 µs	high FH-range

Rise time t_r:100 ns minimum (CLEXT = 0)

The described input signal is first applied to an A/D converter. Conversion takes place with 6 Bits and a nominal frequency of 27 MHz. The digital PLL uses a low pass filter to obtain defined slopes for further measurements (PAL/NTSC applications). In addition the actual high and low level of the signal as well as a threshold value is evaluated and used to calculate the phase error between internal clock and external horizontal sync

pulse. By means of digital PI filtering an increment is gained from this. The PI filter can be set by the I²C-Bus VCR bit so that the lock-in behavior of the PLL is optimal in relation to either the TV or VCR mode. Moreover it is possible to adapt the nominal frequency by means of 5 I²C-Bus bits (INCR4..INCR0) to different horizontal frequencies. An additional bus bit GENMOD offers the possibility to use the PLL as a frequency generator which frequency is controlled by the INCR bits.

Once an increment has been obtained, either from the PI-filter or the I²C Bus, it can be used to operate the Digital Timing Oscillator. The DTO generates a saw-tooth with a frequency that is proportional to the increment. The saw-tooth is converted into a sinusoidal clock signal by means of sin ROM's and D/A converters and applied to an analog PLL which multiplies the frequency by 2 or 4 (depends on mode $1F_H$ or $2F_H$; for detailed explanation see pinning and I²C-Bus description) and minimizes residual jitter. In this manner the required line locked clock is provided to operate the other functional parts of the circuit. If no HSYNC is applied to pin 35 the system holds its momentary frequency for 2040 lines and following resets the PLL to its nominal frequency. The status bit CON indicates the lock state of the PLL.
The system also provides a stable HS-pulse for internal use. The phase between this internal pulse and the external HSYNC is adjustable via I²C-Bus bits HPHASE. It can be shifted over the range of one TV line.
An external clock (CLKI) can be provided by pin selection (CLEXT = H). The clock frequency has to be $864 * f_{HSYNC.}$The external clock mode can not be used with 33.75 kHz and 35 kHz line frequency.

For effective noise suppression the VSYNC has to pass a window at first and is then processed in a flywheel logic. The window allows a VSYNC pulse only after a minimum number of lines from its predecessor and sets an artificial one after a maximum number of lines. The number of H-periods between two subsequent VSYNCs is stored and determines (after several checks) the following V-periods (internal synchronization). If incoincidence is detected between internal and external VSYNC, the system switches after a hysteresis of a defined number of V-periods to external synchronization and the checks are repeated.

Values which influence shape and amplitude of the output signals are transmitted as reduced binary values to the SDA 9361 via I²C Bus. A CPU which is designed for speed reasons in a pipe line structure calculates in consideration of feedback signals (e.g.ABL) values which exactly represent the output signals. These values control after D/A conversion the external deflection and raster correction circuits.

The CPU firmware is stored in an internal ROM.

2.3 Reset Modes

The circuit is completely reset at power-on/off (**timing diagram see figure 11**) or if the pin RESN has L-level (**timing diagram see figure 12**). During standby operation some parts of the circuit are not affected (**timing diagram see figure 12**):

	Power-On-Reset	**External Reset (pin RESN = Low)**	**Standby Mode (I^2C Bit STDBY = 1)**
HD output	Low	Low	Active
H-protection	Inactive	Inactive	Inactive
V-protection	Inactive	Inactive	Inactive
I^2C interface (SDA, SCL)	Tristate	Tristate	Ready
I^2C register 01_H...$1C_H$, $1F_H$	Set to default values	Set to default values	Set to default values
I^2C register 00_H, $1D_H$, $1E_H$, 44_H...48_H	Set to default values	Set to default values	Not affected
Status Bit PONRES	Set to 1[1)]	Set to 1[1)]	Not affected
V_{REFP}, V_{REFH}. V_{REFL}	Not affected	Not affected	Inactive
CPU	Inactive	Inactive	Inactive

[1)] Can only be read after Power-On-Reset is finished

Note: *Power-On-Reset and RESN = Low state are deactivated after ca. 32 cycles of the X1/X2 oscillator clock and ca. 42 cycles of the CLL clock.*
Standby state is deactivated after ca. 42 cycles of the CLL clock.

2.4 Frequency Ranges

H	V	n_L
15.625 kHz	50 Hz	625 I
15.75 kHz	60 Hz	525 I
31.25 kHz	50 Hz 100 Hz	625 NI / 1250I 625 I
31.5 kHz	60 Hz 70 Hz 120 Hz	525 NI / 1050 I 449 NI 525 I
32.4 kHz	60 Hz	1080 I
33.75 kHz[1)]	60 Hz	1125 I
35 kHz[1)]	66.7 Hz	525 NI

[1)] Only with internal clock generation

The allowed deviation of all input line frequencies is max. ±4.5 %.

n_L: number of lines per frame
I: interlaced
NI: non interlaced

If NSA = 0 (subaddress 01_H/$D5_H$) number of lines per field is selfadaptable between 192 and 680 for each specified H-frequency.

2.5 I²C-Bus Control

2.5.1 I²C-Bus Address

1	0	0	0	1	1	0

2.5.2 I²C-Bus Format

write:

S	1	0	0	0	1	1	0	0	A	Subaddress	A	Data Byte	A	*****	A	P

read:

S	1	0	0	0	1	1	0	1	A	Status byte	A	Data Byte n	A	*****	NA	P

Reading starts at the last write address n. Specification of a subaddress in reading mode is not possible.

S: Start condition
A: Acknowledge
P: Stop condition
NA: Not Acknowledge

An automatically address increment function is implemented.

After switching on the IC, all bits are set to defined states.

2.5.3 I²C-Bus Commands

Control item	Sub-addr.	D7	D6	D5	D4	D3	D2	D1	D0	Allowed Range	Effective Range	Can be Disabled by Bit	Default Value if Disabled	Unit
Deflection control 0	00_H	see below								–	–	–	–	–
Deflection control 1	01_H	see below								–	–	–	–	–
Vertical shift	02_H	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Vertical size	03_H	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Vertical linearity	04_H	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Vertical S-correction	05_H	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Vertical EHT compensation [1]	06_H	B7	B6	B5	B4	B3	B2	B1	B0	0..255	0..255	–	–	–
Horizontal size	07_H	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Pin phase	08_H	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Pin amp	09_H	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Upper corner pin correction	$0A_H$	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Lower corner pin correction	$0B_H$	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Horizontal EHT compensation [1]	$0C_H$	B7	B6	B5	B4	B3	B2	B1	B0	0..255	0..255	–	–	–
Horizontal shift	$0D_H$	B6	B5	B4	B3	B2	B1	B0	X	-64..63	-64..63	–	–	1/CLL
Vertical angle	$0E_H$	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
Vertical bow	$0F_H$	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-128..127	–	–	–
PWM start	10_H	B7	B6	B5	B4	B3	B2	B1	B0	0..255	0..215	–	–	4/CLL
D/A [1]	11_H	B5	B4	B3	B2	B1	B0	X	X	-32..31	-32..31	–	–	–
Vertical blanking time [1]	12_H	X	B6	B5	B4	B3	B2	B1	B0	0..127	a)	BSE = 0	b)	lines
Horizontal blanking time	13_H	X	X	B5	B4	B3	B2	B1	B0	0..63	0..63	BSE = 0	H-flyback	4/CLL
Start vertical scan [1]	14_H	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	c)	SSE = 0	9	line
Horizontal blanking phase	15_H	B5	B4	B3	B2	B1	B0			-32..31	-32..31	–	–	4/CLL
Vertical scan width 0 [1]	15_H							B9	B8	0..+3	d)	STE = 0	e)	256 lines
Vertical scan width 1 [1]	16_H	B7	B6	B5	B4	B3	B2	B1	B0	0..255	d)	STE = 0	e)	lines
Guard band [1]	17_H	X	X	B5	B4	B3	B2	B1	B0	0..63	0..63	GBE = 0	3	half lines
Start reduced scan [1]	18_H	X	X	B5	B4	B3	B2	B1	B0	0..63	0, 2..63	SRSE = 0	2	line
Vertical sync control	19_H	see below								–	–	–	–	–
Min. No. of lines / field [1]	$1A_H$	B7	B6	B5	B4	B3	B2	B1	B0	0..255	0..255	–	–	2 lines
Max. No. of lines / field [1]	$1B_H$	B7	B6	B5	B4	B3	B2	B1	B0	0..255	0..255	–	–	2 lines
AFC EHT compensation [1]	$1C_H$	B5	B4	B3	B2	B1	B0	X	X	-32..31	-32..31	–	–	–
Internal PLL control	$1D_H$	see below								–	–	–	–	–
Internal H-sync phase	$1E_H$	B7	B6	B5	B4	B3	B2	B1	B0	-128..127	-96..119	–	–	4/CLL
PWM width	$1F_H$	B7	B6	B5	B4	B3	B2	B1	B0	0..255	0..215	PWM width=0	15	4/CLL
Universal register 1	45_H	see below								–	–	–	–	–
Universal register 3	47_H	see below								–	–	–	–	–
Internal voltage Ref control	48_H	see below								–	–	–	–	–

[1] see 2.5.5: Explanation of some control items

a) The effective range for **Vertical Blanking Time**:

16 ... 127 (absolute value)	if STE = 0
0 ... 127 (offset value)	if STE = 1.

b) The "default value if disabled" for **Vertical Blanking Time**:

21 (absolute value)	if STE = 0
8 (offset value)	if STE = 1.

c) The effective range for **Start Vertical Scan:**

2 ... 127 (absolute value)	if STE = 0
	if STE = 1 and NSA = 1
-128 ... 127 (offset value)	if STE = 1 and NSA = 0.

d) The effective range for **Vertical Scan** (total width: 10 Bit): 160 ... 684 lines.

e) The "default value if disabled" for **Vertical Scan** equals the number of lines of the source signal reduced by the control value for **Start Vertical Scan**. (E.g.: input signal: 262 lines per field; Start vertical scan = 8 lines; then (if SSE = 1, STE = 0) vertical scan = 262 - 8 = 254 lines.

At power on the RAM containing the control items is cleared. Therefore all data are zero by default (if not otherwise defined) before transferring individual values via I^2C Bus.
Allowed values out of the effective range are limited, e. g. Vertical blanking time = 3 is limited to 16 if STE = 0 (that means a minimum of 16 lines is blanked).
There are five bits (SRSE, BSE, SSE, STE, GBE) in the deflection control byte 1 for disabling some control items. If one of these bits is "0", the value of the corresponding control item will be ignored and replaced by the value "default value if disabled" in the table above.

2.5.4 Detailed Description

The **Deflection Control Byte 0** includes the following bits:

VOFF	STDBY	2FH	BD	RABL	VR1	VR0	HDE

VOFF: Vertical off
- 0: normal vertical output due to control items
- 1: vertical saw-tooth is switched off, vertical protection is disabled

Default value depends on pin 44 (VOFFD)
VOFFD = Low: 0
VOFFD = High: 1

STDBY: Stand-by mode
0: normal operation
1: stand-by mode (all internal clocks are disabled)

2FH: Setting of line frequency
0: low range of line frequency (14900 Hz ... 17650 Hz)
1: high range of line frequency (29800 Hz ... 35300 Hz)

*N**ote:** this bit is don't care if pin SELFH1_2 has L-level*

BD: Blanking disable
0: horizontal and vertical blanking enabled
1: horizontal and vertical blanking disabled

RABL: ABL input range
0: 2 V ... 3 V
1: 0 V ... 4 V

VR1 ... VR0: Reduction of the vertical size
00: 100 % V-size (16:9 source on 16:9 display)
01: 75 % V-size (16:9 source on 4:3 display)
10: 66 % V-size (two 4:3 sources on 16:9 display)
11: 50 % V-size (two 16:9 sources on 16:9 display)

HDE: HD enable
0: line is switched off (HD disabled, that is L-level)
1: line is switched on (HD enabled)

Default value depends on pin 40 (SSD)
SSD = Low: 0
SSD = High: 1

The **Deflection Control Byte 1** includes the following bits:

0	X	NSA	STE	GBE	SRSE	SSE	BSE

NSA: No self adaptation
0: self adaptation on
1: self adaptation off

STE: Scan time enable
- 0: control items for vertical scan width 0 and width 1 are disabled
- 1: control items for vertical scan width 0 and width 1 are enabled

GBE: Guard band enable
- 0: control item for guard band is disabled
- 1: control item for guard band is enabled

SRSE: Start reduced scan enable
- 0: control item for start reduced scan is disabled
- 1: control item for start reduced scan is enabled

SSE: Start scan enable
- 0: control item for start vertical scan is disabled
- 1: control item for start vertical scan is enabled

BSE: Blanking select enable
- 0: control items for blanking times are disabled
- 1: control items for blanking times are enabled

The **Vertical Sync Control Byte** includes the following bits:

X	X	SSC	NR	NI	NL2	NL1	NL0

SSC: Sandcastle without VBL
- 0: output SCP with VBL component
- 1: output SCP without VBL component

NR: Noise reduction
- 0: no noise reduction of the vertical sync
- 1: noise reduction of the vertical sync

NI: Non interlace
- 0: interlace depends on source
- 1: no interlace

NL2 ... NL0: Number of lines per field when NR = 1 and no vertical sync at the input is detected

NL2	NL1	NL0	Number of Lines per Field
0	0	0	262.5
0	0	1	312.5
0	1	0	525
0	1	1	562.5
1	X	X	625

The **Internal PLL Control Byte** includes the following bits:

HSWID	GENMOD	VCR	INCR4	INCR3	INCR2	INCR1	INCR0

HSWID: Maximum width of HSYNC
- 0: 6.1 µs for low FH-range
  3.1 µs for high FH-range
- 1: 8.8 µs for low FH-range
  4.0 µs for high FH-range

GENMOD: Clock generator mode
- 0: normal PLL mode
- 1: generator mode (fixed frequency output, controlled by INCR..)

VCR: PLL filter optimized for
- 0: TV mode
- 1: VCR mode

INCR4 ... 0: Nominal PLL output frequency
for low FH-range:
INCR = INT((FH * 110592) / FQ - 64.625)
for high FH-range:
INCR = INT((FH * 55296) / FQ - 64.625)
(for typical values see table below)

specified range for:
GENMOD = 0: $6 \leq INCR \leq 14$
GENMOD = 1: $3 \leq INCR \leq 18$
(FQ = 24.576 MHz)

Application	FH[Hz]	INCR
PAL	15625	6
NTSC	15750	6
PAL (100 Hz)	31250	6
NTSC (120 Hz)	31500	6
ATV	32400	8
MUSE	33750	11
Macintosh	35000	14

Default value: INCR = 6

Warning:

1) A change of INCR or 2FH causes spontaneous changes of the generated clock frequency greater than the specified 4.5 %.
   Switching from PLL mode to Generator mode (GENMOD) with constant INCR values does not result in exceeding the specified frequency deviation range.
2) If pin SSD has H-level the output signal HD starts immediately after power on. In this case the starting horizontal frequency is either 15.75 kHz (if SELFH1_2 has H-level or if SELFH1_2 and FH1_2 have L-level) or 31.5 kHz (if SELFH1_2 has L-level and FH1_2 H-level). Starting with Muse or Macintosh standard requires L-level at SSD so that INCR can be changed before enabling HD with HDE = 1.
3) Using external clock at pin 1, CLKI, (pin 32, CLEXT = 1): no internal protection against missing clock pulses is provided.
4) In order to guarantee error free operation of the build in soft start circuit the input frequency has to be inside the lock range of the PLL (+/-4.5 % of standard input frequency)

The **Universal Register 1 (Subaddress 45_H)** includes the following bit:

0	0	NOISY VCR	0	0	0	0	0

NOISYVCR: Handling of noisy input signals in VCR mode
0: normal handling
1: improved handling
Note: *this bit is don't care if bit VCR = 0 (TV mode)*

The **Universal Register 3 (Subaddress 47_H)** includes the following bits:

0	0	0	KILL_ZIP	TC_3RD	0	0	0

KILL_ZIP: Top flutter suppression
0: no top flutter suppression
1: top flutter suppression
(phase jumps max. ±12 µs for low FH-range
rsp. max. ±6 µs for high FH-range)

TC_3RD: Third time constant
0: slow VCR time constant
1: fast VCR time constant
Note: *this bit is don't care if bit VCR = 0 (TV mode)*

The **Internal Voltage Ref. Control Byte** includes the following bits:

BANDG4	BANDG3	BANDG2	BANDG1	BANDG0	BANDG OFF	BANDG4 OFF	0

BANDG4 ... BANDG0: Adjustment of internal bandgap reference
10000: Reference Output voltage min
:
01111: Reference Output voltage max
Typical adjustment range is 0.5 V.

BANDGOFF: Bandgap Off
0: V_{REFH}, V_{REFL} derived internally from V_{REFP}

1: external references on V_{REFP}, V_{REFH}, V_{REFL} have to be applied (in this case BANDG4OFF must be = 1)

BANDG4OFF: Bandgap 4 V Off
0: internal bandgap reference is used for V_{REFP}
1: external reference on V_{REFP} (4 V) has to be applied

The **Status Byte** includes the following bits:

HPON	VPON	CON	-	-	-	-	PONRES

HPON: protection on
0: normal operation of the line output stage
1: high level on input HPROT has switched off the line

VPON: V-protection on
0: normal operation of the vertical output stage
1: incorrect signal on input VPROT has switched off the line

CON: Coincidence not
0: H-coincidence detected
1: no H-coincidence detected

PONRES: Power-On-Reset
0: after bus master has read the status byte
1: after each detected reset

Note: *PONRES is reset after this byte has been read.*

2.5.5 Explanation of Some Control Items

D/A

This item controls directly a 6 Bit D/A Converter at the output D/A that can be used for general purpose.

Start Vertical Scan

If enabled (SSE = 1) this control item defines the start of calculation of the vertical saw-tooth, the east/west parabola and the vertical function required for the vertical modulated output HD.

Vertical Scan (width0 and width1)

The total width of this control item is 10 Bit. Therefore two registers (width0 and width1) are necessary. If enabled (STE = 1) it defines the duration of the vertical scan. When the vertical period has more lines than the sum of **Start Vertical Scan** and **Vertical Scan**, the calculation of the vertical saw-tooth, the east/west parabola and the vertical parabola required for HD stops so that the corresponding output signals remain unchanged till the next vertical synchron pulse.

Guard Band

This control item is useful for optimizing self adaptation. Video signals with different number of lines in consecutive fields (e. g. VCR search mode) must not start the procedure of self adaptation. But switching between different TV standards has to change the slope of the vertical saw-tooth getting always the same amplitude (self adaptation). To avoid problems with flicker free TV systems which have alternating number of lines per field an average value of four consecutive fields is calculated. If the deviation of these average values (e.g. PAL: 312.5 lines or 625 half lines) is less or equals **Guard Band**, no adaptation takes place. When it exceeds **Guard Band**, the vertical slope will be changed.

Start Reduced Scan

If enabled (SRSE = 1) this item defines the start of the D/A conversion of the calculated vertical saw-tooth. From begin of the vertical flyback to the line defined by **Start Reduced Scan** the output signals VD+, VD- remain unchanged (flyback level). Other outputs are not affected.

a) control bits VR1, VR0 # 00 (reduction of vertical size)
In this case the byte is useful for e.g. displaying 16/9 source format on 4/3 picture tubes without visible RGB lines generated of the automatic cut-off control (partial overscan). It defines the start of the reduced amplitude (factors 0.5, 0.66, 0.75) of the vertical saw-tooth (**refer page 39**). When **Start Reduced Scan** = 0 the reduction takes place over all lines including vertical flyback.

b) control bits VR1, VR0 = 00 (no reduction of vertical size)
If **Start Reduced Scan** > **Start Vertical Scan** the D/A conversion of the saw-tooth starts (**Start Reduced Scan** - **Start Vertical Scan**) lines after begin of the calculation. This causes a jump of the output voltage VD+, VD- from flyback to scan level. It may be useful to hide the automatic cut-off control lines if no overscan is desired (e.g. for VGA display). If **Start Reduced Scan** <= **Start Vertical Scan** this byte has no effect.

Vertical EHT Compensation

This item controls the influence of the beam current dependent input signal ABL on the outputs VD+ and VD- according to the following equation:

$$\Delta V_{VDPP} = \Delta V_{ABL} * \frac{\text{Vertical EHT compensation}}{512} * 0{,}57^{1)} \quad \text{(if RABL = 0)}$$

$$\Delta V_{VDPP} = \Delta V_{ABL} * \frac{\text{Vertical EHT compensation}}{2048} * 0{,}57^{1)} \quad \text{(if RABL = 1)}$$

ΔV_{VDPP}: variation of VD+ and VD- peak-to-peak voltage
ΔV_{ABL}: variation of ABL input voltage

1) The factor 0.57 depends on V_{REFP}, V_{REFH}, V_{REFL}

If **Vertical EHT Compensation** = 0 the outputs VD+ and VD- are independent of the input signal ABL.

Horizontal EHT Compensation

This item controls the influence of the input signal ABL on the output E/W according to the following equation:

$$\Delta V_{EW} = \Delta V_{ABL} * \frac{\text{Horizontal EHT compensation}}{128} * 2{,}12^{1)} \quad \text{(if RABL = 0)}$$

$$\Delta V_{EW} = \Delta V_{ABL} * \frac{\text{Horizontal EHT compensation}}{512} * 2{,}12^{1)} \quad \text{(if RABL = 1)}$$

ΔV_{EW}: variation of E/W output voltage
ΔV_{ABL}: variation of ABL input voltage

1) The factor 2.12 depends on V_{REFP}, V_{REFH}, V_{REFL}

If **Horizontal EHT Compensation** = 0 the output E/W is independent of the input signal ABL.

AFC EHT Compensation

Deviation of the horizontal phase caused by high beam current (e.g. white bar) can be eliminated by this control item. The beam current dependent input signal ABL is multiplied by **AFC EHT Compensation**.

Additional to the control items Vertical angle, Vertical bow and Horizontal shift, this product influences the horizontal phase at the output HD according to the following equation:

$$\Delta\phi = \Delta V_{ABL} * \frac{\text{AFC EHT compensation}}{64} * \frac{52^{1)}}{CLL} \quad \text{(if RABL = 0)}$$

$$\Delta\phi = \Delta V_{ABL} * \frac{\text{AFC EHT compensation}}{256} * \frac{52^{1)}}{CLL} \quad \text{(if RABL = 1)}$$

$\Delta\phi$:variation of horizontal phase at the output HD
(positive values: shift left, negatives values: shift right)
ΔV_{ABL} :variation of ABL input voltage (units: Volt)
CLL :$864 * F_H$

1) The factor 52 depends on V_{REFP}

Vertical Blanking Time (VBT)

VBT defines the vertical blanking pulse VBL which is part of the output signal SCP. VBL is synchronized with the leading edge of HSYNC. It always starts and stops at the beginning of line and never in the center.

a) Case of STE = 0

In this case the control item Vertical blanking time defines the duration of the V-blanking pulse (VBL) exactly in number of lines. Because of IC internal limitations 16 through 127 lines can be blanked. If BSE = 0 the control item Vertical blanking time is disabled and always 21 lines (default value if disabled) are blanked.
After power on the control bit BSE is 0. Therefore 21 lines will be blanked before any programming of the IC. If **Vertical Blanking Time** is less or equals 21 lines, VBL starts (point A in fig. above) always 0 ... 0.5 line (new odd field) or 0.5 ... 1 line (new even field) prior to the vertical flyback. Otherwise VBL is concentric to a fictitious vertical flyback period of 21 lines, that means VBL starts (VBT - 21) / 2 lines at the end of an odd field or (VBT - 20) / 2 at the end of an even field prior to point A. Possible start points are only the beginning of line.

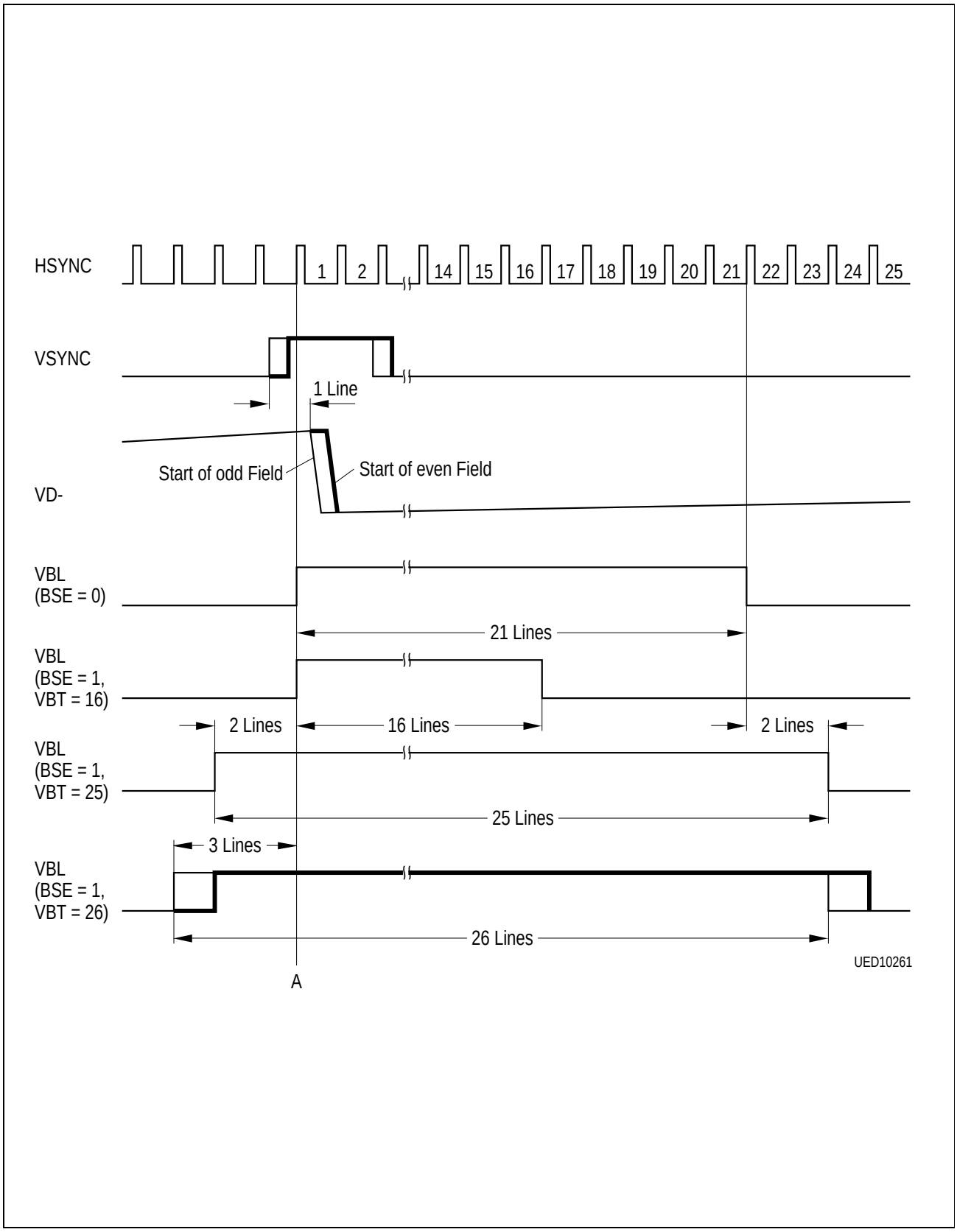


Figure 5
Vertical Blanking Pulse VBL when STE = 0 and Number of Lines per

Field = Constant

b) Case of STE = 1
In this case the control item Vertical blanking time is an extension for the V-blanking pulse.

- If BSE = 1 and VBT = 0 the V-blanking pulse has its minimum: it starts always at end of scan (line B in Fig. below) and ends at start of scan (line C) defined by the control items **Start Vertical Scan** (if SSE = 1) and **Vertical Scan**.
- BSE = 1 and (128 > VBT > 0) extend the V-blanking pulse according to the following relationship
  (If VBT > 127 this value is ignored and replaced by VBT - 128):
  VBL starts VBT / 2 lines (even field) respectively (VBT + 1) / 2 lines (odd field) prior to line B.
  VBL ends (VBT + 1) / 2 lines (even field) respectively VBT / 2 lines (odd field) after end of line C.
  Possible start points are only the beginning of line.
- If BSE = 0 (after power on) the control item **Vertical Blanking Time** is disabled and VBL starts 4 lines prior to end of scan (line B) and ends 4 lines after start of scan (line C).

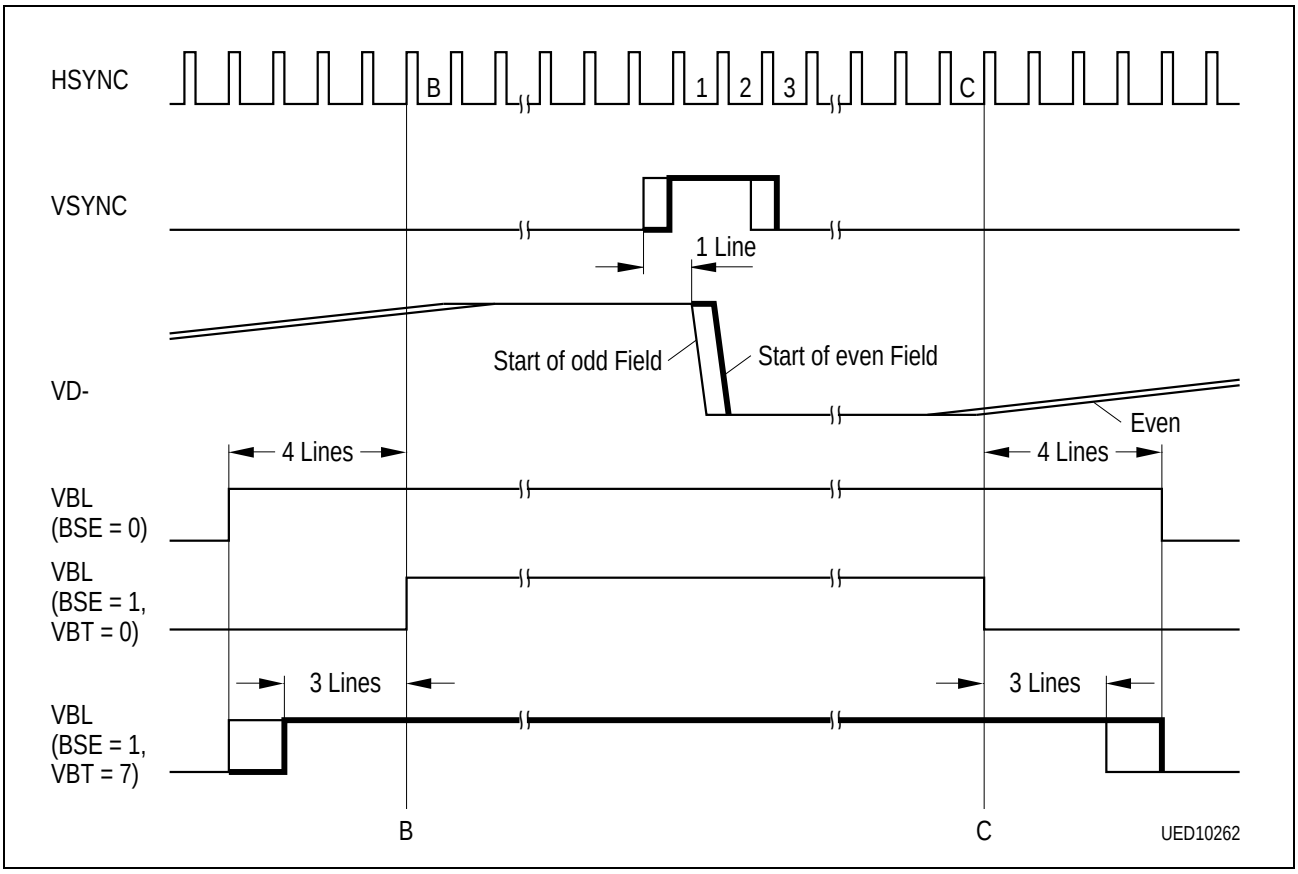


Figure 6
Vertical Blanking Pulse VBL when STE = 1

Minimum Number of Lines per Field

It defines the minimum number of lines per field for the vertical synchronisation. If the TV standard at the inputs VSYNC and HSYNC has less lines per field than defined by **Minimum Number of Lines per Field** no synchronisation is possible.The relationship between **Minimum Number of Lines per Field** and the minimum number of lines is given in the following table:

Minimum Number of Lines per Field	Minimum Number of Lines per Field
0	192
1	194
...	...
127	446
128	448
...	...
254	700
255	702

Maximum Number of Lines per Field

It defines the maximum number of lines per field for the vertical synchronisation. If the TV standard at the inputs VSYNC and HSYNC has more lines per field than defined by **Maximum Number of Lines per Field** no synchronisation is possible. The relationship between **Maximum Number of Lines per Field** and the maximum number of lines is given in the following table:

Maximum Number of Lines per Field	Maximum Number of Lines per Field
0	702
1	192
2	194
...	...
127	444
128	446
...	...
255	700

Most Important V-Deflection Modes for 4:3 CRT

Mode	Description	Characteristics	Notes	VR1 VR0	NSA	SRSE	GBE	STE	SSE
N0	Normal mode (for 4:3 source, Letterbox) with **default** settings	Self adaptation scan start = line 9 start of V-ramp = line 9 scan time: depends on source signal guard band = 1.5 lines	Mode after power on	00	0	0	0	0	0

N1	Normal mode (for 4:3 source, Letterbox) with **user defined** values	Self adaptation
		scan start = **Start Vertical Scan**
		if (**Start Reduced Scan**>**Start Vertical Scan**)
		start of V-ramp = **Start Reduced Scan**
		else
		start of V-ramp = **Start Vertical Scan**
		scan time: depends on source signal
		guard band = **Guard Band**/2 [lines]
			Start of scan adjustable
			start of V-ramp adjustable
			guard band adjustable
				00	0	1	1	0	1

S0	Shrink mode 75% (for 16:9 source) with **default** settings	Self adaptation scan start = line 9 start of reduced V-ramp = line 9 scan time: depends on source signal guard band = 1.5 lines		01	0	0	0	0	0

S1	Shrink mode 75% (for 16:9 source) with **user defined** values	Self adaptation
		scan start = **Start Vertical Scan**
		if (**Start Reduced Scan**>**Start Vertical Scan**)
		start of reduced V-ramp =
		Start Reduced Scan
		else
		start of reduced V-ramp =
		Start Vertical Scan
		scan time: depends on source signal
		guard band = **Guard Band**/2 [lines]
			Start of scan adjustable
			start of reduced V-ramp adjustable
			guard band adjustable
				01	0	1	1	0	1

Most Important V-Deflection Modes for 16:9 CRT

Mode	Description	Characteristics	Notes	VR1 VR0	NSA	SRSE	GBE	STE	SSE
N0	Normal mode (for 16:9 or 4:3 source) with **default** settings	Self adaptation scan start = line 9 start of V-ramp = line 9 scan time: depends on source signal guard band = 1.5 lines	Mode after power on	00	0	0	0	0	0

N1	Normal mode (for 16:9 or 4:3 source) with **user defined** values	Self adaptation
		scan start = **Start Vertical Scan**
		if (**Start Reduced Scan**>**Start Vertical Scan**)
		start of V-ramp = **Start Reduced Scan**
		else
		start of V-ramp = **Start Vertical Scan**
		scan time: depends on source signal
		guard band = **Guard Band**/2 [lines]
			Start of scan adjustable
			start of V-ramp adjustable
			guard band adjustable
				00	0	1	1	0	1

Z	Zoom mode (for 4:3 source, Letterbox)	scan start = (number_of_lines - **Vertical Scan**)/2 + 8 scan time = **Vertical Scan**	Vertical scan controls zoom factor	00	0	X	X	1	0
SC	Scroll mode (for 4:3 source, Letterbox)	Scan start = (number_of_lines - **Vertical Scan**)/2 + 8 + **Start Vertical Scan** scan time = **Vertical Scan**	Like above; Start vertical scan can be additionally used for adjustment of picture phase	00	0	X	X	1	1
M	Manual mode (for 4:3 source, Letterbox)	Scan start = **Start Vertical Scan** scan time = **Vertical Scan**	Scan start and scan time are separately adjustable	00	1	X	X	1	X
S2	Shrink mode 66% (for two 4:3 sources) with **default** settings	Self adaptation scan start = line 9 start of reduced V-ramp = line 9 scan time: depends on source signal guard band =1.5 lines		10	0	0	0	0	0
S3	Shrink mode 50% (for two 16:9 sources) with **default** settings	Self adaptation scan start = line 9 start of reduced V-ramp = line 9 scan time: depends on source signal guard band = 1.5 lines		11	0	0	0	0	0

3 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remark
		min.	max.		
Operating temperature	T_A	-20	70	°C	
Storage temperature	T_{stg}	-40	125	°C	
Junction temperature	T_j		125	°C	
Soldering temperature	T_S		260	°C	
Input voltage	V_I	V_{SS} - 0.3 V	V_{DD} + 0.3 V		
Output voltage	V_Q	V_{SS} - 0.3 V	V_{DD} + 0.3 V		
Supply voltages	V_{DD}	-0.3	6	V	
Supply total voltage differentials		-0.25	0.25	V	1)
Total power dissipation	P_{tot}		0.85	W	
Latch-up protection		-100	100	mA	All inputs/outputs

1) Between any internally non-connected supply pin of the same kind.
All $V_{DD(D)}$ - and $V_{DD(A)}$ - Pins are connected internally by about 3 Ω
The $V_{SS(D)}$-Pins are connected internally by about 3 Ω

***Note**: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this specification is not implied.*

3.1 Recommended Operating Conditions

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
Supply voltages	V_{DD}	4.5	5	5.5	V	
Ambient temperature	T_A	-20	25	70	°C	For analog parameters: 0°C
TTL Inputs: CLKI, VSYNC, TEST, FH1_2, SELFH1_2, CLEXT, SSD, VOFFD, RESN						
H-input voltage	V_{IH}	2.0		V_{DD}	V	
L-input voltage	V_{IL}	0		0.8	V	
Input VPROT						
Threshold V1		1.4	1.5	1.6	V	V_{REFP} = 4 V
Threshold V2		0.9	1.0	1.1	V	V_{REFP} = 4 V
Input HPROT						
Threshold V1		3.9	4	4.1	V	V_{REFP} = 4 V
Threshold V2		2.1	2.4	2.7	V	V_{REFP} = 4 V
Input ABL						
L-input voltage	V_{IL}		2		V	V_{REFP} = 4 V RABL = 0
			0		V	V_{REFP} = 4 V RABL = 1
Full range input voltage			3		V	V_{REFP} = 4 V RABL = 0
			4		V	V_{REFP} = 4 V RABL = 1
Reference Voltage Input Pins (Internal Voltage Ref. Control Byte Reg 48H = 00000110)						
V_{REFP} input voltage	V_{VREFP}		4		V	
V_{REFH} input voltage	V_{VREFH}		2.5		V	
V_{REFL} input voltage	V_{VREFL}		1.2		V	
V_{REFN} input voltage	V_{VREFN}		0		V	
V_{REFC} input voltage	V_{VREFC}		5		V	Independent of register 48_H, max = V_{DD}

3.1 Recommended Operating Conditions (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
Input Φ2						
L-input voltage	V_{IL}	0		0.7	V	V_{REFP} = 4 V
H-input voltage	V_{IH}	2.0		V_{DD}	V	V_{REFP} = 4 V
Input HSYNC (CLEXT = 0)						
Input voltage range	V_{HSpp}	2		V_{DD}	V	See page 12
Input voltage low level	V_{HSmin}	0			V	See page 12
Input voltage high level	V_{HSmax}			V_{DD}		See page 12
Pulse width (HSWID = 0)	t_w	3.0		6.1	µs	Low FH-range
		1.5		3.1	µs	High FH-range
Pulse width (HSWID = 1)	t_w	3.0		8.8	µs	Low FH-range
		1.5		4.0	µs	High FH-range
Rise time	t_r	100			ns	
Input HSYNC (CLEXT = 1)						
L-input voltage	V_{IL}	0		0.8	V	
H-input voltage	V_{IH}	2.0		V_{DD}	V	
Setup time	t_{SU}	4			ns	Referred to **falling** edge of CLKI
Hold time	t_H	12			ns	Referred to **falling** edge of CLKI
Input VSYNC						
Pulse width high		100		$100/f_H$	ns	FH1_2 = 1, NI = 0
Pulse width high		200		$100/f_H$	ns	FH1_2 = 0, NI = 0
Pulse width high		$1.5/f_H$		$100/f_H$		NI = 1

3.1 Recommended Operating Conditions (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
Input CLKI (External Clock Generation, CLEXT = High)						
Input frequency	f_I	12.5	13.5	15	MHz	Low FH-range
		25	27	30	MHz	High FH-range
Quartz Oscillator Input / Output X1, X2						
Crystal frequency			24.576		MHz	Fundamental crystal type, e.g. Saronix 9922 520 00282
Crystal resonant impedance				40	Ω	
External capacitance			27		pF	See Application information
I²C Bus (All Values are Referred to min.(V_{IH}) and max.(V_{IL})						
High-level input voltage	V_{IH}	3		V_{DD}	V	
Low-level input voltage	V_{IL}	0		1.5	V	
SCLK clock frequency	f_{SCLK}	0		400	kHz	
Rise times of SCLK, SDAT	t_R			0.3	µs	f_{SCLK} = 400 kHz
Fall times of SCLK, SDAT	t_F			0.3	µs	
Set-up time DATA	$t_{SU;DAT}$	100			ns	
Hold time DATA	$t_{HD;DAT}$	0			ns	
Load capacitance	C_L			400	pF	

3.2 Characteristics (Assuming Recommended Operating Conditions)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
Average supply current	I_{CC}		90	150	mA	
Stand-by supply current				25	mA	
Output Pins: SCAN, PWM						
Output low level	V_{OL}			0.4	V	I_O = 1 mA
Output high level	V_{OH}	2.8			V	I_O = -1 mA
Input / Output SDAT						
Output low level	V_{OL}			0.6	V	I_O = 6 mA
Output SCP						
Output low level	V_{OL}	0		1	V	I_O = 1 mA
Output HBL level	V_{OHBL}	V_{DD} / 2 -0.4 V	V_{DD} / 2	V_{DD} / 2 +0.4 V		| I_O | = 100 µA
Output high level	V_{OH}	4.0		V_{DD}	V	I_O = -1 mA
DAC Output D/A						
DAC resolution			6		Bit	
DAC output low			1		V	V_{REFP} = 4 V
DAC output high			3.953		V	V_{REFP} = 4 V
Load capacitance	C_L			30	pF	
Output load		20			kΩ	
Offset error		-3 %		3 %		V_{REFP} = 4 V
Gain error		-3 %		3 %		V_{REFP} = 4 V
INL		-1		1	LSB	
DNL		-0.5		0.5	LSB	
DAC Output E/W						
DAC resolution			10		Bit	Linear range: 100 ... 900
DAC output low			1.45		V	Input data = 100[1)]

3.2 Characteristics (Assuming Recommended Operating Conditions) (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
DAC output high			3.48		V	Input data = 900[1)]
Load capacitance	C_L			30	pF	
Output load		20			kΩ	
Zero error		-2 %		2 %		DAC output voltage = 2.5 V[2)]
Gain error		-5 %		5 %		[2)]
INL		-0.2 %		0.2 %		[2)]
DNL		-0.1 %		0.1 %		[2)]

[1)] V_{REFH} = 2.5 V, V_{REFL} = 1.2 V

[2)] V_{REFH} = 2.5 V, V_{REFL} = 1.2 V, Input range = 100 ... 900

DAC Output VD+, VD-						
DAC resolution			14		Bit	Linear range: 1500 ... 15000
DAC output low (VD-)			1.44		V	Input data = 1500[1)]
DAC output high (VD-)			3.58		V	Input data = 15000[1)]
DAC output low (VD-) - (VD+)			-2.12		V	Input data = 1500[1)]
DAC output high (VD-) - (VD+)			2.16		V	Input data = 15000[1)]
Load capacitance	C_L			30	pF	
Output load		20			kΩ	
Zero error		-1 %		1 %		(VD-) - (VD+) = 0 V[2)]
Gain error		-5 %		5 %		[2)]
INL		-0.5 %		0.5 %		[2)]
DNL		Monotonous				Guaranteed by design

[1)] V_{REFH} = 2.5 V, V_{REFL} = 1.2 V

[2)] V_{REFH} = 2.5 V, V_{REFL} = 1.2 V, Input range = 1500 ... 15000

3.2 Characteristics (Assuming Recommended Operating Conditions) (cont'd)

Parameter	Symbol	Limit Values			Unit	Remark
		min.	nom.	max.		
Reference Output V_{REFP} (Adjustable by Reg 48_H, Bit D7 ... D3) (Reg 48_H, Bit D2 = 0, Bit D1 = 0)						
Output voltage min				4.0	V	Bit D7 ... D3 = 10000
Output voltage max		4.0			V	Bit D7 ... D3 = 01111
Output current	I_Q	-50		0	µA	
Reference Output V_{REFH} (Reg 48_H, Bit D2 = 0)						
Output voltage	V_Q	2.4	2.5	2.6	V	V_{REFP} = 4 V
Reference Output V_{REFL} (Reg 48_H, Bit D2 = 0)						
Output voltage	V_Q	1.1	1.2	1.3	V	V_{REFP} = 4 V
Output HD						
Output low level	V_{OL}	0		1	V	I_O = 8 mA
Output high level	V_{OH}	V_{DD} -1 V		V_{DD}		I_O = -8 mA

4 Application Information

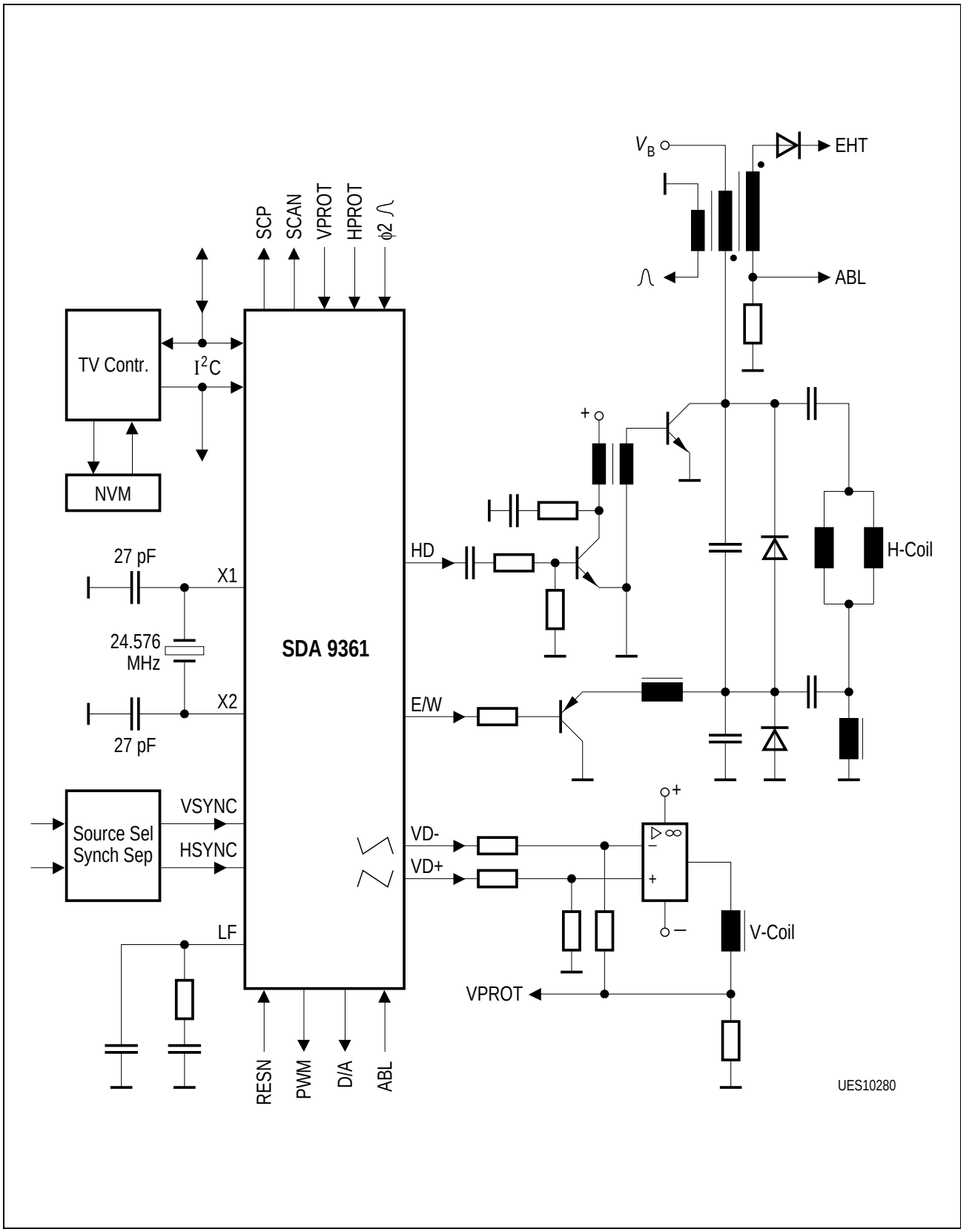
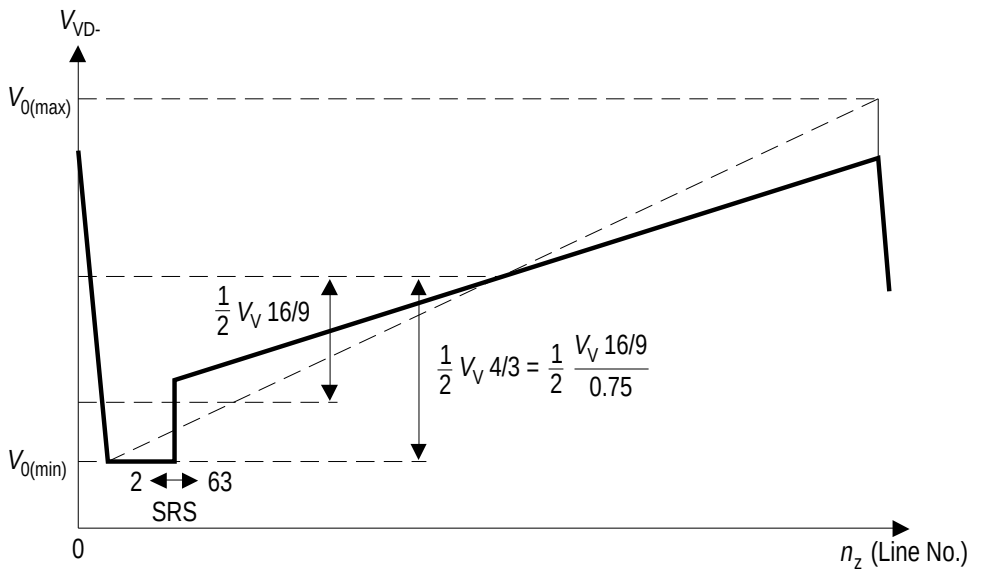


Figure 7

5 Waveforms

5.1 VD- Output Voltage, 4/3-CRT and 16/9-Source



SRSE = 1 Start Reduced Scan (SRS) selectable (line 0, 2...63)

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Figure 8

5.2 Timing Diagram of SCAN

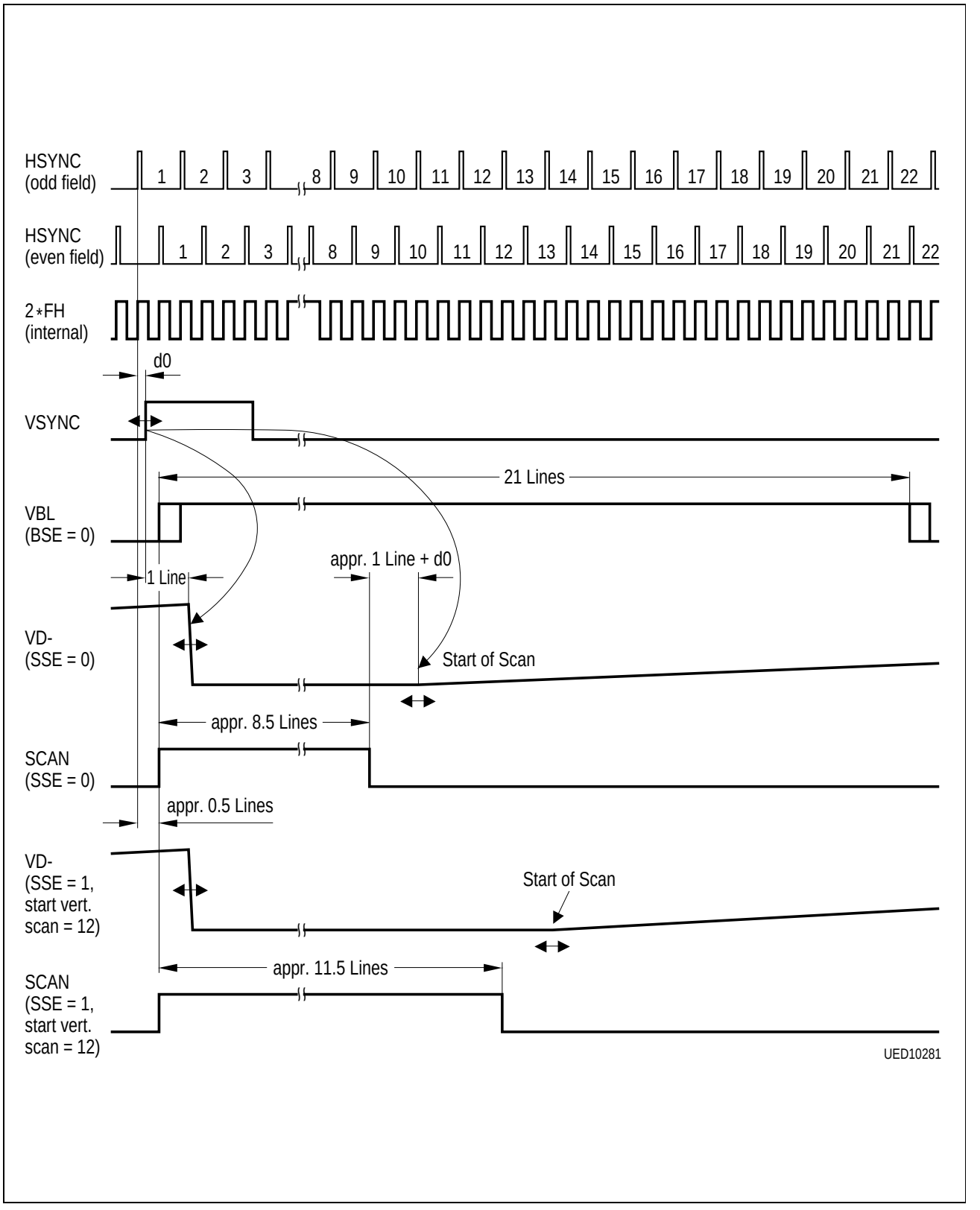


Figure 9
Timing Diagram of SCAN if STE = 0

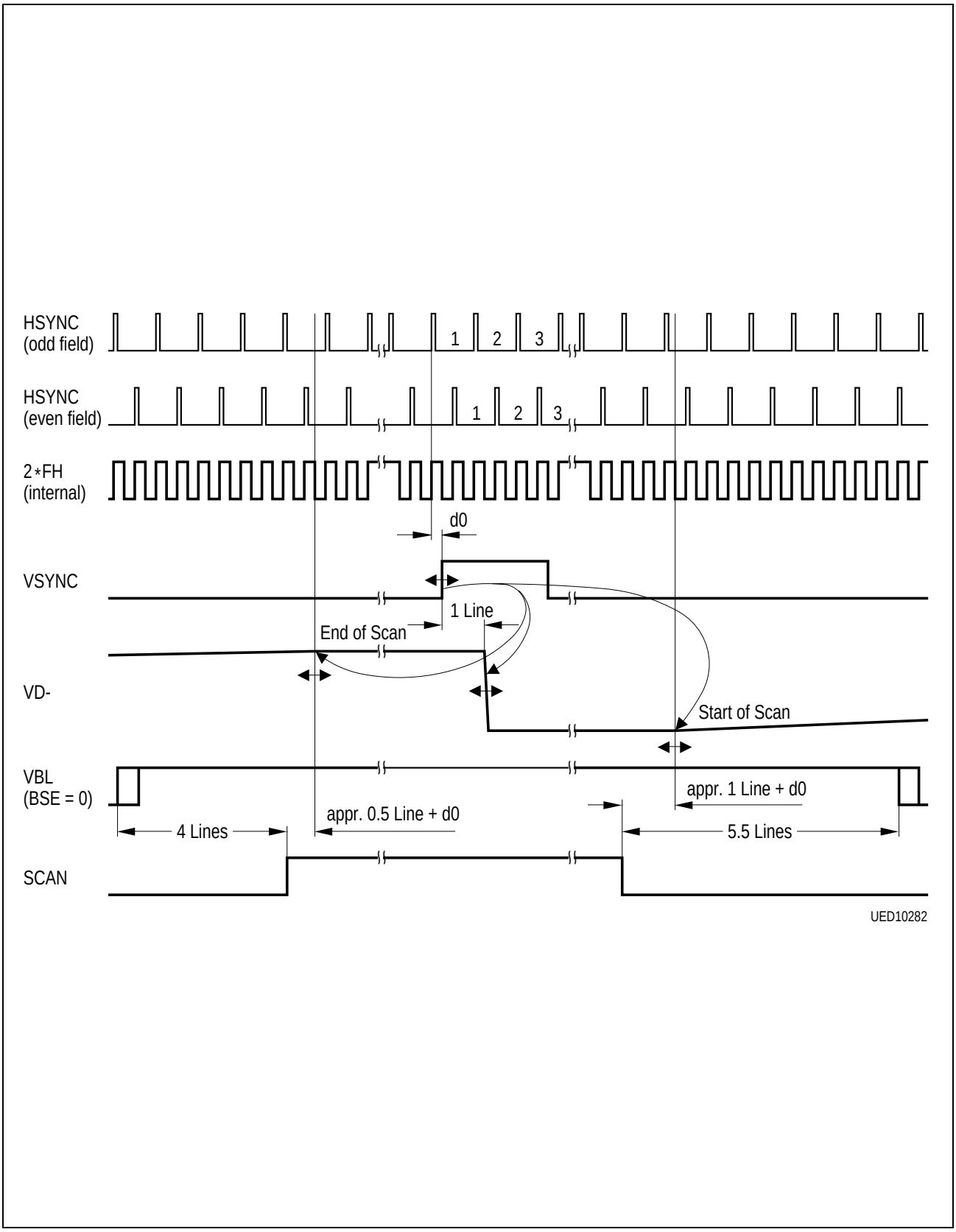
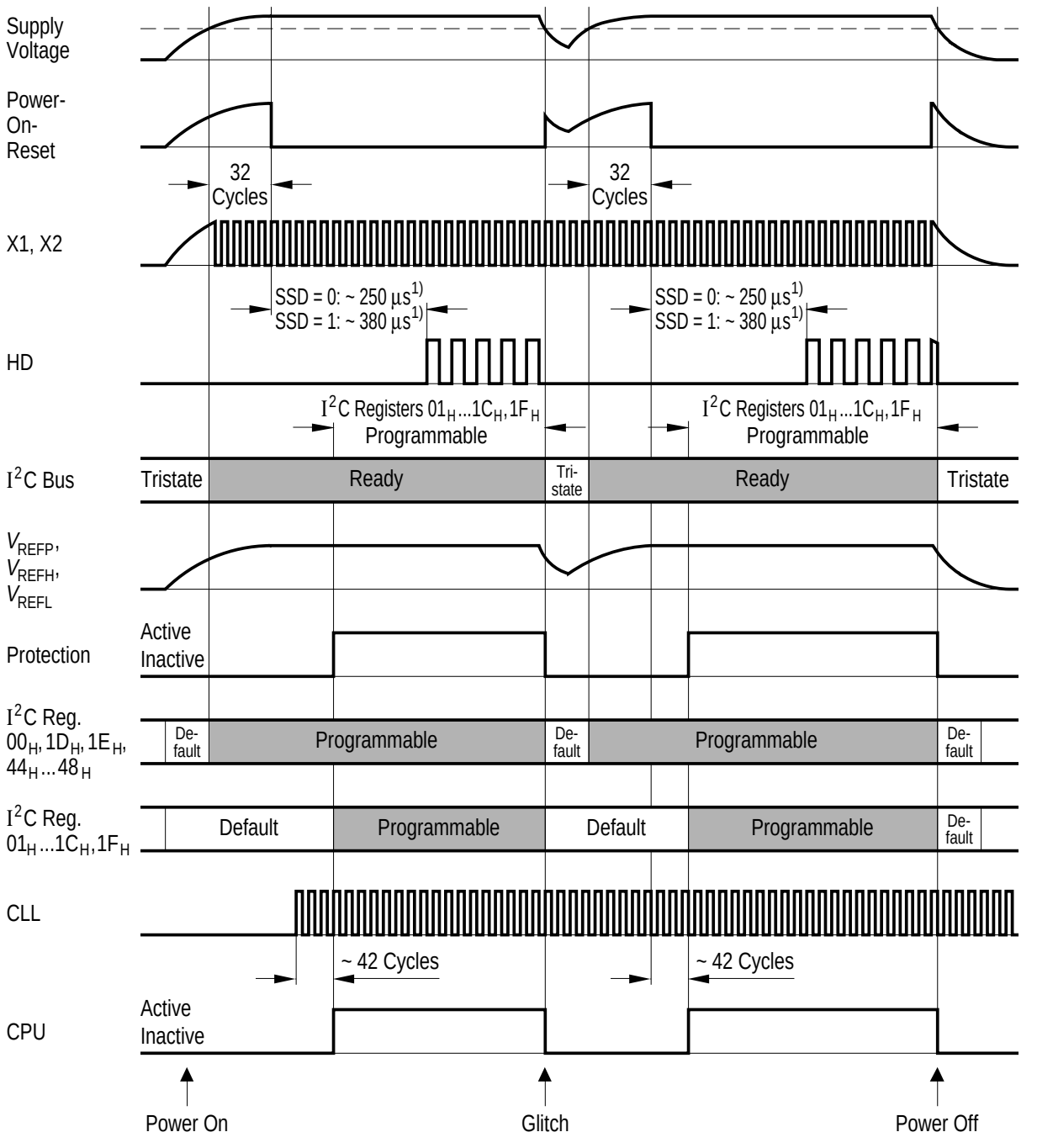


Figure 10
Timing Diagram of SCAN if STE = 1

5.3 Power On/Off Diagram



1) For low FH-range this time has to be multiplied by 2

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Figure 11

5.4 Standby Mode, RESN Diagram

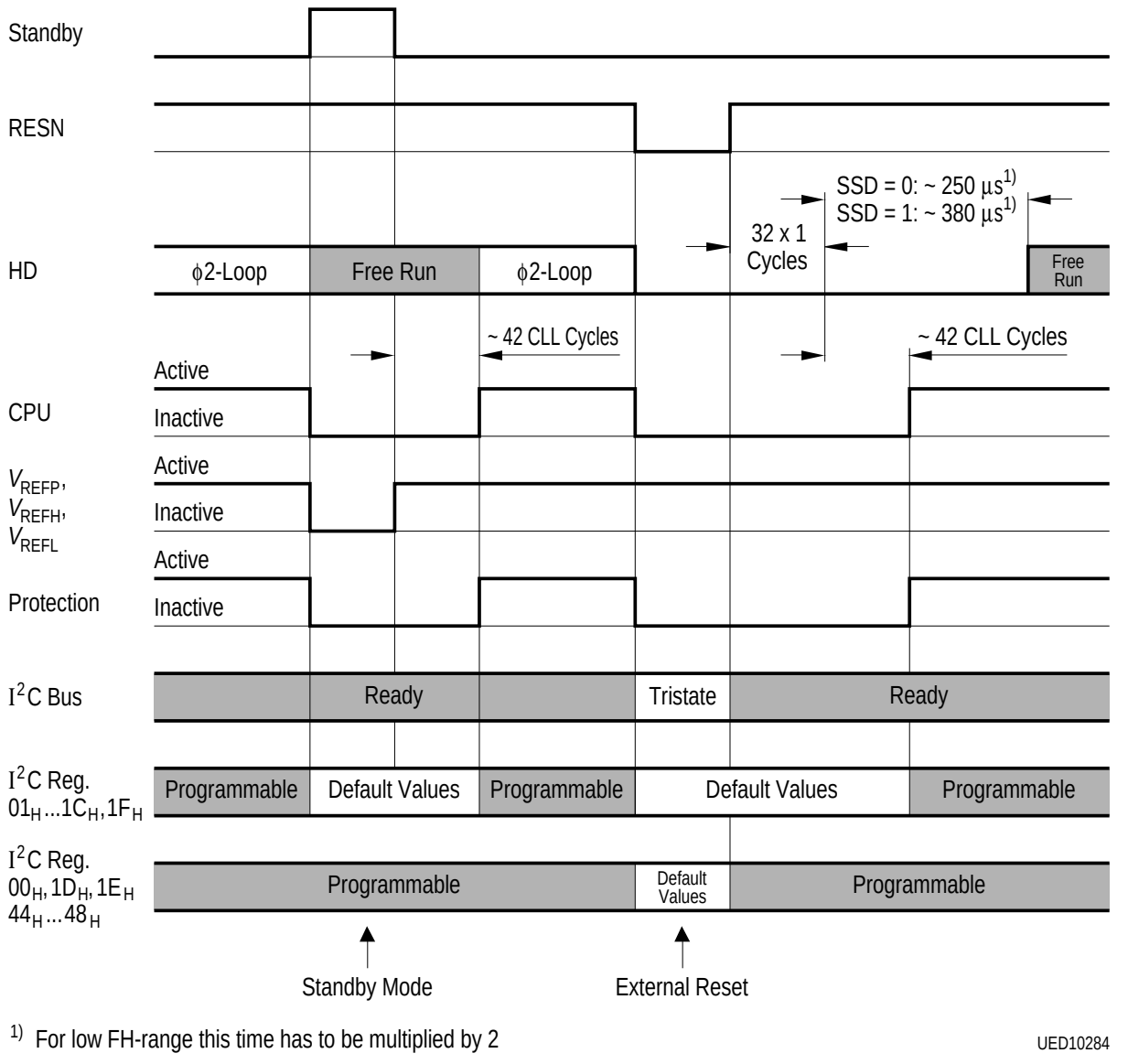
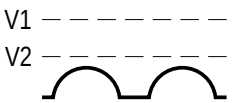
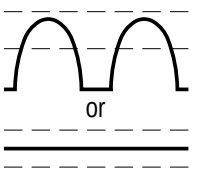
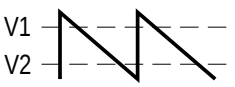
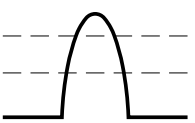
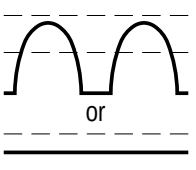
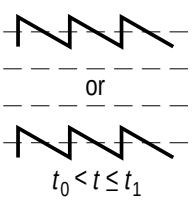
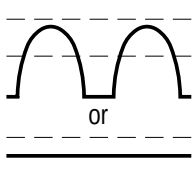
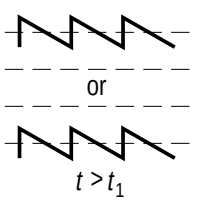
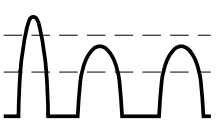
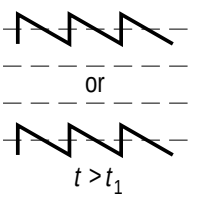


Figure 12

5.5 Function of H,V Protection

	HPROT	VPROT	Mode	SCP	HPON[2] I²C Bus	VPON[2] I²C Bus
1			Start up	Continuous blanking	0	0
2			H, V operation	1)	0	0
3			EHT over-voltage	Continuous blanking after t_2	1 after t_2	0
4			H operation V short failure	Continuous blanking after t_0 if SSC = 0	0	0
5			V longer failure H off after t_1	Continuous blanking after t_0 if SSC = 0	0	1 after t_1
6			EHT short over-voltage	Continuous blanking after t_2	1 after t_2	1 after t_1

$t_0 = 2 / f_v \ldots 3 / f_v$ $t_1 = 64 / f_v \ldots 128 / f_v$ $t_2 = 1 / f_v \ldots 2 / f_v$

1) Depends on I²C-control items

2) HPON or VPON = 1:HD = 0 (OFF)

6 Package Outlines

P-MQFP-44-2
(Plastic Metric Quad Flat Package)

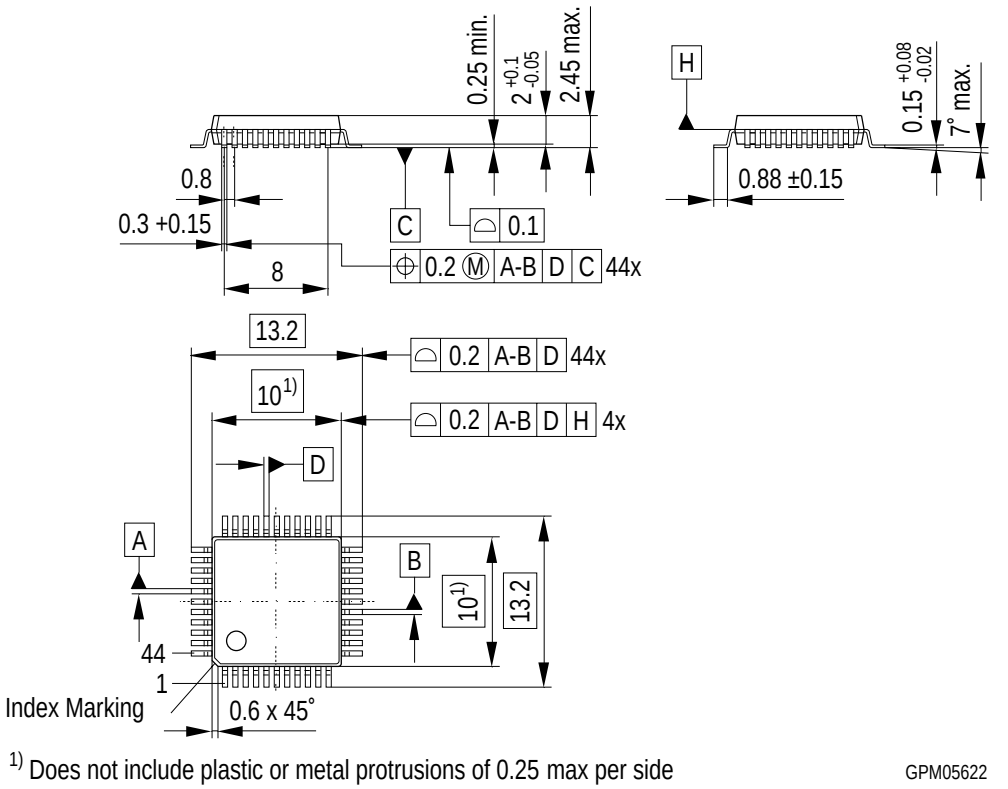


Figure 13

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm