SIEMENS

ICs for Communications

Memory Time Switch Large
MTSL

PEB 2047
PEB 2047-16

Version 2.1

Data Sheet 03.95

Edition 03.95

This edition was realized using the software system FrameMaker.

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PEB 2047 **PEB 2047-16** **Revision History:**		**Current Version: 03.95**
Previous Version:		Data Book 01.94
Page (in Version 01.94)	Page (in new Version)	Subjects (changes since last revision)
124	5	Version 2.1
127	8	Pin No. 6: INT open drain output
135	16	Figure 8: Improved
142	23	STAR: FSAD(2:1) position
143	25	MASK: Write address
148	31	Figure 12: 2 × Data Rate, Figure 13: 1 × Data Rate
153	36	Abs. Max. Ratings: V_S definition
154	37	t_{LA} min. = 15 ns, t_{AH} min. = 15 ns, t_{RWD} min. = 0 ns
157	40	Figure 23: t_{RWD}
158	41	t_S min. = 15 ns
159	42	Sequence of 1., 2. and 3. bit of frame

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **"Processing Guidelines"** and **"Quality Assurance"** for ICs, see our **"Product Overview"**.

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SIEMENS

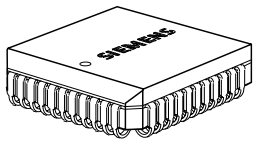
Memory Time Switch Large (MTSL)

PEB 2047
PEB 2047-16

Preliminary Data

CMOS IC

1 Features



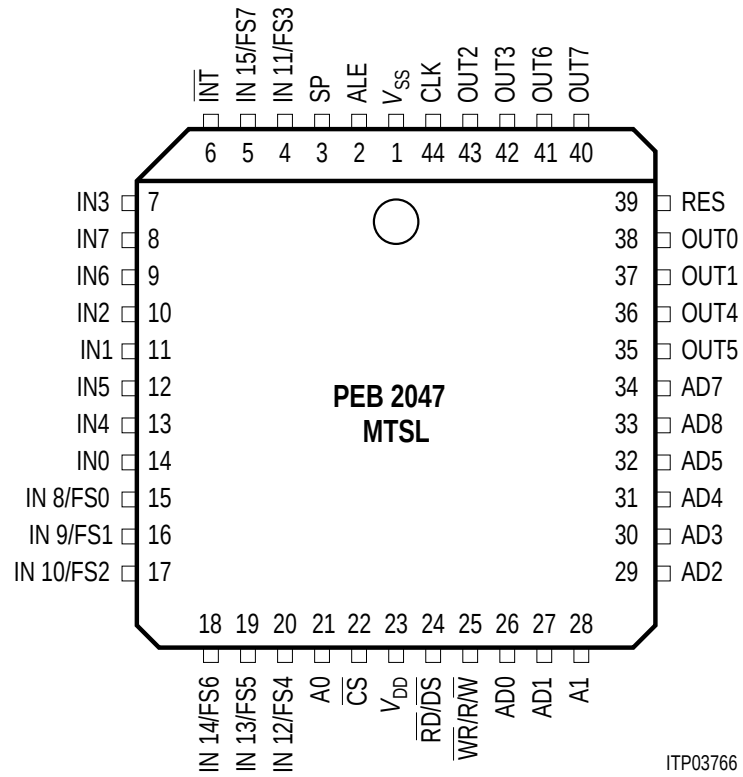
P-LCC-44

- Non-blocking time/space switch for 2048-, 4096-, 8192- or 16 384-kbit/s PCM systems
- Different modes programmable for input and output separately
- Configurable for a 4096-kHz, 8192-kHz or 16 384-kHz device clock
- Switching of up to 1024 incoming PCM channels to up to 1024 outgoing PCM channels
- 16 input and 8 output PCM lines
- Tristate function for further expansion and tandem operation
- µP read-access to PCM data
- Programmable clock shift with half clock step resolution for input and output
- Individual line delay measurement and clock shift mechanism for 8 PCM inputs
- Built-in selftest
- 8-bit Motorola or Intel type µP interface
- Constant or minimal channel-delay programmable on a per time-slot basis
- In-operation adjustment of bit-sampling without bit errors
- Low power consumption
- Single 5 V power supply

Important Note: All 16 384-MHz features described in this data sheet are only available with the PEB 2047-16!

Type	Ordering Code	Package
PEB 2047-N V2.1	Q67100-H6238	P-LCC-44 (SMD)
PEF 2047-N-16 V2.1	Q67100-H6301	P-LCC-44 (SMD)

Pin Configuration
(top view)



1.1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
1	V_{SS}	I	Ground (0 V)
3	SP	I	**Synchronization Pulse:** The MTSL is synchronized to the PCM system via this line.
14 11 10 7 13 12 9 8	IN0 IN1 IN2 IN3 IN4 IN5 IN6 IN7	I I I I I I I I	**PCM-Input Ports:** Serial data is received at standard TTL levels.
15 16 17 4 20 19 18 5	IN8/FS0 IN9/FS1 IN10/FS2 IN11/FS3 IN12/FS4 IN13/FS5 IN14/FS6 IN15/FS7	I I I I I I I I	**PCM-Input Ports or Frame** (Measuring Inputs): These inputs can additionally be used as frame evaluation inputs.
21 28	A0 A1	I I	**Address Bus Bit 0, 1:** These inputs interface to the systems address bus to select an internal register for a read or write access. These pins are only active if a demultiplexed µP interface mode is selected.
22	$\overline{CS}$	I	**Chip Select:** A low level selects the MTSL for a register access operation.
23	V_{DD}	I	**Supply Voltage:** 5 V ± 5 %.
39	RES	I	**Reset:** A high signal on this input forces the MTSL into reset state.
25 $\overline{WR}$	R/$\overline{W}$ 	I I	**Read/Write:** When “high”, identifies a valid µP access as a read operation. When “low”, identifies a valid µP access as a write operation (Motorola bus mode). **Write:** This signal indicates a write operation (Siemens/ Intel bus mode).
24 $\overline{RD}$	$\overline{DS}$ 	I I	**Data Strobe:** The rising edge marks the end of a valid read or write operation (Motorola bus mode). **Read:** This signal indicates a read operation (Siemens/ Intel bus mode).

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
26 27 29 30 31 32 33 34	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address Data Bus:** If the multiplexed address/data µP-interface bus mode is selected these pins transfer data and addresses between the µP and the MTSL. If a demultiplexed mode is used, these bits interface with the system data bus.
38 37 43 42 36 35 41 40	OUT0 OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7	O O O O O O O O	**PCM-Output Port:** Serial data is sent by these lines at standard CMOS- or TTL levels. These pins can be tristated.
44	CLK	I	**Clock:** 4096-kHz, 8192-kHz or 16 384-kHz device clock.
2	ALE	I	**Address Latch Enable:** In the Intel type multiplexed µP-interface mode a logical high on this line indicates an address of an MTSL internal register on the external address/data bus. In the Intel type demultiplexed µP-interface mode this line is hardwired to V_{SS}, in the demultiplexed Motorola type µP-interface mode it should be connected to V_{DD}.
6	$\overline{\text{INT}}$	(OD)	**Interrupt Line:** Active low open drain output.

1.2 Logic Symbol

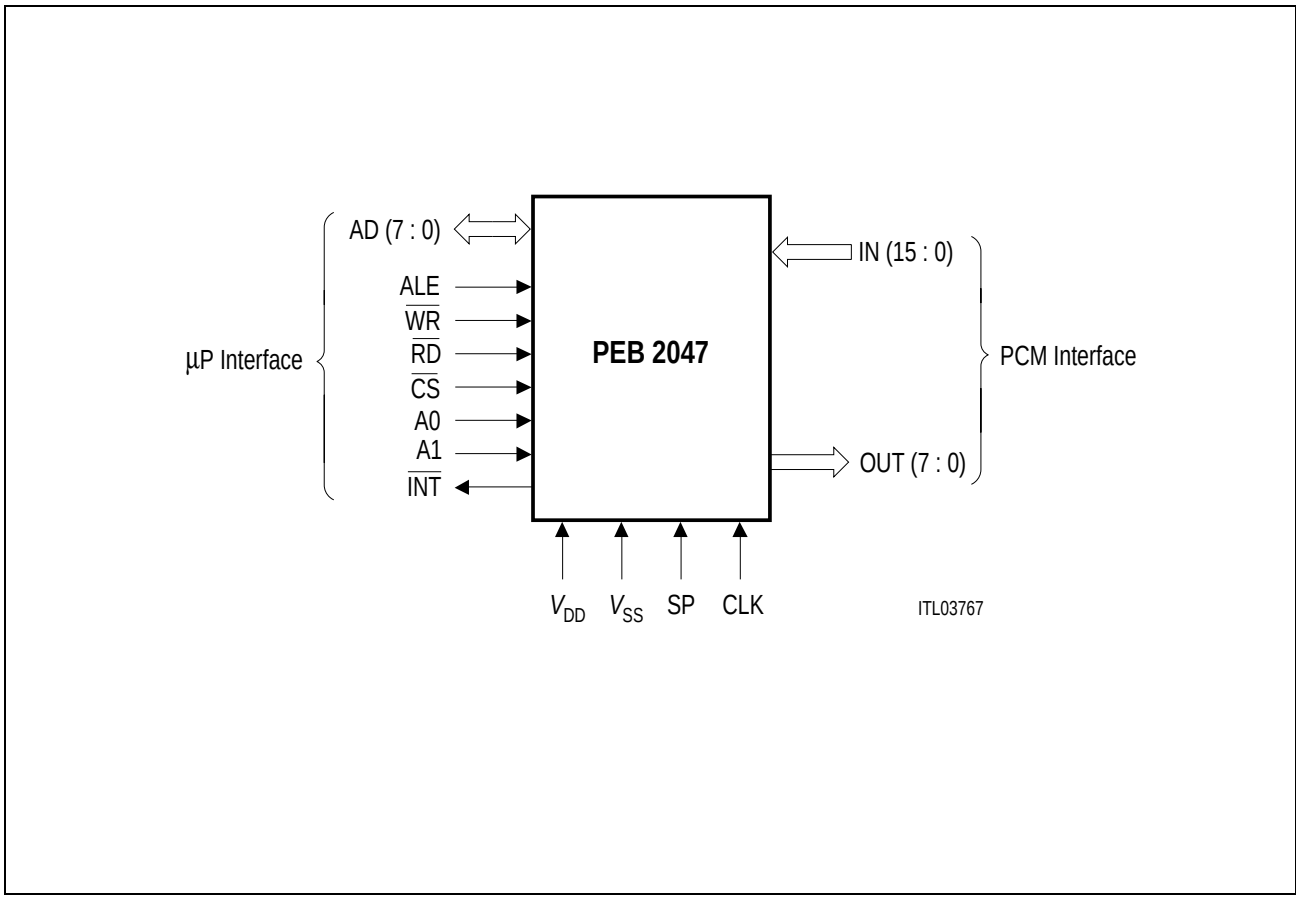


Figure 1
Functional Symbol

1.3 General Device Overview

The Siemens Memory Time Switch Large MTSL (PEB 2047) is an expansion of the MTSC (PEB 2045) regarding capacity and/or functionality. It is a monolithic CMOS switching device capable of connecting maximally 1024 PCM-input time-slots to 1024 output time-slots. A constant frame delay of one frame can be selected for wideband applications (e.g. ISDN H-Channels), whereas for example for voice channels a minimal frame delay is programmable. In order to manage the problem of different line delays, eight of the PCM inputs can be used as frame measurement inputs and eight different input offsets are allowed. Thus a frame wander can be compensated by adjusting the input offset during operation. A special circuitry guarantees that no bit error will occur, when reprogramming the input offsets.

The MTSL on-chip connection memory and data-memory are accessed via the 8-bit standard µP-interface (Motorola or Intel type).

A built-in selftest mechanism – also activated by the µP – ensures proper device operation in the system.

The PEB 2047 is fabricated using the advanced CMOS technology from Siemens and is mounted in a P-LCC-44 package. Inputs and outputs are TTL-compatible.

1.4 System Integration

The main application field for the MTSL (PEB 2047) are central switches with high switching capacity. Two possibilities exist to implement a non-blocking switch for 1024 input and 1024 output channels.

With a 16 384-kHz device clock only one MTSL is needed (**figure 2**), with a 8192-kHz device clock two chips in parallel realize the same functionality (**figure 3**).

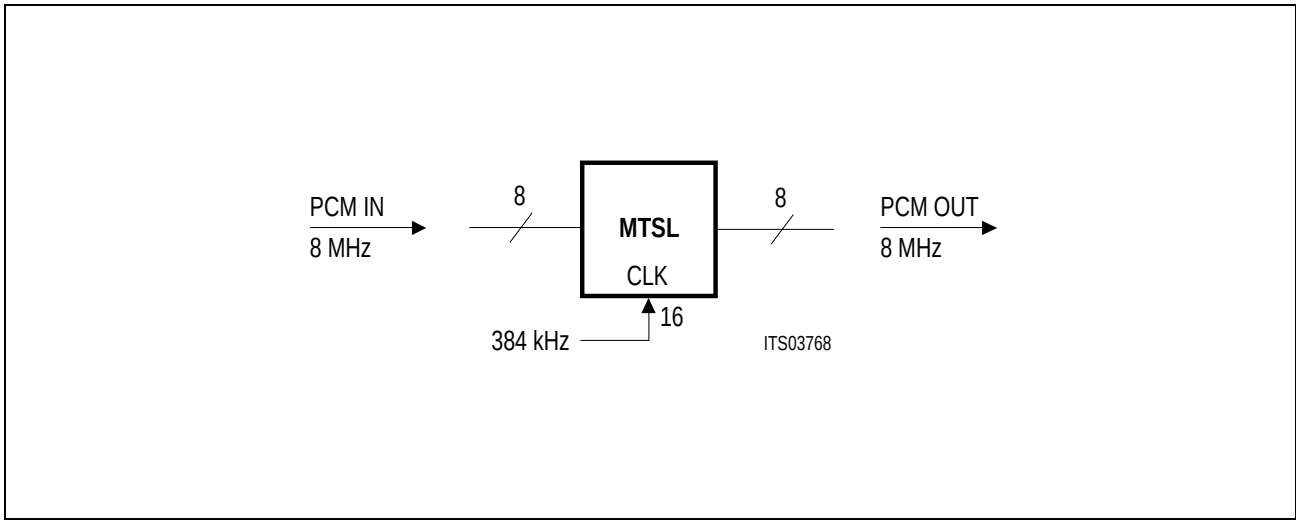


Figure 2
Memory Time Switch for a Non-Blocking 1024-Channel Switch (16 MHz)

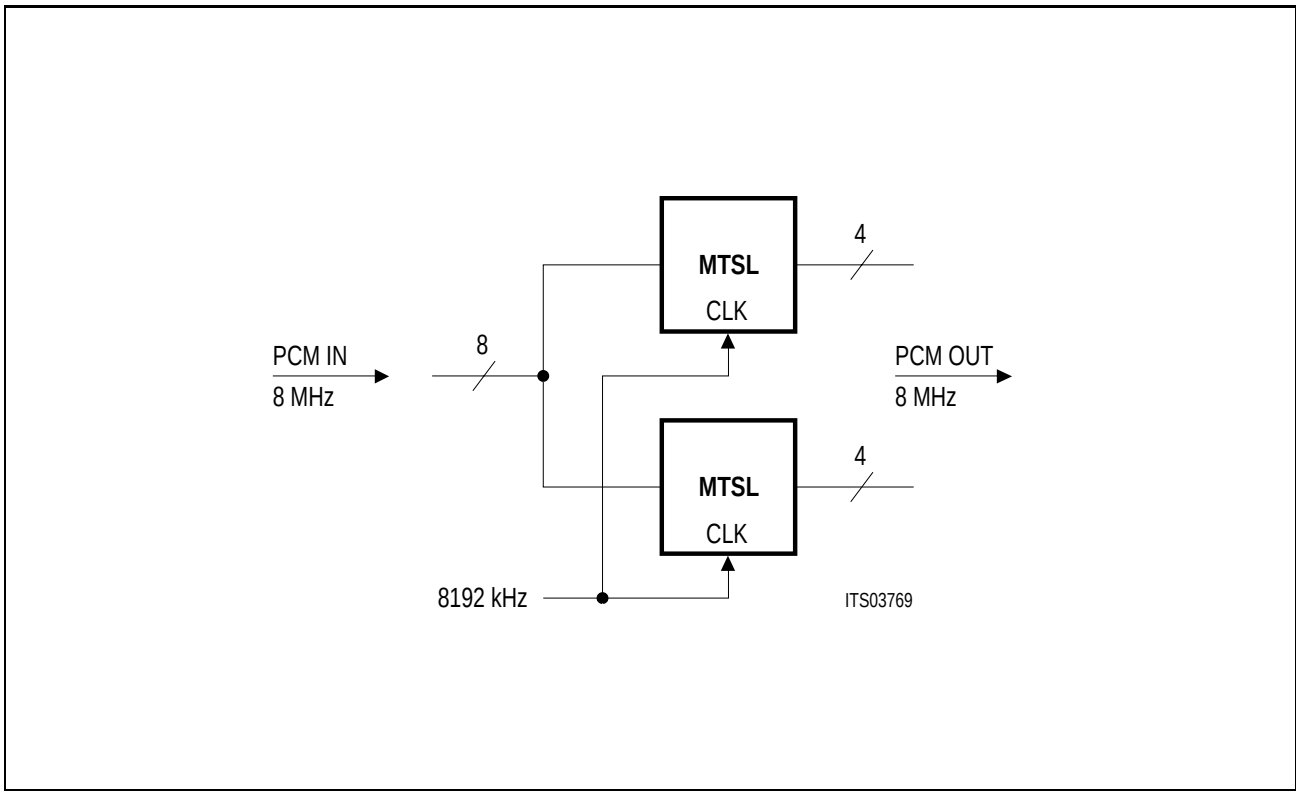


Figure 3
Memory Time Switch for a Non-Blocking 1024-Channel Switch (8 MHz)

Due to the tristate capability of the MTSL larger switches can be easily formed.

Figure 4 and **5** show how 4 devices operating with a 16 384-kHz clock or 8 devices operating with a 8192-kHz clock can be arranged to form non-blocking 2048-channel switches.

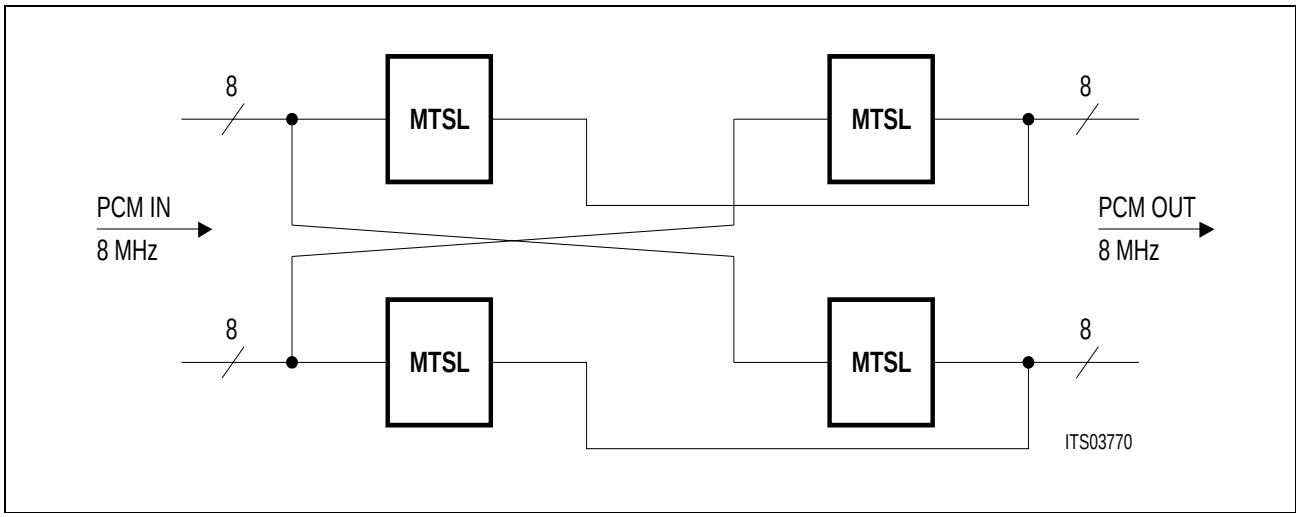


Figure 4
Memory Time Switch for a Non-Blocking 2048-Channel Switch with Four Devices (16-MHz device clock)

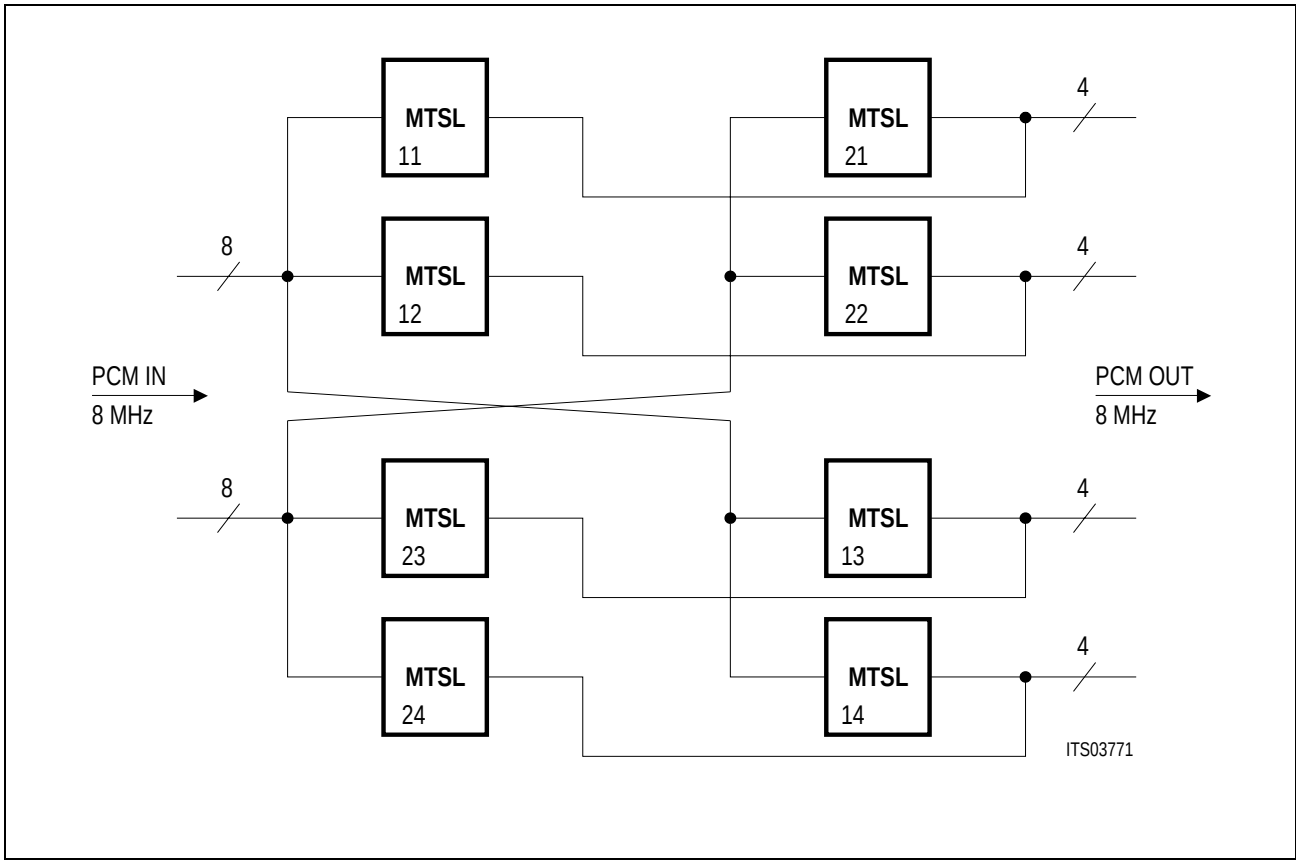


Figure 5
Memory Time Switch for a Non-Blocking 2048-Channel Switch with Eight Devices (8-MHz device clock)

2 Functional Description

The MTSL is a memory time switch device. Operating with a device clock of 8192 kHz it can connect any of 1024 PCM-input channels to any of 512 output channels. With a device clock of 16 384 kHz all 1024 PCM channels can be switched to the output. Additionally a 2048-kbit/s mode with a capacity of 512 × 256 time-slots and a clock frequency of 4096 kHz is possible for systems, which need the frame integrity feature.

A general block-diagram of the MTSL is shown in **figure 7**.

The input information of a complete frame is stored in one of the two on-chip 8-Kbit data memories DM0 and DM1. The incoming 1024 channels of 8 bits each are written in sequence into fixed positions of DM0 or DM1. This is controlled by the input counter in the timing control block with a 8-kHz repetition rate. If MTSL-A1 compatible operation (i.e. no frame integrity guaranteed) is wished, only one of the two data memories is used. Otherwise DM0 and DM1 are filled alternating with input frames.

For outputting, the connection memory (CM) is read in sequence. Each location in the CM points to a location in the data memory. The byte in this data memory location is transferred into the current output time-slot. The read access to the CM is controlled by an output counter. An additional bit (D12) in each location of the CM controls the access to the data memories DM0 and DM1. Three address pointers – two switching aligned to the input frame (DMI, IADP), one switching aligned to the output frame (DMO) – are working in conjunction with D12 implementing the constant/minimal delay function (**see figure 6**).

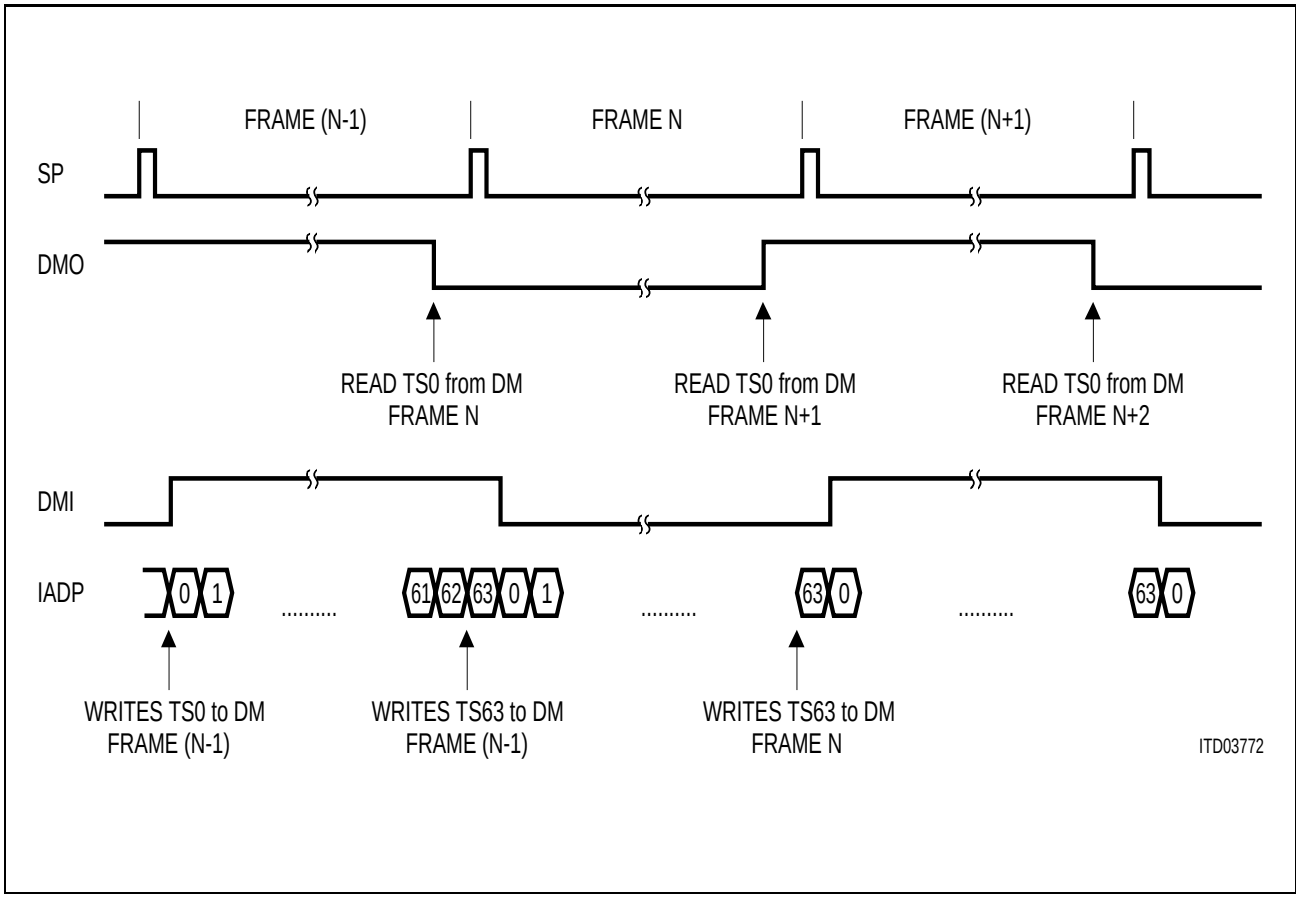


Figure 6

Constant delay (D12 = 0): read output time-slot from data memory (not DMO)

Minimal delay (D12 = 1): if number of input time-slot to be switched to current output ≤ IADP
then
read output time-slot from data memory DMI
else
read output time-slot from data memory (not DMI)

The synchronization of this procedure will be achieved by a rising edge of the synchron pulse SP, which is always sampled with the falling edge of the device clock.

Different modes of operation are configurable at the PCM-input interface (**see table 3**). Furthermore, 8 PCM-input lines can be aligned with individual clock shift values to compensate different line delays. If more than 8 inputs are used one clock shift value controls up to two ports at the same time.

The input lines IN8 to IN15 can be used as additional frame-measurement inputs (FS(0:7)). After synchronizing the device by the SP pulse the FS inputs can be evaluated on a per port basis. This evaluation procedure is started by a microprocessor command. As a result the input counter value on the rising edge of the FS signal can be read from an internal register. Thus delay compensation is easily managed by programming appropriate clock shift values and/or a possible software offset.

During operation of the chip a frame length check is also supplied, which controls correct synchronization by the SP pulse and generates an interrupt in case of lost or achieved synchronization.

The output buffer operation is controlled by mode selection and the chosen clock-rate (4096 kHz, 8192 kHz or 16 384 kHz) (**see table 2**). Shifting of the output frame is also possible, but all output-lines are affected the same way.

The unused output ports are tristated by mode selection, whereas unused time-slots are tristated by an additional bit in the control memory. By using this tristate capability the MTSL can be easily expanded to a time switch of any size (**see figure 2 to 5**).

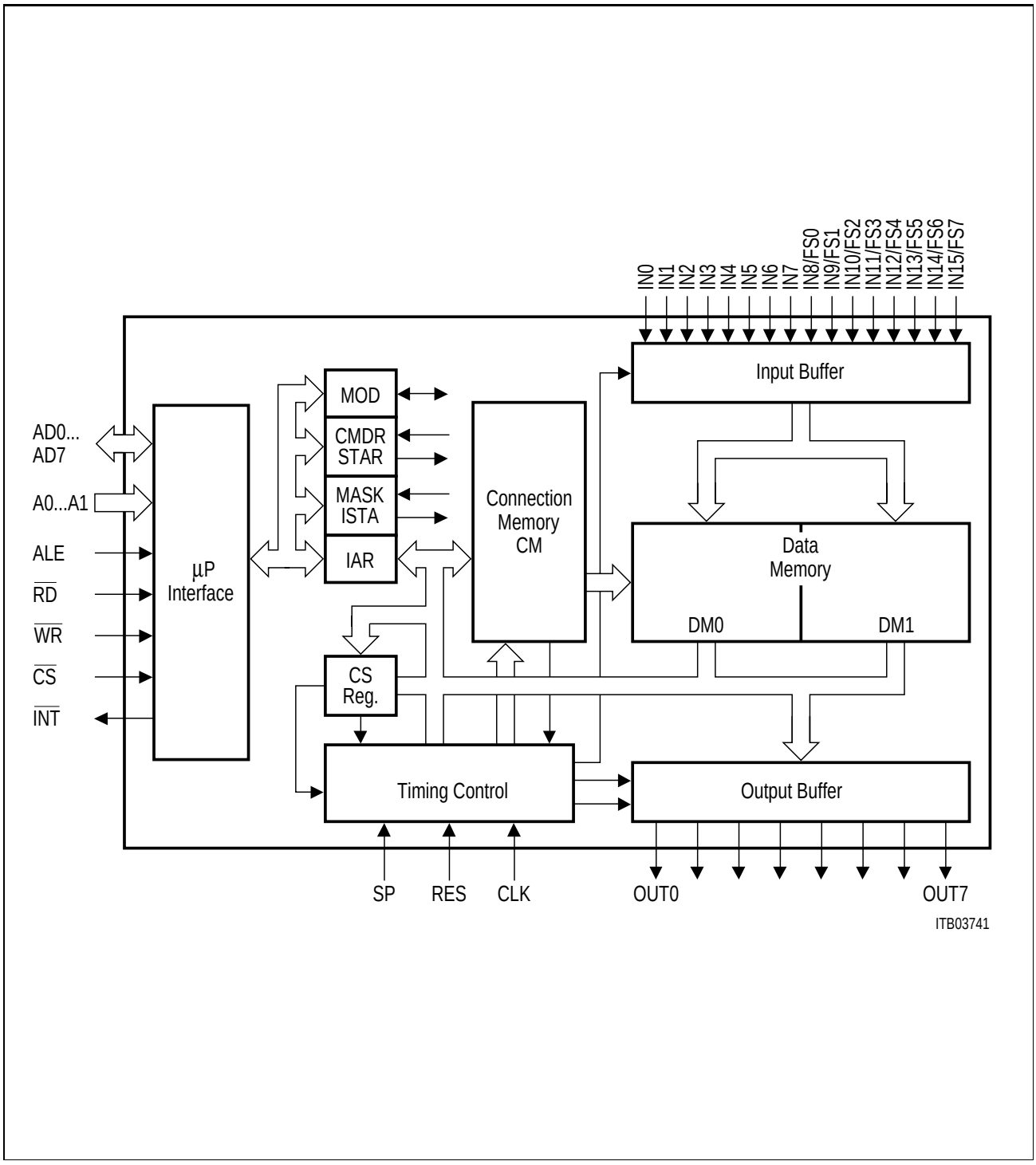


Figure 7
Block Diagram MTSL

The standard 8-bit µP interface can communicate with Intel multiplexed/demultiplexed microprocessors as well as with Motorola demultiplexed processors. It gives access to the internal registers and to the control- and data memory. Five directly addressable registers are provided. All other registers and the memories are accessed by a simple three byte indirect access method (similar to the MTSC PEB 2045).

2.1 MTSL Internal Timing and Channel Delay

Figure 7 shows the chip internal timing of writing and reading the data memory for all possible operation modes.

Control Memory Reset

Initialization of the device after a hardware reset (RES) is easily done with a µP-command “control memory reset”. After finishing this procedure all control memory channels contain the information “tristated”.

Evaluate Frame Measurement Signal

A command and an address (0 … 7) will be given by the µP. The rising edge of the corresponding frame measurement signal (FS0 … FS7) will be evaluated. The exact timing of the FS edge can then be read from an internal 12-bit register (resolution of a complete 8-kHz frame in half 16-MHz clock periods).

MTSL-Selftest

The switching path of the MTSL including input buffer, data memory, control memory, output buffer and timing control can be tested in the system by a built-in selftest. The two data memories DM0 and DM1 require two test procedures. Activating this mechanism takes (2×2.5) ms (4096 kHz), (2×1.25) ms (8192 kHz) or (2×0.625) ms (16 384 kHz). Finally the result “selftest ok/selftest not ok” can be read from the internal status register.

After test completion the control-memory is also reset.

2.2 Special Functions

The activity of all special functions can be read in the status register. Completion of these functions is indicated by interrupts.

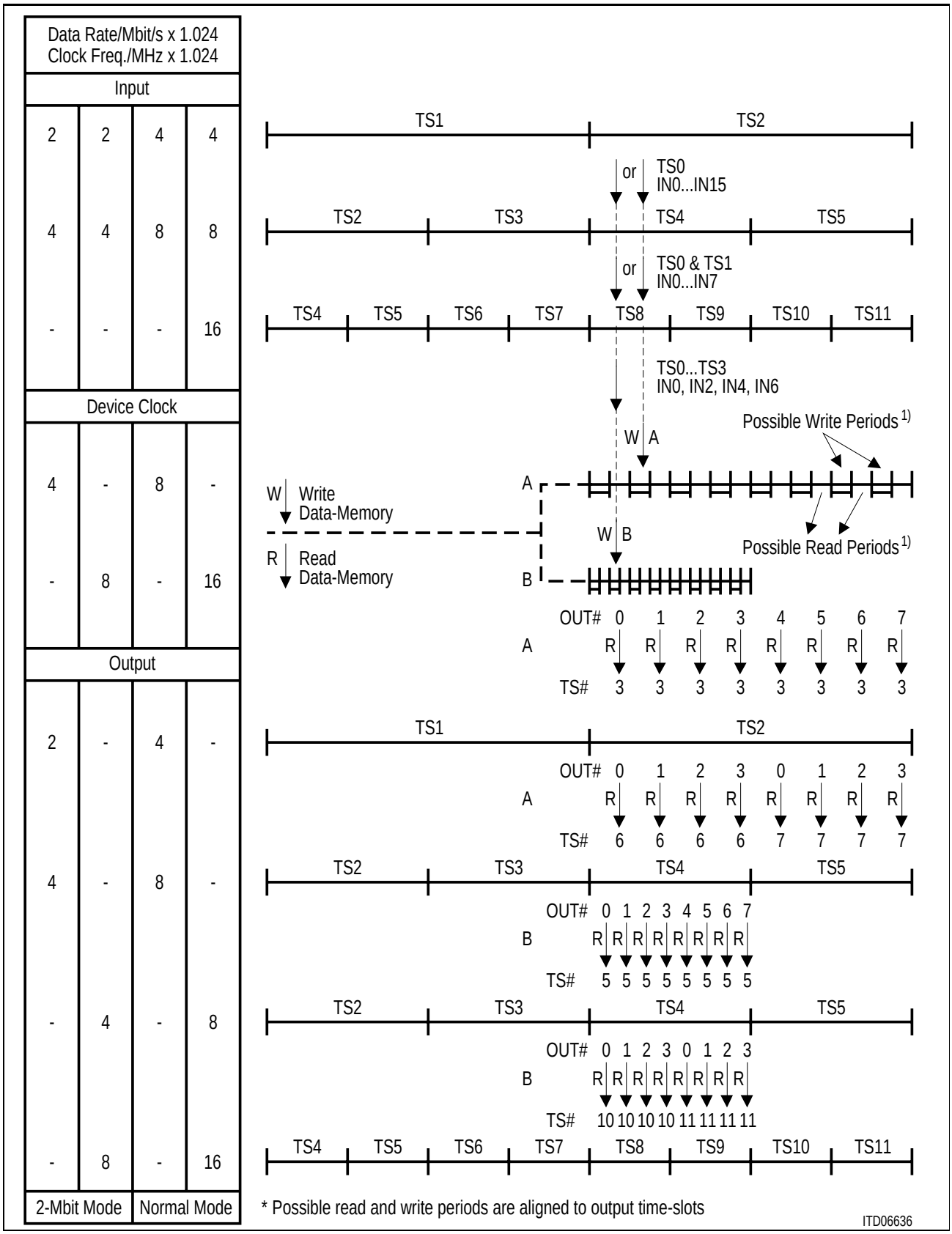


Figure 8
Data Memory Timing

For a system operating with 8192-kHz device clock and 8192-Mbit/s/8192 Mbit/s input/output data rate the following frame delay table can be deduced from the timing diagram:

Table 1

Input Time-Slot		Switched to Output Time-Slot		
Switched to OUT1, 2, 3	0 – 1	6 – 127	0 – 5	–
	2 – 3	8 – 127	0 – 7	–
	4 – 5	10 – 127	0 – 9	–
	.	.	.	.
	.	.	.	.
	.	.	.	.
	118 – 119	124 – 127	0 – 123	–
	120 – 121	126 – 127	0 – 125	–
	122 – 123	–	0 – 127	–
	124 – 125	–	2 – 127	0 – 1
	126 – 127	–	4 – 127	0 – 3
Switched to OUT0	0 – 1	7 – 127	0 – 6	–
	2 – 3	9 – 127	0 – 8	–
	4 – 5	11 – 127	0 – 10	–
	.	.	.	.
	.	.	.	.
	.	.	.	.
	118 – 119	125 – 127	0 – 124	–
	120 – 121	127	0 – 126	–
	122 – 123	–	1 – 127	0
	124 – 125	–	3 – 127	0 – 2
	126 – 127	–	5 – 127	0 – 4
Delay/number of frames	minimal delay	0	1	2
	constant delay	1	1	3

From this table it can be seen, that it is not possible to achieve the constant delay of one frame for all switching paths. Those input time-slots, which are written to the data memory later than they should have been read (for example in the above configuration TS124 – TS127 switched to TS0 or TS1, OUT1, 2, 3), will be delayed by three frames!

3 Operational Description

3.1 Initialization Procedure

For a proper initialization of the MTSL the following procedure is recommended:

First a reset pulse (RES) of at least two CLK clock-periods has to be applied. All registers contain now their reset values. In the next step the connection-memory CM is initialized by the commands CMDR:STP (1:0) = 01 (CM reset) or CMDR:STP (1:0) = 11 (MTSL selftest).

After having programmed a CM-reset command, it takes 4096-clock periods until all tristate-control entries in the CM contain the value “1” (tristated).

If a selftest-command was given, it takes 10 240-clock periods to achieve the same effect. Furthermore the register bit STAR:STOK (selftest o.k.) should still be set to “1” in this case, in order to prove that there is no fault on the chip. From version V2.1 up, the selftest command must be given for each data memory (DM0, DM1) separately. DM1 is tested, when register OPCR contains the reset value FF_H, DM0 is tested by programming OPCR to FB_H.

The activity of the procedures can be monitored in STAR:PACT and an interrupt will indicate their completion.

In all cases it is important, that the outputs are tristated by MOD:PSB = 0.

3.2 Operation Mode

The operation mode of the device is fixed by programming MOD:OMD (1:0) and MOD:IMD (2:0) and by the device clock used at pin CLK (**see table 2 and 3**).

3.3 Indirect Access Register

The connection-memory, data-memory and indirect registers are accessible through the indirect access register (IAR). An indirect access is performed by reading and/or writing three consecutive bytes to/from IAR. An incomplete three-byte access is indicated by STAR:Z = 1. After having read and/or written the third byte the operation selected by IAR:C (1:0), WR/RDQ is started and the bit STAR:B is set to 1. It takes at most 4.5 clock periods (8.5 clock periods for a “read data memory”) until the operation is performed and STAR:B is reset.

3.4 Frame Evaluation

Suppose the following timing at PCM input IN5 (mode 2):

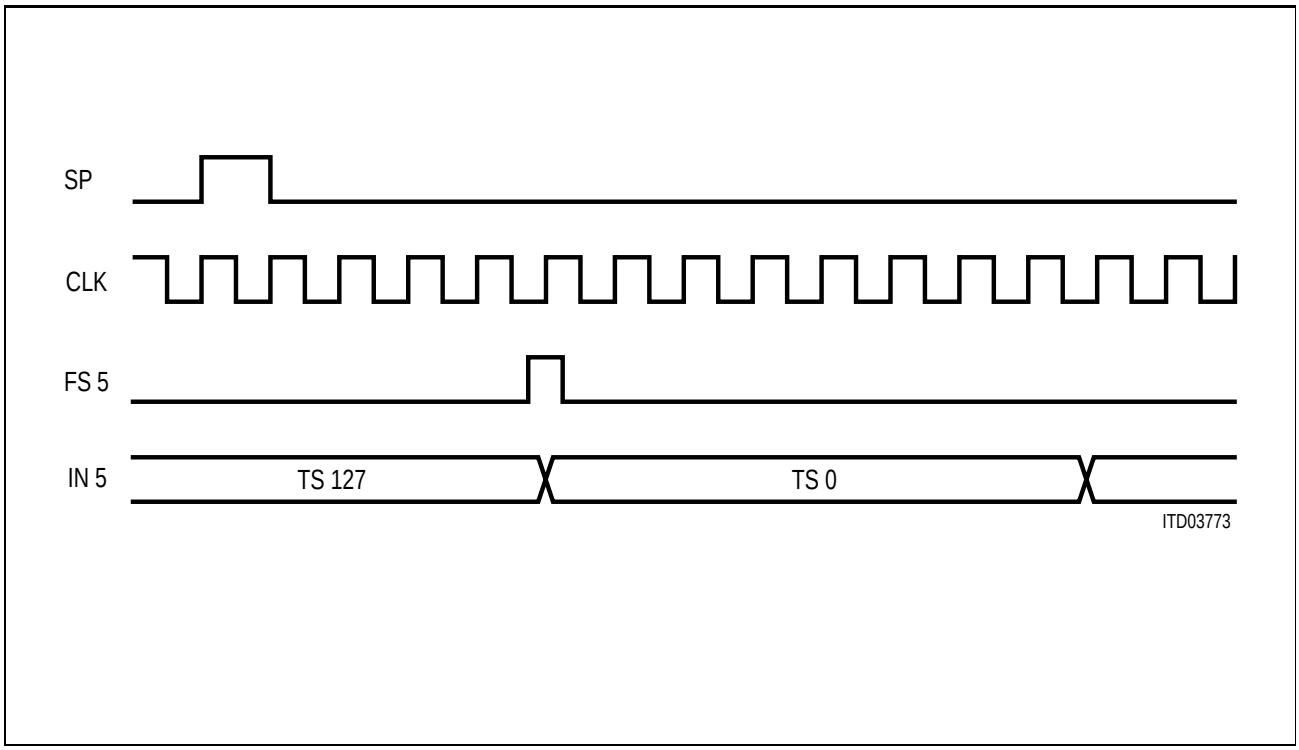


Figure 9

If the device is in synchronized state (STAR:PSS = 1) and the command “frame evaluation at FS5” (CMDR = 58_H) is programmed, the second following rising edge of FS5 is evaluated and creates the following result in register FER:

D (11) = 0
D (10:1) = $3E7_H$
D (0) = 0

D0 is fixed to 0 and doesn’t have a meaning in 8-MHz clock operation modes.

The actual offset of the incoming frame can now be calculated according to the formulas given in **table 9**.

3.5 Input Offset and Output Offset

Based on the results of the frame evaluation procedures the input offsets can be adjusted by programming ICSR (7:0) corresponding to inputs IN (7:0). If data oversampling is used, the values of ICSR (7:0) can be adjusted within some limits during operation without producing bit errors:

a) clockrate = 2 × datarate
possible adjustment is one half clockperiod forward or backward.

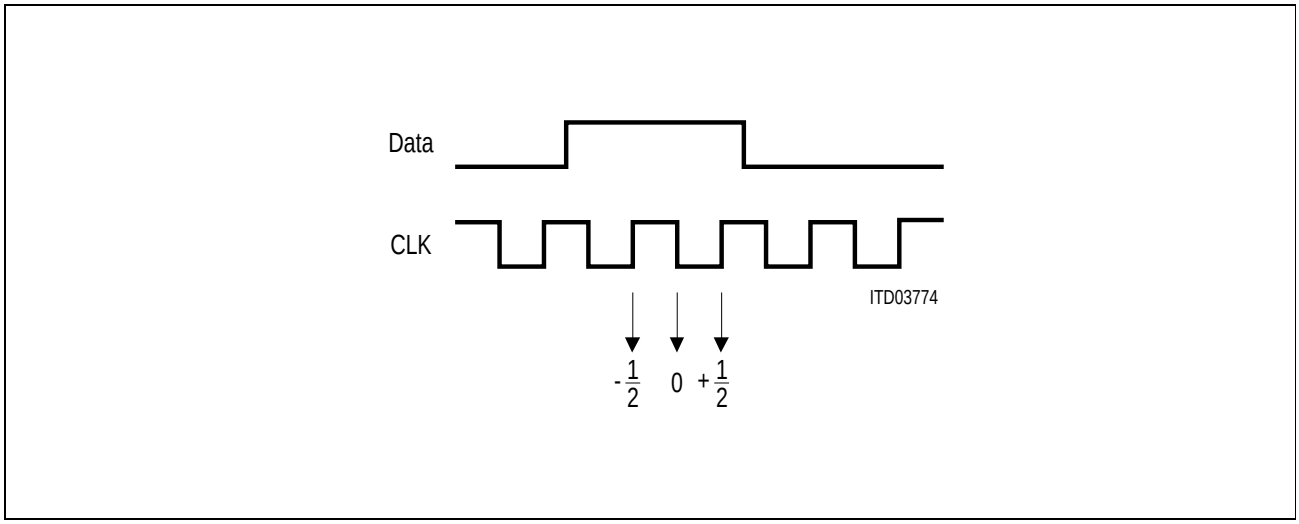


Figure 10

b) clockrate = 4 × datarate
possible adjustment is one clockperiod backward or two clockperiods forward.

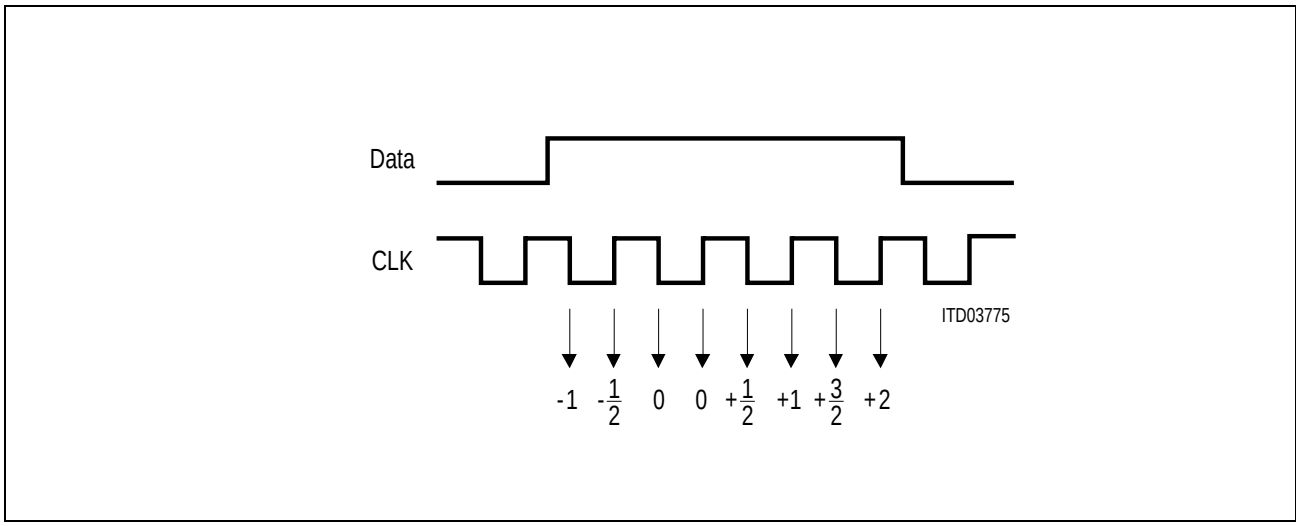


Figure 11

The output offset is the same for all output lines and is fixed in register OCSR.

4 Detailed Register Description

4.1 Mode Register (MOD)

Access in the multiplexed µP-interface mode: Read/write, address: 0_H
Access in a demultiplexed µP-interface mode: Read/write, address: 0_H
Reset value: 00_H

Bit 7							Bit 0
PSB	**MD2**	**0**	**OMD1**	**OMD0**	**IMD2**	**IMD1**	**IMD0**

PSB **PCM Stand By**; a logical 0 switches the PCM-interface outputs to high impedance.

MD2 If set to “1”, the PEB 2047 is able to switch channels with 2048-kHz data rate, when operating with 8.192 MHz (switching capacity 512 × 512 time-slots) or 4.096 MHz (switching capacity 512 × 256 time-slots).

OMD1 … OMD0 **Output Mode 1** and **0**; these bits define the PCM-output mode according to the following table.

Table 2
Output Modes

Device Clock [kHz]	Output Mode OMD (1:0)[1)]	Port Numbers	Number of Ports × Data Rate/kbit/s
4.096	0	OUT (7:0)	8 × 2048
	1	OUT7, OUT5, OUT3, OUT1, OUT2, OUT0	4 × 2048 / 2 × 4096
	3	OUT (3:0)	4 × 4096
8.192	0	OUT (7:0)	8 × 4096
	1	OUT7, OUT5, OUT3, OUT1, OUT2, OUT0	4 × 4096 / 2 × 8192
	3	OUT (3:0)	4 × 8192
16.384	0	OUT (7:0)	8 × 8192
	1	OUT7, OUT5, OUT3, OUT1, OUT2, OUT0	4 × 8192 / 2 × 16384
	3	OUT (3:0)	4 × 16384

1) Input and output mode combinations which use the same device clock frequency have to be selected.

IMD2 … IMD0: **Input Mode 2**, **1** and **0**; these bits define the PCM-input mode according to the following table.

Table 3
Input Modes

Device Clock [kHz]	MD2	Input Mode IMD (2:0)[1)]	Port Numbers	Number of Ports × Data Rate/kbit/s
4.096	1	0	IN (15:0)	16 × 2048
	1	1	IN (15:12), IN (7:4) / IN (3:0)	8 × 2048 / 4 × 4096
	1	2	IN (7:0)	8 × 4096
8.192	0	0	IN (15:0)	16 × 4096
	0	1	IN (15:12), IN (7:4) / IN (3:0)	8 × 4096 / 4 × 8192
	0	2	IN (7:0)	8 × 8192
	1	4	IN (15:0)	16 × 2048
	1	5	IN (15:12), IN (7:4) / IN (3:0)	8 × 2048 / 4 × 4096
	1	6	IN (7:0)	8 × 4096
16.384	0	4	IN (15:0)	16 × 4096
	0	5	IN (15:12), IN (7:4) / IN (3:0)	8 × 4096 / 4 × 8192
	0	6	IN (7:0)	8 × 8192
	0	3	IN6, IN4 / IN (3:0)	2 × 16384 / 4 × 8192
	0	7	IN6, IN4, IN2, IN0	4 × 16984

1) Input and output mode cominations which use the same device clock frequency have to be selected.

4.2 Command Register (CMDR)

Access in the multiplexed µP-interface mode: Write, address 2_H
Access in a demultiplexed µP-interface mode: Write, address 1_H
Address: 01_H

Bit 7 Bit 0

0	FSAD2	FSAD1	FSAD0	SFE	RI	STP1	STP0

FSAD (2:0) **Frame Synchronization** signal **Address** 2 to 0; Address of the chosen FS signal 0 to 7 to be evaluated by the procedure started by SFE.

SFE **Start Frame Evaluation**; a one in this bit position starts the frame evaluation procedure. A read operation on register FER will stop an unfinished frame evaluation procedure.

RI **Reset Incomplete** instruction; if a three byte indirect register access is not completed the internal logic must be initialized again before a new three byte access is possible.

STP0 … STP1 **Start Procedure 1** and **0**.
The following procedures can be activated by these bits:

Table 4
STP Commands

STP1	STP0	Function
X	0	No operation
0	1	Start control memory reset procedure
1	1	Start selftest procedure

Note: Before activating one of these procedures MOD:PSB has to be set to 0. During selftest or CM reset the device will ignore the external synchronization pulse and the user has no access to the internal data memory.

4.3 Status Register (STAR)

Access in the multiplexed µP-interface mode: Read, address: 2_H
Access in a demultiplexed µP-interface mode: Read, address: 1_H
Reset value: 01_H

Bit 7							Bit 0
Z	**FSAD2**	**FSAD1**	**FSAD0**	**B**	**PACT**	**PSS**	**STOK**

Z Incomplete instruction; a three byte indirect instruction is not completed (Z = 1).

FSAD (2:0) **Frame Synchronization** signal **Address** 2 to 0: see CMDR.

B **Busy**; an indirect access is active (memories or indirect registers); the three byte indirect access register is not accessible.

PACT **Procedure Active**; one of the procedures started by the µP (selftest, CM reset or frame evaluation) is active.

PSS **PCM Synchronization Status**; the PCM interface is synchronized (logical 1) or not synchronized (logical 0).

STOK **Selftest O.K**.; after a selftest procedure this bit is set to 1, if no faults are detected.

Note: This bit is only valid, if no power failure or inappropriate clocking occurred during the test (see ISTA:IR); this bit is set to 1 by a start selftest command or by hardware reset.

4.4 Interrupt Status Register (ISTA)

Access in the multiplexed µP-interface mode: Read, address: 4_H
Access in a demultiplexed µP-interface mode: Read, address: 2_H
Reset value: 00_H

Bit 7							Bit 0
0	**0**	**0**	**0**	**FEC**	**PC**	**IR**	**PFI**

FEC **Frame Evaluation Completed**; the indirect register FER contains a valid offset and can be read; this bit is reset by reading ISTA.

PC **Procedure Completed**; the procedure started from the command register (CM reset or MTSL selftest) is finished; this bit is reset by reading ISTA.

IR **Initialization Request**. The connection memory has to be programmed due to a loss of data (IR = 1). The IR bit is set after power failure or inappropriate clocking. This bit is reset by reading ISTA. It can only be retriggered again after a selftest or CM-reset procedure.

PFI **PCM-Framing Interrupt**; this bit being logical 1 indicates the loss or gain of synchronization. Synchronization is considered lost by the MTSL if the SP signal is not repeated within the correct period. Synchronization is considered achieved, if two consecutive SP pulses with the correct period have been received. PFI is reset by reading ISTA.

4.5 Mask Register (MASK)

Access in the multiplexed µP-interface mode: Write, address: 4_H
Access in a demultiplexed µP-interface mode: Write, address: 2_H
Reset value: 00_H

Bit 7							Bit 0
0	**0**	**0**	**0**	**FEC**	**PC**	**IR**	**PFI**

A logical 1 disables the corresponding interrupt as described in ISTA. A masked interrupt is stored internally and reported in ISTA immediately, if the mask is released.

4.6 Indirect Access Register (IAR)

Access in the multiplexed µP-interface mode: Read/write, address: 6_H
Access in a demultiplexed µP-interface mode: Read/write, address: 3_H
Reset value: Only the control bits C (1:0) and WR/RDQ are initialized to 0.

An indirect access is performed by reading/writing three consecutive bytes (first byte = extended control byte, second byte = data byte, third byte = address byte) to/from IAR.

Bit 7 Bit 0

C1	**C0 / D12**	**WR/ RDQ**	**IA9**	**IA8 / D11**	**D10**	**D9**	**D8**

control byte

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

data byte

IA7	**IA6**	**IA5**	**IA4**	**IA3**	**IA2**	**IA1**	**IA0**

address byte

C (1:0) **Code** values to determine the type of access.

WR/RDQ If set to 1 a write access is performed; otherwise a read access is activated.

Table 5
Indirect Access Codes

C1	C0	WR/RDQ	Function	Max. Access Time Clock Periods
0	0	0	No operation	–
0	0	1	Write control memory D12 = 0	4.5
0	1	1	Write control memory D12 = 1	4.5
0	1	0	Read control memory	4.5
1	0	0	Read data memory	8.5
1	1	0	Read indirect register	4.5
1	1	1	Write indirect register	4.5

D12 This bit is only used as a data bit in a read or write control memory operation. Dependent on the contents of register OPCR D12 is interpreted as absolute address for data memories DM0 and DM1 (OPCR = FF_H) or as a switch for constant (D12 = 0) and minimal (D12 = 1) delay (OPCR = FC_H).

D11 This bit is only used as data bit in a read operation of the FER register.

D (10:0) Data value for read/write access; if the control-memory is accessed D10 is used as a tristate control bit (0 = active, 1 = high impedance).

The incoming PCM data are transformed onto the data-memory (control memory data D12, D (10:0)) in the following way:

TSN **Time-Slot Number**

PN **Port Number**

TSC **Tristate Control Value** (0 = active, 1 = high impedance)

MD **Minimal Delay** (1 = minimal, 0 = constant frame delay), if OPCR:OC (1:0) = 00_B. Absolute address of data memories DM0, DM1 if OPCR:OC (1:0) = 11_B.

Table 6
Input Time-Slot Mapping

Input Mode	D (10:0)	Valid for Inputs
0,4	D12 D10 D9 D8 D7 D6 D5 D4 $\overline{D3}$[1] D2 D1 D0 MD TSC TSN PN	IN (15:0)
1,5	D12 D10 D9 D4 $\overline{D3}$[1] 1 D1 D0 MD TSC TSN PN D12 D10 D9 D3 0 D1 D0 MD TSC TSN PN	IN (15:12), IN (7:4) IN (3:0)
2,6	D12 D10 D9 D3 D2 D1 D0 MD TSC TSN PN	IN (7:0)
7	D12 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 $\overline{D0}$* MD TSC TSN (7:2) TSN0 PN ÷ 2 TSN1	IN6, IN4, IN2, IN0
3	D12 D10 D9 D3 0 D1 D0 MD TSC TSN PN D12 D10 D9 D4 D3 1 D1 $\overline{D0}$* MD TSC TSN (7:2) TSN0 PN ÷ 2 TSN1	IN (3:0) IN6, IN4

1) D3 and D0 contain the inverted values in these cases.

Note: D9 must be set to “0”, if MOD = MD2 is set, i.e. in 2-Mbit applications.

PN ÷ 2 means, you have to multiply D (2:1) by two to generate the correct input numbers.

IA9 … IA0 **Indirect Address** for a read/write access

If a indirect register is accessed only IA (3:0) are interpreted as address bits.

The control memory address is transformed to the output time-slots:

Table 7
Output Time-Slot Mapping

Output Mode		Valid for Outputs
0	IA9 IA8 IA3 | IA2 IA1 IA0 TSN | PN	OUT (7:0)
1	IA9 IA8 IA3 | IA2 IA1 1 TSN | PN	OUT7, OUT5, OUT3, OUT1
	IA9 IA8 IA2 | IA1 0 TSN | PN	OUT2, OUT0
3	IA9 IA8 IA2 | IA1 IA0 TSN | PN	OUT (3:0)

Note: IA9 is only valid within applications with a 16.384-MHz device clock. If a 8.192 or 4.096-MHz clock is used, it is internally fixed to 0.

IA8 must be set to “0”, if MOD:MD2 is set, i.e. in 2-Mbit applications.

4.7 Indirect Registers

Input Clock Shift Registers ICSR (7:0)

Read/write at indirect address IA (3:0) = 0_H … 7_H

Reset value: 40_H

Bit 7							Bit 0
ADSR	**1**	**ICS4**	**ICS3**	**ICS2**	**ICS1**	**ICS0**	**RRE**

ADSR **Add Shift Register**; a three bit shift register is inserted into the corresponding input(s).

ICS4 … ICS0 **Input Clock Shift**; the value of ICS (4:0) determines the number of clock cycles by which the bit sampling point is shifted forward in all input modes.

Note: ICS4 has to be set to “0” in input modes 0, 1 and 2.

RRE **Receive** on **Rising Edge**

These eight registers determine the individual clock shift of inputs IN0 to IN7.

If more than eight inputs are used, two inputs are controlled by one ICSR register:

ICSR0	controls	IN0, IN8
ICSR1	”	IN1, IN9
ICSR2	”	IN2, IN10
.		.
.		.
.		.
ICSR7	”	IN7, IN15

Input Timing

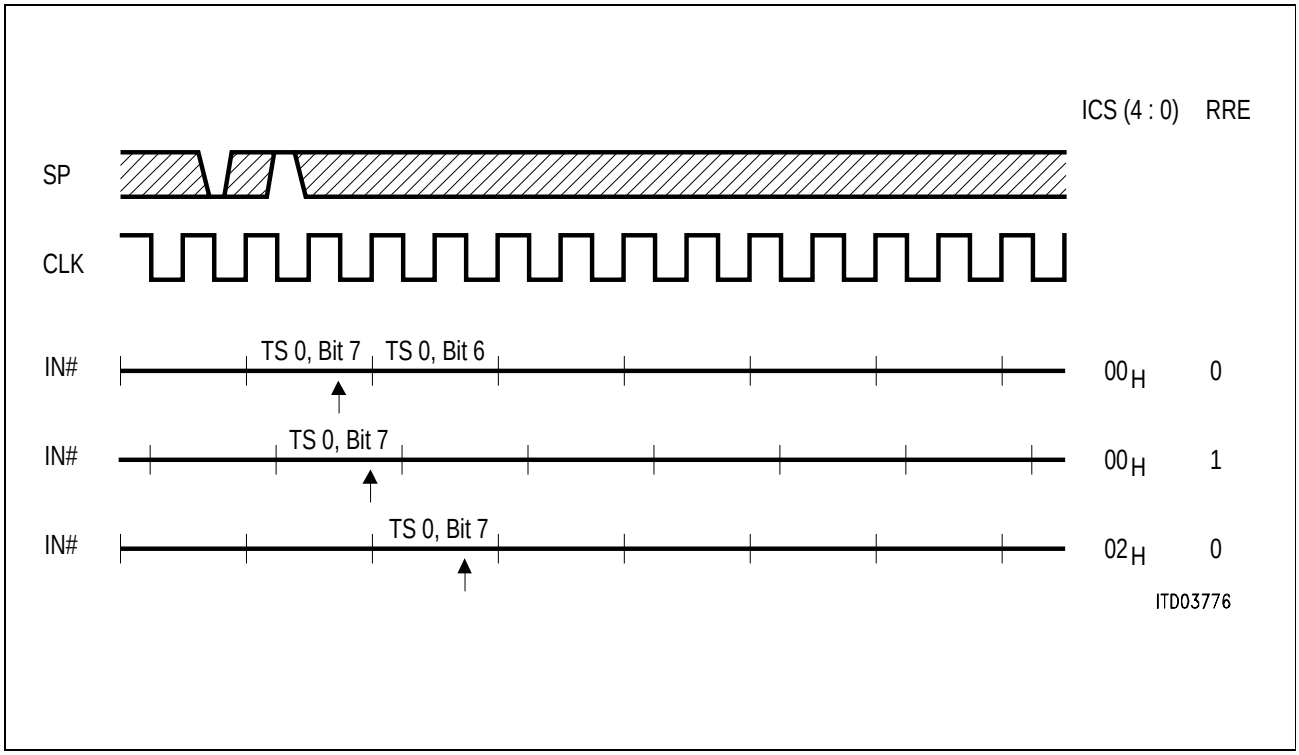


Figure 12
Device Clock = 2 × Data Rate

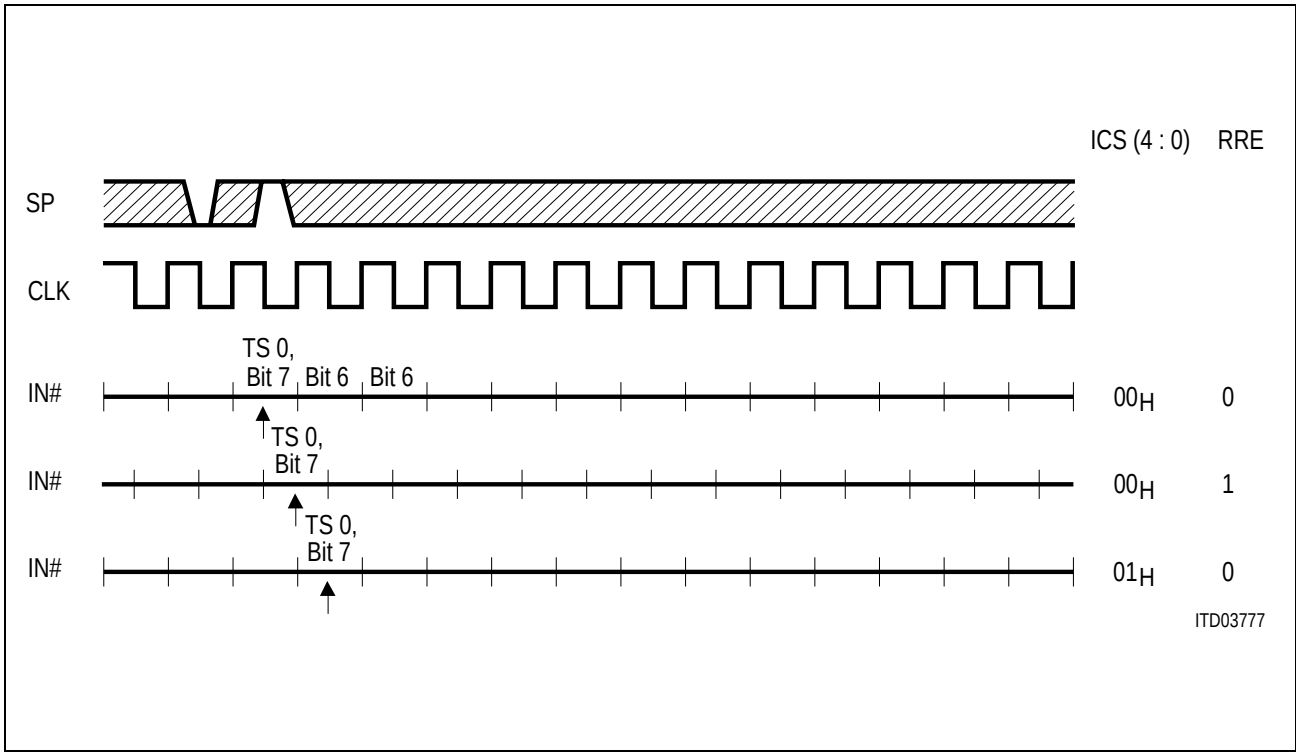


Figure 13
Device Clock = Data Rate

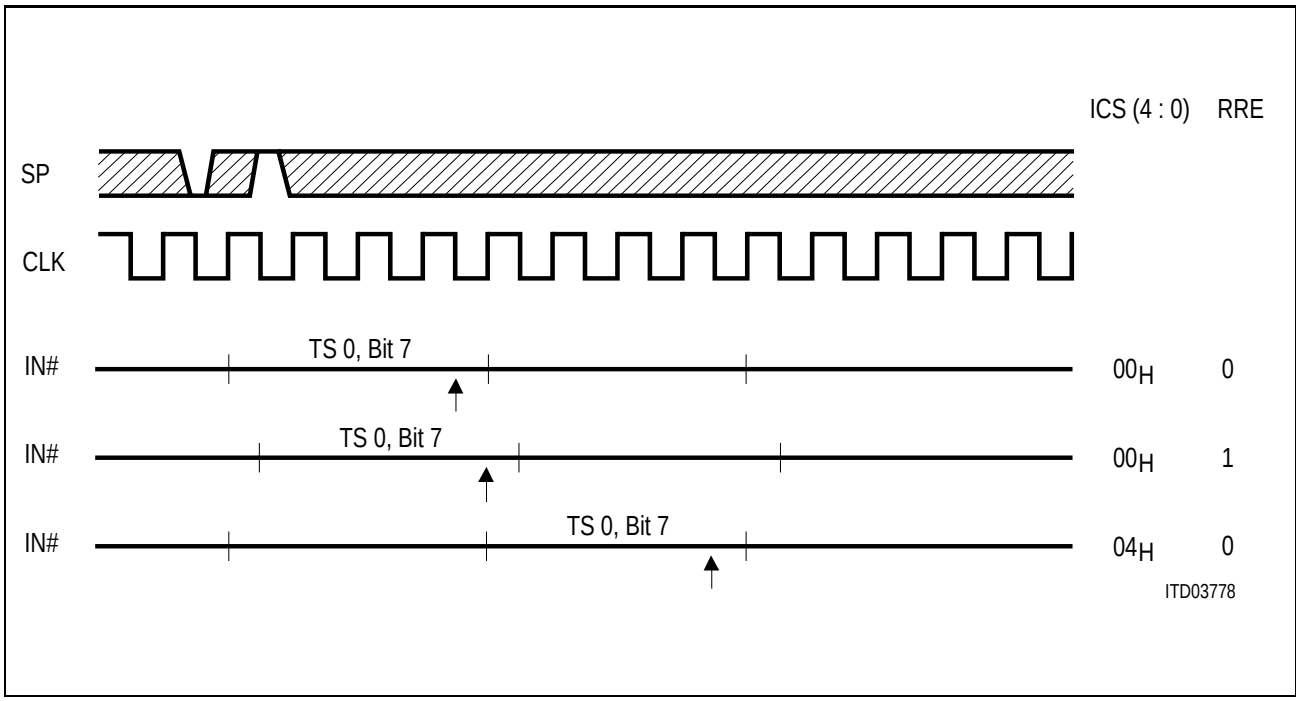


Figure 14
Device Clock = 4 × Data Rate

Operation Control Register (OPCR)

Read/write at indirect address IA (3:0) = D_H

Reset value: FF_H

Bit 7							Bit 0
1	**1**	**1**	**1**	**1**	**SDM**	**OC1**	**OC0**

SDM Select Data Memory; only used in configuration with OC (1:0) = 11_B

OC (1:0) Operation Control; OC (1:0) determine the usage of the two data memory blocks according to the table below.

Table 8

OC1	OC0	Function
1	1	Only one data memory block is used; the absolute address is given by SDM; bit D12 in the control memory is also interpreted as absolute address.
0	0	Both data memory blocks are used; bit D12 in the control memory controls the constant or minimal frame delay function.
0	1	Reserved
1	0	Reserved

Output Clock Shift Register (OSCR)

Read/write at indirect address IA (3:0) = E_H

Reset value: 20_H

This register determines the clock shift for all outputs.

Bit 7							Bit 0
VN2	**VN1**	**VN0**	**OCS3**	**OCS2**	**OCS1**	**OCS0**	**XFE**

OCS (3:0) **Output Clock Shift**

XFE **Transmit** on **Falling Edge**

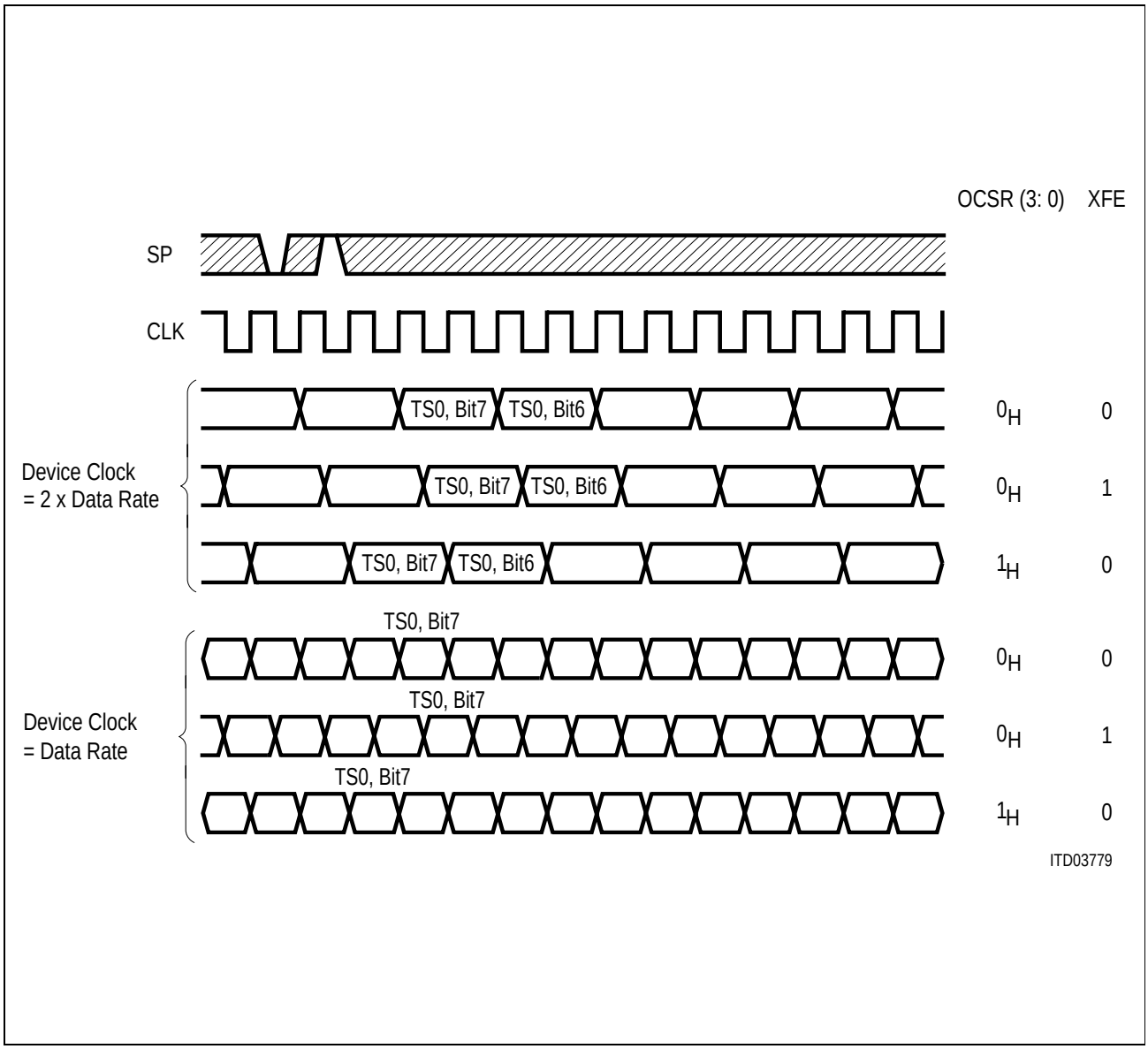


Figure 15
Output Timing and Clock Shift

VN (2:0) **Version Number** according to the table below:

Table 9
Version Number

VN2	VN1	VN0	Device Versions
0	0	0	A1
0	0	1	V2.1 (B1)

Frame Evaluation Register (FER)

Read at indirect address IA (3:0) = F_H

Reset value = XXX

After a frame evaluation procedure this 12-bit register contains the input counter offset between the SP frame and an evaluated FS0 … FS7 frame. The evaluation is performed at the second following rising edge of FS after the command CMDR:SFE = 1 was programmed.

Bit 7 Bit 0

				D11	**D10**	**D9**	**D8**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

D11 The FS-rising edge was sampled during the clock-high phase (D11 = 1), or during the clock-low phase (D11 = 0).

D (10:0) The FS-rising edge was sampled at:
input counter value + 1 if D11 = 1
input counter value + 2 if D11 = 0
With a device clock of 8 MHz D0 is fixed to 0 and D (10:1) contain the input counter value.

The actual offset between the SP frame and an evaluated FS frame can be calculated by the following formulas:

CLK × 1.024 MHz	Offset Value/Number of Clock Periods	D11	FS-Rising Edge at
8	$(D\ (10:1)_H + 01D_H)_{MOD1024}$ $(D\ (10:1)_H + 01E_H)_{MOD1024}$	0 1	CLK low CLK high
16	$(D\ (10:0)_H + 03D_H)_{MOD2048}$ $(D\ (10:0)_H + 03E_H)_{MOD2048}$	0 1	CLK low CLK high
4	$(D\ (9:1)_H + 01D_H)_{MOD512}$ $(D\ (9:1)_H + 01E_H)_{MOD512}$	0 1	CLK low CLK high

Definition of the calculated offset value:

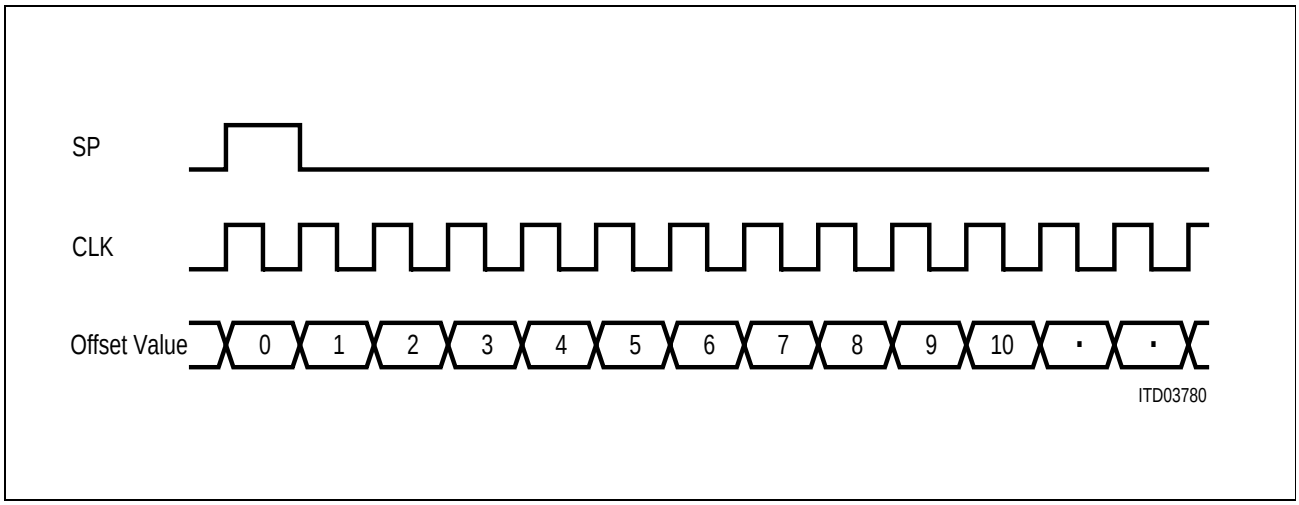


Figure 16
Formulas for Offset Calculation

Note: The device must be synchronized to SP (STAR: PSS = 1) in order to generate a correct result in FER.

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage at any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	7	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Characteristics

Ambient temperature under bias range; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V.

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-input voltage	V_{IL}	– 0.4	0.8	V	
H-input voltage	V_{IH}	2.2	V_{DD} + 0.4	V	
L-output voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA
Operational power supply current f_{CLK} = 8192 kHz f_{CLK} = 16384 kHz	 I_{CC} I_{CC}		 20 34	 mA mA	V_{DD} = 5 V, inputs at 0 V or V_{DD}, no output loads
Input leakage current Output leakage current	I_{LI} I_{LO}		10 10	µA µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

T_A = 25 °C, V_{DD} = 5 V ± 5 %, V_{SS} = 0 V.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
Output capacitance	C_{OUT}		15	pF
I/O capacitance	C_{IO}		20	pF

AC Characteristics

Ambient temperature under bias range, V_{DD} = 5 V ± 5 %.

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

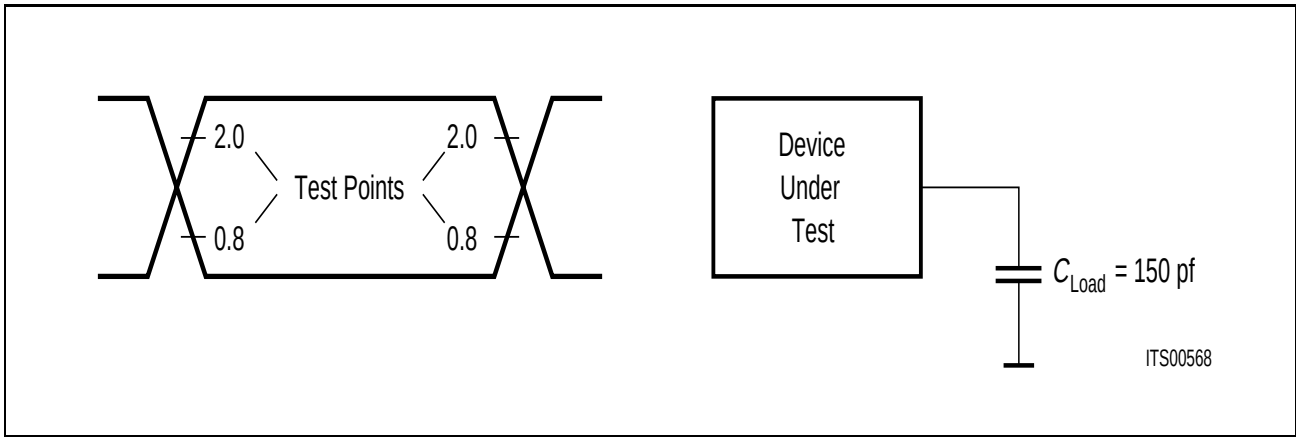


Figure 17
I/O Waveform for AC Tests

µP-Interface Timing Parameters

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	30		ns
Address setup time to ALE	t_{AL}	10		ns
Address hold time from ALE	t_{LA}	15		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	15		ns
$\overline{RD}$ delay after $\overline{WR}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		100	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ + $\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}$ + $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns
R/$\overline{W}$ delay after $\overline{RD}$ setup	t_{RWD}	0		ns

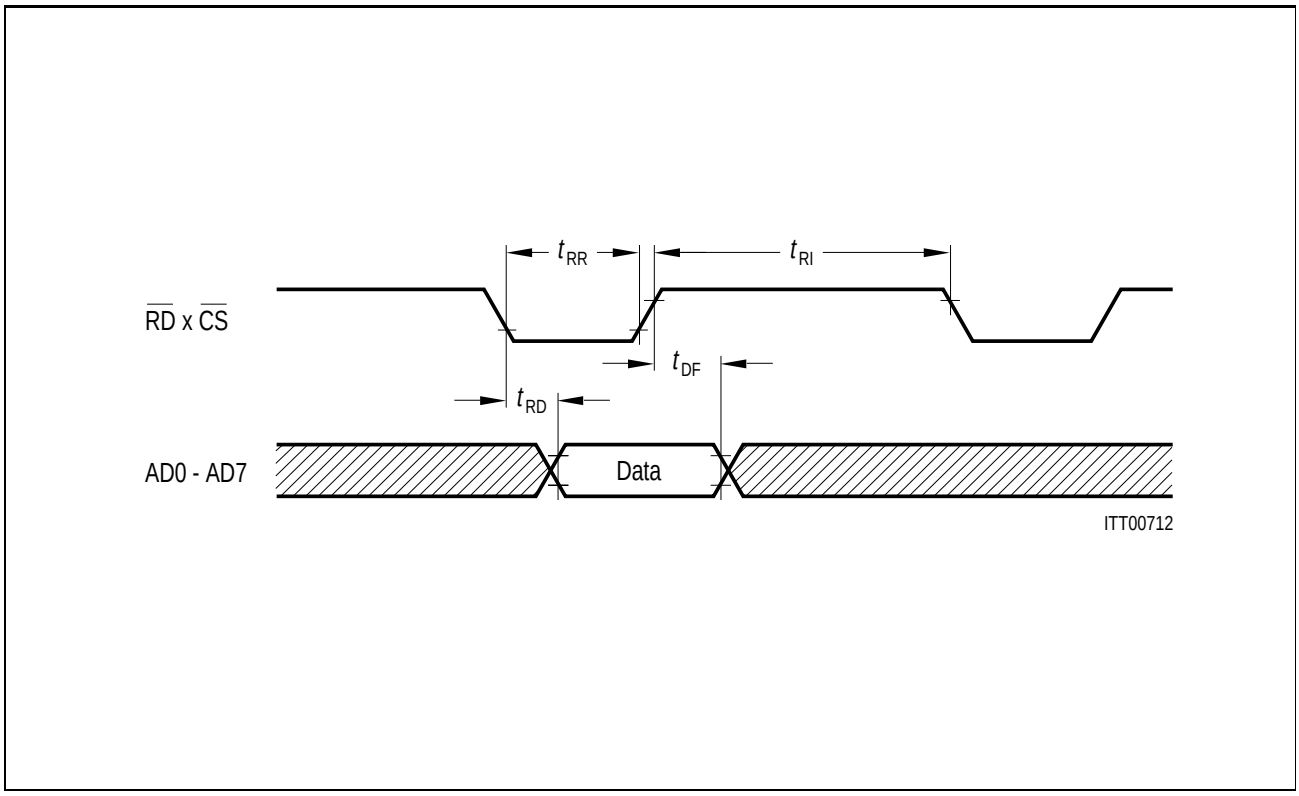


Figure 18
µP-Read Cycle

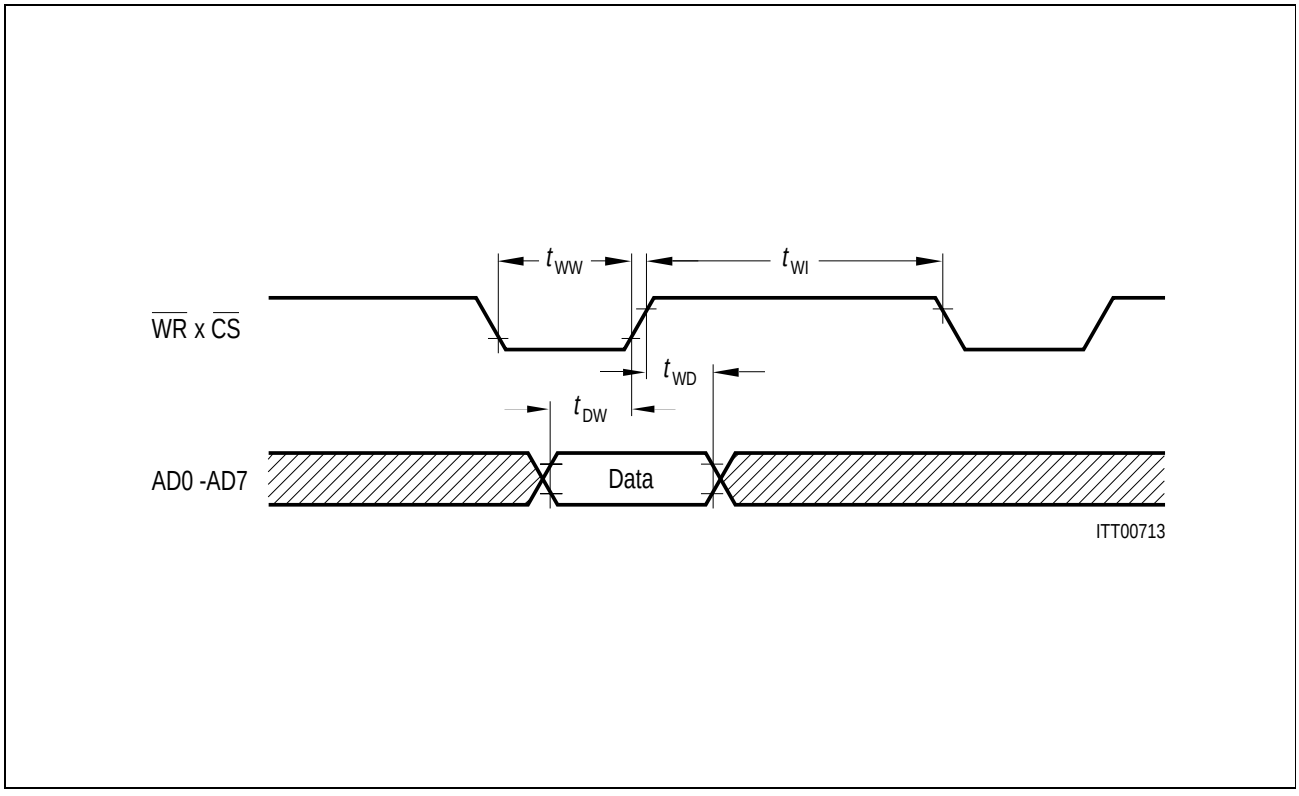


Figure 19
µP-Write Cycle

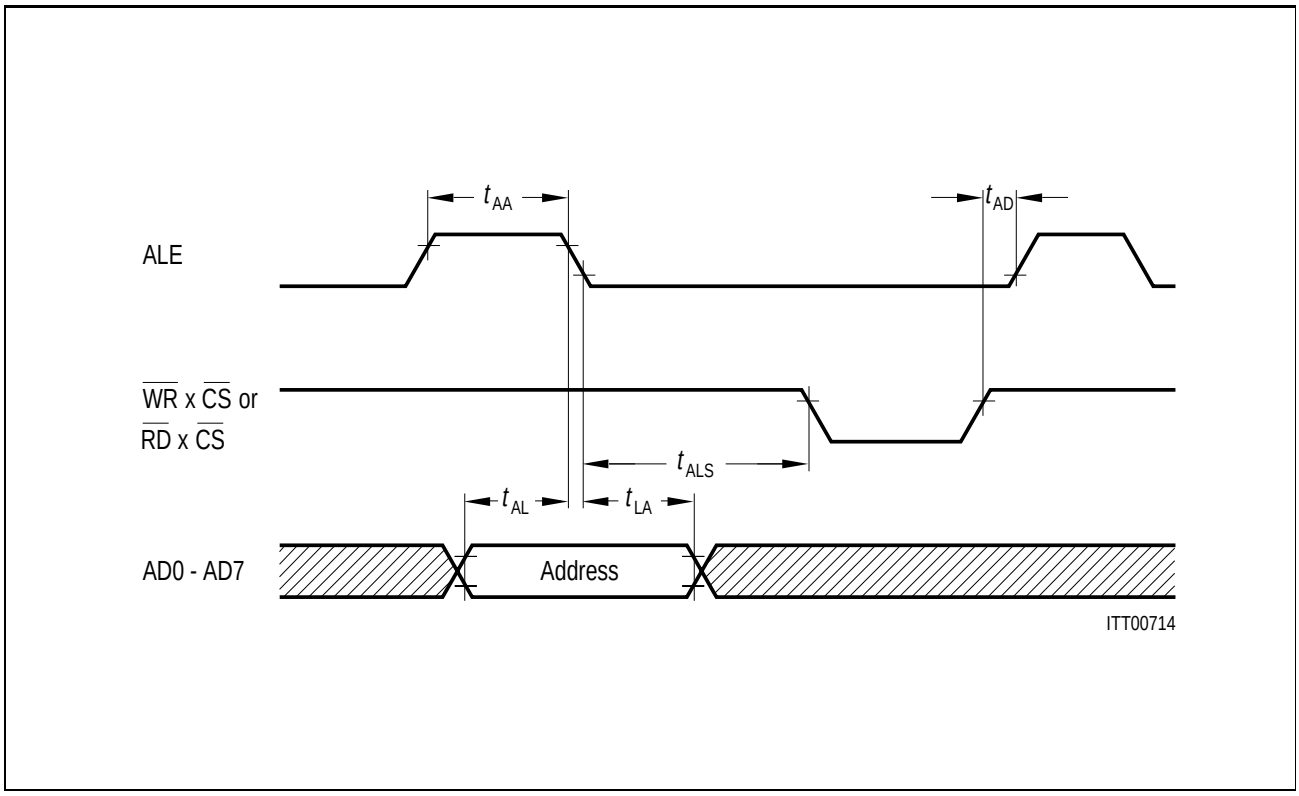


Figure 20
Multiplexed Address Timing

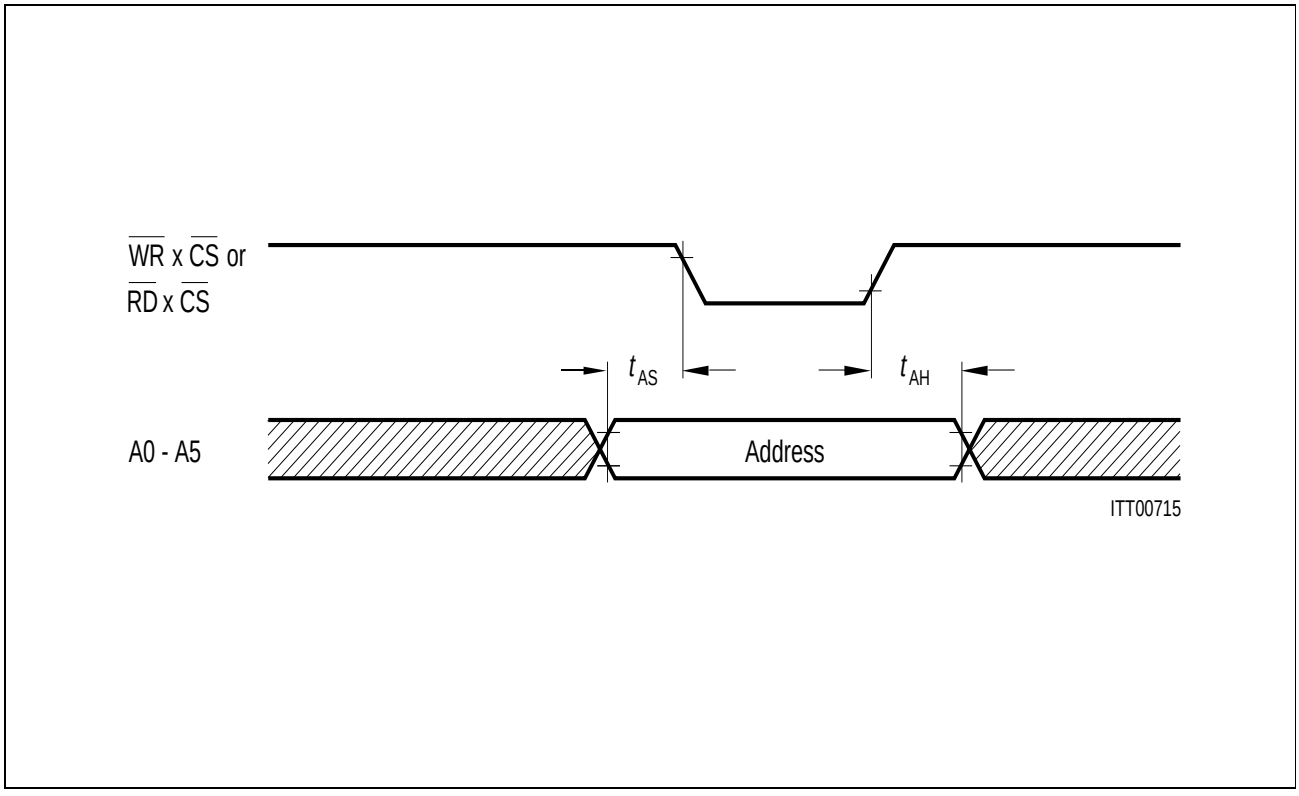


Figure 21
Demultiplexed Address Timing

Motorola Bus Mode

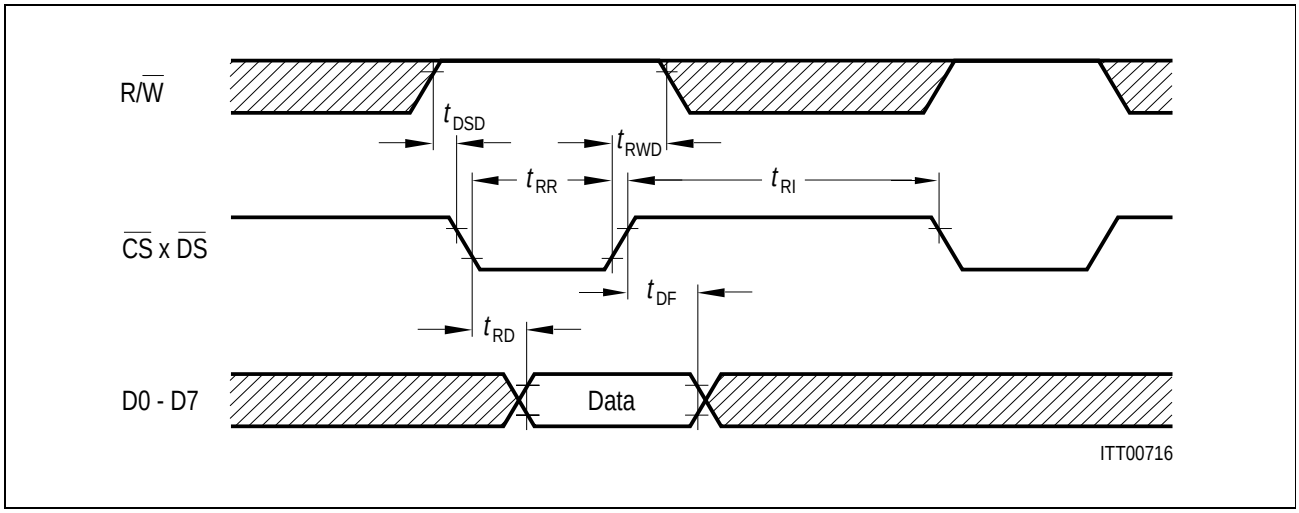


Figure 22
µP-Read Cycle

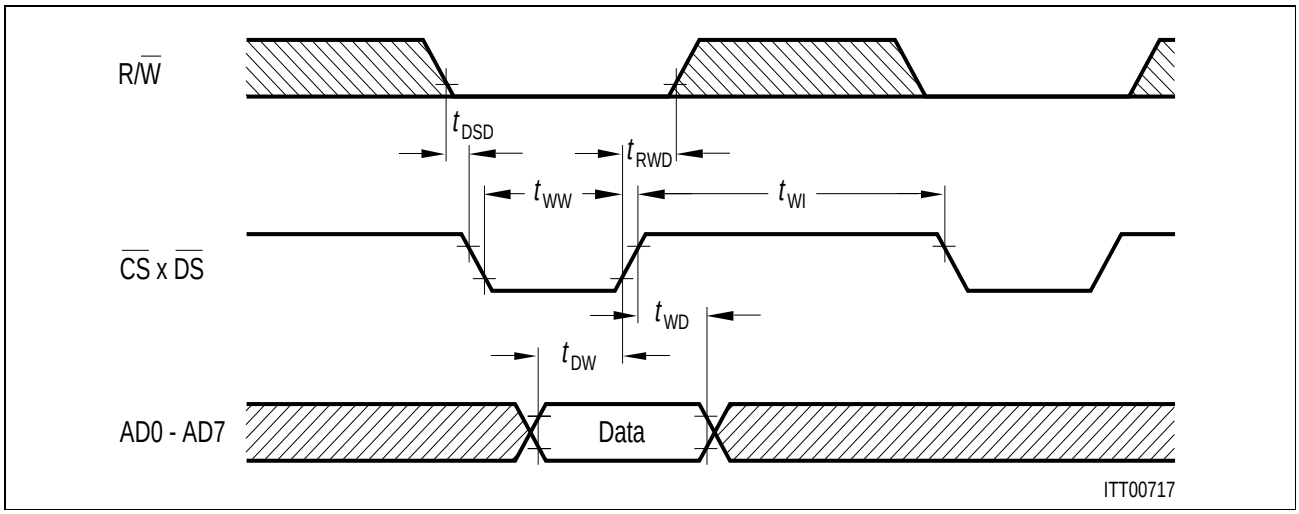


Figure 23
µP-Write Cycle

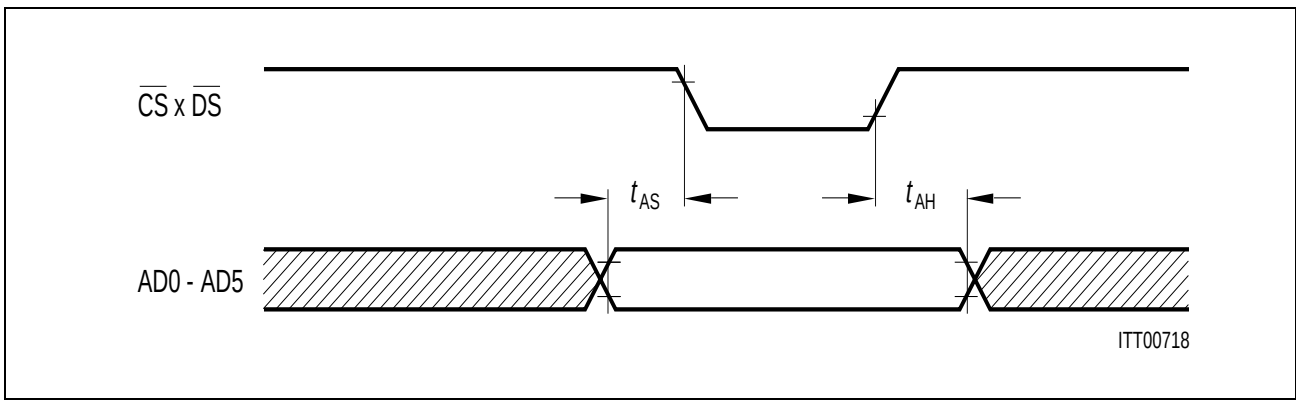


Figure 24
Address Timing

PCM-Interface Characteristics

Parameter	Symbol	Limit Values		Unit	Condition
		min.	max.		
Clock period	t_{CP}	120		ns	PEB 2047
Clock period low	t_{CPL}	50		ns	
Clock period high	t_{CPH}	50		ns	
Clock period	t_{CP}	60		ns	**PEB 2047-16**
Clock period low	t_{CPL}	27		ns	
Clock period high	t_{CPH}	23		ns	
Frame setup time	t_{FS}	15		ns	
Frame hold time	t_{FH}	20		ns	
Serial data input setup time	t_S	15		ns	PCM-input data frequency 8192 kHz
Serial data input hold time	t_H	20		ns	
Serial data input setup time	t_S	15		ns	PCM-input data frequency 16496 kHz
Serial data input hold time	t_H	20		ns	**only PEB 2047-16**
PCM-serial data output delay time	t_D		30	ns	

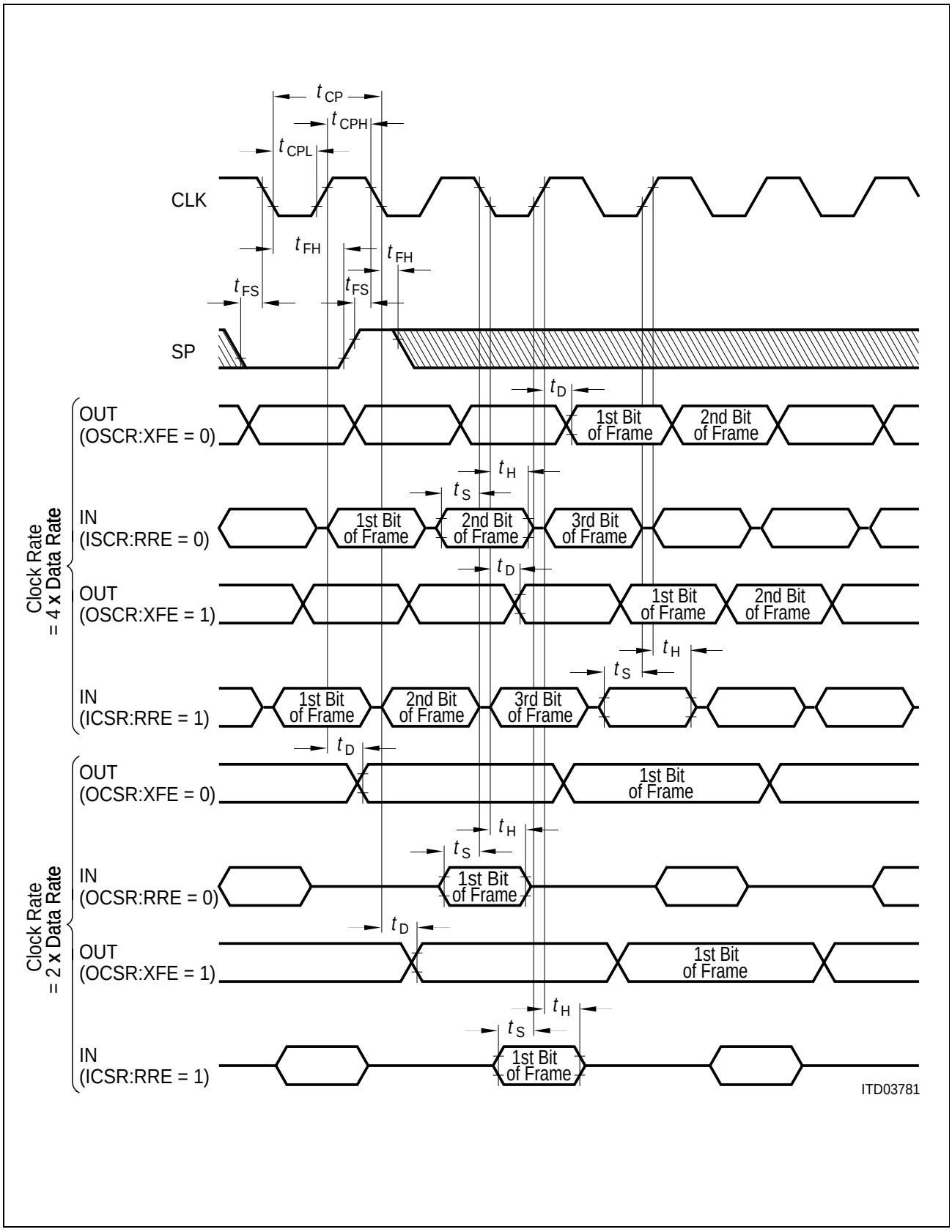


Figure 25
AC Characteristics at the PCM Interface

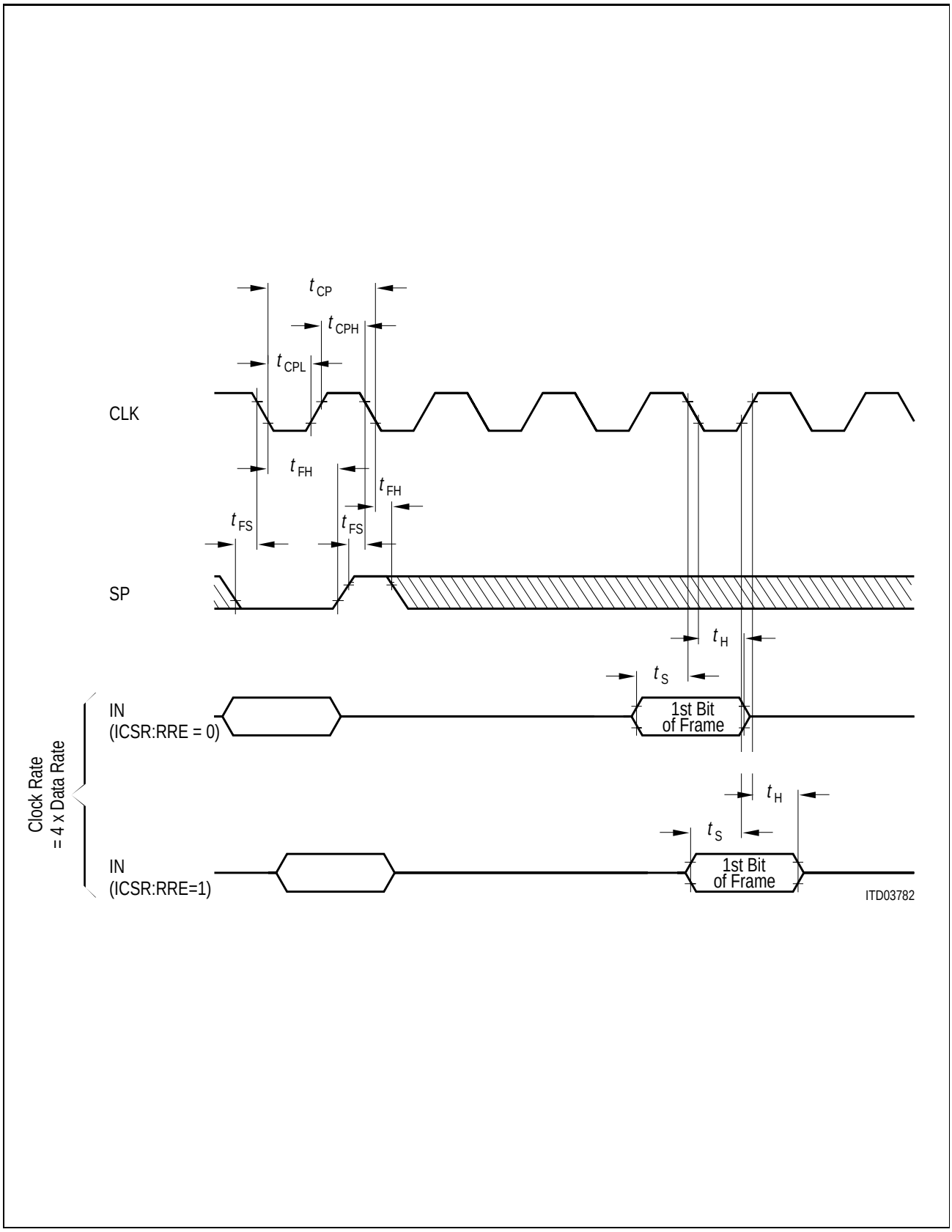


Figure 26
AC Characteristics at the PCM Interface

6 Applications

6.1 Determination of MTSL Frame Delay

When switching time slots from the input of the MTSL to its output, the question often arises whether the incoming channel is transmitted in the same frame (0 frame delay), the next frame (1 frame delay), or even in the frame thereafter (2 frames delay).

Because framing delay is different depending on the selected output port, delay timings have to be calculated separately for all outputs.

The following text advises how to do this calculation and delivers a value for MINIMAL or CONSTANT delay. A CONSTANT delay may be programmed by the control byte bit D12 of IAR-register.

Instructions for Use

1. Determine the data rate for the input data stream and for the output data stream. e.g. 4 Mbit/s for input data stream; 4 Mbit/s for output data stream.
2. Select a device clock. Please note, that not all ouput ports are available for every choice of the device clock (refer to the following table) !! e.g. 8 MHz.
3. Determine the constant T_d for your special configuration by selecting the corresponding row in the table below (a, b, c or d):
   e.g. for a 4 Mbit/s input- /output- data stream with 8 MHz device clock row a) has to be selected. The table delivers a value T_d = 4 for line OUT0 and T_d = 3 for OUT1 … 7.
   A big value for T_d also means a big internal switching delay.

	Input Data Rate [Mbit/s]	**Output Data Rate [Mbit/s]**	**Device CLK [MHz]**	T_d **for OUT0**	T_d **for OUT1**	T_d **for OUT2 … 3**	T_d **for OUT4 … 7**
a)	2, 4[1)] 4, 8	2 4	4 8	4	3	3	3
b)	2, 4[1)] 4, 8	4 8	4 8	7	6	6	not available !!
c)	2 4, 8, 16	4 8	8 16	6	5	5	5
d)	2, 4[1)] 4, 8, 16	8 16	8 16	11	10	10	not available !!

[1)] 2, 4 has the meaning 2,048 Mbit/s or 4,096 Mbit/s

4. Determine the constant M.
   The value for M can be determined by selecting the corresponding row in the table below (a, b or c) for your configuration.
   e.g. for a 4 Mbit/s input- /output- data stream with 8 MHz device clock row a) has to be selected. The table delivers the value M = 1.

The Constant M for Different Data Rates…

	Input Data Rate [Mbit/s]	**Output Data Rate [Mbit/s]**	**Device CLK [MHz]**	**M**
a)	2, 4 4, 8	2 4	4 8	1
b)	2, 4 4, 8 2 4, 8, 16	4 8 4 8	4 8 8 16	2
c)	2, 4 4, 8, 16	8 16	8 16	4

5. Determine the constant K.
   The value for K can be determined by selecting the corresponding row in the table below (a, b or c) for your configuration.
   e.g. for a 4 Mbit/s input- /output- data stream with 8 MHz device clock row a) has to be selected and the table delivers the value K = 1.

	Input Data Rate [Mbit/s]	**Output Data Rate [Mbit/s]**	**Device CLK [MHz]**	**Number of Input TS [K] Sampled at the same Time**
a)	2 2 4 4	2, 4 4, 8 4, 8 8, 16	4 8 8 16	1
b)	4 8 8	2, 4 4, 8 8, 16	4 8 16	2
c)	16	8, 16	16	4

6. By inserting the obtained values for K, M and T_d in the table below, minimal and constant frame delays may be calculated for every timeslot (TS).

Input TS	**Minimal Delay = 0 Frame for Output TS**	**Minimal Delay = 1 frame for Output TS**	**Minimal Delay = 2 Frames for Output TS**
0 × K … (1 × K – 1) 1 × K … (2 × K – 1) 2 × K … (3 × K – 1) 3 × K … (4 × K – 1) . . maxi + 1 – (n + 1) × K … maxi-n × K	T_d + (0 × M) … maxo T_d + (1 × M) … maxo T_d + (2 × M) … maxo T_d + (3 × M) … maxo … . maxo + 1 – (n + 1) × M + T_d … maxo	0 … (T_d – 1 + 0 × M) 0 … (T_d – 1 + 1 × M) 0 … (T_d – 1 + 2 × M) 0 … (T_d – 1 + 3 × M) … . 0 … maxo – (n + 1) × M + T_d	–
maxi + 1 – n × K … maxi – (n – 1) × K . . maxi + 1 – 2 × K … maxi-1 × K maxi + 1 – 1 × K … maxi-0 × K	–	T_d – n × M … maxo . . T_d – 2 × M … maxo T_d – 1 × M … maxo	0 … (T_d – n × M – 1) . . 0 … (T_d – 2 × M – 1) 0 … (T_d – 1 × M – 1)
constant delay in [frames]	1	1	3

The other constants inserted are:

n: This constant is a max. counter value that is obtained by integer division of T_d by M.

maxi: Is the maximal number of input time slots – 1

maxo: Is the maximal number of output time slots – 1

Please note: A negative value means no entry in the table!

Example

The example below will demonstrate the usage for a system with 8 MHz device CLK and 4 Mbit/s input and output data streams.

Before starting the calculation the value n must be found by integer division of T_d by M. With the values T_d = 4 and M = 1 the value for n = 4. With T_d = 3 and M = 1 the value for n = 3.

The maximal number of input time slots : maxi = 64 – 1 = 63

The maximal number of output time slots: maxo = 64 – 1 = 63

Frame Delay for OUT0 with T_d = 4, K = 1, M = 1, n = 4, maxo = 63, maxi = 63:

Input TS	Minimal Delay = 0 frame for Output TS	Mminimal Delay = 1 Frame for Output TS	Minimal Delay = 2 Frames for Output TS
0 1 2 . . 59	4 … 63 5 … 63 6 … 63 . . 63	0 … 3 0 … 4 0 … 5 . . 0 … 62	–
60 61 62 63	–	0 … 63 1 … 63 2 … 63 3 … 63	– 0 0 … 1 0 … 2
constant delay in [frames]	1	1	3

Frame Delay for OUT1 … 7 with T_d = 3, K = 1, M = 1, n = 4, maxo = 63, maxi = 63:

Input TS	Minimal Delay = 0 frame for Output TS	Minimal Delay = 1 Frame for Output TS	Minimal Delay = 2 Frames for Output TS
0 1 2 . . 60	3 … 63 4 … 63 5 … 63 . 63	0 … 2 0 … 3 0 … 4 . . 0 … 62	–
61 62 63	–	0 … 63 1 … 63 2 … 63	– 0 0 0 … 1
constant delay in [frames]	1	1	3

6.2 Example for a MTSL Design guaranteeing Constant Frame Delay for all Time Slots

In order to achieve a constant frame delay of all PCM channels switched from input to output, the following work-around is suggested. The device is operated with a 16-MHz clock and 8×8 MHz PCM lives for input and output respectively. The effective switch capacity is reduced to 512×512.

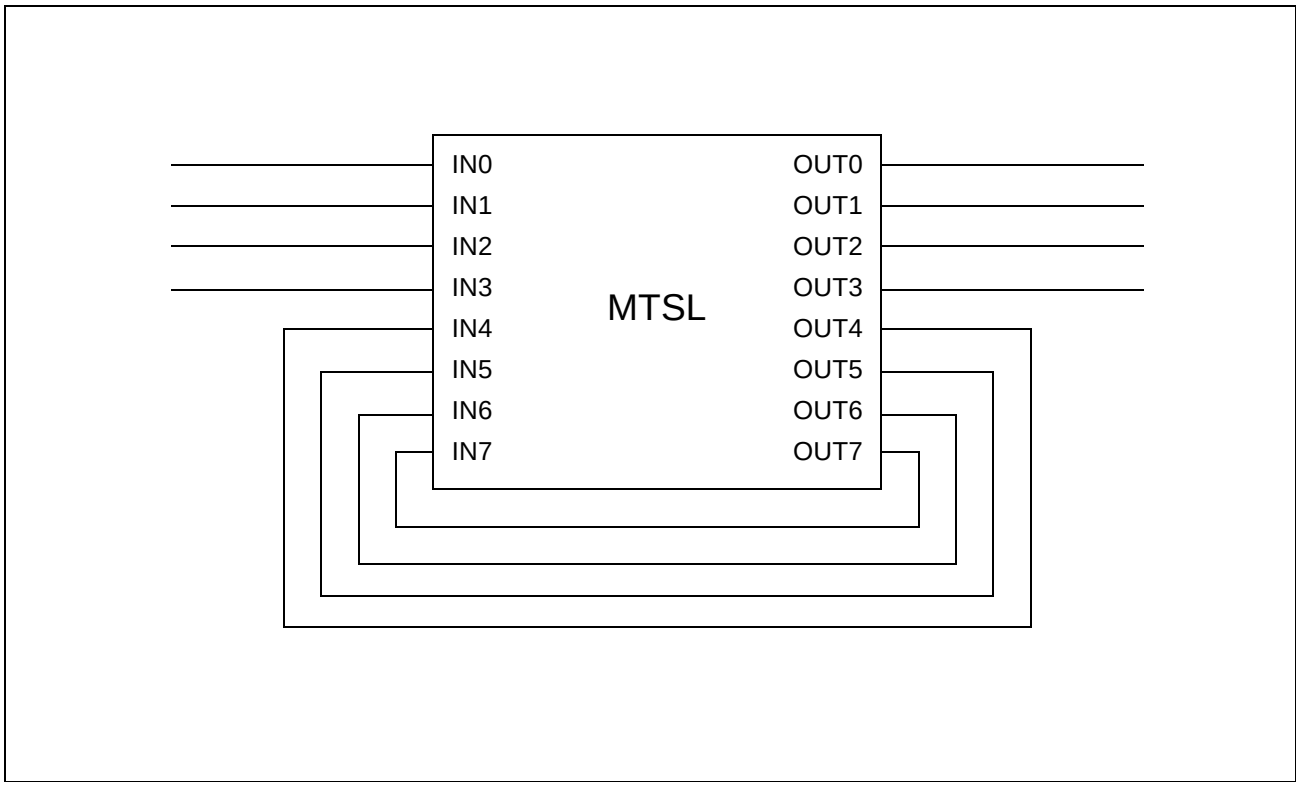


Figure 27
MTSL Operation Mode with Constant Frame Delay (frame delay = 1)

The general idea in this configuration is to switch all input time-slots, which would be passed to the output in the same frame (input TS# + OFFSET < output TS#), to OUT [4:7] followed by a switch from IN [4:7] to the desired output time-slot at OUT [0:3]. Thus a constant frame delay of one frame can be achieved (**refer to table 10**).

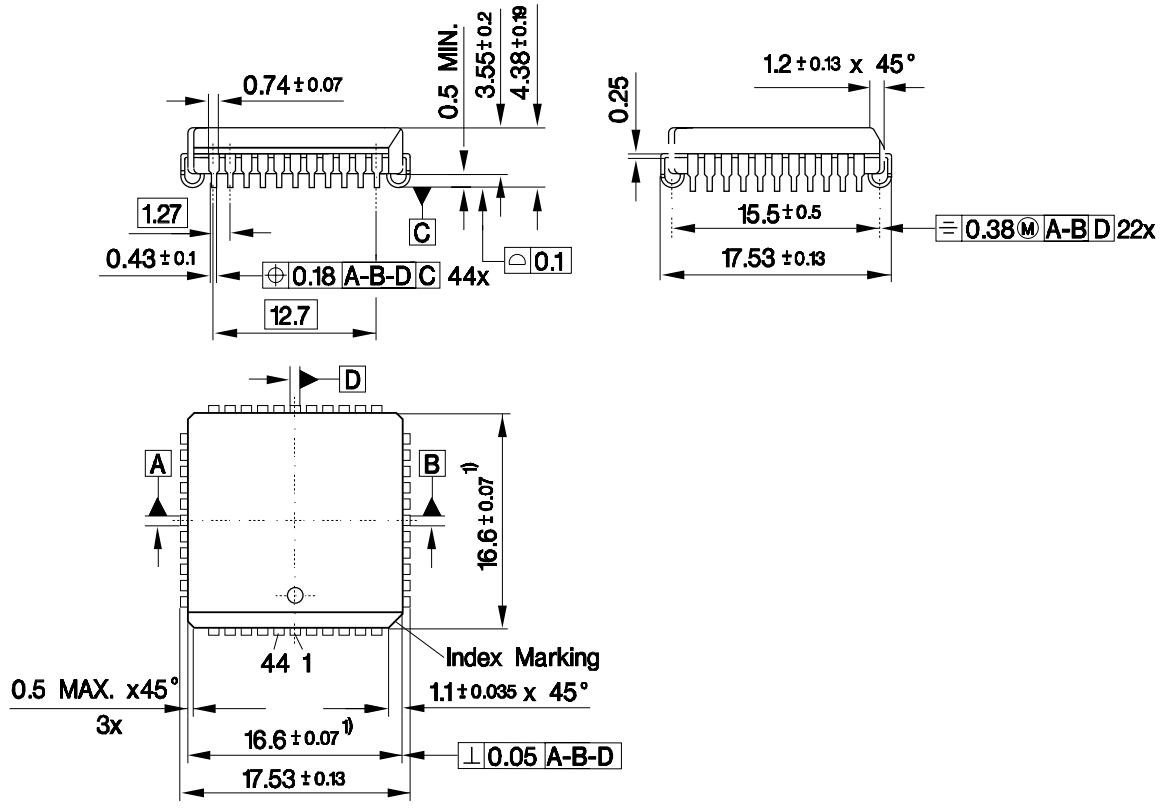
For a 8 MHz/8 MHz-system for example the following frame delay table can be deduced from the timing diagram:

Table 10
Frame Delay

	Input Time-Slot	Switched to Output Time-Slot		
IN0 ... IN4 or (IN4 ... IN7 switched to OUT1 ... OUT3)	0 – 1 2 – 3 4 – 5 . . . 118 – 119 120 – 121 122 – 123 124 – 125 126 – 127	6 – 127 8 – 127 10 – 127 . . . 124 – 125 126 – 127 – – –	0 – 5 0 – 7 0 – 9 . . . 0 – 123 0 – 125 0 – 127 2 – 127 4 – 127	– – . – . . . – – – 0 – 1 0 – 3
IN4 ... IN7 switched to OUT0	0 – 1 2 – 3 4 – 5 . . . 120 121 122 – 123 124 – 125 126 – 127	7 – 127 9 – 127 11 – 127 . . . 127 – – – –	0 – 6 0 – 8 0 – 10 . . . 0 – 126 0 – 127 1 – 127 3 – 127 5 – 127	– – – . . . – – 0 0 – 2 0 – 4
Delay/Number of frames		0	1	2

7 Package Outlines

Plastic Package, P-LCC-44 (SMD)
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPL05102

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm