= Preliminary =

AK4367

Low Power 24-Bit 2ch DAC with HP-AMP & Output Mixer

GENERAL DESCRIPTION

The AK4367 is 24bit DAC with built-in Headphone Amplifier. The AK4367 features an analog mixing circuit that allows easy interfacing in mobile phone and portable communication designs. The integrated headphone amplifier features “click-free” power-on/off, a mute control and delivers 50mW of power at 16Ω. The AK4365 is housed in a 20pin QFN package, making it suitable for portable applications.

FEATURE

- **Multi-bit ΔΣ DAC**
- **Sampling Rate: 8kHz~48kHz**
- **64x Oversampling**
- **On chip perfect filtering 8 times FIR interpolator**
  - **Passband: 20kHz**
  - **Passband Ripple: ±0.02dB**
  - **Stopband Attenuation: 54dB**
- **Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz**
- **System Clock: 256fs/384fs/512fs**
  - **Input Level: CMOS or 0.4Vpp Analog Input**
- **Audio I/F Format: MSB First, 2’s Compliment**
  - **I^2S, 24bit MSB justified, 24bit/20bit/16bit LSB justified**
- **Digital ATT**
- **Analog Mixing Circuit**
- **Mono Lineout**
- **µP Interface: 3-wire/I^2C**
- **Bass Boost Function**
- **Headphone Amplifier**
  - **Output Power: 50mW x 2ch @16Ω, 3.3V**
  - **S/N: 92dB@2.4V**
  - **Click Noise Free at Power-ON/OFF and Mute**
- **Power Supply: 2.2V ~ 3.6V**
- **Power Supply Current: 2.8mA@2.4V (@HP-AMP no-input)**
- **Ta: -40 ~ 85°C**
- **Small Package: 20pin QFN**

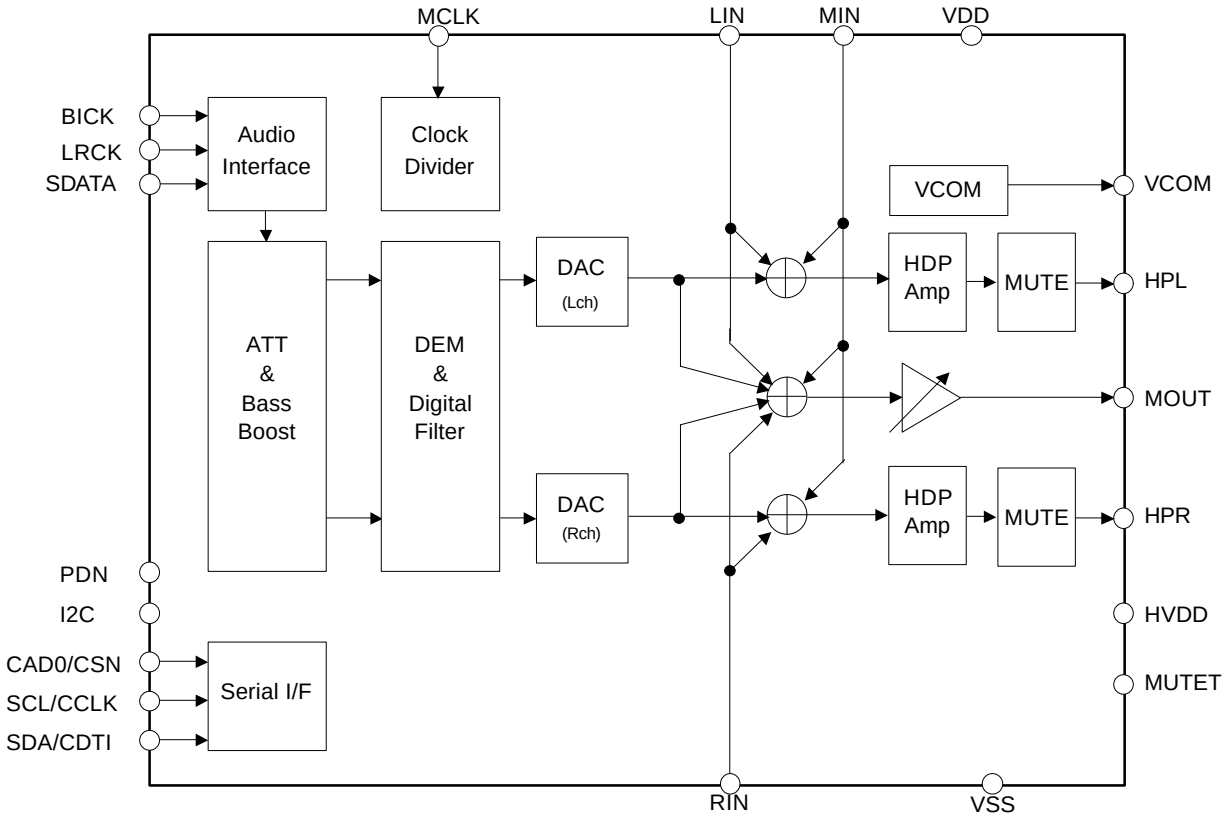
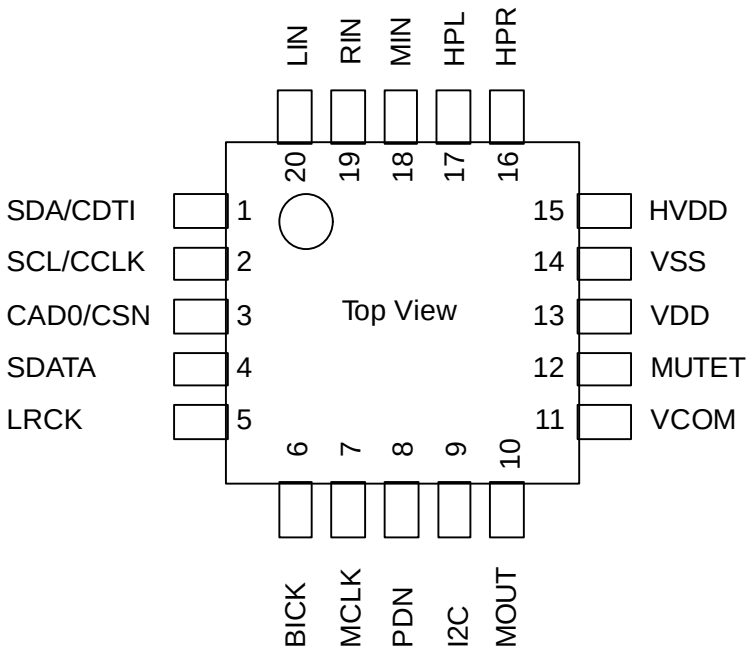


Figure 1. AK4367 Block Diagram

■ Ordering Guide

AK4367VN	-40 ~ +85°C	20pin QFN (0.5mm pitch)
AKD4367	Evaluation board for AK4367	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SDA	I/O	Control Data Input/Output Pin (I2C = "H")
	CDTI	I	Control Data Input Pin (I2C = "L")
2	SCL	I	Control Data Clock Pin (I2C = "H")
	CCLK	I	Control Data Clock Pin (I2C = "L")
3	CAD0	I	Chip Address 0 Select Pin (I2C= "H")
	CSN	I	Control Data Chip Select Pin (I2C= "L")
4	SDATA	I	Audio Serial Data Input Pin
5	LRCK	I	L/R Clock Pin This clock determines which audio channel is currently being input on SDATA pin.
6	BICK	I	Serial Bit Clock Pin This clock is used to latch audio data.
7	MCLK	I	Master Clock Input Pin
8	PDN	I	Power-down & Reset Pin When at "L", the AK4367 is in power-down mode and is held in reset. The AK4367 should always be reset upon power-up.
9	I2C	I	Control Mode Select Pin (Internal Pull-down Pin) "H": I^2C Bus, "L": 3-wire Serial
10	MOUT	O	Mono Analog Output Pin
11	VCOM	O	Common Voltage Output Pin Normally connected to VSS pin with 0.1μF ceramic capacitor in parallel with a 2.2μF electrolytic capacitor.
12	MUTET	O	Mute Time Constant Control Pin Connected to VSS pin with a capacitor for mute time constant.
13	VDD	-	Power Supply Pin
14	VSS	-	Ground Pin
15	HVDD	-	Power Supply Pin for Headphone Amp
16	HPR	O	Rch Headphone Amp Output Pin
17	HPL	O	Lch Headphone Amp Output Pin
18	MIN	I	Mono Analog Input Pin
19	RIN	I	Rch Analog Input Pin
20	LIN	I	Lch Analog Input Pin

Note: All digital input pins except internal pull-down pin must not be left floating.

ABSOLUATE MAXIMUM RATING

(VSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog, Digital	VDD	-0.3	4.6	V
	HP-AMP	HVDD	-0.3	4.6	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Input Voltage		VIN	-0.3	VDD+0.3 or 4.6	V
Ambient Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog, Digital	VDD	2.2	2.4	3.6	V
(Note 2)	HP-AMP	HVDD	2.2	2.4	3.6	V

Note 1. All voltages with respect to ground.
Note 2. VDD should be same voltage as HVDD.

* AKM assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=HVDD=2.4V, VSS=0V; fs=44.1kHz; BOOST OFF; Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Headphone-Amp: Load impedance is a serial connection with R_L =16Ω and C_L=220μF. (Refer to Figure 32); Mono output: R_L =16Ω; unless otherwise specified)

Parameter			min	typ	max	Units
DAC Resolution			-	-	24	bit
LINEIN: (LIN/RIN/MIN pins)						
Analog Input Characteristics						
Input Resistance			TBD	40	TBD	kΩ
Gain						
LIN/RIN→MOUT			TBD	-6	TBD	dB
MIN→MOUT			TBD	0	TBD	dB
LIN/MIN→HPL, RIN/MIN→HPR			TBD	+1.8	TBD	dB
Headphone-Amp: (HPL/HPR pins) (Note 3)						
Analog Output Characteristics						
THD+N	(-3dBFS Output, Po=15mW@16Ω, 2.4V)		-	-58	TBD	dB
	(-3dBFS Output, Po=28mW@16Ω, 3.3V)		-	-58	-	dB
D-Range	(-60dBFS Output, A-weighted, 2.4V)		TBD	92	-	dB
	(-60dBFS Output, A-weighted, 3.3V)		-	94	-	dB
S/N	(A-weighted, 2.4V)		TBD	92	-	dB
	(A-weighted, 3.3V)		-	94	-	dB
Interchannel Isolation			TBD	80	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.2	TBD	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance		(Note 4)	16	-	-	Ω
Load Capacitance				-	-	300
Output Voltage	(-3dBFS Output)	(Note 5)	TBD	1.39	TBD	Vpp
Max Output Power	(R_L=16Ω, 2.4V)		-	26	-	mW
	(R_L=16Ω, 3.3V)		-	50	-	mW
Mono Output: (MOUT pin) (Note 6)						
Analog Output Characteristics:						
THD+N	(0dBFS Output)		-	-60	TBD	dB
S/N	(A-weighted)		TBD	92	-	dB
DC Accuracy						
Gain Drift			-	200	-	ppm/°C
Load Resistance		(Note 4)	10	-	-	kΩ
Load Capacitance			-	-	25	pF
Output Voltage		(Note 7)	TBD	1.58	TBD	Vpp
Output Volume: (MOUT pin)						
Step Size			TBD	2	TBD	dB
Gain Control Range			-30	-	0	dB

Note 3. DACL=DACR= "1", MINL=MINR=LINL=RINR= "0", ATTL=ATTR=0dB.

Note 4. AC Load

Note 5. Output voltage is proportional to VDD voltage. Vout = 0.58 x VDD(typ)@-3dBFS.

Note 6. DACM= "1", DACL=DACR= "0", LINM=RINM=MINM= "0", ATTL=ATTR=ATTM=0dB, and common mode signal is input to L/Rch of DAC.

Note 7. Output voltage is proportional to VDD voltage. Vout = 0.66 x VDD(typ).

Power Supplies					
Power Supply Current					
Normal Operation (PDN= "H")	(Note 8)				
VDD		-	1.8	TBD	mA
HVDD		-	1.0	TBD	mA
Power-Down Mode (PDN= "L")	(Note 9)	-	1	TBD	μA

Note 8. PMDAC=PMHPL=PMHPR=PMMO= "1", MUTEN= "1" and HP-Amp output is off.

Note 9. All digital input pins including clock pins (MCLK, BICK and LRCK) are held at VDD or VSS. PDN pin is held at VSS.

FILTER CHARACTERISTICS

(Ta=25°C; VDD, HVDD=2.2 ~ 3.6V; fs=44.1kHz; De-emphasis = "OFF")

Parameter			Symbol	min	typ	max	Units
DAC Digital Filter: (Note 10)							
Passband	-0.05dB	(Note 11)	PB	0	-	20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband		(Note 11)	SB	24.1	-	-	kHz
Passband Ripple			PR	-	-	±0.02	dB
Stopband Attenuation			SA	54	-	-	dB
Group Delay		(Note 12)	GD	-	20.8	-	1/fs
Group Delay Distortion			ΔGD	-	0	-	μs
DAC Digital Filter + Analog Filter: (Note 10) (Note 13)							
Frequency Response	0 ~ 20.0kHz		FR	-	±0.5	-	dB
Analog Filter: (Note 14)							
Frequency Response	0 ~ 20.0kHz		FR	-	±1.0	-	dB
BOOST Filter:	(Note 13) (Note 15)						
Frequency Response	MIN	20Hz	FR	-	5.76	-	dB
		100Hz		-	2.92	-	dB
		1kHz		-	0.02	-	dB
	MID	20Hz	FR	-	10.80	-	dB
		100Hz		-	6.84	-	dB
		1kHz		-	0.13	-	dB
	MAX	20Hz	FR	-	16.06	-	dB
		100Hz		-	10.54	-	dB
		1kHz		-	0.37	-	dB

Note 10. BOOST OFF (BST1-0 = "00")

Note 11. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.05dB), SB=0.546*fs(@-54dB).

Note 12. This is the calculated delay time caused by digital filtering. This time is measured from the setting of the 24bit data of both channels to the input registers to the output of the analog signal.

Note 13. DAC → HPL, HPR, MOUT

Note 14. MIN → HPL/HPR/MOUT, LIN → HPL/MOUT, RIN → HPR/MOUT

Note 15. These frequency responses scale with fs. If high-level signal is input, the AK4367 clips at low frequency.

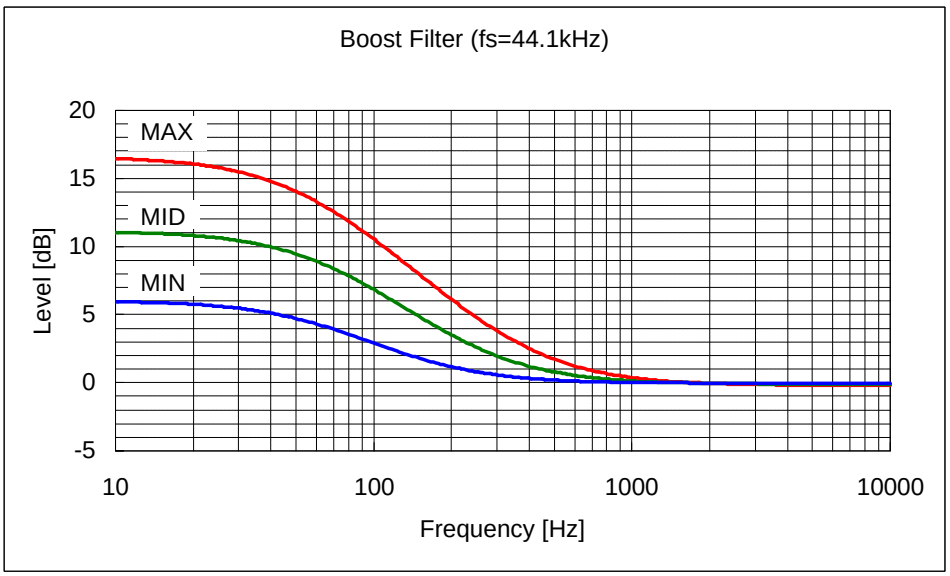


Figure 2. Boost Frequency (fs=44.1kHz)

DC CHARACTERISTICS

(Ta=25°C; VDD, HVDD=2.2 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage		VIH	70%DVDD	-	-	V
Low-Level Input Voltage		VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling	(Note 16)	VAC	0.4	-	-	Vpp
Low-Level Output Voltage	(Iout = 3mA)	VOL	-	-	0.4	V
Input Leakage Current	(Note 17)	Iin	-	-	±10	μA

Note 16. Only MCLK pin. (Figure 32)

Note 17. I2C pin has internal pull-down device, nominally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta=25°C; VDD, HVDD=2.2 ~ 3.6V; C_L = 20pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	2.048	-	24.576	MHz
Pulse Width Low	(Note 18)	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	(Note 18)	tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width	(Note 21)	tACW	20	-	-	ns
LRCK Timing						
Frequency		fs	8	44.1	48	kHz
Duty Cycle:		Duty	45	-	55	%
Serial Interface Timing (Note 19)						
BICK Period		tBCK	1/(64fs)	-	-	ns
BICK Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
LRCK Edge to BICK "↑"	(Note 20)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge	(Note 20)	tBLR	50	-	-	ns
SDATA Hold Time		tSDH	50	-	-	ns
SDATA Setup Time		tSDS	50	-	-	ns
Control Interface Timing (3-wire Serial mode)						
CCLK Period		tCCK	200	-	-	ns
CCLK Pulse Width Low		tCCKL	80	-	-	ns
Pulse Width High		tCCKH	80	-	-	ns
CDTI Setup Time		tCDS	40	-	-	ns
CDTI Hold Time		tCDH	40	-	-	ns
CSN "H" Time		tCSW	150	-	-	ns
CSN "↑" to CCLK "↑"		tCSS	50	-	-	ns
CCLK "↑" to CS "↑"		tCSH	50	-	-	ns

Note 18. Except AC coupling.

Note 19. Refer to "Serial Data Interface".

Note 20. BICK rising edge must not occur at the same time as LRCK edge.

Note 21. Pulse width to ground level when MCLK is connected to a capacitor in series and a resistor is connected to ground. (Refer to Figure 3.)

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus mode): (Note 22)					
SCL Clock Frequency	fSCL	-	-	100	kHz
Bus Free Time Between Transmissions	tBUF	4.7	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	4.0	-	-	μs
Clock Low Time	tLOW	4.7	-	-	μs
Clock High Time	tHIGH	4.0	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	4.7	-	-	μs
SDA Hold Time from SCL Falling (Note 23)	tHD:DAT	-		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.25	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	4.0	-	-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 24)	tPD	150	-	-	ns

Note 22. I^2C is a registered trademark of Philips Semiconductors.
Note 23. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 24. The AK4367 can be reset by bringing PDN= "L" to "H" only upon power up.

Purchase of Asahi Kasei Microsystems Co., Ltd I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conform to the I^2C specifications defined by Philips.

■ Timing Diagram

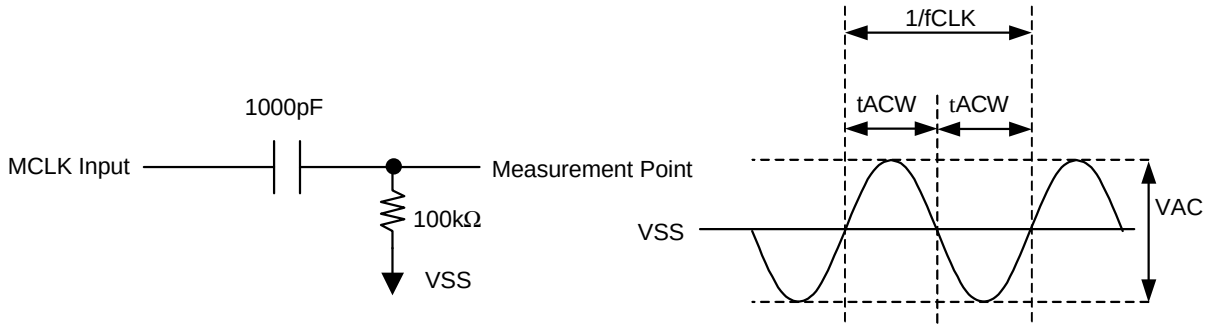


Figure 3. MCLK AC Coupling Timing

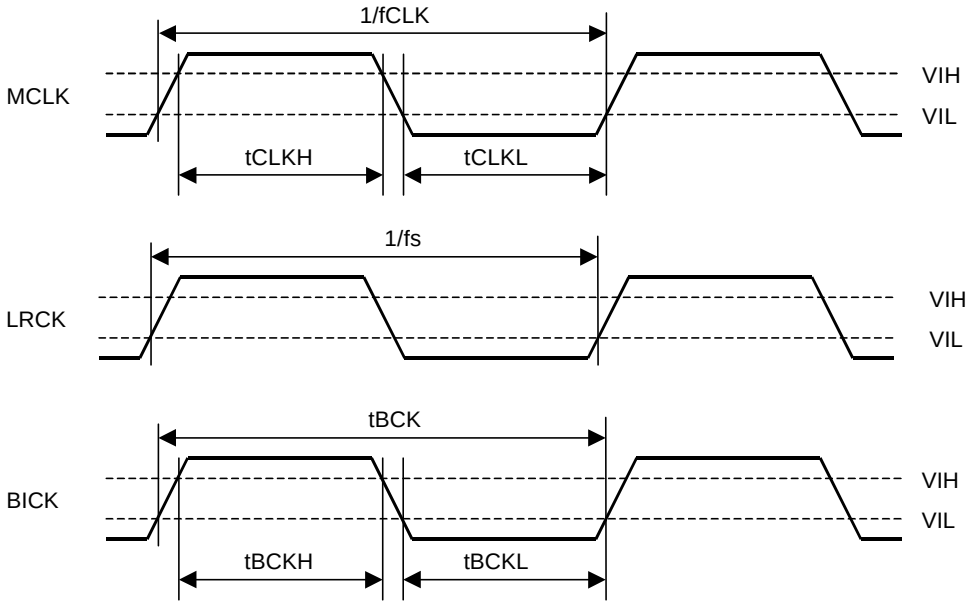


Figure 4. Clock Timing

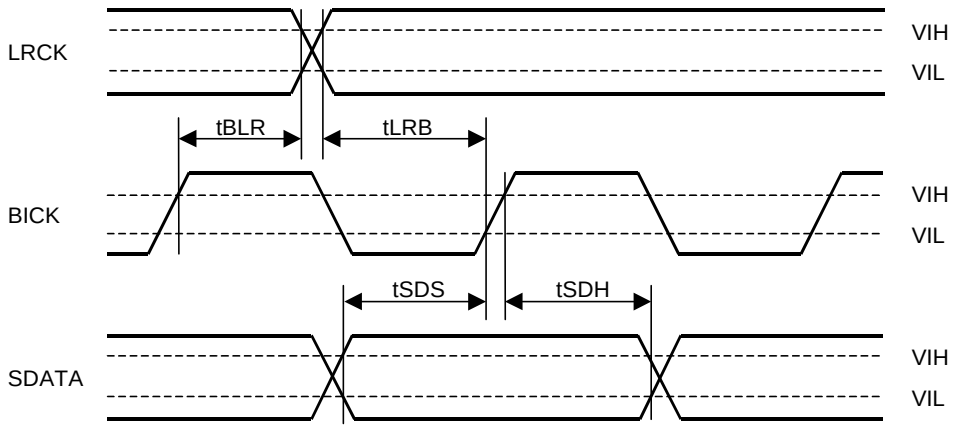


Figure 5. Serial Interface Timing

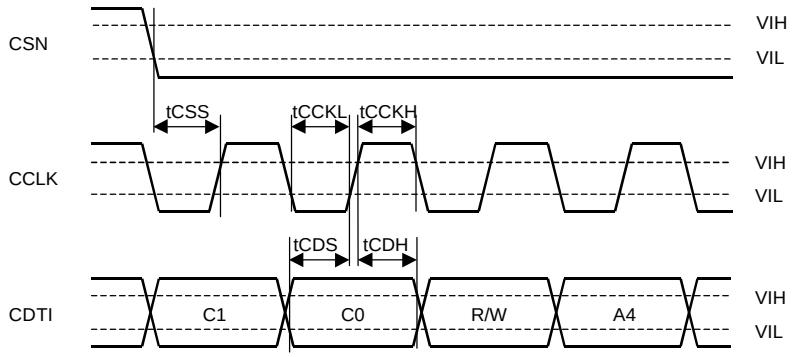


Figure 6. WRITE Command Input Timing

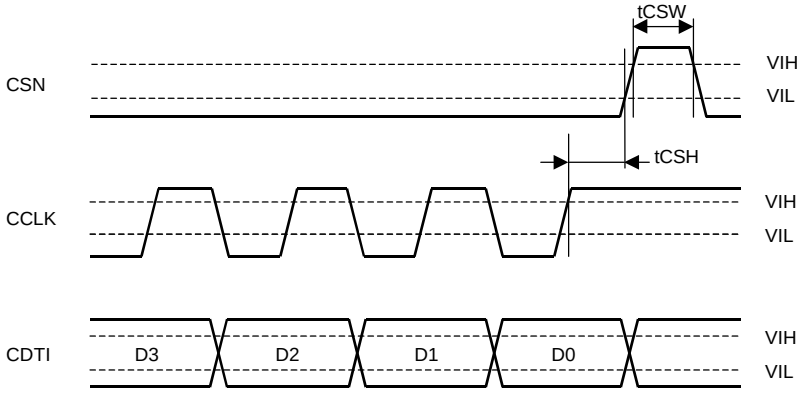


Figure 7. WRITE Data Input Timing

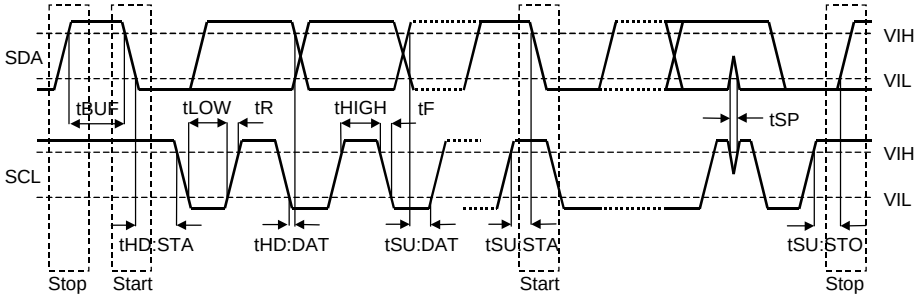


Figure 8. I^2C Bus Mode Timing

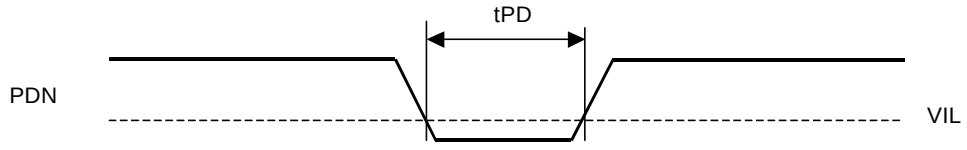


Figure 9. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks required to operate the AK4367 are MCLK(256fs/384fs/512fs), LRCK(fs) and BICK. The master clock (MCLK) should be synchronized with sampling clock (LRCK). The phase between these clocks does not matter. The frequency of MCLK is detected automatically, and the internal master clock becomes the appropriate frequency. Table 1 shows system clock example. When the sampling frequency is changed during normal operation (PMDAC bit = "1"), the DAC output should be soft-muted or "0" data should be input to avoid click noise.

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
8kHz	2.048	3.072	4.096	0.512
11.025kHz	2.8224	4.2336	5.6448	0.7056
12kHz	3.072	4.608	6.144	0.768
16kHz	4.096	6.144	8.192	1.024
22.05kHz	5.6448	8.4672	11.2896	1.4112
24kHz	6.144	9.216	12.288	1.536
32kHz	8.192	12.288	16.384	2.048
44.1kHz	11.2896	16.9344	22.5792	2.8224
48kHz	12.288	18.432	24.576	3.072

Table 1. System Clock Example

All external clocks (MCLK, BICK and LRCK) should always be present whenever the DAC is in normal operation mode (PMDAC bit = "1"). If these clocks are not provided, the AK4367 may draw excess current and will not operate properly because it utilizes these clocks for internal dynamic refresh of registers. If the external clocks are not present, the DAC should be placed in power-down mode (PMDAC bit = "0"). When MCLK is input with AC coupling, the MCKAC bit should be set to "1".

For low sampling rates, DR and S/N degrade because of the outband noise. DR and S/N are improved by setting DFS1 bit to "1". Table 2 shows S/N of DAC output for both the HP-amp and MOUT. When the DFS1 bit is "1", MCLK needs 512fs.

DFS1	DFS0	Over Sample Rate	fs	MCLK	S/N (fs=8kHz, A-weighted)		
					HP-amp	MOUT	
0	0	64fs	8kHz~48kHz	256fs/384fs/512fs	56dB	56dB	Default
0	1	128fs	8kHz~24kHz	256fs/384fs/512fs	75dB	75dB	
1	x	256fs	8kHz~12kHz	512fs	92dB	90dB	

Table 2. Relationship among fs, MCLK frequency and S/N of HP-amp and MOUT

■ Serial Data Interface

The AK4367 interfaces with external system via the SDATA, BICK and LRCK pins. Five data formats are available and are selected by setting DIF2, DIF1 and DIF0 bits (Table 3). Mode 0 is compatible with existing 16bit DACs and digital filters. Mode 1 is a 20bit version of Mode 0. Mode 4 is a 24bit version of Mode 0. Mode 2 is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In Modes 2 and 3 with BICK≥48fs, the following formats are also valid: 16-bit data followed by eight zeros (17th to 24th bits) and 20-bit data followed by four zeros (21st to 24th bits). In all modes, the serial data is MSB first and 2's complement format.

DIF2 bit	DIF1 bit	DIF0 bit	MODE	BICK	Figure	
0	0	0	0: 16bit, LSB justified	32fs ≤ BICK ≤ 64fs	Figure 10	
0	0	1	1: 20bit, LSB justified	40fs ≤ BICK ≤ 64fs	Figure 11	
0	1	0	2: 24bit, MSB justified	48fs ≤ BICK ≤ 64fs	Figure 12	Default
0	1	1	3: I^2S Compatible	BICK=32fs or 48fs ≤ BICK ≤ 64fs	Figure 13	
1	0	0	4: 24bit, LSB justified	48fs ≤ BICK ≤ 64fs	Figure 11	

Table 3. Audio Data Format

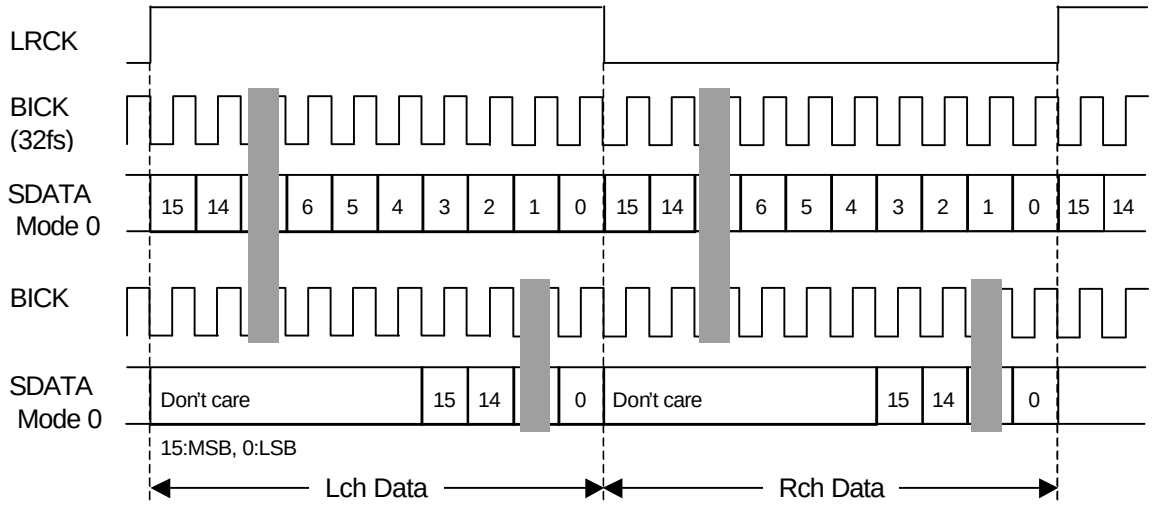


Figure 10. Mode 0 Timing

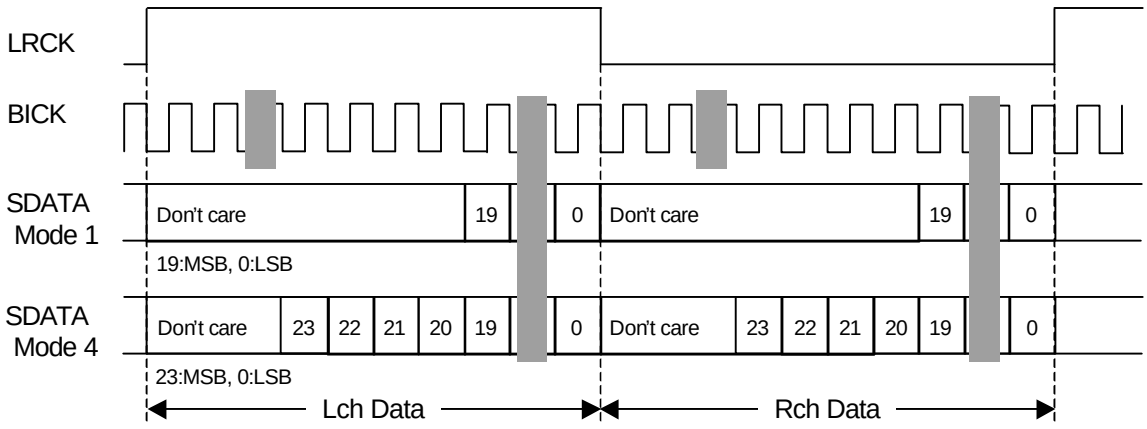


Figure 11. Mode 1, 4 Timing

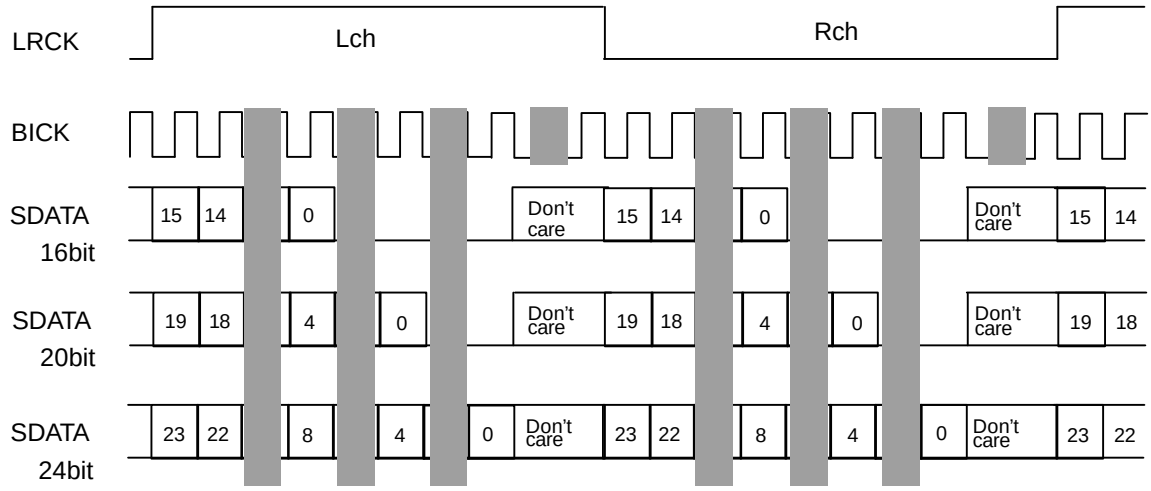


Figure 12. Mode 2 Timing

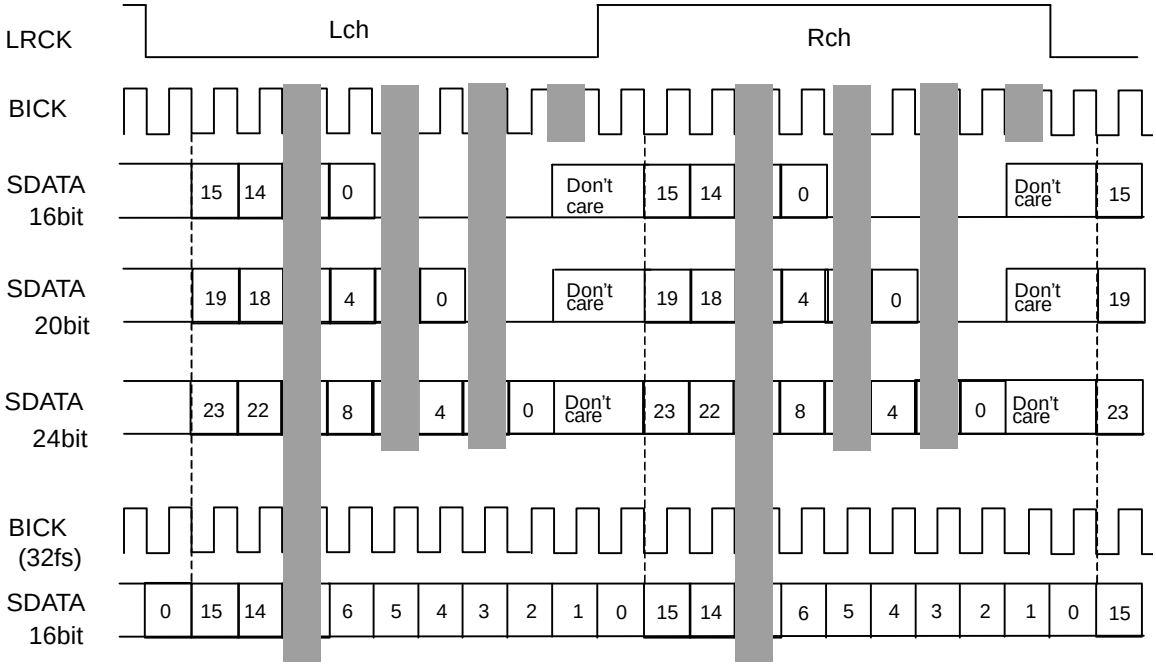


Figure 13. Mode 3 Timing

■ Digital Attenuator

The AK4367 has a channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before the D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to -127dB or MUTE) for each channel (Table 4). At DATTC= "1", ATTL7-0 bits control both Lch and Rch attenuation levels. At DATTC= "0", ATTL7-0 bits control the Lch level and ATTR7-0 bits control the Rch level. When HPM= "1", (L+R)/2 summation is done after volume control.

ATTL7-0 ATTR7-0	Attenuation	
FFH	0dB	
FEH	–0.5dB	
FDH	–1.0dB	
FCH	–1.5dB	
:	:	
:	:	
02H	–126.5dB	
01H	–127.0dB	
00H	MUTE (–∞)	Default

Table 4. Digital Volume ATT values

The ATS bit sets the transition time between set values of ATT7-0 bits as either 1061/fs or 7424/fs (Table 5). When ATS= "0", a soft transition between the set values occurs(1062 levels). It takes 1061/fs (24ms@fs=44.1kHz) from FFH(0dB) to 00H(MUTE). The ATTs are 00H when the PMDAC bit is "0". When the PMDAC returns to "1", the ATTs fade to their current value. Digital attenuator is independent of the soft mute function.

ATS	ATT speed		
	0dB to MUTE	1 step	
0	1061/fs	4/fs	Default
1	7424/fs	29/fs	

Table 5. Transition time between set values of ATT7-0 bits

MOUT volume is controlled by ATTM3-0 bits when MMUTE= "0" (Table 6). Click noise occurs when ATT3-0 bits are changed.

MMUTE	ATTM3-0	Attenuation	
0	0FH	0dB	
	0EH	–2dB	
	0DH	–4dB	
	0CH	–6dB	
	:	:	
	:	:	
	01H	–28dB	
	00H	–30dB	
1	x	MUTE	Default

Table 6. MOUT Volume ATT values

■ Soft Mute

Soft mute operation is performed at digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 5) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

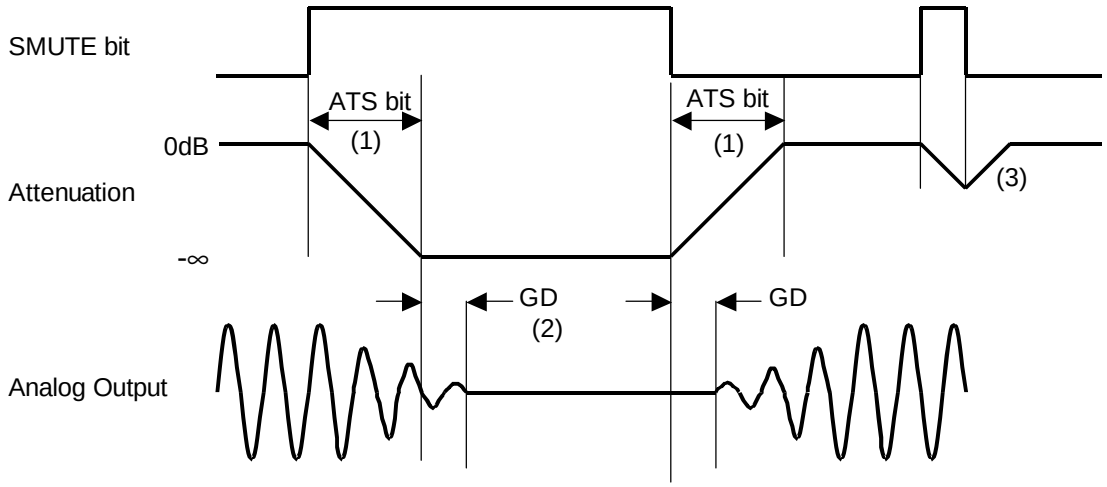


Figure 14. Soft Mute Function

Notes:

(1) ATT_DATA×ATT transition time (Table 5. Transition time between set values of ATT7-0 bits). For example, this time is 3712LRCK cycles (3712/fs) at ATT_DATA=128.

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

■ De-emphasis Filter

The AK4367 includes a digital de-emphasis filter (tc = 50/15μs) by IIR filter corresponding to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter is enabled by setting DEM1-0 bits (Table 7).

DEM1 bit	DEM0 bit	De-emphasis	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 7. De-emphasis Filter Frequency Select

■ Bass Boost Function

By controlling BST1-0 bits, the low frequency boost signal can be output from DAC. The setting value is common in Lch and Rch (Table 8).

BST1 bit	BST0 bit	BOOST	
0	0	OFF	Default
0	1	MIN	
1	0	MID	
1	1	MAX	

Table 8. Low Frequency Boost Select

■ System Reset

The AK4367 should be reset once by bringing PDN "L" upon power-up. After exiting reset, VCOM, DAC, HPL, HPR and MOUT switch to the power-down state. The contents of the control register are maintained until the reset is done.

DAC exits reset and power down state by MCLK after PMDAC bit is changed to "1", and then DAC is powered up and the internal timing starts clocking by LRCK "↑". DAC is in power-down mode until MCLK and LRCK are input.

■ Headphone Output

Power supply voltage for the Headphone-amp is supplied from the HVDD pin and centered on the MUTET voltage. The Headphone-amp output load resistance is min.16Ω. When the MUTEN bit is "1" at PMHPL=PMHPR= "1", the common voltage rises to 0.45 x VDD. When the MUTEN bit is "0", the common voltage of Headphone-amp falls and the outputs (HPL and HPR pins) go to VSS. A capacitor between the MUTET pin and ground reduces pop noise at power-up/down.

[Example] : A capacitor between the MUTET pin and ground = 1.0μF:
Time constant of rise/fall time: τ = 100ms

When PMHPL and PMHPR bits are "1", the Headphone-amp is powered-down, and the outputs (HPL and HPR pins) go to VSS.

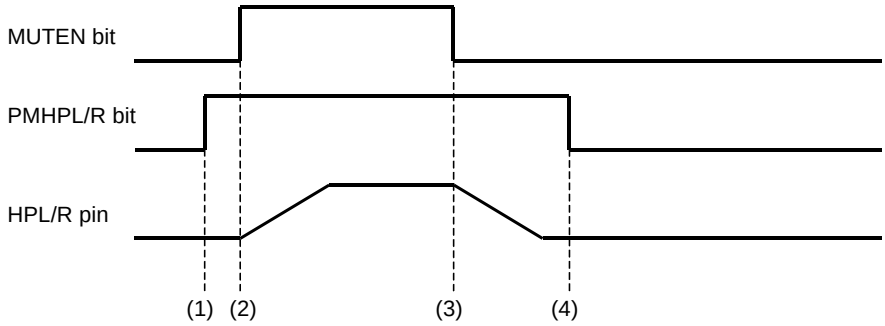


Figure 15. Power-up/Power-down Timing for Headphone-amp

(1) Headphone-amp power-up (PMHPL and PMHPR bits= "1"). The outputs are still VSS.
(2) Headphone-amp common voltage rise up (MUTEN bit= "1"). Common voltage of Headphone-amp is rising. This rise time depends on the capacitor value connected with the MUTET pin. The time constant is τ = 100k x C when the capacitor value on MUTET pin is "C".
(3) Headphone-amp common voltage fall down (MUTEN bit= "0"). Common voltage of Headphone-amp is falling to VSS. This fall time depends on the capacitor value connected with the MUTET pin. The time constant is τ = 100k x C when the capacitor value on MUTET pin is "C".
(4) Headphone-amp power-down (PMHPL, PMHPR bits= "0"). The outputs are VSS. If the power supply is switched off or Headphone-amp is powered-down before the common voltage goes to VSS, some POP noise occurs.

The cut-off frequency of Headphone-amp output depends on the external resistor and capacitor used. Table 9 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at HVDD = 2.4, 3.0 and 3.3V. The output voltage of headphone is 0.58 x VDD (Vpp)@-3dBFS.

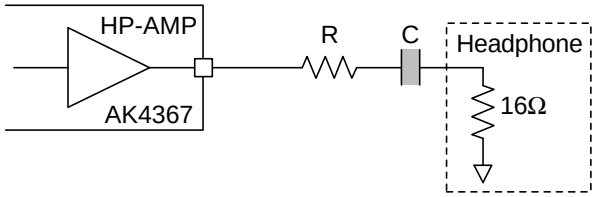


Figure 16. External Circuit Example of Headphone

R [Ω]	C [μF]	fc [Hz] BOOST=OFF	fc [Hz] BOOST=MIN	Output Power [mW]		
				2.4V	3.0V	3.3V
0	220	45	17	15	24	29
	100	100	43			
6.8	100	70	28	7	12	14
	47	149	78			
16	100	50	19	4	6	7
	47	106	47			

Table 9. Relationship of external circuit, output power and frequency response

■ Power-Up/Down Sequence

1) DAC → HP-amp

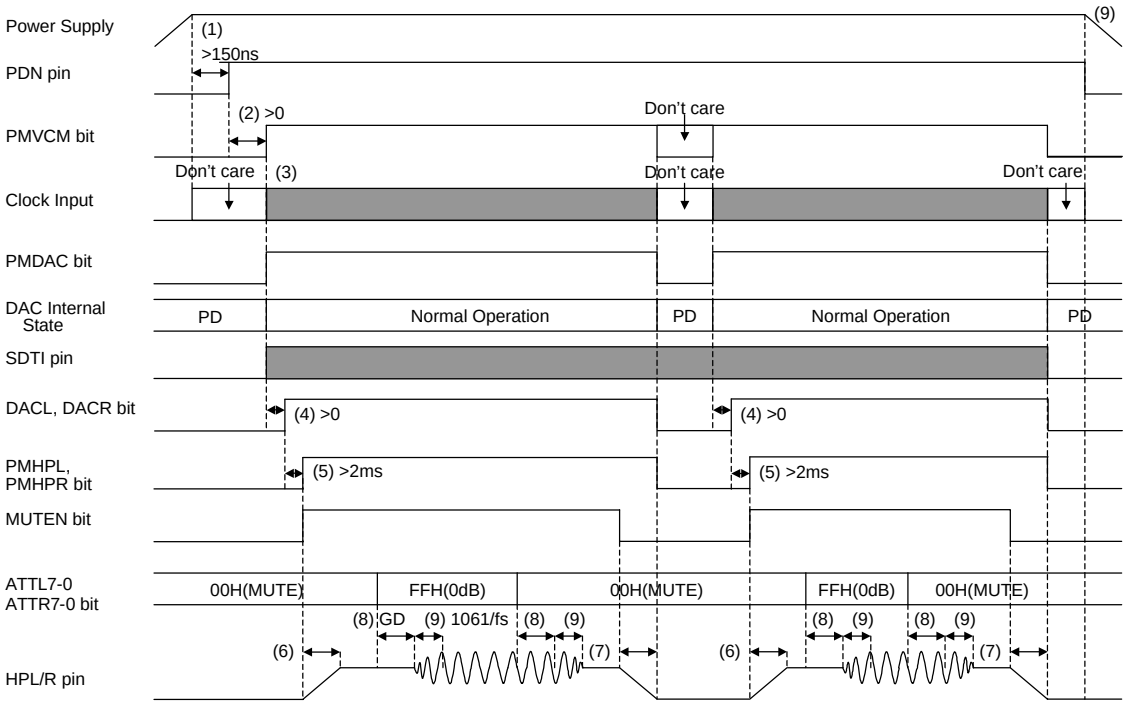


Figure 17. Power-up/down sequence of DAC and HP-amp

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) PMVCM and PMDAC bits should be changed to "1" after PDN pin goes to "H".
(3) External clocks (MCLK, BICK, LRCK) are needed to operate DAC. When PMDAC= "0", these clocks can be stopped. Headphone amp can operate without these clocks.
(4) DACL and DACR bits should be changed to "1" after PMDAC bit is changed to "1".
(5) PMHPL, PMHPR and MUTEN bits should be changed to "1" at least 2ms after DACL and DACR bits are changed to "1".
(6) Rise time of headphone amp is determined by external capacitor (C) of MUTET pin. Time constant is 100k x C. When C=1µF, time constant is 100ms.
(7) Fall time of headphone amp is determined by external capacitor (C) of MUTET pin. Time constant is 100k x C. When C=1µF, time constant is 100ms.
PMHPL, PMHPR, DACL and DACR bits should be changed to "0" after HPL and HPR pins go to VSS.
(8) Analog output corresponding to digital input has the group delay (GD) of 20.8/fs(=472µs@fs=44.1kHz).
(9) ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).
(10) Power supply should be switched off after headphone amp is powered down (HPL/R pins become "L").

2) DAC → MOUT

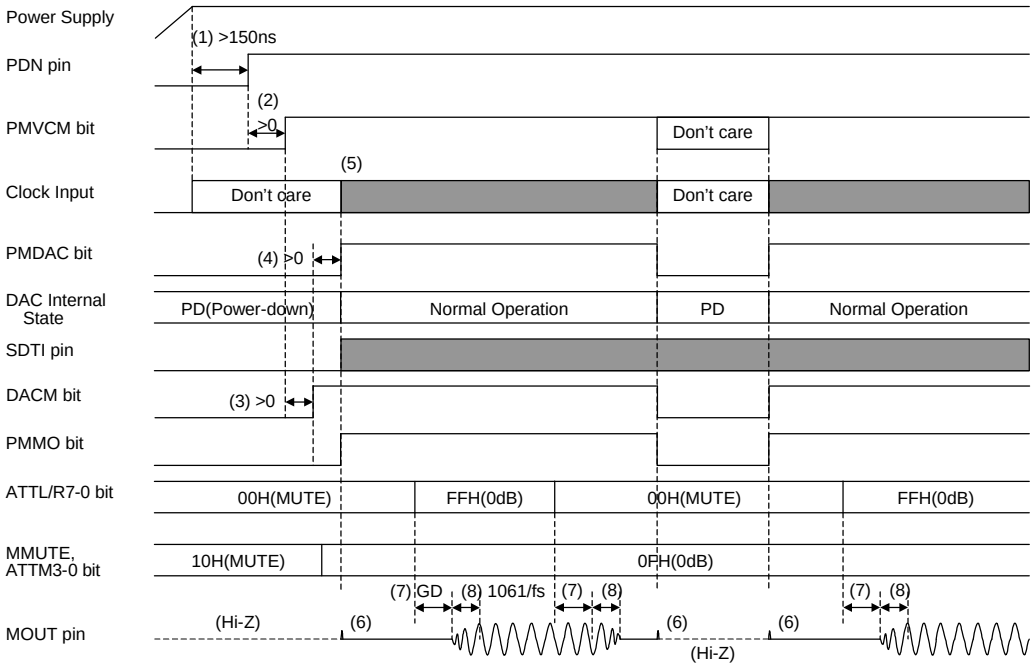


Figure 18. Power-up/down sequence of DAC and MOUT

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) PMVCM bit should be changed to "1" after PDN pin goes to "H".
(3) DACM bit should be changed to "1" after PMVCM bit is changed to "1".
(4) PMDAC and PMMO bits should be changed to "1" after DACM bit is changed to "1".
(5) External clocks (MCLK, BICK, LRCK) are needed to operate DAC. When PMDAC= "0", these clocks can be stopped. MOUT buffer can operate without these clocks.
(6) When PMMO bit is changed, click noise is output from MOUT pin.
(7) Analog output corresponding to digital input has the group delay (GD) of 20.8/fs(=472μs@fs=44.1kHz).
(8) ATS bit sets transition time of digital attenuator. Default value is 1061/fs(=24ms@fs=44.1kHz).

3) LIN/RIN/MIN → HP-amp, MOUT

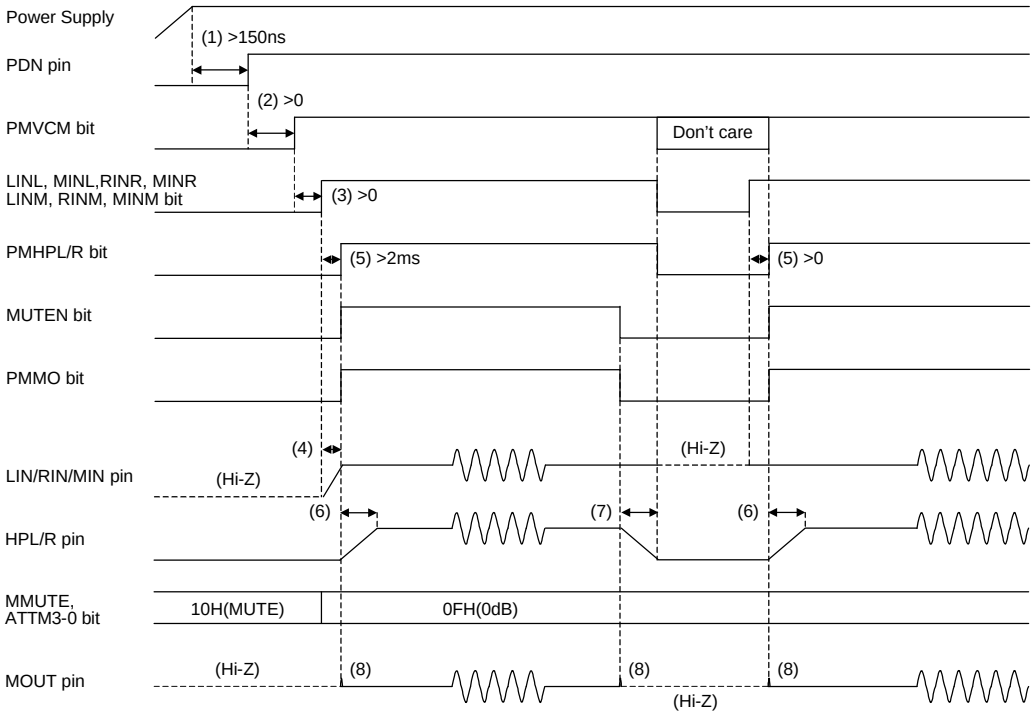


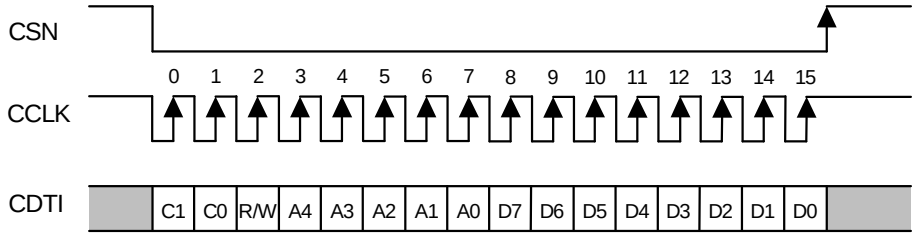
Figure 19. Power-up/down sequence of LIN/RIN/MIN, HP-amp and MOUT

(1) PDN pin should be set to "H" at least 150ns after the power is supplied.
(2) PMVCM bit should be changed to "1" after PDN pin goes to "H".
(3) LINL, MINL, RINR, MINR, LINM, RINM and MINM bits should be changed to "1" after PMVCM bit is changed to "1".
(4) When LINL, MINL, RINR, MINR, LINM, RINM or MINM bit is changed to "1", LIN, RIN or MIN pin is biased to 0.45 x VDD voltage.
(5) PMHPL, PMHPR, MUTEN and PMMO bits should be changed to "1" at least 2ms after LINL, MINL, RINR, MINR, LINM, RINM and MINM bits are changed to "1".
(6) Rise time of headphone amp is determined by external capacitor (C) of MUTET pin. Time constant is 100k x C. When C=1μF, time constant is 100ms.
(7) Fall time of headphone amp is determined by external capacitor (C) of MUTET pin. Time constant is 100k x C. When C=1μF, time constant is 100ms.
PMHPL, PMHPR, LINL, MINL, RINR, MINR, LINM, RINM and MINM bits should be changed to "0" after HPL and HPR pins go to VSS.
(8) When PMMO bit is changed, click noise is output from MOUT pin.

■ Serial Control Interface

(1) 3-wire Serial Control Mode (I2C pin = "L")

Internal registers may be written via to the 3 wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of Chip address (2bits, Fixed to "01"), Read/Write (1bit, Fixed to "1", Write only), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK. For write operations, data is latched after a low-to-high transition of CSN. The clock speed of CCLK is 5MHz(max). The value of internal registers is initialized at PDN= "L".



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 20. 3-wire Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")

The AK4367 supports the standard-mode I²C-bus (max: 100kHz). The AK4367 does not support a fast-mode I²C-bus system (max: 400kHz).

(2)-1. WRITE Operations

Figure 21 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 27). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next two bits are CAD1 and CAD0 (device address bits). These two bits identify the specific device on the bus. The hard-wired input pins (CAD1 and CAD0 pins) set these device address bits (Figure 22). If the slave address matches that of the AK4367, the AK4367 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 28). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4367. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 23). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 24). The AK4367 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 27).

The AK4367 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4367 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 08H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 29) except for the START and STOP conditions.

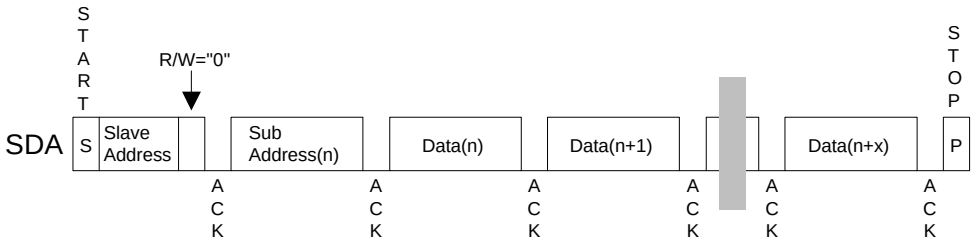


Figure 21. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	0	CAD0	R/W

(Those CAD0 should match with CAD0 pin)

Figure 22. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 23. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 24. Byte Structure after the second byte

(2)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4367. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 08H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4367 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ

The AK4367 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4367 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4367 ceases transmission.

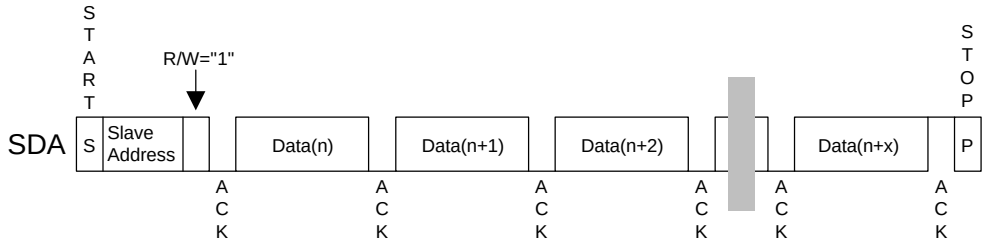


Figure 25. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK4367 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4367 ceases transmission.

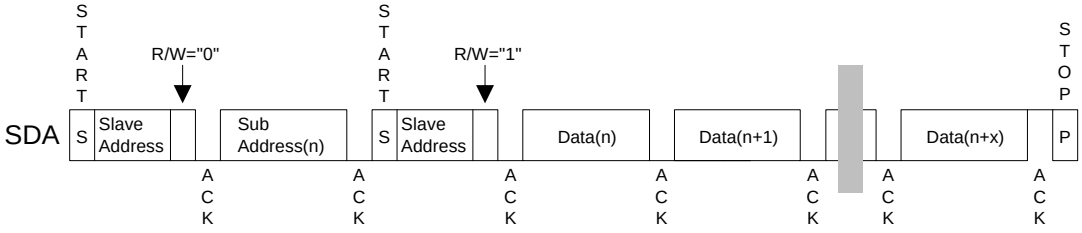


Figure 26. RANDOM ADDRESS READ

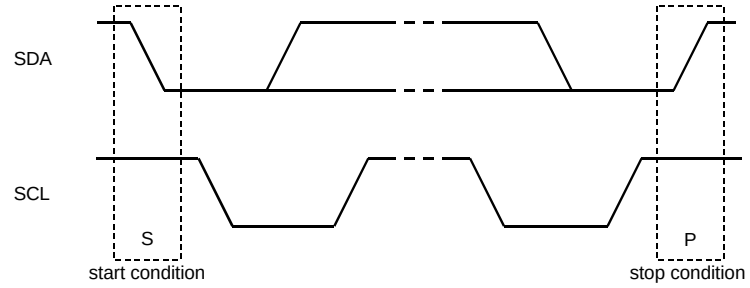


Figure 27. START and STOP Conditions

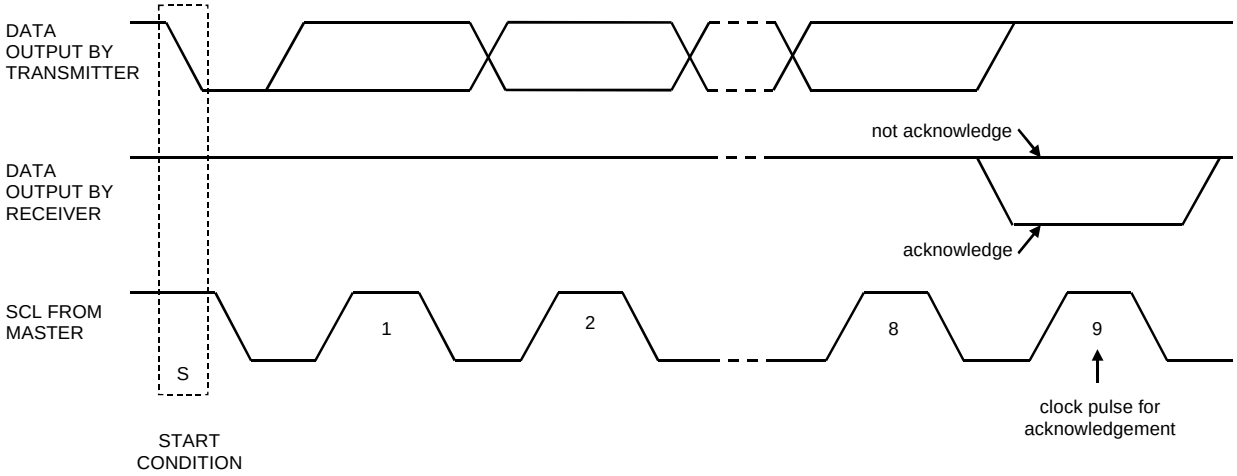


Figure 28. Acknowledge on the I^2C-Bus

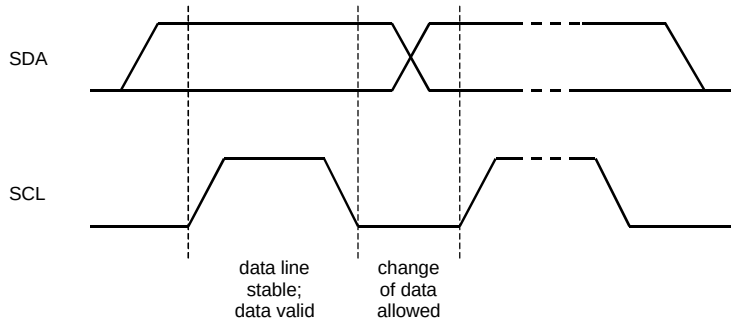


Figure 29. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	PMMO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
01H	Mode Control 0	0	MCKAC	HPM	DIF2	DIF1	DIF0	DFS1	DFS0
02H	Mode Control 1	0	0	MMUTE	SMUTE	BST1	BST0	DEM1	DEM0
03H	Mode Control 2	0	0	0	0	ATS	DATTC	BCKP	LRP
04H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
05H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
06H	Output Select 0	0	0	MINR	MINL	RINR	LINL	DACR	DACL
07H	Output Select 1	0	0	0	0	MINM	RINM	LINM	DACM
08H	MOUT ATT	0	0	0	0	ATTM3	ATTM2	ATTM1	ATTM0

All registers inhibit writing at PDN pin = "L".

For addresses from 09H to 1FH, data must not be written.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	PMMO	MUTEN	PMHPR	PMHPL	PMDAC	PMVCM
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCM: Power Management for VCOM Block
0: Power OFF (Default)
1: Power ON

PMDAC: Power Management for DAC Blocks
0: Power OFF (Default)
1: Power ON
When PMDAC bit is changed from "0" to "1", DAC is powered-up to the current register values (ATT value, sampling rate, etc).

PMHPL: Power Management for Lch of Headphone Amp
0: Power OFF (Default). HPL pin becomes VSS(0V).
1: Power ON

PMHPR: Power Management for Rch of Headphone Amp
0: Power OFF (Default). HPR pin becomes VSS(0V).
1: Power ON

MUTEN: Headphone Amp Mute Control
0: Mute (Default). HPL and HPR pins go to VSS(0V).
1: Normal operation. HPL and HPR pins go to 0.45 x VDD.

PMMO: Power Management for Mono Output
0: Power OFF (Default) MOUT pin becomes Hi-Z.
1: Power ON

All blocks can be powered-down by setting the PDN pin to "L" regardless of register values setup. All blocks can be also powered-down by setting all power management bits to "0". In this case, control register values are maintained.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Mode Control 0	0	MCKAC	HPM	DIF2	DIF1	DIF0	DFS1	DFS0
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

DFS1-0: Oversampling Speed Select (Table 2)
Default: "00" (64fs)

DIF2-0: Audio Data Interface Format Select (Table 3)
Default: "10" (Mode 2)

HPM: Mono Output Select of Headphone (Table 10)
0: Normal Operation (Default)
1: Mono. (L+R)/2 signals from the DAC are output to both Lch and Rch of headphone.

DACL	DACR	HPM	HPL pin Output	HPR pin Output	
0	0	x	No output from DAC	No output from DAC	Default
0	1	0	No output from DAC	Output from Rch of DAC by 0dB	
		1	No output from DAC	Output from Rch of DAC by –6dB	
1	0	0	Output from Lch of DAC by 0dB	No output from DAC	
		1	Output from Lch of DAC by –6dB	No output from DAC	
1	1	0	Output from Lch of DAC by 0dB	Output from Rch of DAC by 0dB	
		1	Output (L+R)/2 from DAC	Output (L+R)/2 from DAC	

Table 10. Mono Output Select of Headphone (x: Don't care)

MCKAC: MCLK Input Mode Select
0: CMOS input (Default)
1: AC coupling input

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Mode Control 1	0	0	MMUTE	SMUTE	BST1	BST0	DEM1	DEM0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis Filter Frequency Select (Table 7)
Default: "01" (OFF)

BST1-0: Low Frequency Boost Function Select (Table 8)
Default: "00" (OFF)

SMUTE: Soft Mute Control
0: Normal operation (Default)
1: DAC outputs soft-muted

MMUTE: Mute control for MOUT (Table 6)
0: Normal operation. ATTM3-0 bits control attenuation value.
1: Mute. ATTM3-0 bits are ignored. (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 2	0	0	0	0	ATS	DATTC	BCKP	LRP
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LRP: LRCK Polarity Select
0: Normal
1: Invert

BCKP: BICK Polarity Select
0: Normal
1: Invert

DATTC: DAC Digital Attenuator Control Mode Select
0: Independent (Default)
1: Dependent
At DATTC= "1", ATTL7-0 bits control both Lch and Rch attenuation level, while register values of ATTL7-0 bits are not written to ATTR7-0 bits. At DATTC= "0", ATTL7-0 bits control Lch level and ATTR7-0 bits control Rch level.

ATS: Digital attenuator transition time setting (Table 5)
Default: "00" (1061/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
05H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTL7-0: Setting of the attenuation value of output signal from DACL (Table 4)
ATTR7-0: Setting of the attenuation value of output signal from DACR (Table 4)
Default: "00H" (MUTE)

The AK4566 has channel-independent digital attenuator (256 levels, 0.5dB step). This digital attenuator is placed before D/A converter. ATTL/R7-0 bits set the attenuation level (0dB to -127dB or MUTE) of each channel. Digital attenuator is independent of soft mute function.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Output Select 0	0	0	MINR	MINL	RINR	LINL	DACR	DACL
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACL: DAC Lch output signal is added to Lch of headphone amp.
0: OFF (Default)
1: ON

DACR: DAC Rch output signal is added to Rch of headphone amp.
0: OFF (Default)
1: ON

LINL: Input signal to LIN pin is added to Lch of headphone amp.
0: OFF (Default)
1: ON

RINR: Input signal to RIN pin is added to Rch of headphone amp.
0: OFF (Default)
1: ON

MINL: Input signal to MIN pin is added to Lch of headphone amp.
0: OFF (Default)
1: ON

MINR: Input signal to MIN pin is added to Rch of headphone amp.
0: OFF (Default)
1: ON

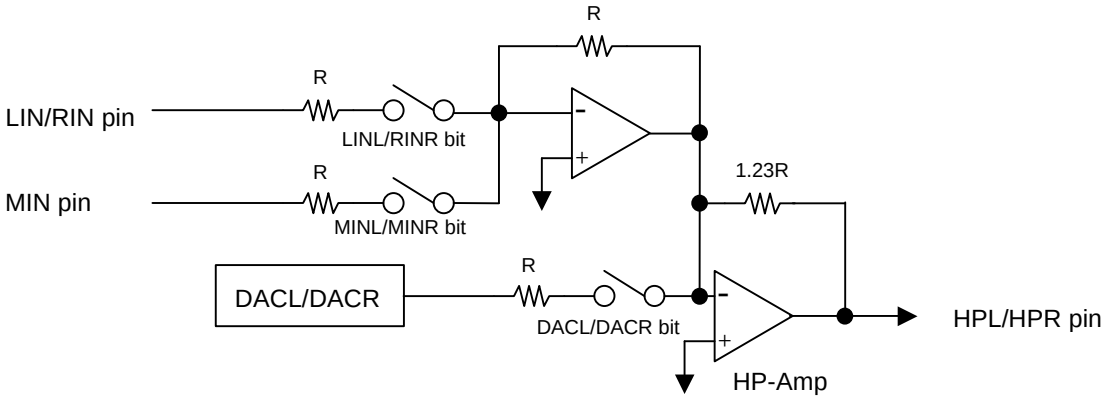


Figure 30. Summation circuit for headphone amp output

At HPM=0, gain of summation is +1.8dB for all input path.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Output Select 1	0	0	0	0	MINM	RINM	LINM	DACM
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DACM: DAC Lch and Rch outputs are added to MOUT buffer amp. Summation gain is -6dB for each channel.
0: OFF (Default)
1: ON

LINM: Input signal to LIN pin is added to MOUT buffer amp.
0: OFF (Default)
1: ON

RINM: Input signal to RIN pin is added to MOUT buffer amp.
0: OFF (Default)
1: ON

MINM: Input signal to MIN pin is added to MOUT buffer amp.
0: OFF (Default)
1: ON

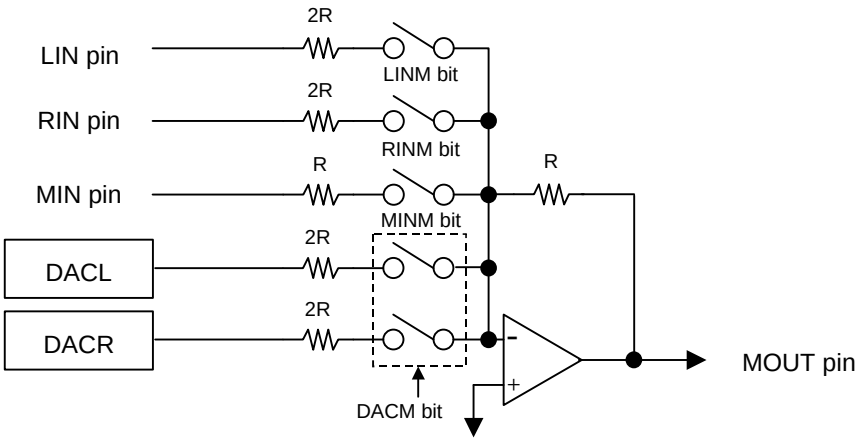


Figure 31. Summation circuit for MOUT

Gain of summation is 0dB for MIN and -6dB for LIN, RIN, DACL and DACR.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	MOUT ATT	0	0	0	0	ATTM3	ATTM2	ATTM1	ATTM0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATTM3-0: Analog volume control for MOUT (Table 6)
Default: MMUTE= “1”, ATTM3-0= “0000” (MUTE)

Setting of ATTM3-0 bits is enabled at MMUTE bit is “0”.

SYSTEM DESIGN

Figure 32 shows the system connection diagram. An evaluation board [AKD4367] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

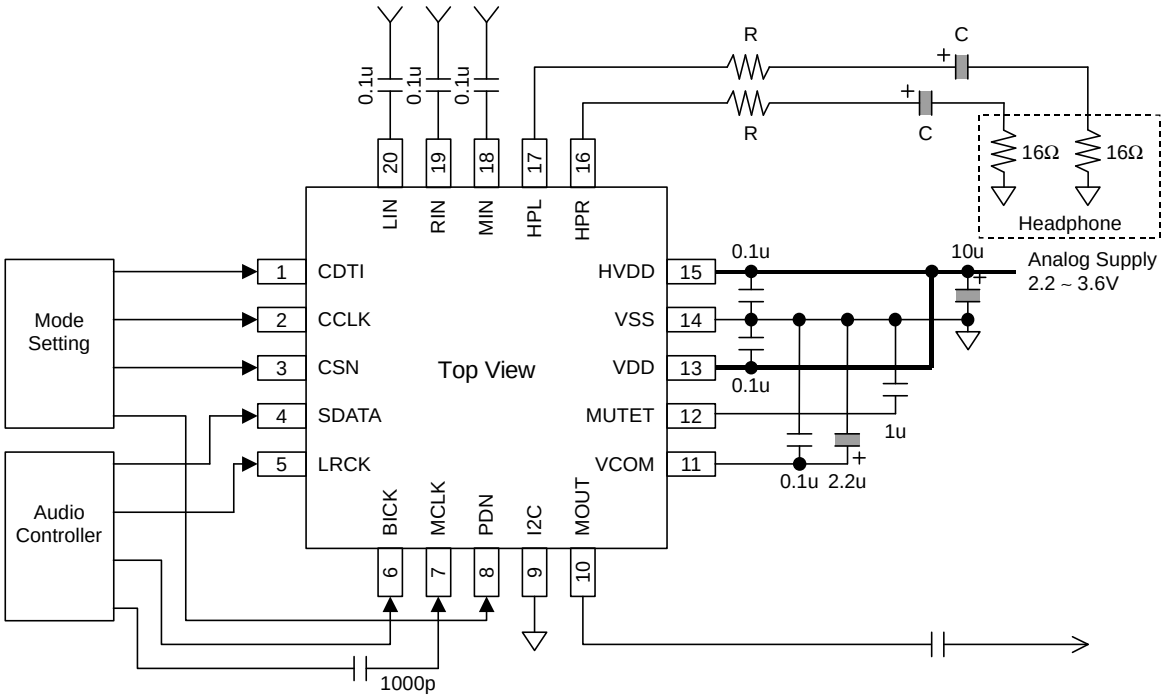


Figure 32. Typical Connection Diagram (In case of AC coupling to MCLK)
(3-wire serial mode)

1. Grounding and Power Supply Decoupling

The AK4367 requires careful attention to power supply and grounding arrangements. VDD and HVDD are usually supplied from the analog power supply in the system. When VDD and HVDD are supplied separately, VDD must be powered-up at the same time or earlier than HVDD. When the AK4367 is powered-down, HVDD must be powered-down at the same time or later than VDD. VSS must be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close to the AK4367 as possible, with the small value ceramic capacitors being the nearest.

2. Voltage Reference

The input voltage to VDD pin sets the analog output range. A 0.1μF ceramic capacitor and a 10μF electrolytic capacitor is connected between VDD and VSS pins, normally. VCOM is a signal ground of this chip (0.45 x VDD). An electrolytic 2.2μF in parallel with a 0.1μF ceramic capacitor attached between VCOM and VSS pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clock, should be kept away from VDD and VCOM pins in order to avoid unwanted coupling into the AK4367.

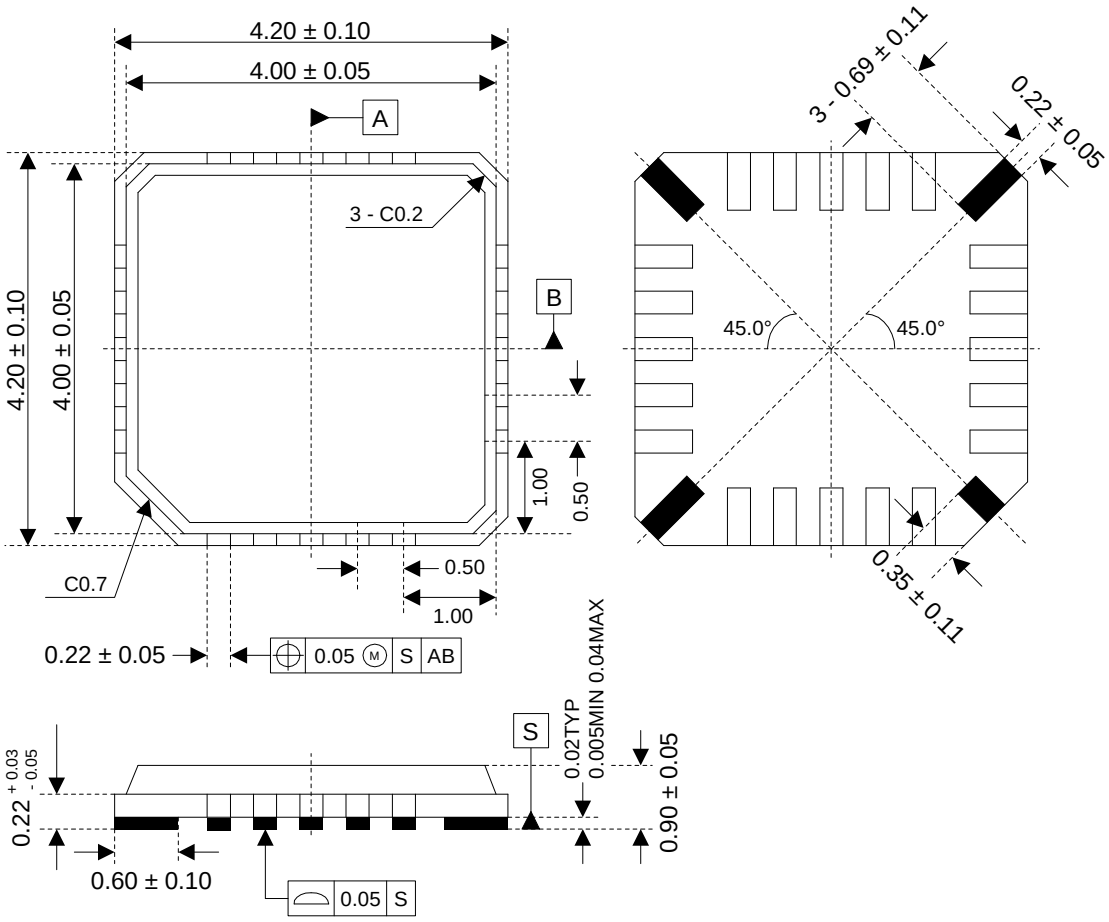
3. Analog Outputs

The analog outputs are single-ended outputs, and 0.58xVDD Vpp(typ)@-3dBFS for headphone amp and 0.66xVDD Vpp(typ) for MOUT centered on the VCOM voltage. The input data format is 2's compliment. The output voltage is a positive full scale for 7FFFFFH(@24bit) and negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). If the noise generated by the delta-sigma modulator beyond the audio band causes problems, attenuation by an external filter is required.

DC offsets on the analog outputs is eliminated by AC coupling since the analog outputs have a DC offset equal to VCOM plus a few mV.

PACKAGE

20pin QFN (Unit: mm)

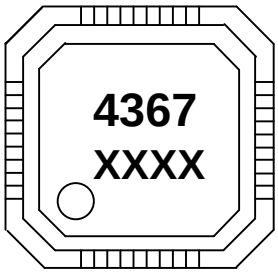


Note: The black parts of back package should be open.

■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXX : Date code identifier (4 digits)

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