Matched N-Channel JFET Pairs

Product Summary

Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (pA)	$\|V_{GS1} - V_{GS2}\|$ Typ (mV)
U430	–1 to –4	–25	10	–15	25
U431	–2 to –6	–25	10	–15	25

Features

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 15 pA
- Low Noise
- High CMRR: 75 dB

Benefits

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signals

Applications

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters

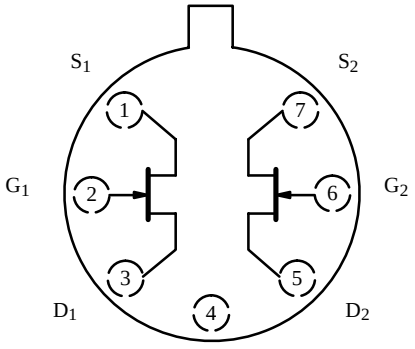
Description

The U430/431 are matched JFET pairs assembled in a TO-78 package. These devices offer good power gain even at frequencies beyond 250 MHz.

The TO-78 package is available with full military processing (see Military Information).

For similar products, see the low-noise U/SST401 series, the high-gain 2N5911/5912, and the low-leakage U421/423 data sheets.

TO-78



Case
Top View

Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 10 mA
Lead Temperature ($^1/_{16}$" from case for 10 sec.) . . . . . 300 °C
Storage Temperature . . . . . –65 to 200°C
Operating Junction Temperature . . . . . –55 to 150°C

Power Dissipation :
Per Side[a] . . . . . 300 mW
Total[b] . . . . . 500 mW

Notes
a. Derate 2.4 mW/°C above 25°C
b. Derate 4 mW/°C above 25°C

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70249.

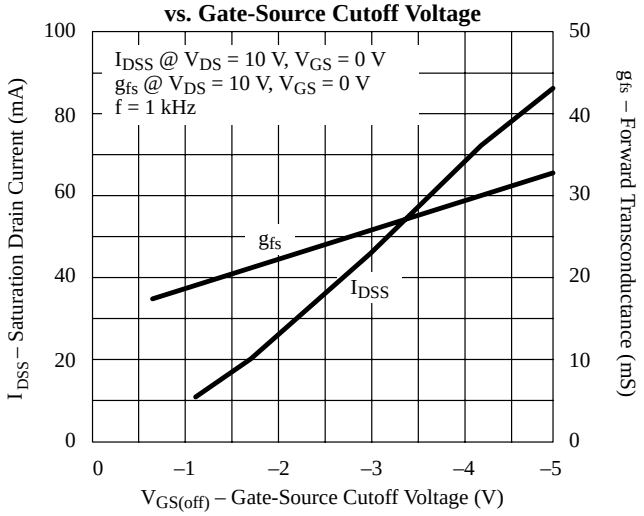
Specifications[a]

Parameter	Symbol	Test Conditions	Typ[b]	Limits U430 Min	Limits U430 Max	Limits U431 Min	Limits U431 Max	Unit
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 µA, V_{DS} = 0 V	–35	–25		–25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 nA		–1	–4	–2	–6	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 10 V, V_{GS} = 0 V		12	30	24	60	mA
Gate Reverse Current	I_{GSS}	V_{GS} = –15 V, V_{DS} = 0 V	–5		–150		–150	pA
		T_A = 150°C	–10		–150		–150	nA
Gate Operating Current	I_G	V_{DG} = 10 V, I_D = 5 mA	–15					pA
		T_A = 150°C	–10					nA
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 10 mA , V_{DS} = 0 V	0.8		1		1	V
Dynamic								
Common-Source Forward Transconductance[c]	g_{fs}	V_{DS} = 10 V, I_D = 10 mA , f = 1 kHz	15	10		10		mS
Common-Source Output Conductance[c]	g_{os}		100		250		250	µS
Common-Source Input Capacitance	C_{iss}	V_{GS} = –10 V, V_{DS} = 0 V, f = 1 MHz	4.5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2		2.5		2.5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, I_D = 10 mA f = 100 Hz	6					$nV/\sqrt{Hz}$
High Frequency								
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 10 mA f = 100 MHz	14					mS
Common-Source Output Conductance	g_{os}		0.13					
Power-Match Source Admittance	g_{ig}		12					
Matching								
Differential Gate-Source Voltage	$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 10 mA	25					mV
Saturation Drain Current Ratio[d]	$\frac{I_{DSS1}}{I_{DSS2}}$	V_{DS} = 10 V, V_{GS} = 0 V	0.95	0.9	1	0.9	1	
Transconductance Ratio[d]	$\frac{g_{fs1}}{g_{fs2}}$	V_{DS} = 10 V, I_D = 10 mA, f = 1 kHz	0.95	0.9	1	0.9	1	
Gate-Source Cutoff Voltage Ratio[d]	$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	V_{DS} = 10 V, I_D = 1 nA	0.95	0.9	1	0.9	1	
Differential Gate Current	$\lvert I_{G1}-I_{G2}\rvert$	V_{DG} = 10 V, I_D = 5 mA	–2					pA
Common Mode Rejection Ratio	CMRR	V_{DG} = 5 to 10 V, I_D = 10 mA	75					dB

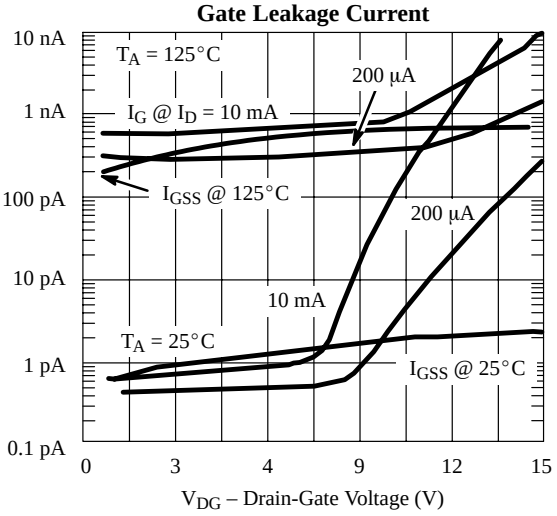
Notes
a. T_A = 25°C unless otherwise noted. NZBD
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Pulse test: PW ≤ 300 µs duty cycle ≤ 3%.
d. Assumes smaller value in the numerator.

Typical Characteristics

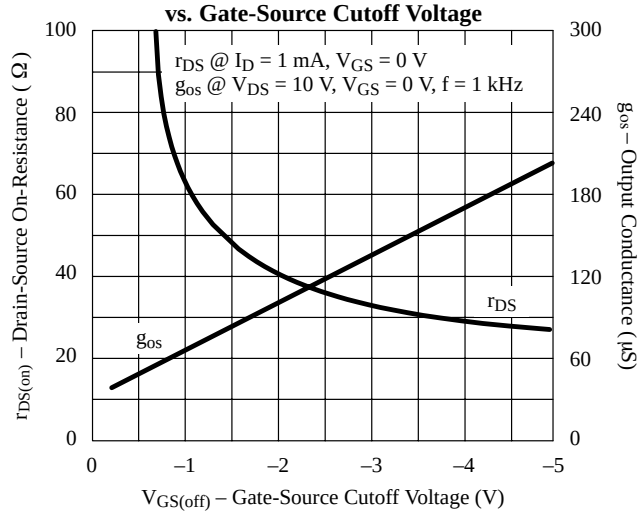
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



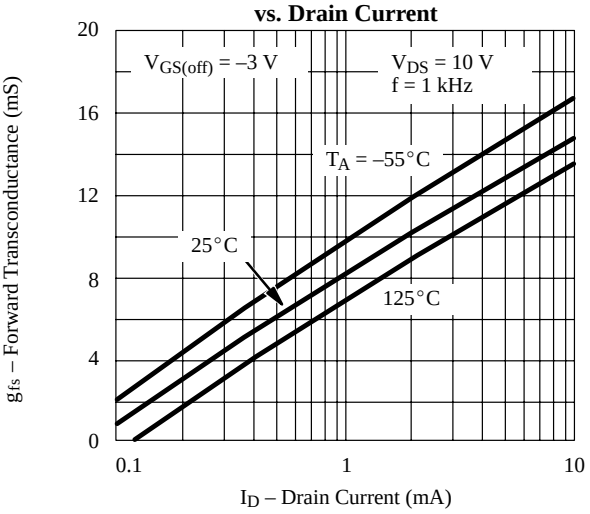
Gate Leakage Current



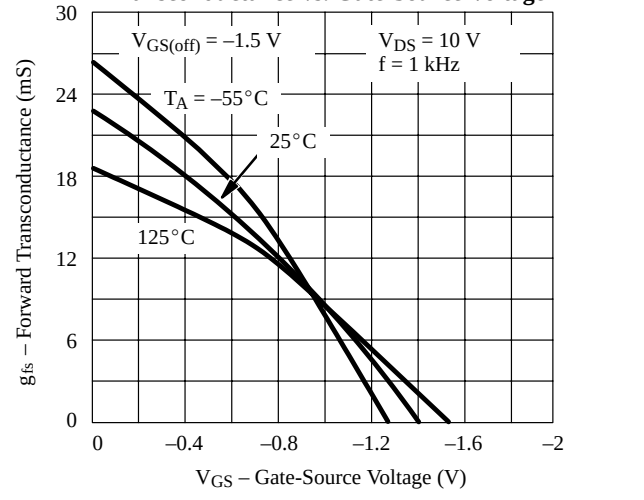
On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



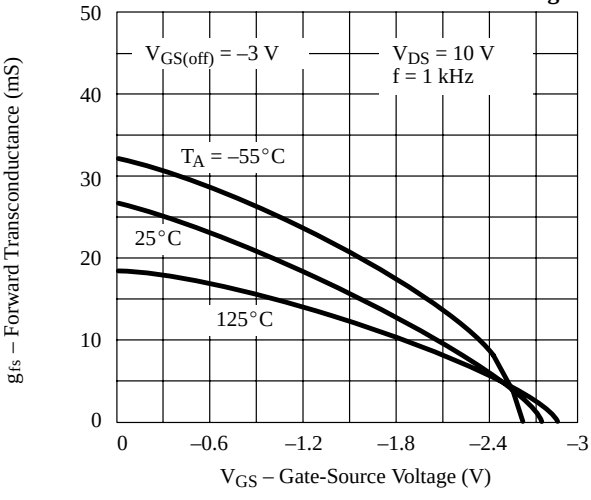
Common-Source Forward Transconductance vs. Drain Current



Transconductance vs. Gate-Source Voltage

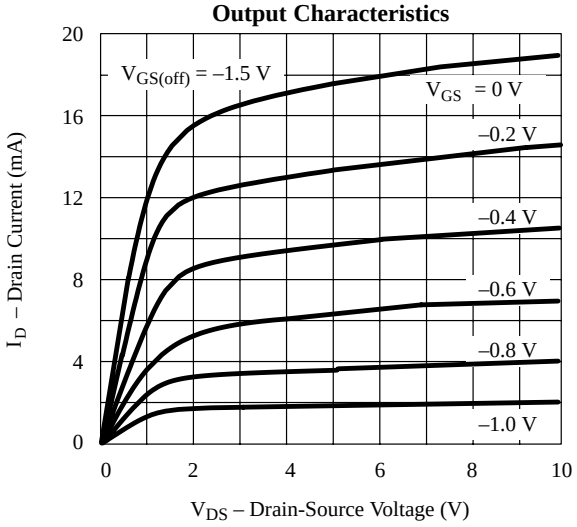


Transconductance vs. Gate-Source Voltage

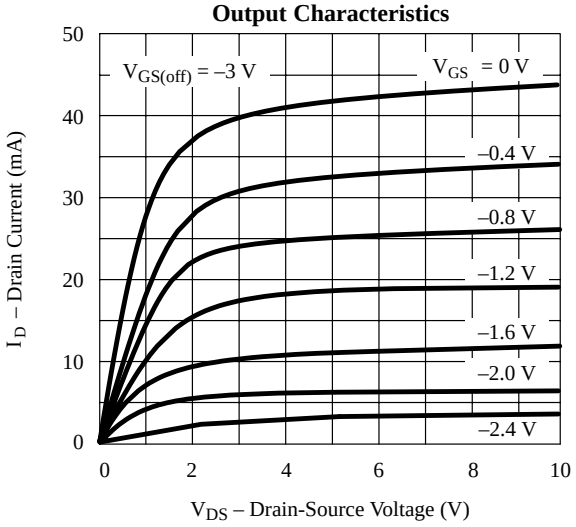


Typical Characteristics (Cont'd)

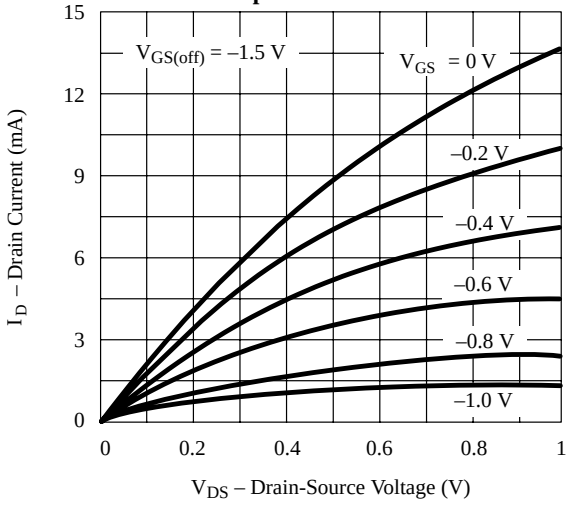
Output Characteristics



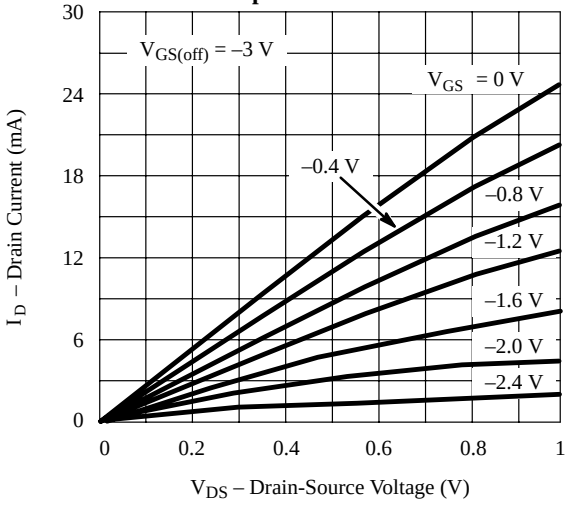
Output Characteristics



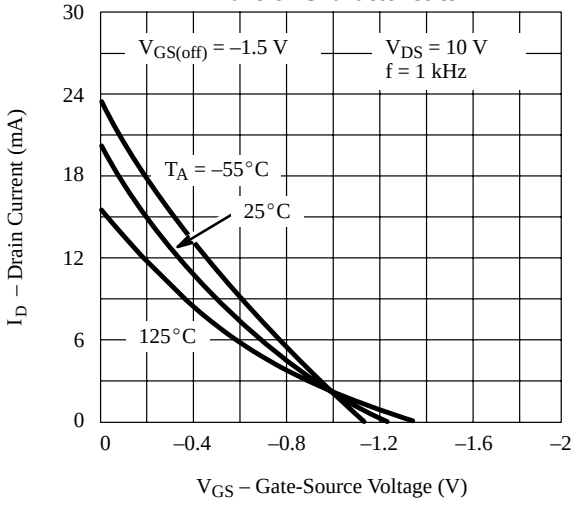
Output Characteristics



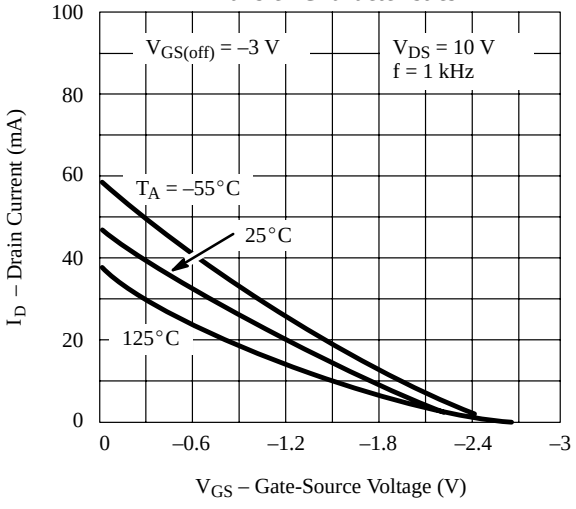
Output Characteristics



Transfer Characteristics

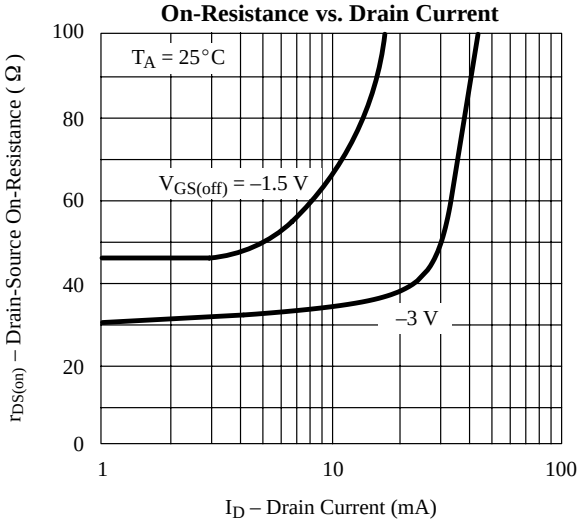


Transfer Characteristics

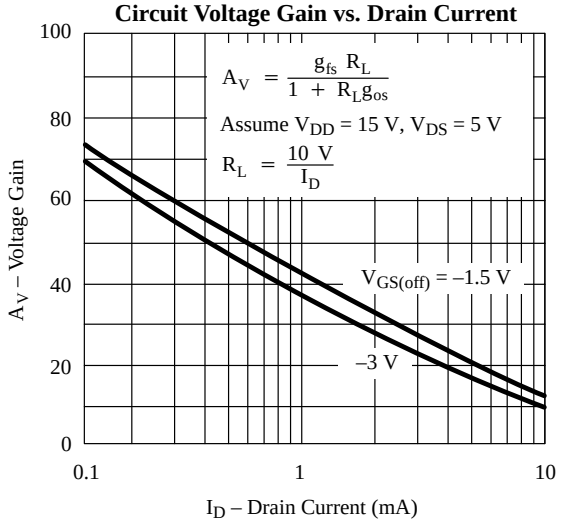


Typical Characteristics (Cont'd)

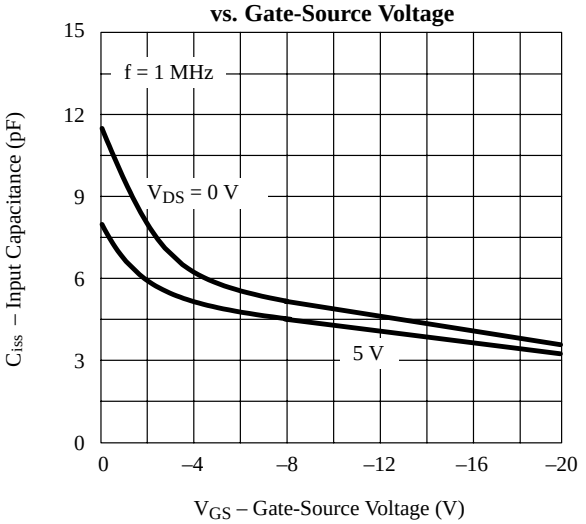
On-Resistance vs. Drain Current



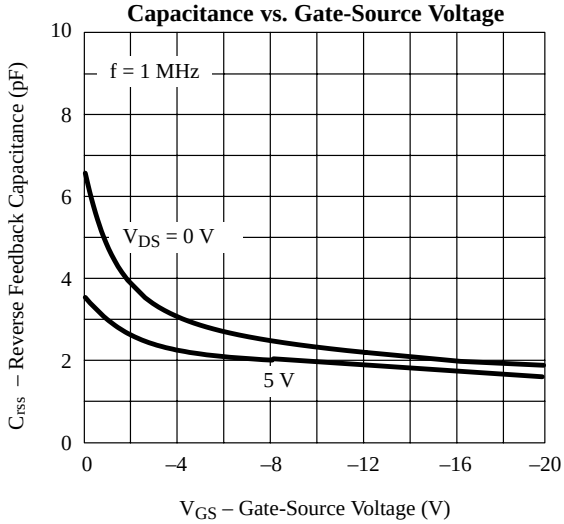
Circuit Voltage Gain vs. Drain Current



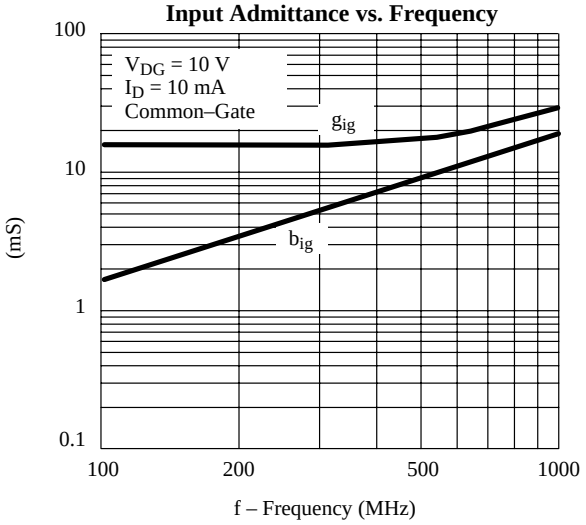
Common-Source Input Capacitance vs. Gate-Source Voltage



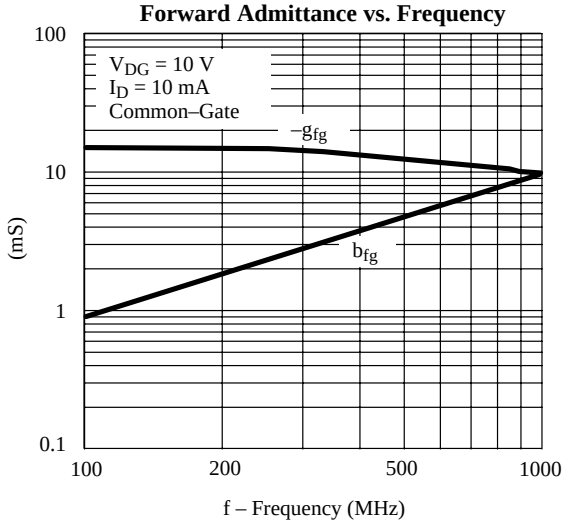
Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage



Input Admittance vs. Frequency

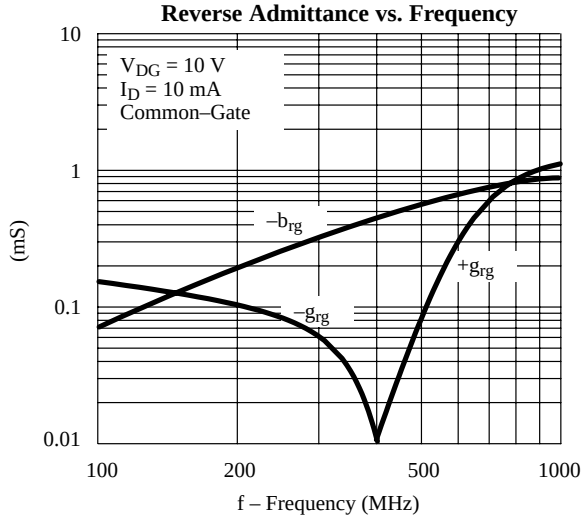


Forward Admittance vs. Frequency

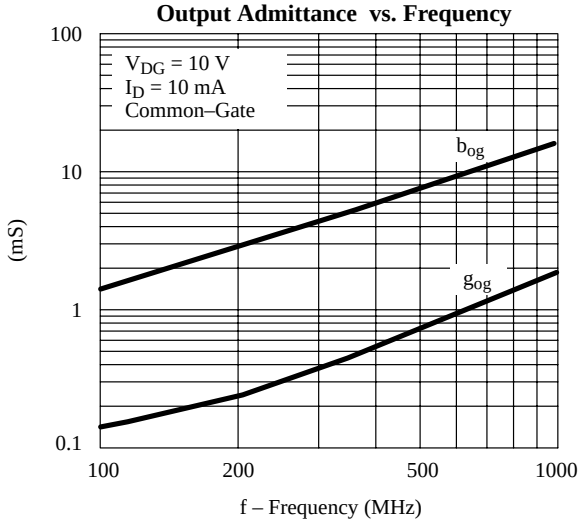


Typical Characteristics (Cont'd)

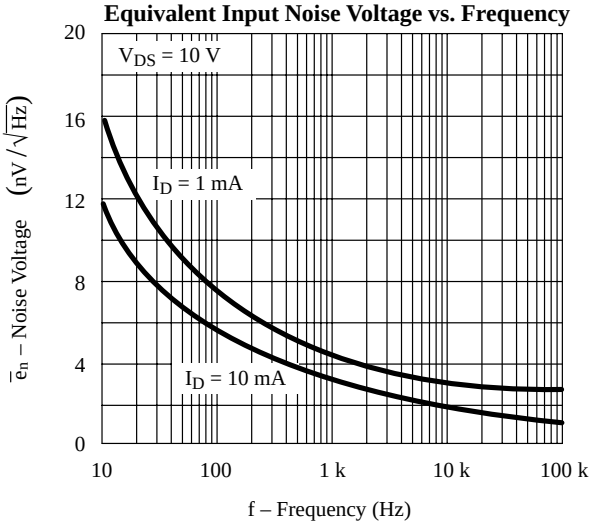
Reverse Admittance vs. Frequency



Output Admittance vs. Frequency



Equivalent Input Noise Voltage vs. Frequency



Output Conductance vs. Drain Current