LSI LOGIC
CORPORATION

1551 McCarthy Blvd.
Milpitas, CA 95035
(408) 433-8000
Telex 172153

L64745
JPEG CODER

ADVANCE INFORMATION

GENERAL DESCRIPTION

The IVLC is a variable length encoder-decoder used to implement the quantization, zig-zag run length coding and the variable length coding and decoding of events as specified in the proposed baseline JPEG standard. The device includes four quantization tables and two AC and DC variable length coding tables.

When encoding, the processor will accept 11-bit DCT coefficients as generated by the L64735 or similar device. The coefficients are quantized, coded and buffered into 32-bit words. An 32-word output fifo makes it possible to read the data in bursts. The device can encode one event per cycle making it possible to cascade the IVLC with the DCT (DCT processor) for high-speed image compression systems.

When decoding, the device accepts 32-bit words from the buffer and decodes the events and reconstructs the DCT coefficients which are output in format suitable for processing by the L64735.

The encoding and decoding operations can process one pixel and/or event each cycle and will not limit the processing rates of a pipelined image compression system.

The device can also be used to perform the lossless (two-dimensional) DPCM coding excluding the two-dimensional prediction.

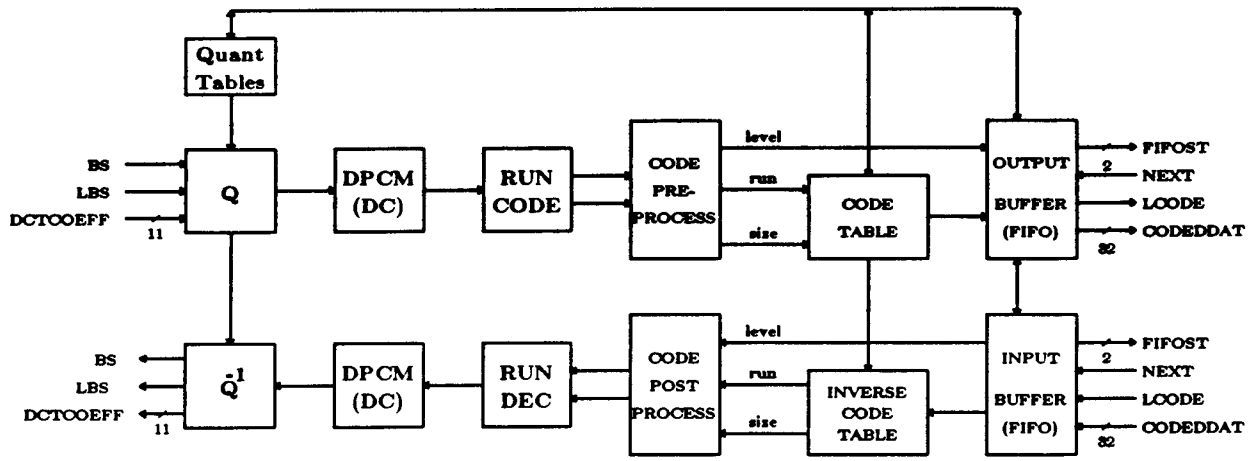
FEATURES

- Compatible with Proposed JPEG Standard
- Performs Quantization, Run Coding and Variable Length Coding
- 32-word Coded Data FIFO
- Two Downloaded AC and DC Code Tables
- Four Downloaded Quantization Tables
- Can be Cascaded with DCT in Encoder and Decoder Modes
- Can be Used in non-JPEG Systems
- 20/27 MHz Data Rates
- 68-pin PGA or PLCC

IVLC PIN LISTING AND DESCRIPTION

DCTCOEFF.10:0	11-bit DCT coefficient I/O bus. In encoder mode, the DCT coefficients to be coded are input on this bus. In decoder mode, the reconstructed DCT coefficients are output on this bus.
BS	Block Start I/O. Used to indicate the beginning of a new block of input or output DCT coefficients on the DCTCOEFF bus.
LBS	Last Block Start I/O. Used to indicate the beginning of the last block (of the image) of input or output DCT coefficients on the DCTCOEFF bus.
CODEDDAT.31:0	32-bit CODED DATA I/O bus. This is the coded data going to or from the FIFO.
LCODE	Last CODE I/O. When HIGH indicates that the last word of coded data is being input or output on the CODEDDAT bus.
FIFOST.1:0	2-bit FIFO STatus output indicator. Used to indicate the internal FIFO is either empty, low and full. The threshold for low can be set by the user.
NEXT	When HIGH, causes the FIFO to output the next data word in encoder mode or to accept the next data word in decoder mode. In initialization mode (INIT HIGH), NEXT causes the next 8 or 16 bit word of the operating parameters to be output or accepted on the CODEDDAT bus.
HIGH16	Only used when the internal control bit, 32BIT is LOW. When HIGH, indicates that the HIGH (or most significant) 16-bits of a coded data word are being input or output on the CODEDDAT.15:0 pins. Otherwise, the least significant 16-bits of a word are accessed on these pins. Has no effect when INIT is HIGH.
RW	Read-Write Select input. When HIGH and INIT is HIGH, the internal control, code table and quantization table values can be read from the CODEDDAT bus. When LOW and INIT is HIGH, the values on the CODEDDAT bus is loaded into the device.
INIT	When HIGH, the data in the internal control registers, quantization tables and code tables can be written or read. When LOW, the device is normal encoding or decoding mode.
RESET	Resets the device to begin processing a new image frame. The coded data buffers are cleared at this time.
CLK	System Clock. Controls the positive edge triggered data latches and pipeline registers.
OEN	Output ENable. When HIGH, the DCTCOEFF and CODEDDAT busses and SYNC are enabled. When OEN is LOW, the signals float.
TESTO	Test output. Should be left unconnected.

IMAGE VARIABLE LENGTH CODER BLOCK DIAGRAM



ARCHITECTURE DESCRIPTION

There are two primary functional blocks within the IVLC: the encoder and the decoder. Only one functional block is active at any given time.

The encoder consists of the quantizer (Q), the DC predictor (DPCM), the run coder, the code preprocess block, the code table and the output buffer. The block of DCT coefficients is input in zig-zag format (as generated by the L64735). The DCT coefficients are quantized using the frequency dependent quantization step sizes stored in one of the two quantization tables. The quantized DC coefficients are coded using a DPCM scheme. The data is then run length coded to for events (consisting of a run and a level). The events are preprocessed to determine the size of the level information which indicates the number of useful (and stored) bits in the level field. The code words for the combination of run and size are stored in the CODE TABLE. This variable length code word is then combined with useful bits of level and packed into 32-bit words by the output buffer. The output buffer operates as a 32-word FIFO, allowing some number words to collect before being read. The FIFOST bits are used to indicate the status of the buffer, including: overflow, ready, empty, not_ready. The user can set the threshold for ready/not_ready to be any value between 0 and 31. If is important that the buffer not be allowed to overflow as data will be lost.

The CODEDDAT bus width was chosen to be 32-bits to guarantee that in the worst case, the IVLC can process each DCT coefficient in one clock cycle. This makes it possible for the DCT and IVLC to be cascaded in a pipeline system.

The decoder operations are performed in the reverse order of those in encoder mode. Data is accepted into the INPUT BUFFER in 32-bit words over the CODEDDAT I/O bus. For this case, the FIFOST bits indicate the states: ready, not_ready, underflow and full. The system is responsible to supply data such that underflow of the fifo does not occur.

The INVERSE CODE TABLE is used to decode the run and size information. The level information is then extracted from the INPUT BUFFER and combined with the run and size information to reconstruct the events. The events are decoded into a block of quantized coefficients. The inverse quantizer generates the reconstructed DCT coefficients which are buffered and output in a contiguous block of 64 coefficients.

The user must load the parameters describing the number of components, sampling ratios and the tables to be used for each component. The processor will than automatically select the proper quantization and code tables for each data block.

The encoder and decoder will always process one data block in 64 consecutive cycles making high-speed pipelined systems possible.

LOSSLESS MODE

The device can be used to perform lossless compression with data up to 11-bits and up to four components. Each component can access one of two code tables. LL should be set HIGH for lossless mode.

Three prediction choices are available. In the first case, the raw data is to be coded without prediction. In this case, NOPRED is set HIGH and the input data will be coded directly. Another possibility is to employ an external predictor. Again, NOPRED is set HIGH, and the prediction error is supplied to the coder input. Finally, a one-dimensional internal predictor can be employed by setting NOPRED LOW. In this case, the previous value of a component is used to predict the current value of the component.

In all lossless modes, BS HIGH signifies a valid data value is on the DCTCOEFF bus and LBS HIGH signifies the end of a coding operation.

When operating in lossless mode, the values in the quantization tables and the AC code tables are not used. The two active code tables are stored in the DC code table memories.

FIFO OPERATION

A fifo is used to allow the coded data stream to be accessed in bursts. The fifo is 32-bits wide and 32-words deep. The occupancy of the fifo is reflected in the FIFOST bits and the host system must ensure that fifo overflow or underflow does not occur (by supplying or accepting coded data at a sufficiently high rate). Data transfers occur in each cycle in which NEXT is HIGH. NEXT is brought HIGH to read and write the next word in encode and decode modes, respectively.

The fifo status bits, FIFOST, reflect the number of words of data in the fifo (FL) in relation to the user set threshold (FIFOTH). In decode mode, the fifo states are indicated as shown:

FIFOST.1:0	State	Comment
00	ready	Data can written into the fifo (FL < FIFOTH)
01	not_ready	Fifo has sufficient data (FL >= FIFOTH)
10	full	Fifo is Full (FL = 32)
11	underflow	Fata Error!! (FL < 0)

In encode mode, the fifo states are indicated as shown:

FIFOST.1:0	State	Comment
00	ready	Data can read from the fifo (FL > FIFOTH)
01	not_ready	Fifo has sufficient capacity (FL <= FIFOTH)
10	empty	Fifo is Empty (FL = 0)
11	overflow	Fata Error!! (FL > 32)

It should be noted that reading the fifo when it is empty will cause useless to be read and writing into the fifo when it is full will cause data to be lost.

The fifo threshold, FIFOTH, should be set according to the speed at which the device accepting or generating data on the CODEDDAT bus operates. Fast devices can set the threshold very near

the limits of overflow and underflow in encode and decode modes, respectively. Devices that can not respond quickly to remove or supply data to the FIFO should set the threshold level more conservatively. In general, FIFOTH words should be supplied or removed from the FIFO in decode and encode modes, respectively. If, however, after these FIFOTH transfers the fifo status bits do not indicate not_ready, additional transfers should be made.

INITIALIZATION

After power up and every time the coding parameters are changed or read from the device, an initialization sequence is executed. This is accomplished by setting INIT HIGH. RW selects read mode when HIGH and write mode when LOW. The data is organized into nine groups which can be randomly accessed when loading parameters and serially accessed when reading parameters. The data within each group is always accessed serially. The NEXT pin is used to control the transfer of data on the CODEDDAT bus. NEXT is brought HIGH to signify the completion of both read and write cycles.

The coding parameters can be loaded in 16-bit or 8-bit words (to accommodate common ROM widths). All parameters are read back in 16-bit words.

When loading parameters, the first 8-bit word placed on the CODEDDAT bus signifies the loading width (8 or 16 bits) and the group number to be loaded. After all data in the group has been loaded, the process can be repeated to load as many or as few groups as desired. When all parameters have been loaded INIT is brought LOW.

Group Identity

The group identity and bit width are always specified in the first byte of any group load operation. The bits are placed on the CODEDDAT bus as shown:

CODEDDAT				
4	3	2	1	0
8BIT	G.3	G.2	G.1	G.0

When 8BIT is HIGH, all parameters are loaded as 8-bit words: words longer than 8 bits are loaded in 8-bit pieces. If 8BIT is LOW, all parameters are loaded in a single 16-bit word. G.3:0 is the group identity and is defined below. In addition, the number of 8 and 16 bit words for each group in encode and decode mode is shown.

G	Group	Num 8-bit Words		Num 16-bit Words	
		Decode	Encode	Decode	Encode
0	Configuration	6	6	6	6
1	Quant Table 0	64	64	64	64
2	Quant Table 1	64	64	64	64
3	Quant Table 2	64	64	64	64
4	Quant Table 3	64	64	64	64
5	DC Code Table 0	160	48	80	24
6	DC Code Table 1	160	48	80	24
7	AC Code Table 0	2560	356	1280	178
8	AC Code Table 1	2560	356	1280	178

The Configuration

Six words specify the configuration or function being performed by the device and these 8-bit words are always loaded on the 8 LSBs of the CODEDDAT bus in the order shown below. The control bits should be set before any other group.

Order	CODEDDAT							
	7	6	5	4	3	2	1	0
1	0	ENC	LL	NOPRED	32BIT	W.2	W.1	W.0
2	0	0	0	0	C3	C2	C1	C0
3	Q3.1	Q3.0	Q2.1	Q2.0	Q1.1	Q1.0	Q0.1	Q0.0
4	N1.3	N1.2	N1.1	N1.0	N0.3	N0.2	N0.1	N0.0
5	N3.3	N3.2	N3.1	N3.0	N2.3	N2.2	N2.1	N2.0
6	0	0	0	FIFOTH.4	FIFOTH.3	FIFOTH.2	FIFOTH.1	FIFOTH.0

The functions of these bits is summarized in the following table.

Bit(s)	Function
ENC	Selects encode mode when HIGH, Decode mode when LOW
LL	Selects Lossless mode when HIGH, DCT mode when LOW
NOPRED	Disables the internal predictor for lossless mode when HIGH
32BIT	Sets the CODEDDAT bus to operate in 32-bit mode when HIGH and 16-bit mode when LOW (for normal operation only).
W	Indicates the width of the input data in lossless mode. The input word is W+4 bits wide.
C0-C3	Indicates the active code table to use for components 0 to 3, respectively. When HIGH, code table one is used; otherwise code table zero is used.
Q0-Q3	Indicates the active quantization table to use for components 0 to 3, respectively. Each component may use any of four tables.
N0-N3	Composite (product of horizontal and vertical) sampling ratio for components 0 to 3, respectively. Values of zero indicate the component is not used.
FIFOTH	Threshold value for the FIFO read/not_ready flag.

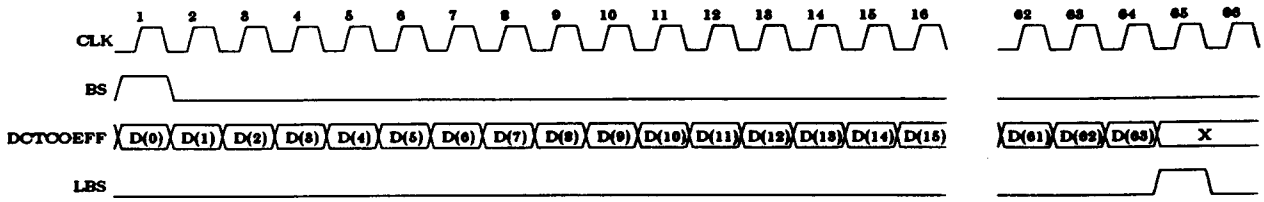
Quantization Tables

Quantization tables are loaded in zig-zag order. The 8-bit quantization values are supplied on the CODEDDAT.7:0 bits.

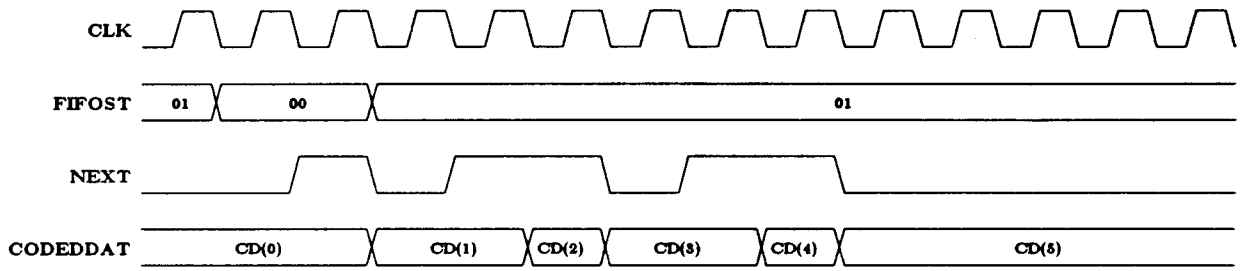
Code Tables

Code tables are loaded differently depending on the selection of the bit width and the setting of the ENC bit.

FUNCTIONAL WAVEFORMS (32-Bit I/O)



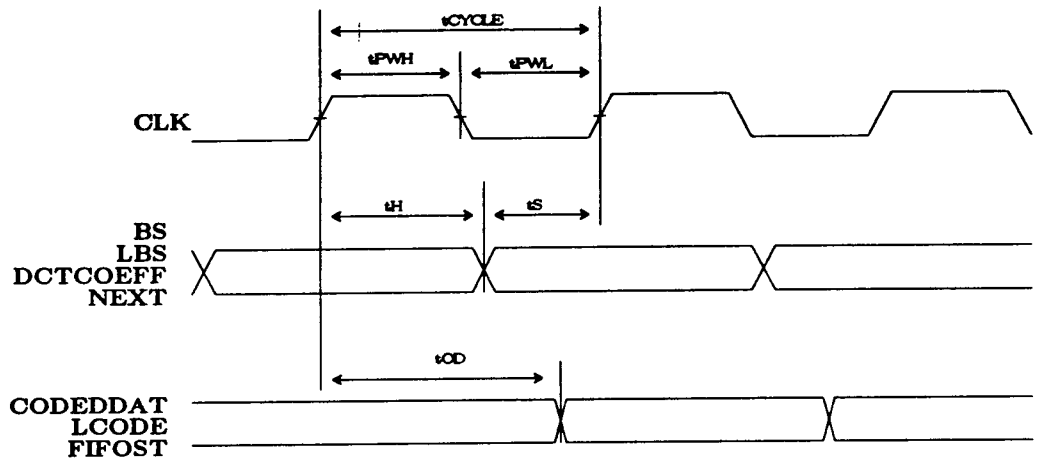
Operation on the DCTCOEFF bus for both encode and decode modes is shown above. When BS goes HIGH, the DC coefficient of a block is on the DCTCOEFF bus. The remaining coefficients will appear on the bus in the 63 following cycles in zig-zag order. If LBS goes HIGH in place of BS, the last block is signaled. In this case, the data on DCTCOEFF is ignored and the processor goes to a reset state, ready for a new image to be processed.



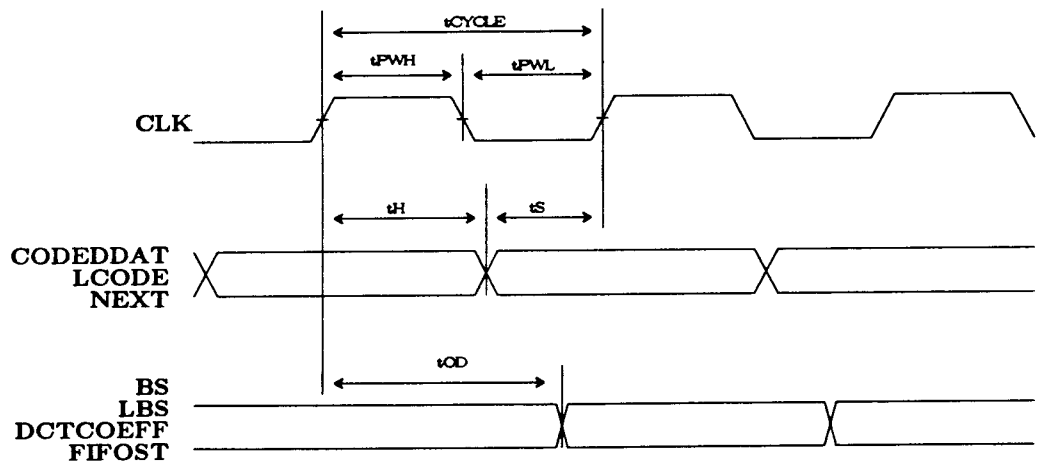
Operation on the CODEDDAT bus for both encode and decode modes is shown above. The bus is inactive when the FIFOST bits indicate not_ready (code 01). During this time the internal FIFO is filling (encode mode) or being emptied (decode mode). When additional transfers of data are required as set by the user via the FIFOTH parameter, the FIFOST bits will indicate ready (code 00). A number of transfers will take place, a word being latched each cycle NEXT is HIGH. In general, FIFOTH transfers should take place. Slow devices may make additional transfers.

The device can also be operated in a 16-bit I/O mode. The operation is very similar to 32-bit operation except that every input and output operation is performed in two steps. When decoding, NEXT is clocked every two cycles. HIGH16 is toggled to indicate that the upper 16-bits is being loaded in the first cycle and the lower 16-bits is being loaded in the second cycle. In encode mode, NEXT goes HIGH every two cycles to read a new 32-bit word. HIGH16 is used to select either the upper or lower 16-bits for output.

AC TIMING WAVEFORMS (32-Bit I/O)

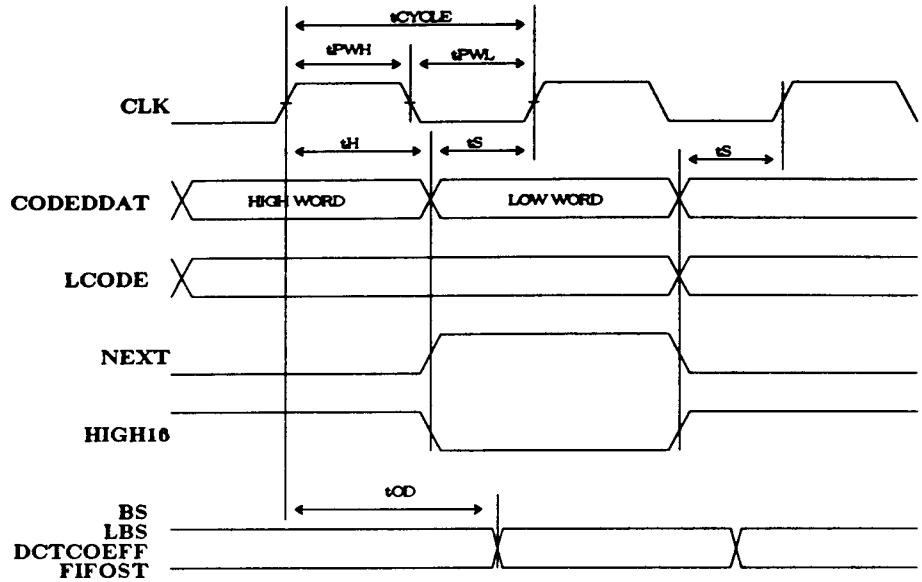


Encode Mode

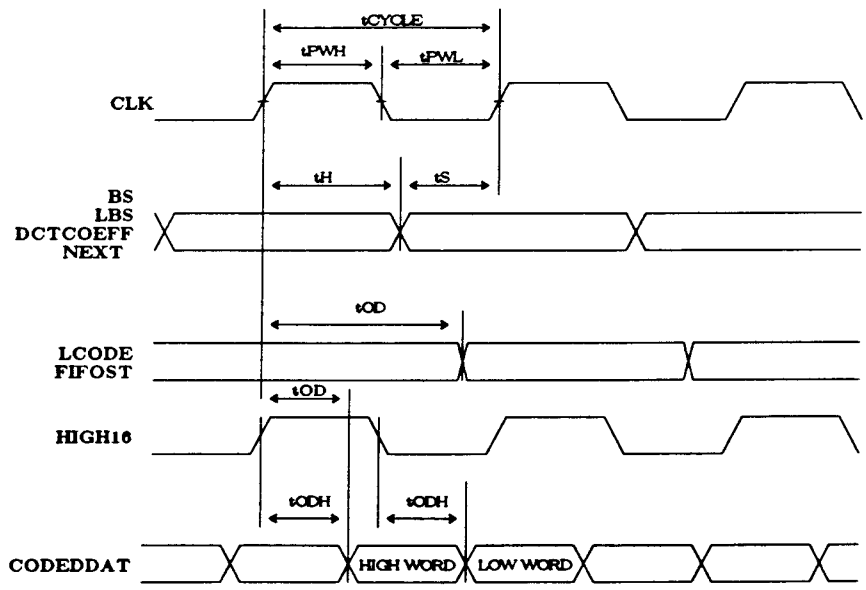


Decode Mode

AC TIMING WAVEFORMS (16-Bit I/O)



Encode Mode



Decode Mode

AC SWITCHING CHARACTERISTICS

(all times in nanoseconds)

Commercial (T_A = 0°C to 70°C, VDD = 4·75V to 5·25V)

SYMBOL	L64745-27 PARAMETER	L64745-20 Min	L64745-20 Max	Min	Max
tCYCLE	CLK cycle time	37		50	
tPWH	Min CLK pulse width, HIGH	17		20	
tPWL	Min CLK pulse width, LOW	17		20	
tS	Input setup time to CLK	9		11	
tH	Input hold time to CLK	2		2	
tOD	DO Output Delay from CLK		24*		29*
tODH	DO Output Delay from HIGH16		24*		29*

* - output loading = 50 pF.