3.3 V Low Profile 168-pin PC133 Registered SDRAM Modules for 1U Server Applications

PC133 128 MByte Module
PC133 256 MByte module
PC133 512 MByte Module
PC133 1024 MByte Module

- 168-pin Registered 8 Byte Dual-In-Line SDRAM Module for Workstation and Server main memory applications with 1,2" inch (30,40 mm) height
- One bank 16M × 72, 32M x 72 and 64M × 72 and two bank 128Mx72 organization
- Optimized for ECC applications with very low input capacitances
- JEDEC standard Synchronous DRAMs (SDRAM) with 128Mb, 256Mb and 512Mb memory density. Stacked components for two bank modules
- Single + 3.3 V (± 0.3 V) power supply
- Auto Refresh (CBR) and Self Refresh
- Serial Presence Detect with E^2PROM
- Programmable $\overline{CAS}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- All inputs and outputs are LVTTL compatible
- Utilizes SDRAMs in TSOPII-54 packages with on-board registers and PLL.
- Card Sizes :
  RawCard "F" and "G" 133.35 mm x 30,40 with gold contact pads
- These modules all fully compatible with the current industry standard PC133 specifications and fully backward compatible to PC100 applications

- Performance:

		-7.5	Unit
f_{CK3}	Clock Frequency (max.) @ CL = 3	133	MHz
t_{AC3}	Clock Access Time (min.)@ CL = 3	5.4	ns
f_{CK2}	Clock Frequency (max.) @ CL = 2	100	MHz
t_{AC2}	Clock Access Time (min.)@ CL = 2	6	ns

The HYS 72Vxx5/6x0GR-7.5 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 16M × 72, 32M x 72, 64M × 72 and 128M x 72 high speed memory arrays designed with x4 or x8 organised Synchronous DRAMs (SDRAMs) for ECC applications. All control and address signals are registered on-DIMM and the design incorporates a PLL circuit for the Clock inputs. Use of an on-board register reduces capacitive loading on the input signals but are delayed by one cycle in arriving at the SDRAM devices. Decoupling capacitors are mounted on the PC board. The DIMMs use a serial presence detects scheme implemented via a serial E^2PROM using the 2-pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint. This module family is designed with 30,40 mm (1.2 inch) maximum height for 1U Server Applications b ased on JEDEC standard RawCards "F" and "G".

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
1.2” height:			
HYS 72V16600GR-7.5	PC133R-333-542-F	one bank 128 MB Reg. DIMM	128 MBit (x8)
HYS 72V32501GR-7.5	PC133R-333-542-G	one bank 256 MB Reg. DIMM	128 MBit (x4)
HYS 72V32600GR-7.5	PC133R-333-542-F	one bank 256 MB Reg. DIMM	256 Mbit (x8)
HYS 72V64500GR-7.5	PC133R-333-542-G	one bank 512 MB Reg. DIMM	256 Mbit (x4)
HYS 72V64601GR-7.5	PC133R-333-542-F	one bank 512 MB Reg. DIMM	512 MBit (x8)
HYS 72V128520GR-7.5	PC133R-333-542-G	two banks 1024 MB Reg. DIMM	256 Mbit (x4) stacked

Note: All part numbers end with a place code (not shown), designating the die revision. Consult factory for current revision. Example: HYS 64V16600GR-7.5-C2, indicating Rev.C2 dies are used for SDRAM components.

Pin Definitions and Functions

A0 - A11, A12	Address Inputs (A12 is used for 256Mbit and 512Mbit based modules only)	DQMB0 - DQMB7	Data Mask
BA0, BA1	Bank Selects	$\overline{CS0}$ - $\overline{CS3}$	Chip Select
DQ0 - DQ63	Data Input/Output	REGE *)	Register Enable “H” or N.C = registered mode “L” = buffered mode
CB0 - CB7	Check Bits	V_{DD}	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read/Write Input	SDA	Serial Data Out
CKE0	Clock Enable	N.C.	No Connection
CLK0 - CLK3	Clock Input	–	–

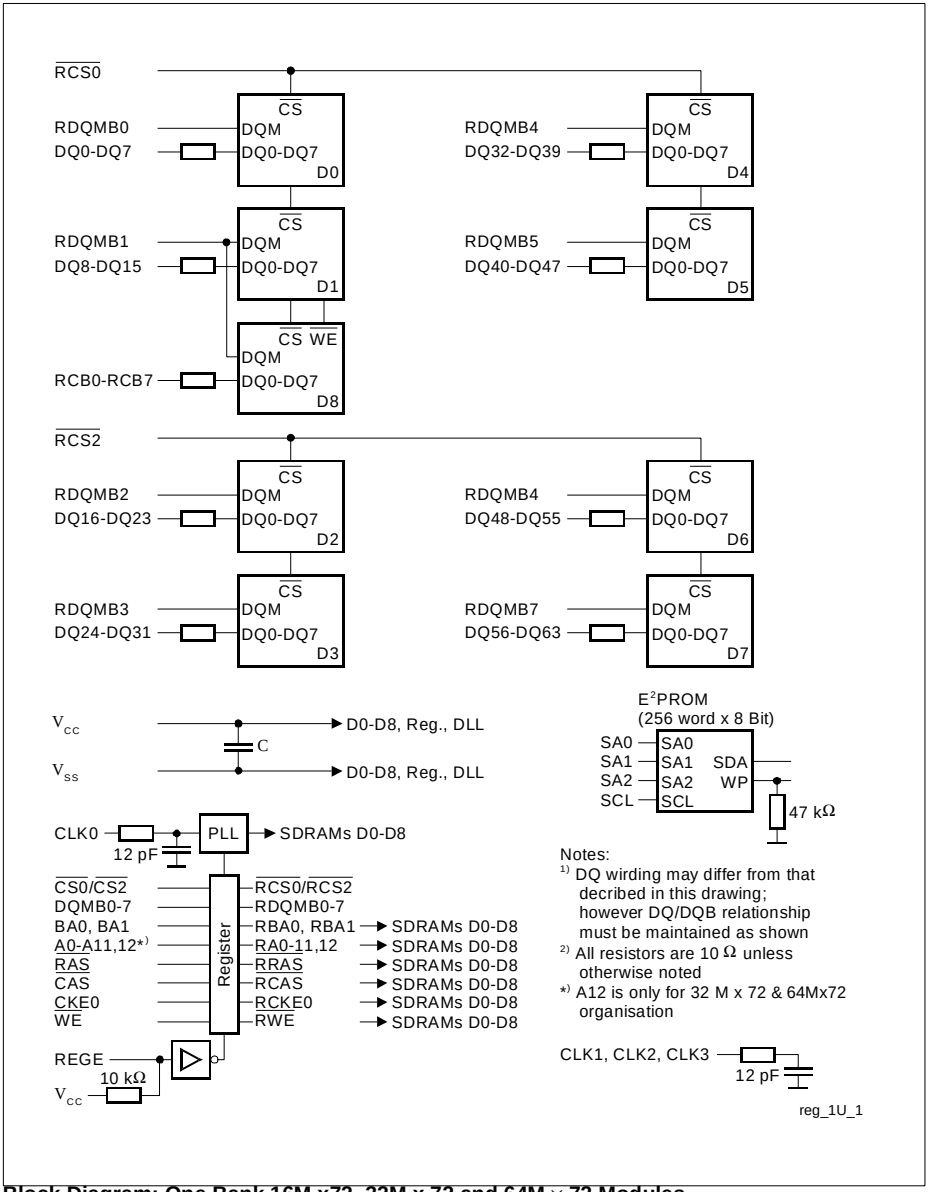
*) note : To confirm to this specification, motherboards must pull this pin to high state or no connect.

Address Format

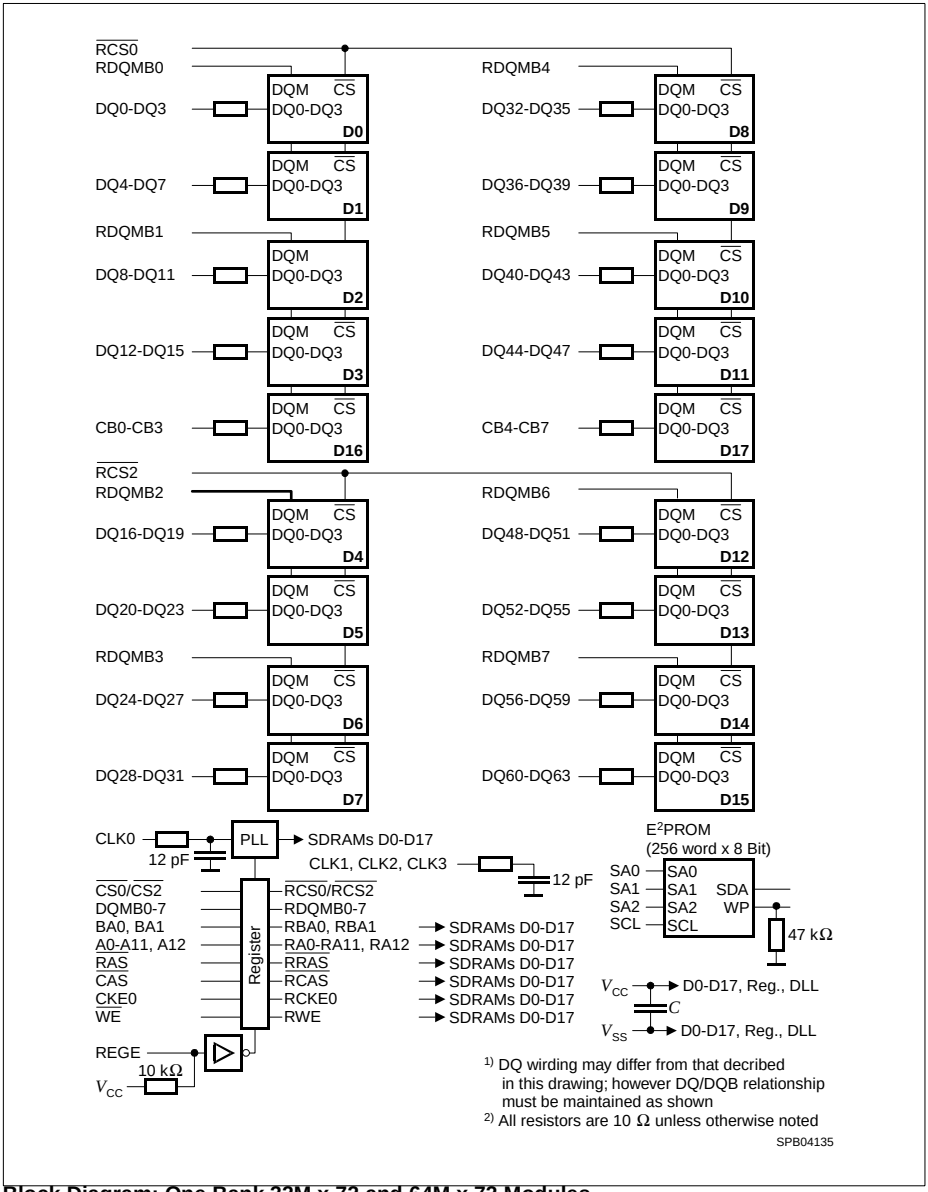
Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
128 MB	16M × 72	1	16M x 8	9	12/2/10	4k	64 ms	15.6 µs
256 MB	32M x 72	1	32M x 4	18	12/2/11	4k	64 ms	15.6 µs
256 MB	32M x 72	1	32M x 8	9	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 72	1	64M × 4	18	13/2/11	8k	64 ms	7.8 µs
512 MB	64M × 72	1	64M × 8	9	13/2/12	8k	64 ms	7.8 µs
1 GB	128M x 72	2	64M × 4	36	13/2/11	8k	64 ms	7.8 µs

Pin Configuration

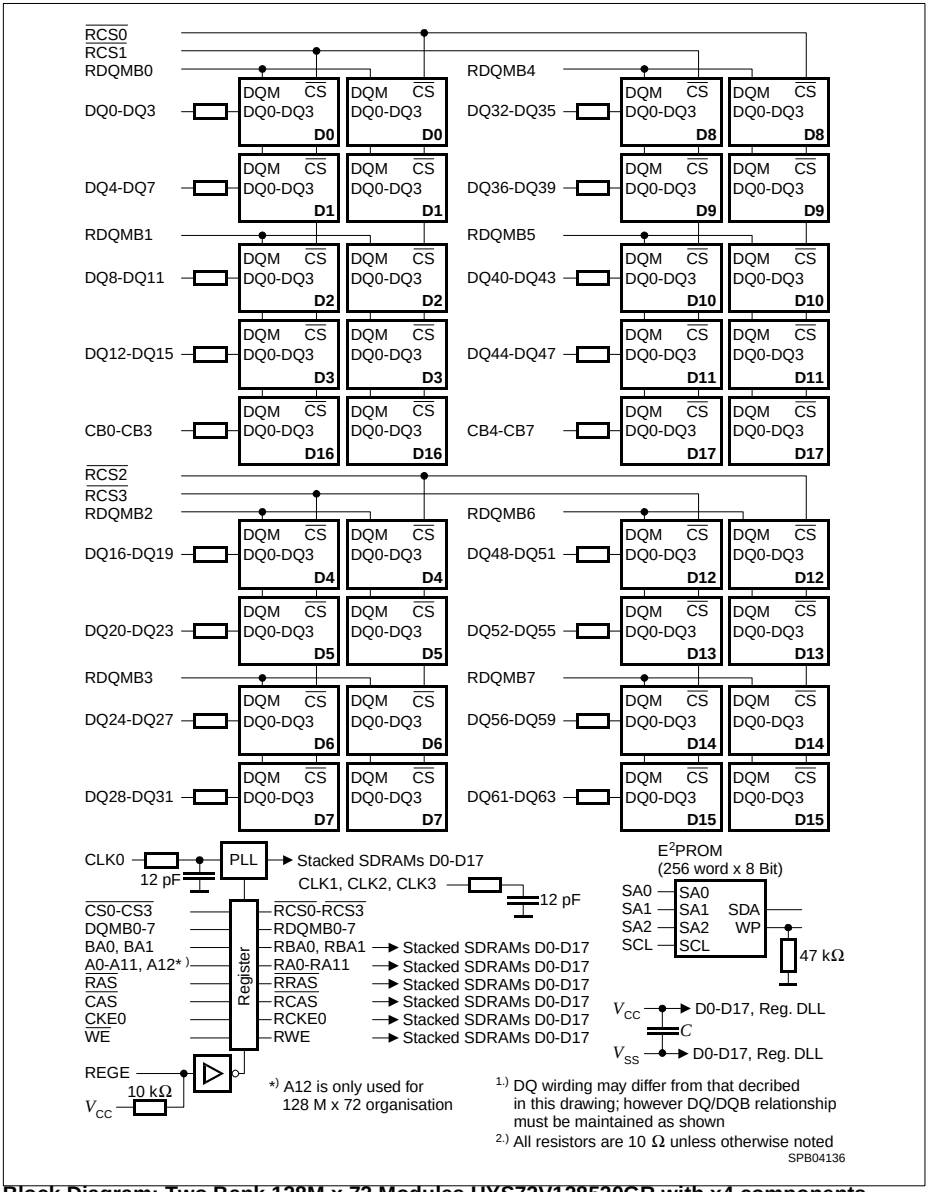
PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	$\overline{CS2}$	87	DQ33	129	$\overline{CS3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	DU	90	V_{DD}	132	N.C.
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	N.C.	92	DQ37	134	N.C.
9	DQ6	51	N.C.	93	DQ38	135	N.C.
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	N.C.	103	DQ46	145	N.C.
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	N.C.	105	CB4	147	REGE
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	N.C.	66	DQ22	108	N.C.	150	DQ54
25	N.C.	67	DQ23	109	N.C.	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{CS0}$	72	DQ27	114	$\overline{CS1}$	156	DQ59
31	DU	73	V_{DD}	115	$\overline{RAS}$	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10 (AP)	80	N.C.	122	BA0	164	N.C.
39	BA1	81	WP	123	A11	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V_{DD}	126	A12	168	V_{DD}



Block Diagram: One Bank 16M x72, 32M x 72 and 64M × 72 Modules
HYS72V16600, HYS72V32600 & HYS72V64601GR using x8 organized SDRAMs (RawCard F)



Block Diagram: One Bank 32M x 72 and 64M x 72 Modules
HYS72V32501GR and HYS72V64500GR with x4 components (RawCard G)



Block Diagram: Two Bank 128M x 72 Modules HYS72V128520GR with x4 components (RawCard G)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	– 1.0	4.6	V
Power supply voltage on V_{DD}	V_{DD}	– 1.0	4.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation (per SDRAM component)	P_D	–	1	W
Data out current (short circuit)	I_{OS}	–	50	mA

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

DC Characteristics

T_A = 0 to 70 °C [1]; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5	0.8	V
Output High Voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V
Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 10	10	µA
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	– 10	10	µA

Capacitance

T_A = 0 to 70 °C [1]; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		One Bank Modules	Two Bank Modules	
Input Capacitance (all inputs except CLK and CKE)	C_{IN}	10	20	pF
Input Capacitance (CLK)	C_{CLK}	30	30	pF
Input Capacitance (CKE)	C_{CKE}	17	30	pF
Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	10	17	pF
Input Capacitance (SCL, SA0 - 2)	C_{SC}	8	8	pF
Input/Output Capacitance (SDA)	C_{SD}	8	8	pF

Operating Currents per SDRAM Component
T_A = 0 to 70 °C [1], V_{DD} = 3.3 V ± 0.3 V

(Recommended Operating Conditions unless otherwise noted)

Parameter	Test Condition	Symbol	128Mb	256Mb	512 Mb	Unit	Note
			max.				
Operating current $t_{RC} = t_{RC(MIN.)}$, $t_{CK} = t_{CK(MIN.)}$ Outputs open, Burst Length = 4, CL = 3. All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	–	I_{CC1}	160	230	270	mA	2)
Precharge stand-by current in Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, CKE ≤ $V_{IL(MAX.)}$	t_{CK} = min.	I_{CC2P}	1.5	2	4	mA	2)
Precharge Stand-by Current in Non-Power Down Mode $\overline{CS} = V_{IH\ (MIN.)}$, CKE ≥ $V_{IH(MIN.)}$	t_{CK} = min.	I_{CC2N}	40	40	36	mA	2)
No operating current t_{CK} = min., $\overline{CS} = V_{IH(MIN.)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	50	50	35	mA	2)
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}	10	10	11	mA	2)
Burst operating current t_{CK} = min., Read command cycling	–	I_{CC4}	100	150	255	mA	2), 3)
Auto refresh current t_{CK} = min., Auto Refresh command cycling	–	I_{CC5}	230	240	440	mA	2)
Self refresh current Self Refresh Mode,CKE = 0.2 V	–	I_{CC6}	1.5	3	4	mA	2)

AC Characteristics (SDRAM Device Specification) [4), 5)]
T_A = 0 to 70 °C [1)]; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

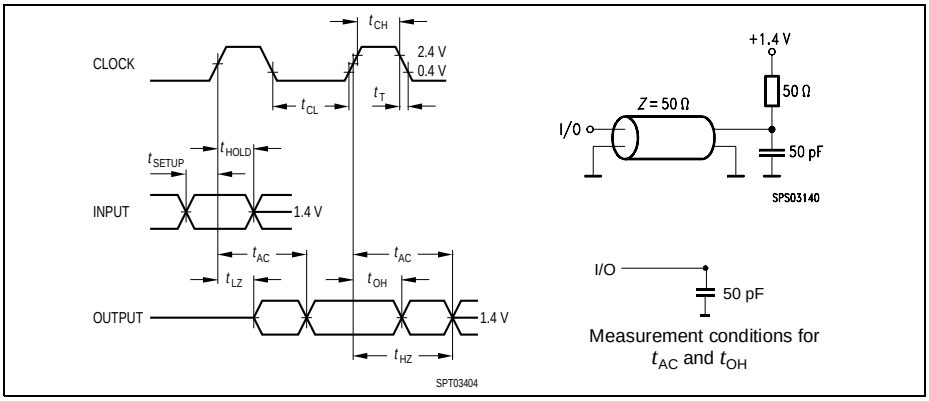
Parameter	Symbol	Limit Values		Unit	Note
		-7.5			
		min.	max.		
Clock and Access Time					
Clock Cycle Time	t_{CK}				–
$\overline{CAS}$ Latency = 3		7.5	–	ns	
$\overline{CAS}$ Latency = 2		10	–	ns	
Clock Frequency	f_{CK}				–
$\overline{CAS}$ Latency = 3		–	133	MHz	
$\overline{CAS}$ Latency = 2		–	100	MHz	
Access Time from Clock	t_{AC}				–
$\overline{CAS}$ Latency = 3		–	5.4	ns	
$\overline{CAS}$ Latency = 2		–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	ns	–
Clock Low Pulse Width	t_{CL}	2.5	–	ns	–
Transition Time	t_T	0.5	10	ns	–
Setup and Hold Parameters					
Input Setup Time	t_{IS}	1.5	–	ns	–
Input Hold Time	t_{IH}	0.8	–	ns	–
Power Down Mode Entry Time	t_{SB}	–	1	CLK	–
Power Down Mode Exit Setup Time	t_{PDE}	1	–	CLK	–
Mode Register Setup Time	t_{RCS}	2	–	CLK	–
Common Parameters					
Row to Column Delay Time	t_{RCD}	20	–	ns	–
Row Precharge Time	t_{RP}	20	–	ns	–
Row Active Time	t_{RAS}	45	100k	ns	–
Row Cycle Time	t_{RC}	67.5	–	ns	–
Activate (a) to Activate (b) Command Period	t_{RRD}	2	–	CLK	–
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period	t_{CCD}	1	–	CLK	–

AC Characteristics (SDRAM Device Specification) (cont'd) [4), 5)]
T_A = 0 to 70 °C [1)]; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values		Unit	Note
		-7.5			
		min.	max.		
Refresh Cycle					
Refresh Period	t_{REF}				–
128MBit SDRAM Based Modules		–	15.6	µs	
256 & 512MBit SDRAM Based Modules		–	7.8	µs	
Self Refresh Exit Time	t_{SREX}	1	–	CLK	[6)]
Read Cycle					
Data Out Hold Time	t_{OH}	3	–	ns	–
Data Out to Low Impedance Time	t_{LZ}	0	–	ns	[7)]
Data Out to High Impedance Time	t_{HZ}	3	7	ns	[7)]
DQM Data Out Disable Latency	t_{DQZ}	–	2	CLK	–
Write Cycle					
Data Input to Precharge (write recovery)	t_{WR}	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	CLK	–

Notes

1. The registered DIMM modules are designed to operate under system operating conditions between 0-55 deg C ambient, maximum sustained bandwidth and 0 LFM airflow. Operating at higher ambient temperatures needs sufficient air flow to limit the case temperature of the SDRAM components do not exceed 85°C.
2. These parameters depend on the cycle rate. All values are measured at 133 MHz operation frequency. Input signals are changed once during tck excepts for Icc6 and for standby currents when tck = infinity.
3. These parameters are measured with continous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the data-out current is excluded.
4. An initial pause of 100 µs is required after power-up. Then a Precharge All Banks command must be given followed by eight Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin. Also the on-DIMM PLL must be given enough clock cycles to stabilize (t_{STAB}) before any operation can be guaranteed.
5. AC timing tests have V_{IL} = 0.8 V and V_{IH} = 2.0 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.
6. Self Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied after the Self Refresh Exit command is registered.
7. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.



Serial Presence Detect

A serial presence detect storage device - E²PROM 34C02 - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E²PROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus).

SPD-Table for -7.5 Registered DIMM Modules

Byte#	Description	SPD Entry Value	Hex						
			128 MB 1 Bank	256 MB 1 Bank[1)]	256 MB 1 Bank[2)]	512 MB 1 Bank[*)]	512 MB 2 Banks	512 MB 1 Bank[**)]	1 GB 2 Banks
0	Number of SPD Bytes	128	80						
1	Total Bytes in Serial PD	256	08						
2	Memory Type	SDRAM	04						
3	Number of Row Addresses)	12/13	0C	0C	0D	0D	0D	0D	0D
4	Number of Column Addresses	10/11/12	0A	0B	0A	0B	0A	0C	0B
5	Number of DIMM Banks	1,2	01	01	01	01	02	01	02
6	Module Data Width	72	48						
7	Module Data Width (cont'd)	0	00						
8	Module Interface Levels	LVTTL	01						
9	Cycle Time at CL = 3	7.5 ns	75						
10	Access Time from Clock at CL = 3	5.4 ns	54						
11	DIMM Config (Error Det/Corr.)	ECC	02						
12	Refresh Rate/Type	15.6/7.8 µs	80	80	82	82	82	82	82
13	SDRAM Width, Primary	x4, x8	08	04	08	04	08	08	04
14	Error Checking SDRAM Data Width	x4, x8	08	04	08	04	08	08	04
15	Minimum t_{CCD}	1 CLK	01						
16	Burst Length Supported	1, 2, 4, 8	0F						
17	Number of SDRAM Banks	4	04						
18	SDRAM Supported $\overline{CAS}$ Latencies	2 & 3	06						
19	SDRAM $\overline{CS}$ Latencies	0	01						
20	SDRAM $\overline{WE}$ Latencies	0	01						
21	SDRAM DIMM Module Attributes	Registered with PLL	1F						
22	SDRAM Device Attributes	V_{DD} tol +/– 10%	0E						
23	Min. Clock Cycle Time at CL = 2	10 ns	A0						
24	Max. Access Time from Clock for CL = 2	6.0	60						
25	Min. Clock Cycle Time at CL = 1	not supported	00						
26	Max. Access Time from Clock at CL = 1	not supp.	00						
27	SDRAM Minimum t_{RP}	20 ns	14						
28	SDRAM Minimum t_{RRD}	15 ns	0F						
29	SDRAM Minimum t_{RCD}	20 ns	14						
30	SDRAM Minimum t_{RAS}	45 ns	2D						
31	Module Bank Density (per bank)	128 M/ 256M/ 512 MB	20	40	40	80	40	80	80
32	SDRAM Input Setup Time	1.5 ns	15						
33	SDRAM Input Hold Time	0.8 ns	08						
34	SDRAM Data Input Setup Time	1.5 ns	15						

SPD-Table for -7.5 Registered DIMM Modules (cont'd)

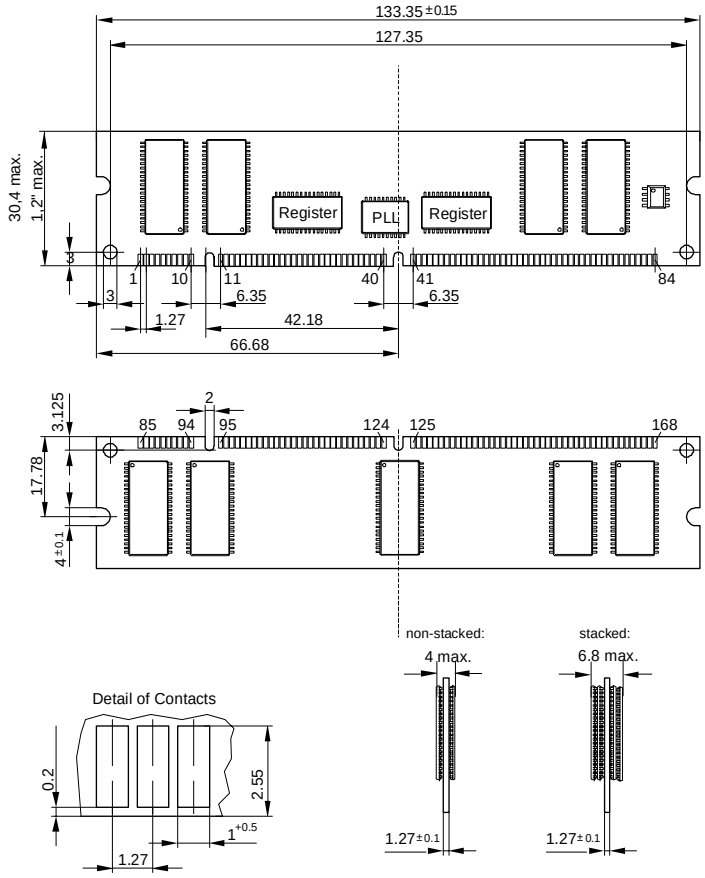
Byte#	Description	SPD Entry Value	Hex						
			128 MB 1 Bank	256 MB 1 Bank[1)]	256 MB 1 Bank[2)]	512 MB 1 Bank[*)]	512 MB 2 Banks	512 MB 1 Bank[**)]	1 GB 2 Banks
35	SDRAM Data Input Hold Time	0.8 ns	08						
36-61	Superset Information(may be used in future)	–	00						
62	SPD Revision	JEDEC 2	12						
63	Checksum for Bytes 0 - 62	–	60	79	83	BC	84	BD	BD
64	Manufacturers JEDEC ID Code		C1						
65-71	Manufacturer		INFINEO(N)						
72	Module Assembly Location								
73-90	Module Part Number								
91-92	Module Revision Code								
93-94	Module Manufacturing Date								
95-98	Module Serial Number								
99-125									
126	Frequency Specification	–	64						
127	Details of Clocks	–	8F						
128-255	Open for Customer Use	–							

Note: 1) HYS72V32501GR-7.5 (128Mbit x4 based), 2) HYS72V32600GR-7.5 (256Mbit x8 based)
*) HYS72V64500GR-7.5 (256Mbit based) **) HYS72V64601GR-7.5 (512Mbit based)

Package Outlines Raw Card F

Module Package
JEDEC MO-161
Registered DIMM Modules (Raw Card F) L-DIM168-51

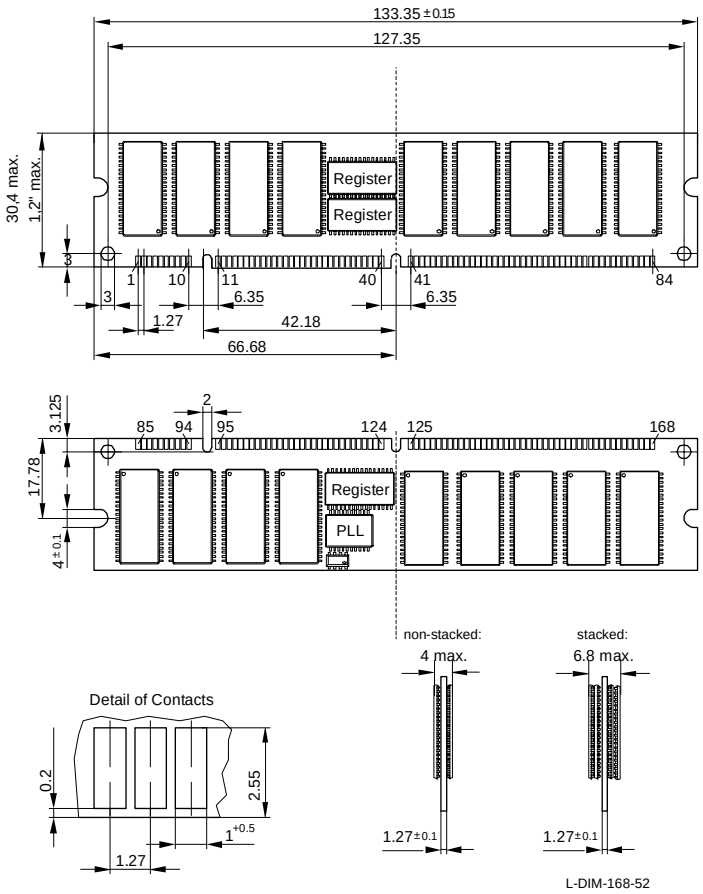
128MB, 256MB & 512MB modules based on x8 SDRAM components



note: all outline dimensions and tolerances are in accordance with the JEDEC standard

Package Outlines Raw Card G

Module Package
JEDEC MO-161
Registered DIMM Modules (Raw Card G) L-DIM168-52



note: all outline dimensions and tolerances are in accordance with the JEDEC standard

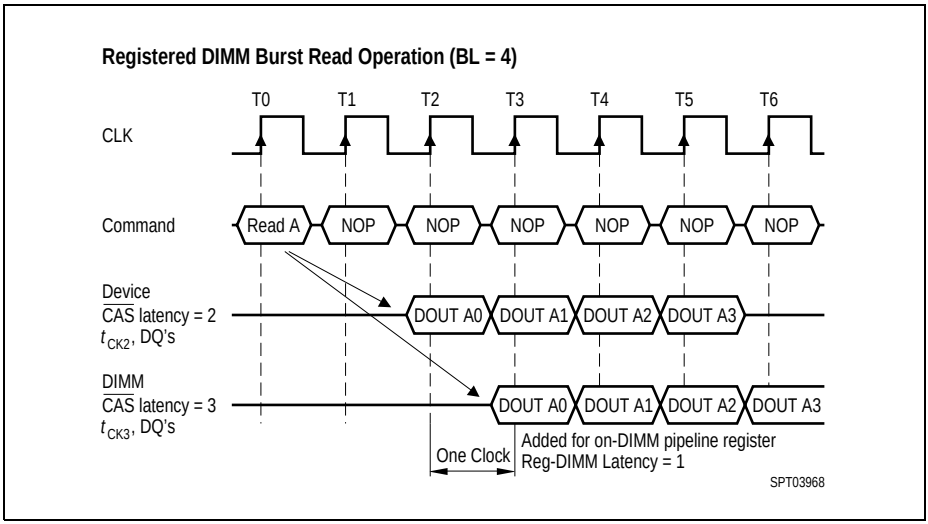
Functional Description

All these PC133 168-pin Registered DIMMs conform to a compatible set of timing and operation characteristics intended to comply with the 133 MHz standards. The Registered DIMMs achieve high speed data transfer rate up to 133 MHz, when in “registered mode”. The “registered mode” is achieved when the REGE input signal is in “high” state or the pin is not connected. Operation in “buffered mode” (REGE = “low”) needs careful system design to compensate all input signals for the extra delay time of the register components when in “buffered mode”. “Buffered mode” is limited to 66 Mhz operation and is beyond the scope of this datasheet.

Registered Mode:

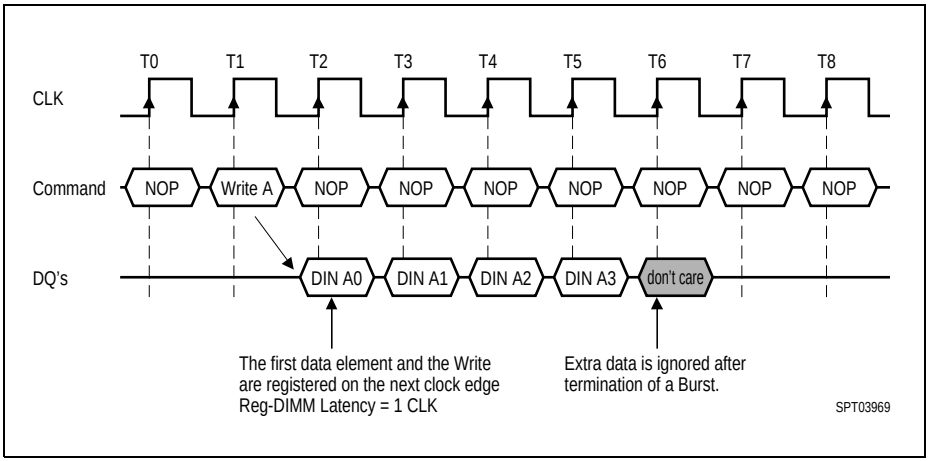
All control and address signals are synchronized with the positive edge of externally supplied clocks and are registered on-DIMM and hence delayed by one clock cycle in arriving at the SDRAM devices. The use of the on-board register reduces the capacitive loading of the DIMM on input control and address signals. The SDRAM device data lines (DQ) are connected directly to the DIMM tabs through 10 Ohm series resistors. All the following timing diagrams and explanations show DIMM operation at the tabs, not SDRAM operation.

The picture below depicts an overview of the effect of the Registered Mode on the data outputs (DQs) for a Read operation. Without the registers, the data is delayed according to the device $\overline{\text{CAS}}$ latency, in the case two clocks. With the register, the data is delayed according to the device $\overline{\text{CAS}}$ latency plus an additional clock cycle. This is known as the DIMM $\overline{\text{CAS}}$ latency, and in this example is four three. The data path can be thought of as a pipeline in which the register effectively lengthens the pipe by one clock cycle.



In case of a Burst Write Command the data-in is delayed one clock due the op-DIMM pipeline register also. Therefore, data for the first Burst Write cycle must be applied on the DQ pins on the next clock cycle after the Write command is issued. the remaining data inputs must be supplied on

each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.



Registered DIMM Burst Write Operation (BL = 4)

Change List

12.00	Rev. 0.1	First revision
18.1.2001	Rev. 0.1	Clarification of “buffered mode”operation (not tested)
23.1.2001	Rev. 0.1	Height reduced from 1.2” (nominal) to 1.155” (max) according to the lastest IBM drawings for RawCard F
12.02.2001	Rev.0.2	PM decided to stay with 1.2” inch height
19.02.2001	Rev. 0.3	New PCB L-DIM-168-56 with 1.125” height
27.02.2001	Rev. 0.4	Both Gerber Files (1,125” and 1.2”) are now in the target datasheet
04.04.2001	Rev. 0.5	x4 based modules on L-DIM-168-52 added
11.04.2001	Rev. 0.5b	Info from Mr. Pammer AIT Rgb: L-DIM-168-51 is based on Raw Card A and L-DIM-168-52 is based on Raw Card B Block Diagram for stacked x8 module changed for use of x8 stacks with one CKE and two CS
29.05.2001	Rev. 0.6	HYS72V32501GR-7.5 (128Mbit x4 based 256MByte) added
21.06.2001	Rev. 0.7	Outline Drawings changed to L-DIM-168-51,52 & 56
28.06.2001	Rev. 0.8	Product Marketing Decision : Remove all 1,125” inch modules Datasheet changed from “target” to “preliminary” RawCards and therefore the Compliance Code changed according to JEDEC naming conventions, RawCard F for x8 and RawCard G for x4 (non-stackd and stacked)
06.09.2001	Rev. 0.9	SCR: Thickness of modules changed from 4 to 4 max and 6.4 to 6.8 max
17.12.2001	Final 1.0	SCR-028-2001-11-12 PC133 / TPCR_08 / JC42.5 Item 1138.5 : JEDEC changed Byte 62h (SPD Revision) from 02h to 12h Checksum changed therefore also