16 Megabit FlashBank Memory

SST38VF166

Data Sheet

FEATURES:

- **Single 2.7-3.6V Read and Write Operations**
- **Separate Memory Banks for Code or Data**
  - Simultaneous Read and Write Capability
- **Superior Reliability**
  - Endurance:
    E^2 bank - 500,000 Cycles (typical)
    Flash bank - 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Current, Read: 15 mA (typical)
  - Active Current, Concurrent Read while Write: 40 mA (typical)
  - Standby Current: 3 µA (typical)
  - Auto Low Power Mode Current: 3 µA (typical)
- **Fast Write Operation**
  - Flash Bank-Erase + Program: 8 sec (typical)
  - Flash Block-Erase + Program: 500 ms (typical)
  - Flash Sector-Erase + Program: 30 ms (typical)
  - E^2 bank Word-Write: 9 ms (typical)
- **Fixed Erase, Program, Write Times**
  - Remain constant after cycling
- **Read Access Time**
  - 70 ns
- **Latched Address and Data**
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **E^2 Bank:**
  - Word-Write (Auto Erase before Program)
  - Sector-Erase (32 Words) + Word-Program (same as Flash bank)
- **Flash Bank: Two Small Erase Element Sizes**
  - 1 KWords per Sector or 32 KWords per Block
  - Erase either element before Word-Program
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Packages Available**
  - 48-Pin TSOP (12mm x 20mm)
- **Continuous Hardware and Software Data Protection (SDP)**
- **A One Time Programmable (OTP) E^2 Sector**

PRODUCT DESCRIPTION

The SST38VF166 consists of three memory banks, 2 each 512K x16 bits sector mode flash EEPROM plus a 4K x16 bits word alterable E^2PROM manufactured with SST's proprietary, high performance SuperFlash Technology. The SST38VF166 erases and programs with a single power supply. The internal Erase/Program in the E^2 bank is transparent to the user. The device conforms to (proposed) JEDEC standard pinouts for word-wide memories.

The SST38VF166 device is divided into three separate memory banks, 2 each 512K x16 Flash banks and a 4K x16 E^2 bank. Each Flash bank is typically used for program code storage and contains 512 sectors, each of 1 KWords or 16 blocks, each of 32 KWords. The Flash banks may also be used to store data. The E^2 bank is typically used for data or configuration storage and contains 128 sectors, each of 32 words. Any bank may be used for executing code while writing data to a different bank. Each memory bank is controlled by separate Bank Enable (BE#) lines.

The SST38VF166 inherently uses less energy during Erase, Program, and Write than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter Erase time, the total energy consumed during any Erase, Program, or Write operation is less than alternative flash technologies. The Auto Low Power mode automatically reduces the active read current to approximately the same as standby; thus, providing an average read current of approximately 1 mA/MHz of Read cycle time.

The SuperFlash technology provides fixed Erase, Program, and Write times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

Device Operation

The SST38VF166 operates as two independent 8-Megabit Word-Program, Sector-Erase flash EEPROMs with the additional functionality of a 64 Kbit word-alterable E^2PROM. All banks are superimposed in the same memory address space. All three memory banks share common address lines, I/O lines, WE#, and OE#. Memory bank selection is by bank enable. BE#1 selects the first

Flash bank, BE#2 selects the second Flash bank, BE#3 selects the E^2 bank. WE# is used with SDP to control the Write or Erase and Program operation in each memory bank.

The SST38VF166 provides the added functionality of being able to simultaneously read from one memory bank while writing, erasing, or programming to one other memory bank. Once the internally controlled Write, Erase, or Program cycle in a memory bank has commenced, a different memory bank can be accessed for read. Also, once WE# and the applicable BE# are high during the SDP load sequence, a different bank may be accessed to read. If multiple bank enables are asserted simultaneously, the outputs will tri-state and no new memory operations can be initiated. Only one bank may be written, erased, or programmed at any given time. The device ID and Common Flash Interface (CFI) functions cannot be accessed while any bank is writing, erasing, or programming.

The **Auto Low Power Mode** automatically puts the device in a near standby mode after data has been accessed with a valid Read operation. This reduces the I_{DD} active read current from typically 15mA to typically 3µA. The Auto Low Power mode reduces the typical I_{DD} active read current to the range of 1mA/MHz of Read cycle time. The device exits the **Auto Low Power Mode** with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty.

Flash Bank Read

The Read operation of the SST38VF166 Flash Bank is controlled by BE#1 or BE#2 and OE#, a bank enable and output enable both have to be low for the system to obtain data from the outputs. BE#1 is used for Flash bank 1 selection. When BE#1 is high, the Flash bank 1 is deselected. BE#2 is used for Flash bank 2 selection. When BE#2 is high, the Flash bank 2 is deselected. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the timing waveforms for further details (Figure 2 or 3).

E^2 Bank Read

The Read operation of the E^2 bank is controlled by BE#3 and OE#, both have to be low for the system to obtain data from the outputs. BE#3 is used for E^2 bank selection. When BE#3 is high, the E^2 bank is deselected. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the timing waveforms for further details (Figure 4).

Write Modes

The SST38VF166 device has separate Write modes for the E^2 bank and Flash banks. The conventional E^2PROM Word-Write with internally timed automatic Erase before Program is the most convenient and easy method for the user to alter data in the E^2 bank with the Word-Write operation, the word being written is the only word that is altered. Bank- or Sector-Erase plus Word-Program operations may also be used for the E^2 bank. For both banks of the Flash array, the SST38VF166 offers Bank-, Block-, and Sector-Erase plus Word-Program operations.

Write

All Write operations are initiated by first issuing the Software Data Protect (SDP) entry sequence for Bank-, Block-, or Sector-Erase then Word-Program in the selected Flash bank; or for Word-Write or for Sector-Erase and Word-Program in the E^2 bank. Word-Write, Word-Program, and all Erase commands have a fixed duration, that will not vary over the life of the device, i.e., are independent of the number of Erase/Program cycles endured.

Either Flash bank may be read during the internally controlled E^2 bank Write cycle, e.g., the Flash bank may be accessed to fetch instructions or data when the E^2 bank is being written, erased, or programmed. Additionally, the alternate Flash bank may be read while erasing or programming the other Flash or E^2 bank. At any given time, only one bank may be performing a Write operation, during that time any other bank is available for read.

The Write Status command may be used to determine if any bank is being written, at any given time. This may be required if the system does not use a timer or does not monitor toggle bit or data# polling when writing a specific bank. In order to implement the Write Status command, address 5XXXH in the E^2 bank address space is reserved. This address is outside the normal address space of the E^2 bank; therefore, will not interfere with normal reading within the E^2 bank address space.

The device is always in the Software Data Protected mode for all Write operations in both the Flash bank and E^2 bank. Write operations are controlled by toggling WE# or BE#. The falling edge of WE# or BE#, whichever occurs last, latches the address. The rising edge of WE# or BE#, whichever occurs last, latches the data and initiates the Erase, Program, or Write cycle.

The SDP Erase, Program, or Write commands are all BE# specific. Whichever BE# is used for the first SDP bus cycle (except for Read operation with WE# high), that BE# must be used for all subsequent SDP bus cycles, for the command to be executed. If a different BE# is pulsed during a

subsequent bus cycle, when WE# is low, in the SDP command sequence, the device will abort the attempted SDP command and revert to the Read mode. Note, the SDP command sequence may be suspended by taking WE# high. A different BE# may then be pulsed to read from either of the banks not involved with the SDP command sequence.

For the purposes of simplification, the following descriptions will assume WE# is toggled to initiate an Erase, Program, or Write. Toggling the applicable BE# will accomplish the same function. Note, there are separate timing diagrams to illustrate both WE# and BE# controlled Program or Write commands.

Flash Bank Word-Program

The Flash bank Word-Program operation consists of issuing the SDP Word-Program command, initiated by forcing BE#1 or BE#2 and WE# low, and OE# high. The words to be programmed must be in the erased state, prior to programming. The Word-Program command programs the desired addresses word-by-word. During the Word-Program cycle, the addresses are latched by the falling edge of WE#. The data is latched by the rising edge of WE#. See Figure 5 or 7 for WE# or 6 and 8 for BE# controlled Word-Program cycle timing waveforms, Table 6 for the command sequence, and Figure 49 for a flowchart.

During the Flash bank Erase or Program operation, the only valid reads from that bank are Data# Polling and Toggle Bit. The other Flash bank or the E^2 bank may be read.

The specified Bank-, Block-, or Sector-Erase time is the only time required to erase. There are no preprogramming or other commands or cycles required either internally or externally to erase the bank, block, or sector.

E^2 Bank Word-Write

The E^2 bank Word-Write operation consists of issuing the SDP command, initiated by forcing BE#3 and WE# low, and OE# high; followed by the Word Load cycle to the SST38VF166. The internally controlled Write cycle stores the data loaded in the word buffer into the E^2 bank. The address selected is then erased and programmed, by internally controlled signals. During the Word Load cycle, the address is latched by the falling edge of WE#. The data is latched by the rising edge of WE#. The internal write cycle is initiated on the rising edge of WE#. The Write cycle, once initiated, will continue to completion, typically within 7 ms. See Figure 9 for WE# or 10 for BE# controlled write cycle timing waveforms, Table 7 for the command sequence, and Figure 48 for a flowchart.

The Write operation has two functional cycles: the Word Load cycle and the internal Write cycle. The Word Load cycle consists of loading 1 word of data into the word buffer at the completion of the SDP sequence. The internal Write cycle consists of the write timer operation, to erase and program the selected address. Note, the word does NOT have to be erased prior to writing. During the Write operation, the only valid reads are Data# Polling and Toggle Bit from the E^2 bank or normal read from either of the Flash banks.

E^2 Bank Word-Program

The E^2 bank Word-Program operation consists of issuing the SDP Word-Program command, initiated by forcing BE#3 and WE# low and OE# high. The Word-Program command programs the desired addresses word-by-word. The words to be programmed must be in the erased state, prior to programming, unlike the Word-Write operation. During the Word-Program cycle, the addresses are latched by the falling edge of WE#. The data is latched by the rising edge of WE#. See Figure 11 for WE# or 12 for BE#3 controlled Program cycle timing waveforms, Table 7 for the command sequence and Figure 50 for a flowchart.

During the E^2 bank Erase or Program operation, the only valid reads from the bank are Data# Polling and Toggle Bit. Either Flash bank may be read.

The specified Bank- or Sector-Erase time is the only time required to erase. There are no preprogramming or other commands or cycles required either internally or externally to erase the bank or sector.

Erase Operations

The Bank-Erase is initiated by a specific six-word load sequence See Tables 6 and 7. A Bank-Erase will typically be less than 70 ms.

An alternative to the Bank-Erase in the Flash bank is the Block-Erase or Sector-Erase. The Block-Erase will erase an entire Block (32 KWords) in typically 15 ms. The Sector-Erase will erase an entire sector (1024 words) in typically 15 ms. The Sector-Erase provides a means to alter a single sector using the Sector-Erase and Word-Program modes. The Sector-Erase is initiated by a specific six-word load sequence, see Table 6.

The E^2 bank may also use a Sector-Erase, instead of Bank-Erase. An E^2 bank sector consists of 32 words that will typically erase in 7 ms. The Sector-Erase is initiated by a specific six-word load sequence, see Table 7. Sector- or Bank-Erase and Word-Program is an alternative to Word-Write as a means to alter the E^2 bank.

During any Sector-, Block-, or Bank-Erase within a bank, any other bank may be read. During the Word-Write of the E^2 bank, either Flash bank may be read.

Flash Bank Bank-Erase

The SST38VF166 provides a Flash Bank-Erase mode, which allows the user to clear the Flash bank to the "1" state. This is useful when the entire Flash must be quickly erased.

The software Flash Bank-Erase mode is initiated by issuing the specific six-word loading sequence, as in the Software Data Protection operation. After the loading cycle, the device enters into an internally timed cycle. See Table 6 for specific codes, Figure 13 or 16 for the timing waveform, and Figure 44 for a flowchart.

Flash Bank Block-Erase

The SST38VF166 provides a Block-Erase mode, which allows the user to clear any block in the Flash bank to the "1" state.

The software Block-Erase mode is initiated by issuing the specific six-word loading sequence, as in the Software Data Protect operation. After the loading cycle, the device enters into an internally timed Erase cycle. See Table 6 for specific codes, Figure 14 or 17 for the timing waveform, and Figure 45 for a flowchart. During the Erase operation, the only valid reads are Data# Polling and Toggle Bit from the selected bank, other banks may perform normal read.

Flash Bank Sector-Erase

The SST38VF166 provides a Sector-Erase mode, which allows the user to clear any sector in the Flash bank to the "1" state.

The software Sector-Erase mode is initiated by issuing the specific six-word loading sequence, as in the Software Data Protect operation. After the loading cycle, the device enters into an internally timed Erase cycle. See Table 6 for specific codes, Figure 15 or 18 for the timing waveform, and Figure 47 for a flowchart. During the Erase operation, the only valid reads are Data# Polling and Toggle Bit from the selected bank, other banks may perform normal read.

E^2 Bank Bank-Erase

The SST38VF166 provides a E^2 Bank-Erase mode, which allows the user to clear the E^2 bank to the "1" state. This is useful when the entire E^2 bank must be quickly erased. The E^2 bank Bank-Erase command is disabled if the E^2 bank OTP option is enabled.

The E^2 Bank-Erase mode is initiated by issuing the specific six-word loading sequence, as in the Software Data Protection operation. After the loading cycle, the device enters into an internally timed cycle. See Table 7 for specific codes, Figure 19 for the timing waveform, and Figure 44 for a flowchart.

E^2 Bank Sector-Erase

The SST38VF166 provides a Sector-Erase mode, which allows the user to clear any sector in the E^2 bank to the "1" state. The software Sector-Erase mode is initiated by issuing the specific six-word loading sequence, as in the Software Data Protect operation. After the loading cycle, the device enters into an internally timed. See Tables 6 and 7 for specific codes, Figure 20 for the timing waveform, and Figure 46 for a flowchart. During the Erase operation, the only valid reads are Data# Polling and Toggle Bit in the E^2 bank or normal read from either of the Flash banks.

Write Operation Status Detection

The SST38VF166 provides two software means to detect the completion of a E^2 bank or a Flash bank Program cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write Detection mode is enabled after the rising edge of WE#, which initiates the internal Write, Erase, or Program cycle.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system will possibly get an erroneous result, i.e. valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious device rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Additionally, a Write Status read may be executed to determine if any bank has an Erase, Program, or Write operation in progress. A Write Status read may be used when, for any reason, the system may have lost track of the status of a Write, Erase, or Program operation in any bank. Although normally, a Word-Write, Word-Program, Sector-Erase, or Block-Erase will be completed prior to recovery from a system reset, if a Bank-Erase was initiated prior to the reset, the system may need to verify the Bank-Erase is no longer in progress. Note, a Bank-Erase will not be performed on the bank containing the boot code, so there will

be no issue when recovering from the system reset. See Table 6 or 7 for the specific codes and Figure 40 for a timing waveform.

There is no provision to abort an Erase, Program, or Write operation, once initiated. For the SST SuperFlash technology, the associated Erase, Program, and Write times are so fast, relative to system reset times, there is no value in aborting the operation. Note, reads can always occur from any bank not performing an Erase, Program, or Write operation.

Should the system reset, while a Block- or Sector-Erase or Word-Program is in progress in the bank where the boot code is stored, the system must wait for the completion of the operation before reading that bank. Since the maximum time the system would have to wait is 25 ms (for a Block-Erase), the system ability to read the boot code would not be affected.

Data# Polling (DQ_7) - Flash Bank

When the SST38VF166 is in the internal Flash bank Program cycle, any attempt to read DQ_7 of the last word loaded during the Flash bank Word Load cycle will receive the complement of the true data. Once the Write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 21 or 22 for the Flash bank Data Polling timing waveforms and Figure 51 for a flowchart.

Data# Polling (DQ_7) - E^2 Bank

When the SST38VF166 is in the internal E^2 bank Write cycle, any attempt to read DQ_7 of the last word loaded during the E^2 bank Word Load cycle will receive the complement of the true data. Once the Write cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Figure 23 for E^2 bank Data Polling timing waveforms and Figure 51 for a flowchart.

Toggle Bit (DQ_6) - Flash Bank

During the Flash bank internal Write cycle, any consecutive attempts to read DQ_6 will produce alternating 0s and 1s, i.e. toggling between 0 and 1. When the Write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 24 or 25 for Flash bank Toggle Bit timing waveforms and Figure 51 for a flowchart.

Toggle Bit (DQ_6) - E^2 Bank

During the E^2 bank internal Write cycle, any consecutive attempts to read DQ_6 will produce alternating 0s and 1s, i.e. toggling between 0 and 1. When the Write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 26 for E^2 bank Toggle Bit timing waveforms and Figure 51 for a flowchart.

Data Protection

The SST38VF166 provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5 volts.

Write Inhibit Mode: Forcing OE# low, BE#1 and BE#2 high, or WE# high will inhibit the Write operation to the Flash bank. Forcing OE# low, BE#3 high, or WE# high will inhibit the Write operation to the E^2 bank. This prevents inadvertent writes during power-up or power-down.

A One Time Programmable E^2 Sector

The first sector of the E^2 bank offers the option of OTP (One Time Programmable) prevention of write for the first sector, i.e., addresses A_5 to A_{13} are “0” (0000H to 001FH). Once the OTP software instruction is executed, no Write, Erase, or Program operation can be performed on these 32 words. This is permanent and non-reversible. Additionally, if the OTP prevention is enabled, the Bank-Erase for the E^2 bank will not function. See Table 7 for specific codes and Figure 39 for a timing waveform.

Software Data Protection (SDP)

The SST38VF166 provides the JEDEC approved Software Data Protection scheme as a requirement for initiating a Write, Erase, or Program operation. With this scheme, any Write operation requires the inclusion of a series of three word-load operations to precede the Word-Write or Word-Program operation. The three-word load sequence is used to initiate the Write or Program cycle, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. The six-word sequence is required to initiate any Bank-, Block-, or Sector-Erase operation.

The requirements for JEDEC compliant SDP are in byte format. The SST38VF166 is organized by word; therefore, the contents of DQ_8 to DQ_{15} are "Don't Care" during any SDP (3-word or 6-word) command sequence.

During the SDP load command sequence, the SDP load cycle is suspended when WE# is high. This means a read may occur to any other bank during the SDP load sequence.

The SDP load sequence is bank specific, i.e., the same BE# must be low for each bus cycle. If the command sequence is aborted, e.g., a different BE# is brought low (except for Read operation with WE# high), an incorrect address is loaded, or incorrect data is loaded, the device will return to the Read mode within T_{RC} of execution of the load error.

Concurrent Read and Write Operations

The SST38VF166 provides the unique benefit of being able to read any bank, while simultaneously writing, erasing, or programming one other bank. This allows data alteration code to be executed from one bank, while altering the data in another bank. The following table lists all valid states.

TABLE 1: CONCURRENT READ/WRITE STATE

Flash Bank 1	Flash Bank 2	E^2 Bank
Read	No Operation	Write
Read	Write	No Operation
Write	Read	No Operation
No Operation	Read	Write
Write	No Operation	Read
No Operation	Write	Read

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Note: For the purposes of this table, write means to Word-Write; Block-, Sector-, or Chip-Erase; or Word-Program as applicable to the appropriate bank.

SST does not recommend that any two of the bank enable signals BE#1, BE#2 or BE#3 be simultaneously asserted.

The device will ignore all SDP commands and toggling of WE# when an Erase, Program, or Write operation is in progress. Note, both Product Identification and the Common Flash Interface entry commands use SDP; therefore, these commands will also be ignored while an Erase, Program, or Write operation is in progress.

Product Identification

The product identification mode identifies the device manufacturer as SST and provides a code to identify each bank. The manufacturer ID is the same for each bank; however, each bank has a separate device ID. Each bank is individually accessed using the applicable BE# and a software command. Users may wish to use the device ID operation to identify the write algorithm requirements for each bank. For details, see Table 6 or 7 for software operation and Figures 27, 28, or 29 for timing waveforms.

TABLE 2: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	00BFH
Device ID		
Flash Bank 1	0001H	2791H
Flash Bank 2	0001H	2792H
E^2 Bank	0001H	2793H

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Device IDs are unique to each bank. Should a chip ID be required, any of the bank IDs may be used as the chip ID. While in the read software ID mode or CFI mode, no other operation is allowed until after exiting these modes.

Product Identification Mode Exit

In order to return to the standard Read mode, the Product Identification mode must be exited. Exit is accomplished by issuing the Software ID exit command, which returns the device to normal operation. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. For details, see Table 6 or 7 for software operation and Figures 30, 31, or 32 for timing waveforms.

Common Flash Interface (CFI)

The SST38VF166 also contains the CFI information in each bank, to describe the characteristics of that bank. See Tables 8 through 16 for the CFI contents for each bank. Both flash banks use the same information, as each bank operates the same. The E^2 bank contains the applicable information for that bank.

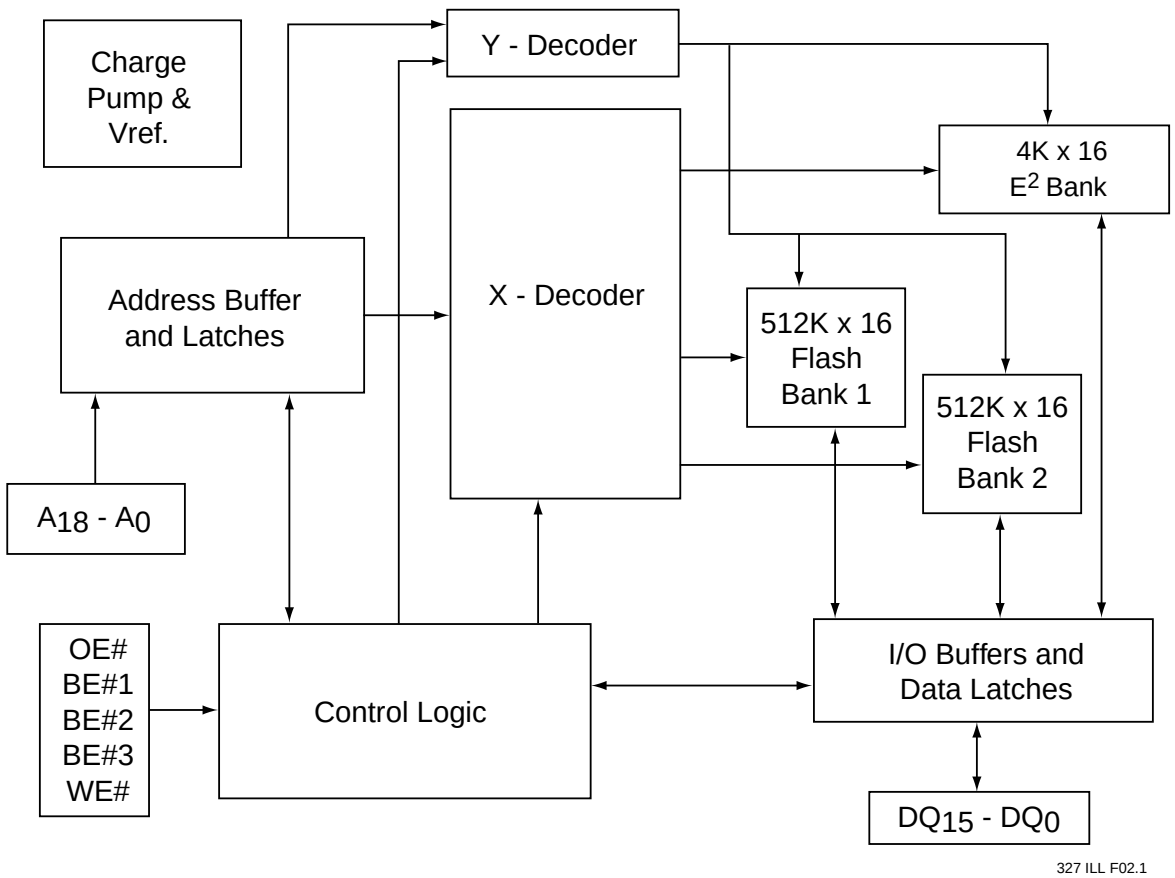
In order to obtain the CFI information, the CFI memory space is accessed by using the CFI entry command. For details, see Table 6 or 7 for software operation and Figures 33, 34, or 35 for timing waveforms.

CFI Mode Exit

In order to return to the standard Read mode, the CFI mode must be exited. Exit is accomplished by issuing the CFI exit command, which returns the device to normal operation. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. For details, see Table 6 or 7 for software operation and Figures 36, 37, or 38 for timing waveforms.

CFI is specified for byte wide information. Since the SST38VF166 is organized word wide, the first byte (2 nibbles) of each CFI word is always 00H.

FUNCTIONAL BLOCK DIAGRAM



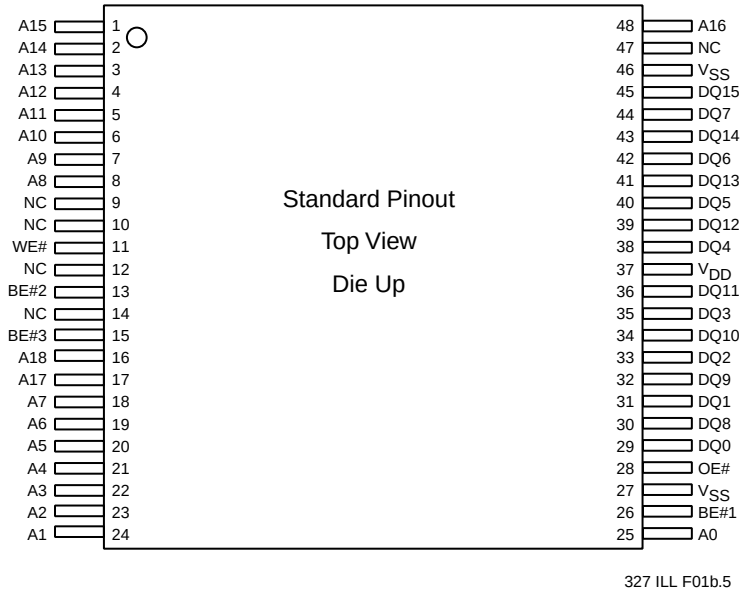


FIGURE 1: PIN ASSIGNMENTS FOR 48-PIN TSOP (12MM X 20MM)

TABLE 3: PIN DESCRIPTION

Symbol	Name	Functions
A_{18}-A_0	Flash Bank Addresses	To provide Flash Bank addresses
A_{11}-A_0	E^2 Bank Addresses	To provide E^2 Bank addresses
A_{18}-A_{15}	Flash Bank Block Addresses	To select a Flash Bank Block for erase
A_{18}-A_{10}	Flash Bank Sector Addresses	To select a Flash Bank Sector for erase
A_{11}-A_5	E^2 Bank Sector Addresses	To select an E^2 Bank Sector for erase
DQ_{15}-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high or BE#1, BE#2, and BE#3 are high.
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable 1	To control the Write, Erase, or Program operations
V_{DD}	Power Supply	To provide 2.7-3.6V power supply
V_{SS}	Ground	
NC	No Connect	Unconnected pins

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TABLE 4: OPERATION MODES SELECTION FOR FLASH BANK

Array Operation Mode	BE#1	BE#2	BE#3	OE#	WE#	DQ	Address
Read							
Flash Bank 1	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Flash Bank 2	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Block-Erase							
Flash Bank 1	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Flash Bank 2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Sector-Erase							
Flash Bank 1	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Flash Bank 2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Program							
Flash Bank 1	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Flash Bank 2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Standby	V_{IH}	V_{IH}	V_{IH}	X	X	High Z	X
Write Inhibit							
Flash Bank 1	V_{IH}	X	X	V_{IL}	V_{IH}	X	X
Flash Bank 2	X	V_{IH}	X	V_{IL}	V_{IH}	X	X
Flash Bank-Erase							
Flash Bank 1	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Flash Bank 2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Status Operation Mode	**BE#1**	**BE#2**	**BE#3**	**OE#**	**WE#**	**DQ**	**Address**
Write Status Read	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}[1]	5XXXXH
Illegal State	V_{IL}	V_{IL}	V_{IL}	X	X	High Z	X[2]
Illegal State	V_{IL}	V_{IL}	X	X	X	High Z	X[2]
Illegal State	V_{IL}	X	V_{IL}	X	X	High Z	X[2]
Illegal State	X	V_{IL}	V_{IL}	X	X	High Z	X[2]
Product Identification							
Flash Bank 1	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	See Tables 6 and 7
Flash Bank 2	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	See Tables 6 and 7
Common Flash Interface							
Flash Bank 1	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	See Tables 6 and 7
Flash Bank 2	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	See Tables 6 and 7

T4.5 327

1. If Flash Bank 1 is writing, DQ_1 is low. If Flash Bank 2 is writing, DQ_2 is low. If E^2 Bank is writing, DQ_3 is low.
2. Entering an illegal state during an Erase, Program, or Write operation will not affect the operation, i.e., the erase, program, or write will continue to normal completion.

TABLE 5: OPERATION MODES SELECTION FOR E^2 BANK

Read Operation Mode	BE#1	BE#2	BE#3	OE#	WE#	DQ	Address
Read E^2 Bank	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}[1]	
Write E^2 Bank	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Sector-Erase E^2 Bank	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Program E^2 Bank	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Standby	V_{IH}	V_{IH}	V_{IH}	X	X	D_{IN}	See Tables 6 and 7
Write Inhibit E^2 Bank	X	X	V_{IH}	V_{IL}	V_{IH}	High Z	X
Erase E^2 Bank	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
OTP Enable E^2 Bank	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Tables 6 and 7
Status Operation Mode	**BE#1**	**BE#2**	**BE#3**	**OE#**	**WE#**	**DQ**	**Address**
Write Status Read	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}[2]	5XXXXH
Illegal State	V_{IL}	V_{IL}	V_{IL}	X	X	High Z	X[3]
Illegal State	V_{IL}	V_{IL}	X	X	X	High Z	X[3]
Illegal State	V_{IL}	X	V_{IL}	X	X	High Z	X[3]
Illegal State	X	V_{IL}	V_{IL}	X	X	High Z	X[3]
Product Identification							
E^2 Bank	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	See Tables 6 and 7
Common Flash Interface							
E^2 Bank	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	See Tables 6 and 7

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1. A_{11}-A_0 are valid addresses; A_{15}-A_{12} are “Don’t Care”; A_{18}-A_{16} cannot be 5H
2. If Flash Bank 1 is writing, DQ_1 is low. If Flash Bank 2 is writing, DQ_2 is low. If E^2 Bank is writing, DQ_3 is low.
3. Entering an illegal state during an Erase, Program, or Write operation will not affect the operation, i.e., the erase, program, or write will continue to normal completion.

TABLE 6: SOFTWARE COMMAND SEQUENCE FOR FLASH BANKS

Command Code	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H	[3]					
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H	[4]					
Flash Bank Word-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA[5]	Data In				
Flash Bank Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA[6]	30H
Flash Bank Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA[6]	50H
Flash Bank Bank-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
CFI Entry	5555H	AAH	2AAAH	55H	5555H	98H	[7]					
CFI Exit	5555H	AAH	2AAAH	55H	5555H	F0H	[4]					

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1. Command Code Address format A_{14}-A_0 (Hex), Addresses > A_{14} are “Don’t Care” for Command sequences
2. Data format DQ_7 -DQ_0 (Hex), DQ_{15} - DQ_8 are “Don’t Care”
3. With A_{14}-A_1 = 0; SST Manufacturer’s ID = 00BFH, is read with A_0 = 0
   SST38VF166 Device ID = 2791H, 2792H, and 2793H is read with A_0 = 1 for the applicable BE# active
4. The device does not remain in Software Product ID Mode or CFI Mode if powered down.
5. WA = Word address
6. SA = Sector address
   BA = Block address
7. There is a separate CFI for each bank. See Tables 8 through 16

TABLE 7: SOFTWARE COMMAND SEQUENCE FOR E^2 BANKS

Command Code	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H	[3]					
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H	[4]					
E^2 Bank Word-Write	5555H	AAH	2AAAH	55H	5555H	A0H	WA[5]	Data In				
E^2 Bank Word-Program	5555H	AAH	2AAAH	55H	5555H	A5H	WA[5]	Data In				
E^2 Bank Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA[6]	30H
E^2 Bank Bank-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
E^2 Bank OTP Enable	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	70H
CFI Entry	5555H	AAH	2AAAH	55H	5555H	98H	[7]					
CFI Exit	5555H	AAH	2AAAH	55H	5555H	F0H	[4]					

T7.4 327

1. Command Code Address format A_{14}-A_0 (Hex), Addresses > A_{14} are “Don’t Care” for Command sequences
2. Data format DQ_7 -DQ_0 (Hex), DQ_{15} - DQ_8 are “Don’t Care”
3. With A_{14}-A_1 = 0; SST Manufacturer’s ID = 00BFH, is read with A_0 = 0
   SST38VF166 Device ID = 2791H, 2792H, and 2793H is read with A_0 = 1 for the applicable BE# active
4. The device does not remain in Software Product ID Mode or CFI Mode if powered down.
5. WA = Word address
6. SA = Sector address
7. There is a separate CFI for each bank. See Tables 8 through 16

TABLE 8: CFI QUERY IDENTIFICATION STRING FOR FLASH BANK 1

Address	Data	Data
10H	0051H	Query Unique ASCII string “QRY”
11H	0052H	
12H	0059H	
13H	0001H	Primary OEM command set (JEP-137)
14H	0008H	
15H	0000H	Address for Primary Extended Table (00H = none exists)
16H	0000H	
17H	0000H	Alternate OEM command set (00H = none exists)
18H	0000H	
19H	0000H	Address for Alternate OEM extended Table (00H = none exits)
1AH	0000H	

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TABLE 9: SYSTEM INTERFACE INFORMATION FOR FLASH BANK 1

Address	Data	Data
1BH	0027H	V_{DD} Min (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1CH	0036H	V_{DD} Max (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1DH	0000H	V_{PP} min. (00H = no V_{PP} pin)
1EH	0000H	V_{PP} max. (00H = no V_{PP} pin)
1FH	0004H	Typical time out for Word-Program 2^N µs
20H	0000H	Typical time out for min. size Page-Write 2^N µs (00H = not supported)
21H	0004H	Typical time out for individual Sector-Erase 2^N ms
22H	0006H	Typical time out for Bank-Erase 2^N ms
23H	0001H	Maximum time out for Word-Program 2^N times typical
24H	0000H	Maximum time out for Page-Write 2^N times typical (00H = not supported)
25H	0001H	Maximum time out for individual Sector-Erase 2^N times typical
26H	0001H	Maximum time out for Chip-Erase 2^N times typical

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TABLE 10: DEVICE GEOMETRY INFORMATION FOR FLASH BANK 1

Address	Data	Data
27H	0014H	Bank size = 2^N Byte (14H > 2^{20} = 1 MByte = 8 Mbits)
28H	0001H	Flash Bank Device Interface description (Refer to CFI JESD-68) (x16 asynchronous)
29H	0000H	
2AH	0000H	Maximum number of bytes in Page-Write = 2^N (00H = not supported)
2BH	0000H	
2CH	0002H	Number of Erase Block Regions within device
2DH	00FFH	Erase Block Region 1 Information (Sector)
2EH	0001H	(Refer to the CFI specification or JESD-68)
2FH	0008H	y = 511 + 1 = 512 sectors (01FFH = 511)
30H	0000H	z = 2 KBytes/sector = 8 x 256 Bytes
31H	000FH	Erase Block Region 2 Information (Block)
32H	0000H	(Refer to the CFI specification or JESD-68)
33H	0000H	y = 15 + 1 = 16 blocks
34H	0001H	z = 64 KBytes/block = 256 x 256 Bytes (0100H = 64K)

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TABLE 11: CFI QUERY IDENTIFICATION STRING FOR FLASH BANK 2

Address	Data	Data
10H	0051H	Query Unique ASCII string “QRY”
11H	0052H	
12H	0059H	
13H	0001H	Primary OEM command set (JEP-137)
14H	0008H	
15H	0000H	Address for Primary Extended Table (00H = none exists)
16H	0000H	
17H	0000H	Alternate OEM command set (00H = none exists)
18H	0000H	
19H	0000H	Address for Alternate OEM extended Table (00H = none exits)
1AH	0000H	

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TABLE 12: SYSTEM INTERFACE INFORMATION FOR FLASH BANK 2

Address	Data	Data
1BH	0027H	V_{DD} Min (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1CH	0036H	V_{DD} Max (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1DH	0000H	V_{PP} min. (00H = no V_{PP} pin)
1EH	0000H	V_{PP} max. (00H = no V_{PP} pin)
1FH	0004H	Typical time out for Word-Program 2^N µs
20H	0000H	Typical time out for min. size Page-Write 2^N µs (00H = not supported)
21H	0004H	Typical time out for individual Sector-Erase 2^N ms
22H	0006H	Typical time out for Bank-Erase 2^N ms
23H	0001H	Maximum time out for Word-Program 2^N times typical
24H	0000H	Maximum time out for Page-Write 2^N times typical (00H = not supported)
25H	0001H	Maximum time out for individual Sector-Erase 2^N times typical
26H	0001H	Maximum time out for Chip-Erase 2^N times typical

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TABLE 13: DEVICE GEOMETRY INFORMATION FOR FLASH BANK 2

Address	Data	Data
27H	0014H	Bank size = 2^N Byte (14H > 2^{20} = 1 MByte = 8 Mbits)
28H	0001H	Flash Bank Device Interface description (Refer to CFI JESD-68) (x16 asynchronous)
29H	0000H	
2AH	0000H	Maximum number of bytes in Page-Write = 2^N (00H = not supported)
2BH	0000H	
2CH	0002H	Number of Erase Block Regions within device
2DH	00FFH	Erase Block Region 1 Information (Sector)
2EH	0001H	(Refer to the CFI specification or JESD-68)
2FH	0008H	y = 511 + 1 = 512 sectors (01FFH = 511)
30H	0000H	z = 2 KBytes/sector = 8 x 256 Bytes
31H	000FH	Erase Block Region 2 Information (Block)
32H	0000H	(Refer to the CFI specification or JESD-68)
33H	0000H	y = 15 + 1 = 16 blocks
34H	0001H	z = 64 KBytes/block = 256 x 256 Bytes (0100H = 64K)

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TABLE 14: CFI QUERY IDENTIFICATION STRING FOR E^2 BANK

Address	Data	Data
10H	0051H	Query Unique ASCII string “QRY”
11H	0052H	
12H	0059H	
13H	0001H	Primary OEM command set (JEP-137)
14H	0009H	
15H	0000H	Address for Primary Extended Table (00H = none exists)
16H	0000H	
17H	0000H	Alternate OEM command set (00H = none exists)
18H	0000H	
19H	0000H	Address for Alternate OEM extended Table (00H = none exits)
1AH	0000H	

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TABLE 15: SYSTEM INTERFACE INFORMATION FOR E^2 BANK

Address	Data	Data
1BH	0027H	V_{DD} Min (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1CH	0036H	V_{DD} Max (Program/Erase) DQ_7-DQ_4: Volts, DQ_3-DQ_0: 100 millivolts
1DH	0000H	V_{PP} min. (00H = no V_{PP} pin)
1EH	0000H	V_{PP} max. (00H = no V_{PP} pin)
1FH	0005H	Typical time out for Word-Program 2^N µs
20H	0000H	Typical time out for min. size Page-Write 2^N µs (00H = not supported)
21H	0003H	Typical time out for individual Sector-Erase 2^N ms
22H	0006H	Typical time out for Bank-Erase 2^N ms
23H	0001H	Maximum time out for Word-Program 2^N times typical
24H	0000H	Maximum time out for Page-Write 2^N times typical (00H = not supported)
25H	0001H	Maximum time out for individual Sector-Erase 2^N times typical
26H	0001H	Maximum time out for Chip-Erase 2^N times typical

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TABLE 16: DEVICE GEOMETRY INFORMATION FOR E^2 BANK

Address	Data	Data
27H	000DH	Device size = 2^N Byte (DH > 2^{13} = 8 KBytes = 64 Kbits)
28H	0001H	Flash Bank Device Interface description (Refer to CFI JESD-68) (x16 asynchronous)
29H	0000H	
2AH	0001H	Maximum number of bytes in Page-Write = 2^N (00H = not supported)
2BH	0000H	
2CH	0001H	Number of Erase Block Regions within device
2DH	007FH	Erase Block Region 1 Information (Sector)
2EH	0000H	(Refer to the CFI specification or JESD-68)
2FH	0001H	y = 127 + 1 = 128 sectors (007FH = 127)
30H	0000H	z = 32 Bytes/sector = 1 x 256 Bytes

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to V_{DD} + 1.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current[1] . . . . . 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE:

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 10 ns
Output Load . . . . . C_L = 30 pF
See Figures 42 and 43

TABLE 17: DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.6V

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min $V_{DD}=V_{DD}$ Max
	Read		35	mA	BE#1,BE#2, or BE#3=V_{IL}, WE#=V_{IH}, all I/Os open
	Write: Flash Bank		40	mA	BE#1/2=WE#=V_{IL}, OE#=V_{IH} $V_{DD}=V_{DD}$ Max or E^2 Bank BE#3=WE#=V_{IL}, OE#=V_{IH} $V_{DD}=V_{DD}$ Max
	Read: Flash Bank plus Write/Program/Erase: E2 Bank or Flash Bank		75	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min WE#=V_{IH}, $V_{DD}=V_{DD}$ Max BE#1,BE#2, or BE#3=V_{IL}, OE#=WE#=V_{IH},
I_{SB}	Standby V_{DD} Current (CMOS inputs)		50	µA	BE#1,BE#2, or BE#3=V_{IHC}, V_{DD} = V_{DD} Max
I_{ALP}	Auto Low Power Mode (CMOS inputs)		50	µA	BE#1,BE#2, or BE#3=V_{ILC}, WE#= V_{IHC}, all I/Os open, Address input = V_{IHC}/V_{IHC} and static $V_{DD}=V_{DD}$ Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{DD}, V_{DD} = V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{DD}, V_{DD} = V_{DD} Max
V_{IL}	Input Low Voltage		0.3V_{DD}	V	V_{DD} = V_{DD} Min
V_{ILC}	Input Low Voltage (CMOS)		0.2	V	
V_{IH}	Input High Voltage	0.7V_{DD}		V	V_{DD} = V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.2		V	V_{DD} = V_{DD} Max
V_{OL}	Output Low Voltage		0.2	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2		V	I_{OH} = -100 µA, V_{DD} = V_{DD} Min

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TABLE 18: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T18.1 327

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 19: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 20: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance - Flash Bank Endurance - E2 Bank	10,000 100,000	Cycles/Sector Cycles/Word	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T20.0 327

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 21: READ CYCLE TIMING PARAMETERS

Symbol	Parameter	SST38VF166-70		Units
		Min	Max	
T_{RC}	Read Cycle Time	70		ns
T_{BE}	Bank Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		30	ns
T_{CLZ}[1]	CE# Low to Active Output	0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		ns
T_{CHZ}[1]	CE# High to High-Z Output		20	ns
T_{OHZ}[1]	OE# High to High-Z Output		20	ns
T_{OH}[1]	Output Hold from Address Change	0		ns

T21.1 327

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 22: WRITE, ERASE, PROGRAM CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{WC}	Word-Write Cycle (Erase and Program)		12.5	ms
T_{BPE}	Word-Program Time - E^2 Bank		40	µs
T_{BPF}	Word-Program Time - Flash Bank		20	µs
T_{SEF}	Sector-Erase Time - Flash Bank		25	ms
T_{LEF}	Block-Erase Time - Flash Bank		25	ms
T_{BEF}	Bank-Erase Time - Flash Bank		100	ms
T_{SEE}	Sector-Erase Time - E^2 Bank		12.5	ms
T_{BEE}	Bank-Erase Time - E^2 Bank		100	ms
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{BES}	BE# Setup Time	0		ns
T_{BEH}	BE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	0		ns
T_{WP}	Write Pulse Low Width	40		ns
T_{WPH}	Write Pulse High Time	30		ns
T_{DS}	Data Setup Time	40		ns
T_{DH}	Data Hold Time	0		ns
T_{VDDR}[1]	V_{DD} Rise Time	0.1	50	ms
T_{DBR}	Time to DATA# Polling Read	35		ns
T_{TBR}	Time to Toggle Bit Read	35		ns
T_{IDA}	Time to ID or CFI Read/Exit Cycle		150	ns
T_{BS}	Bank Enable Setup Time for Concurrent Operation	0		ns

T22.0 327

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TIMING DIAGRAMS **Address and data format are in hexadecimal**

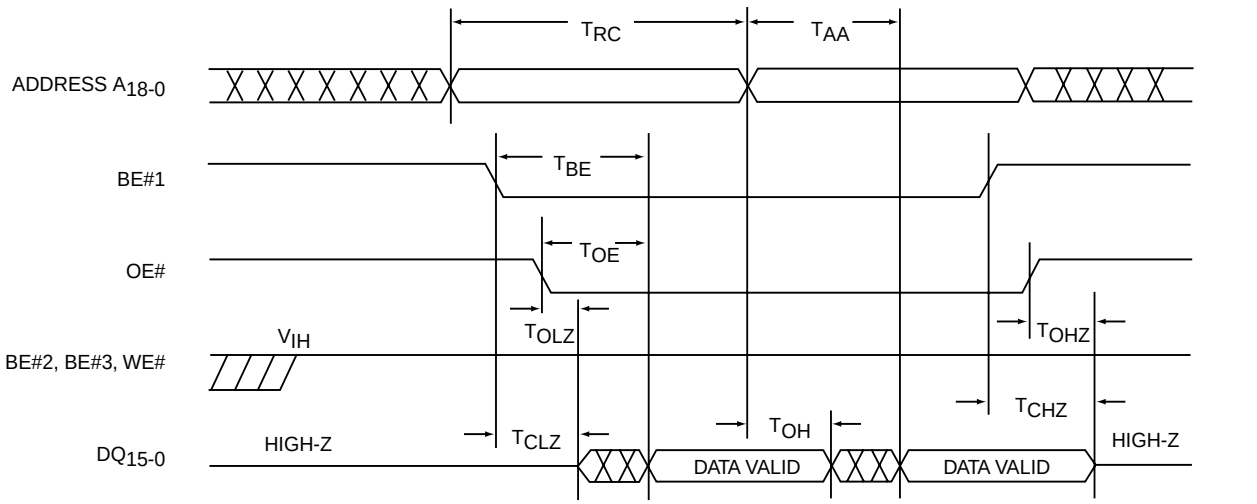


FIGURE 2: FLASH BANK 1, READ CYCLE TIMING DIAGRAM

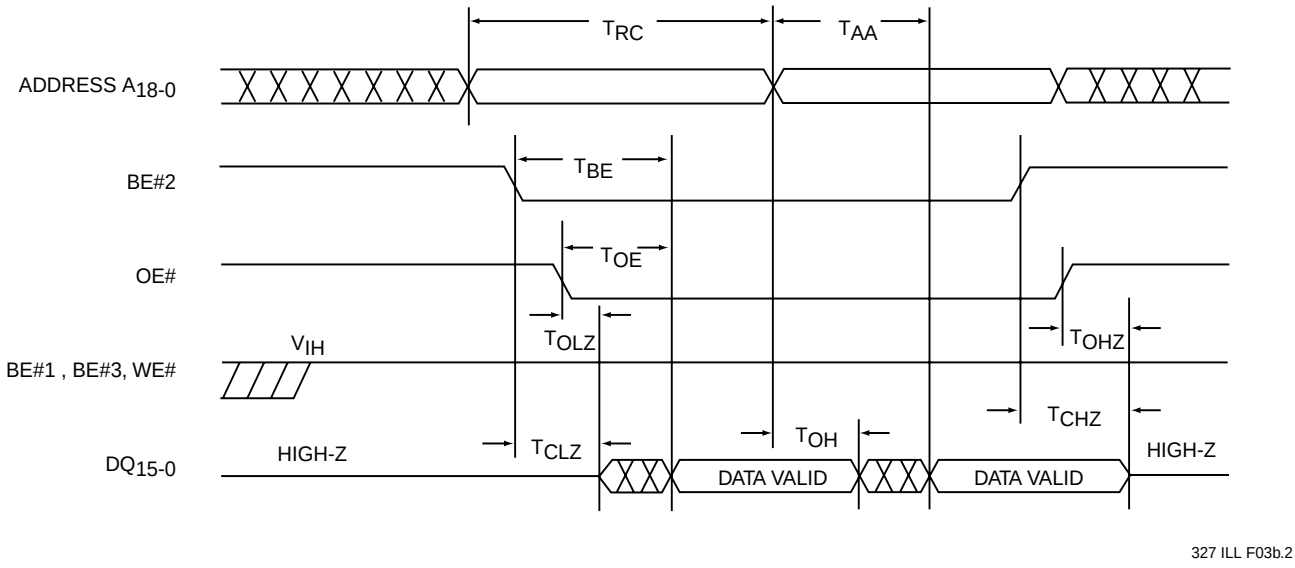


FIGURE 3: FLASH BANK 2, READ CYCLE TIMING DIAGRAM

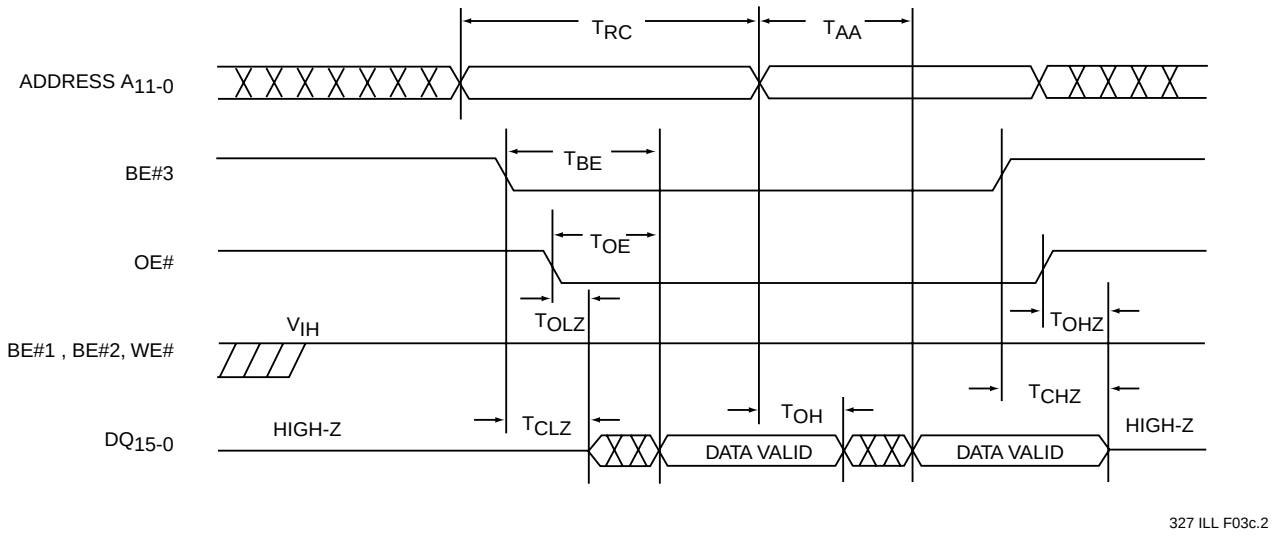


FIGURE 4: E² BANK, READ CYCLE TIMING DIAGRAM

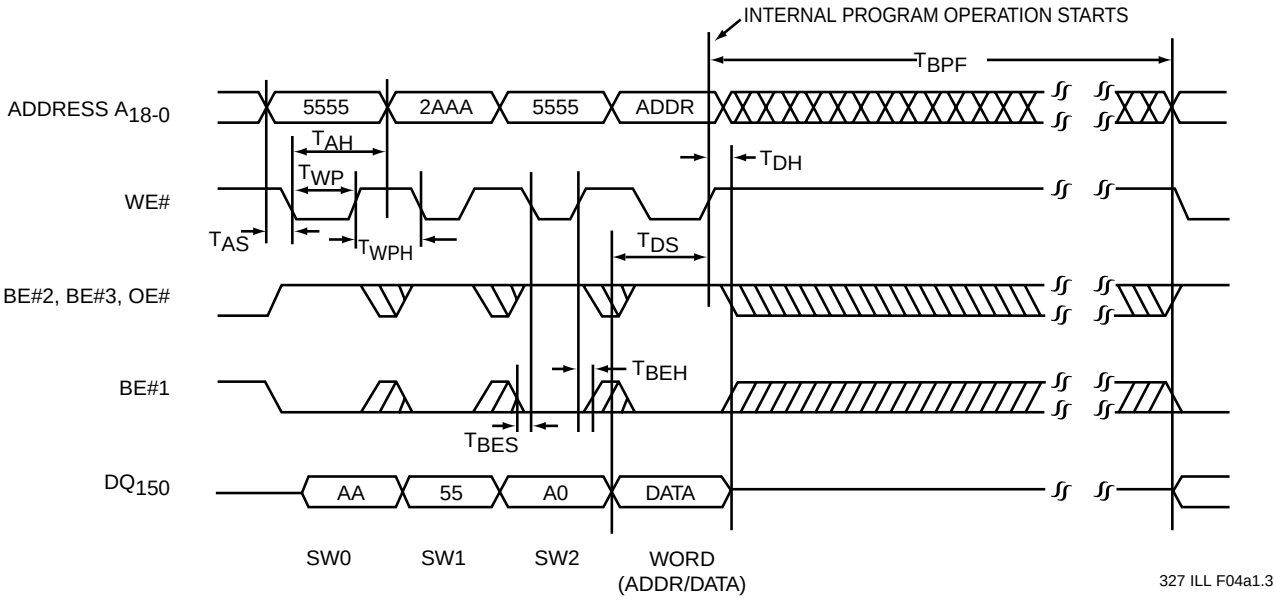


FIGURE 5: FLASH BANK 1, WE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM

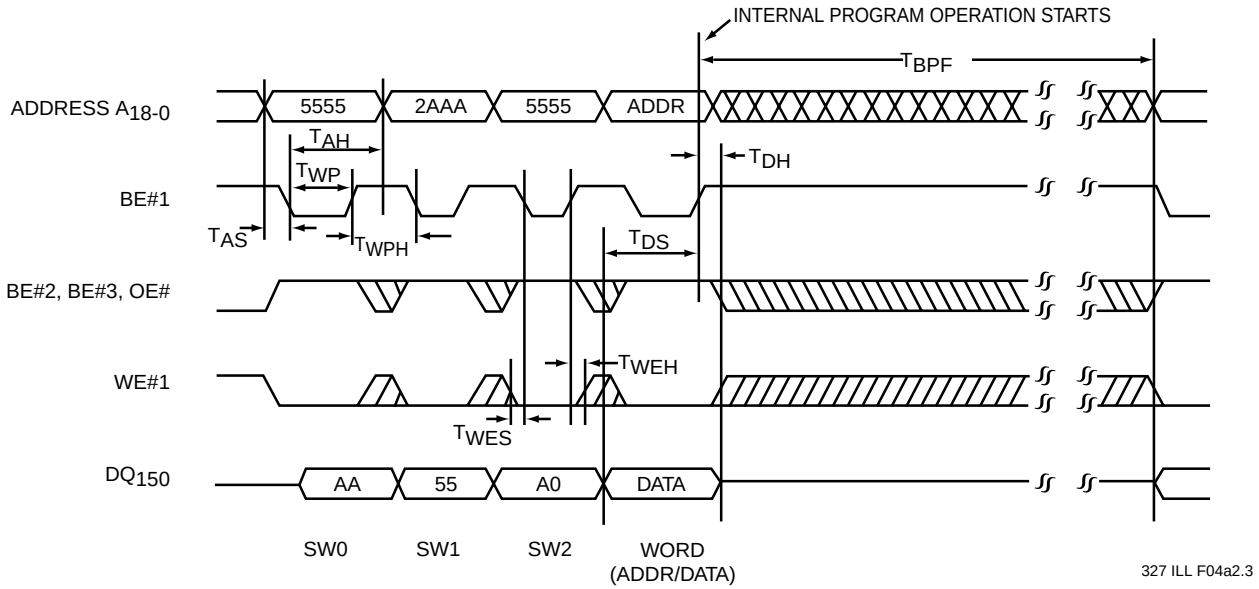


FIGURE 6: FLASH BANK 1, BE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM

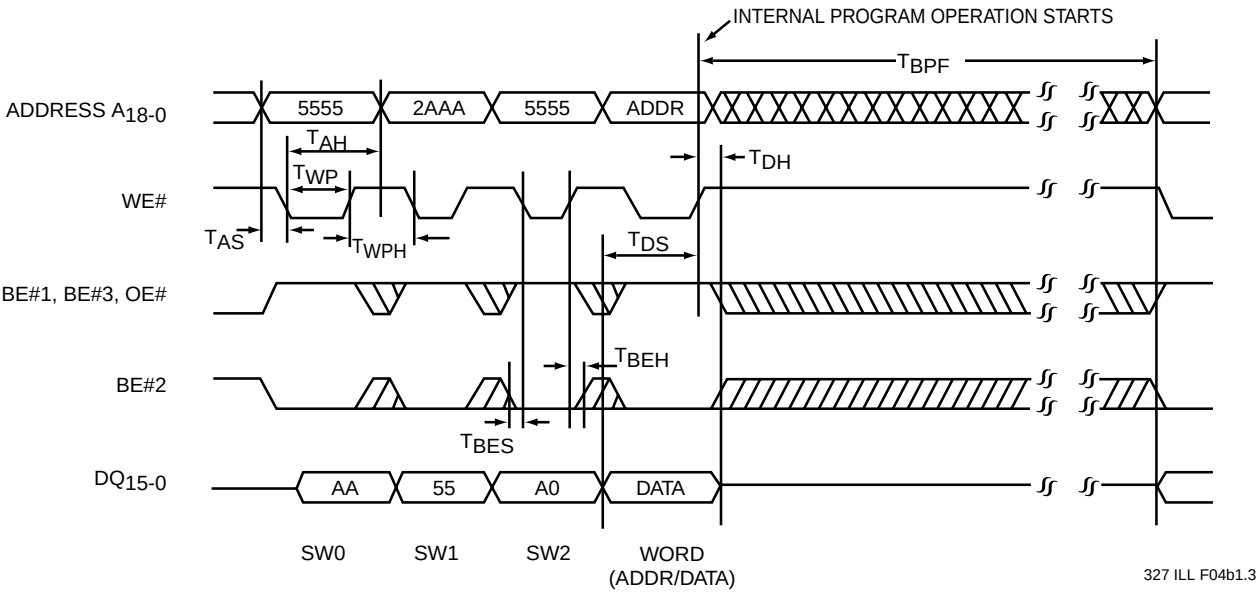


FIGURE 7: FLASH BANK 2, WE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM

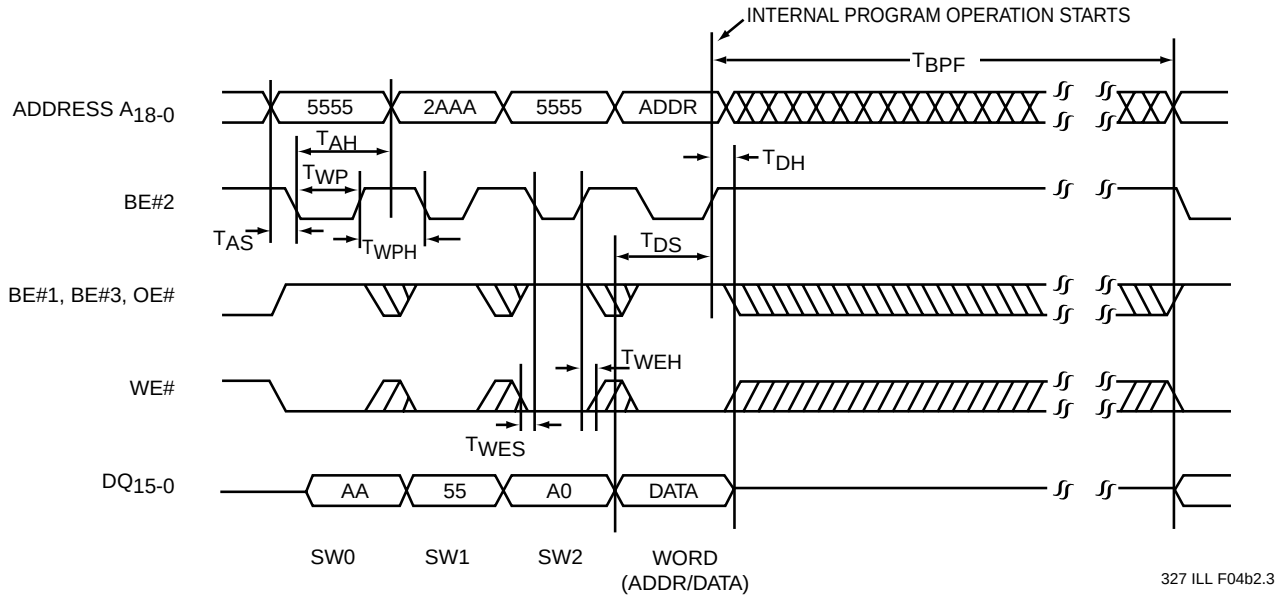


FIGURE 8: FLASH BANK 2, BE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM

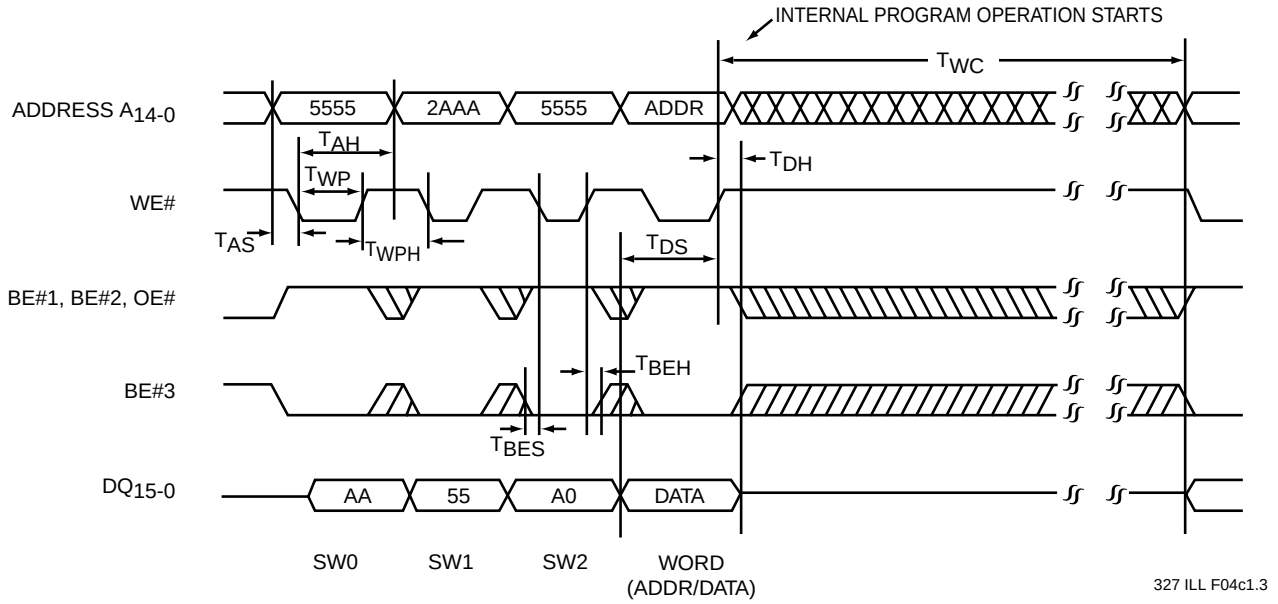


FIGURE 9: E2 BANK, WE# CONTROLLED WORD-WRITE CYCLE TIMING DIAGRAM

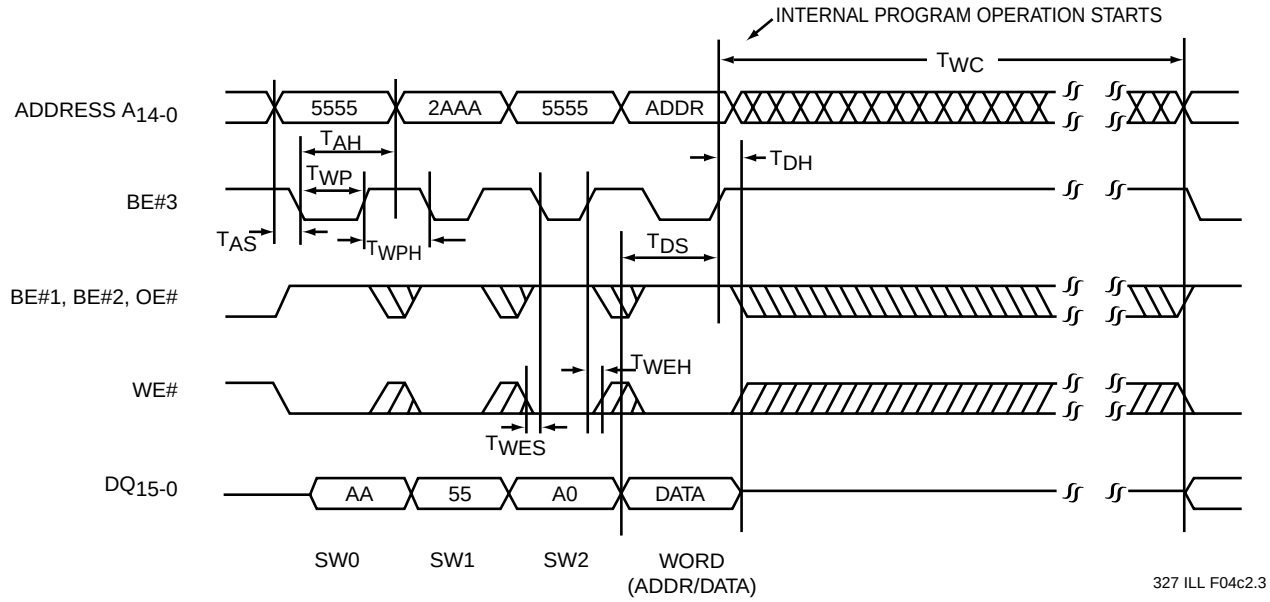


FIGURE 10: E² BANK, BE# CONTROLLED WORD-WRITE CYCLE TIMING DIAGRAM

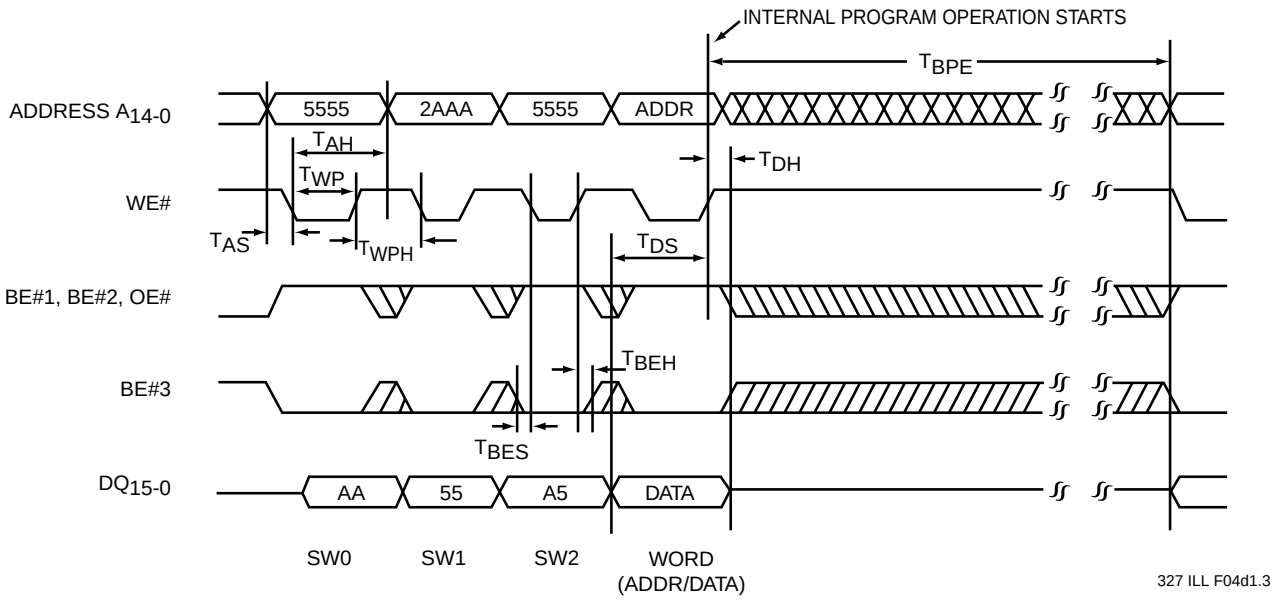


FIGURE 11: E² BANK, WE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM

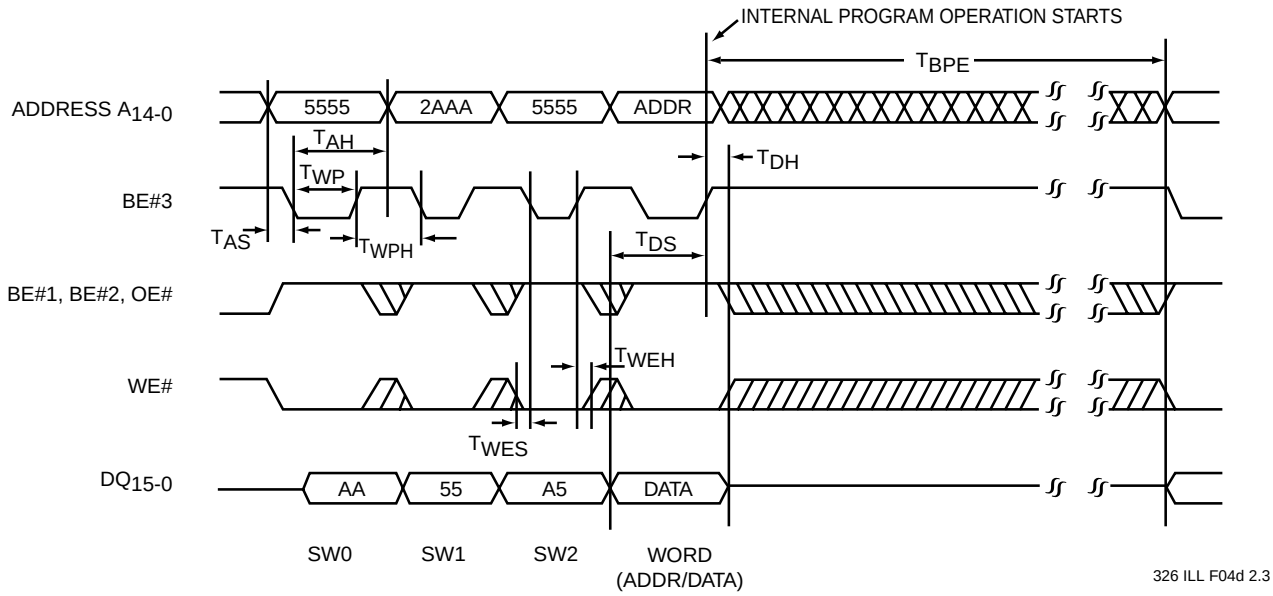


FIGURE 12: E² BANK, BE# CONTROLLED WORD-PROGRAM CYCLE TIMING DIAGRAM

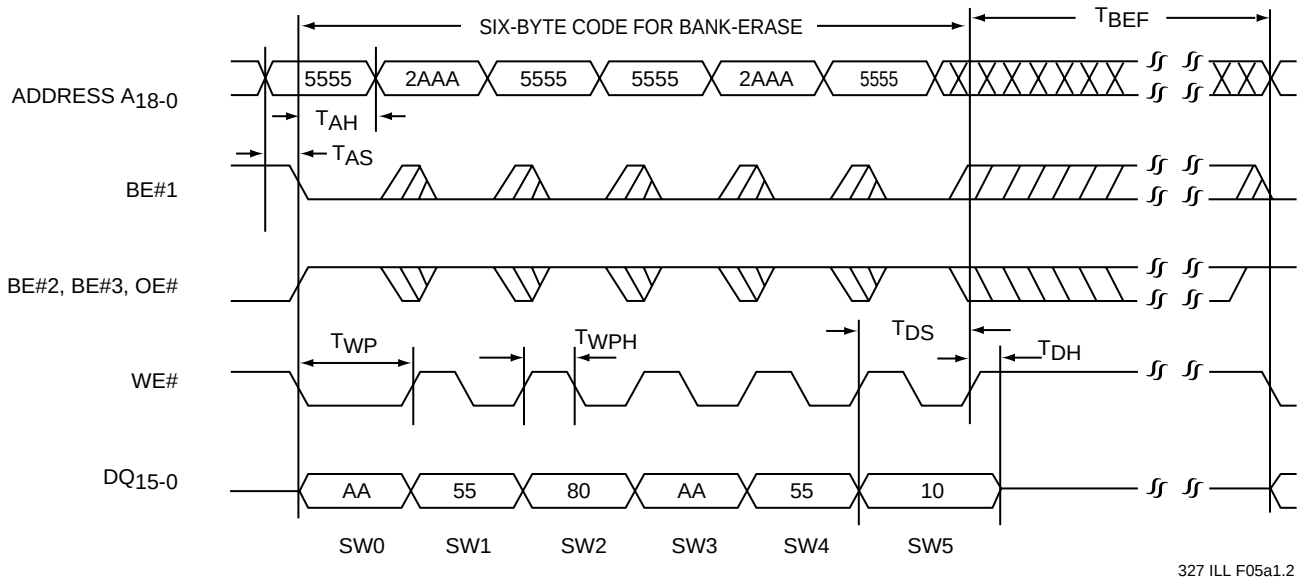


FIGURE 13: FLASH BANK 1, BANK-ERASE TIMING DIAGRAM

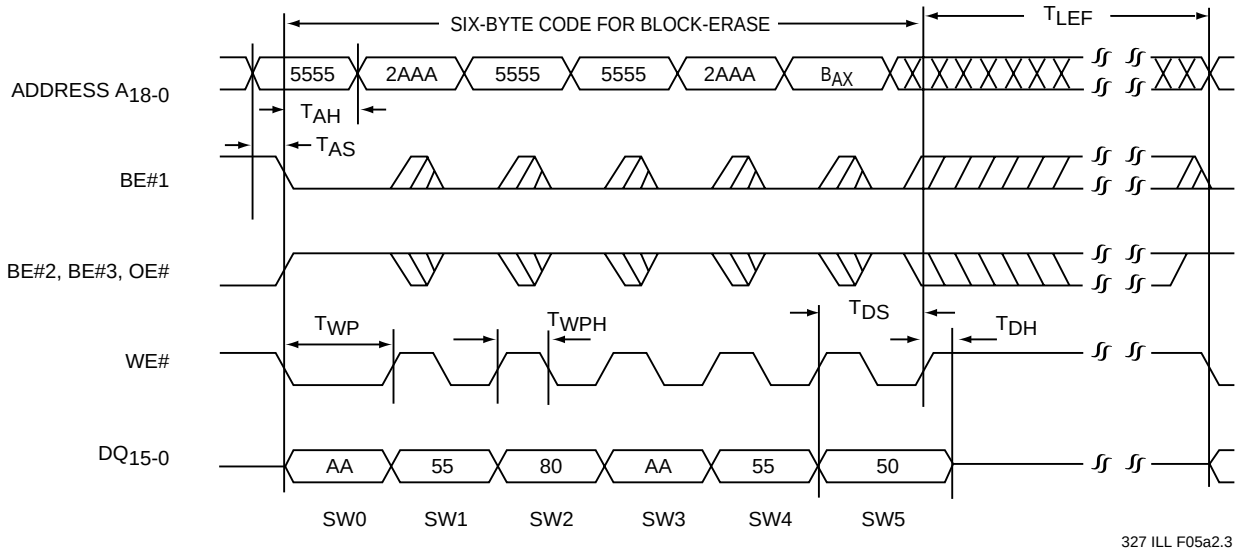


FIGURE 14: FLASH BANK 1, BLOCK-ERASE TIMING DIAGRAM

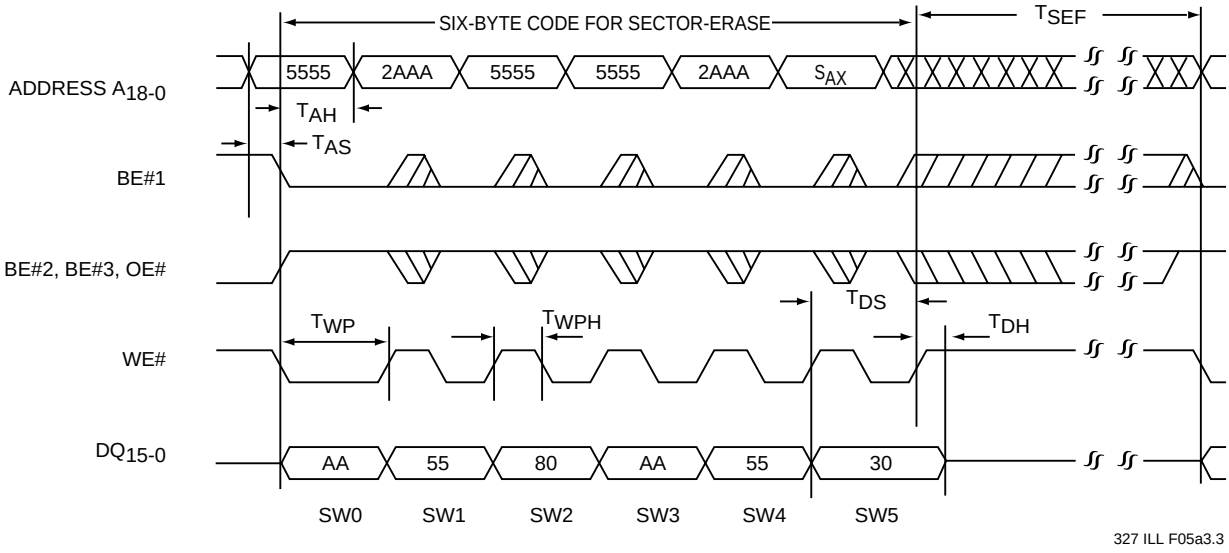


FIGURE 15: FLASH BANK 1, SECTOR-ERASE TIMING DIAGRAM

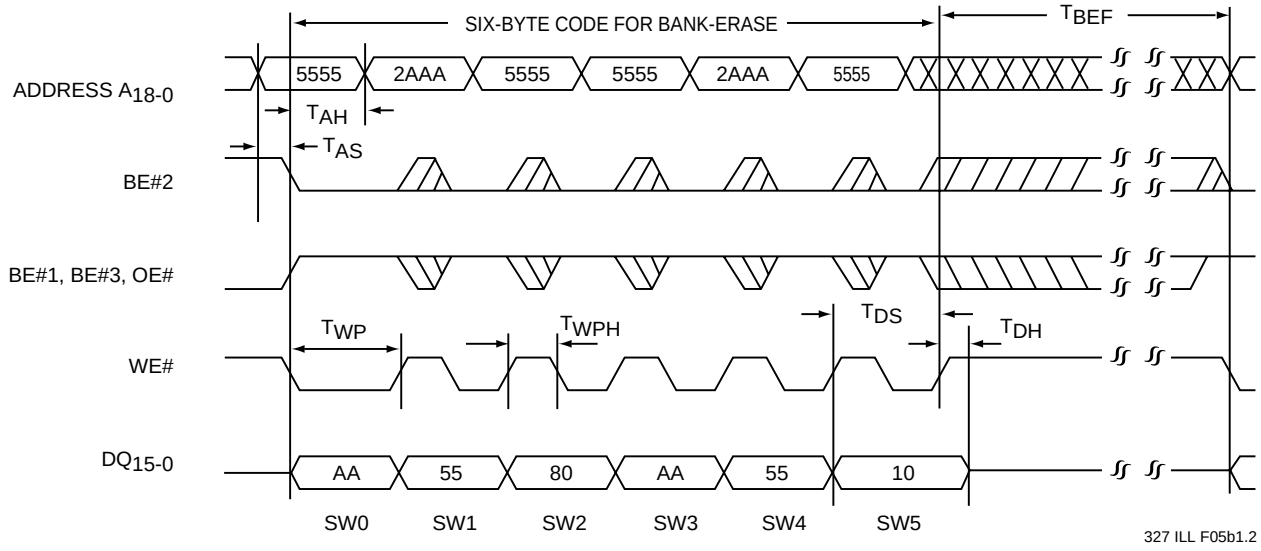


FIGURE 16: FLASH BANK 2, BANK-ERASE TIMING DIAGRAM

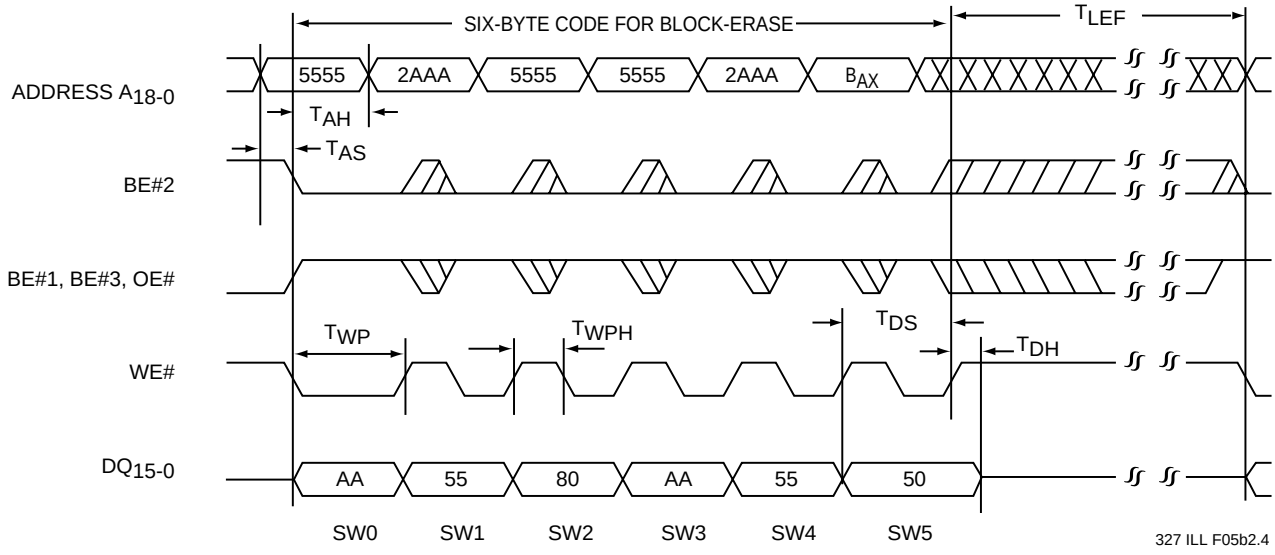


FIGURE 17: FLASH BANK 2, BLOCK-ERASE TIMING DIAGRAM

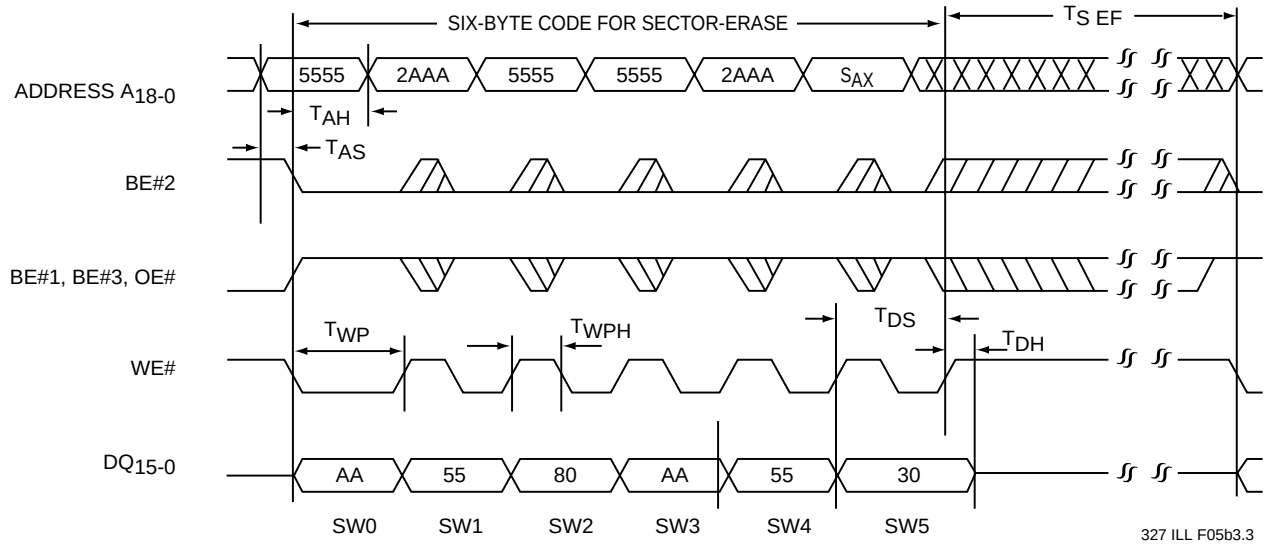


FIGURE 18: FLASH BANK 2, SECTOR-ERASE TIMING DIAGRAM

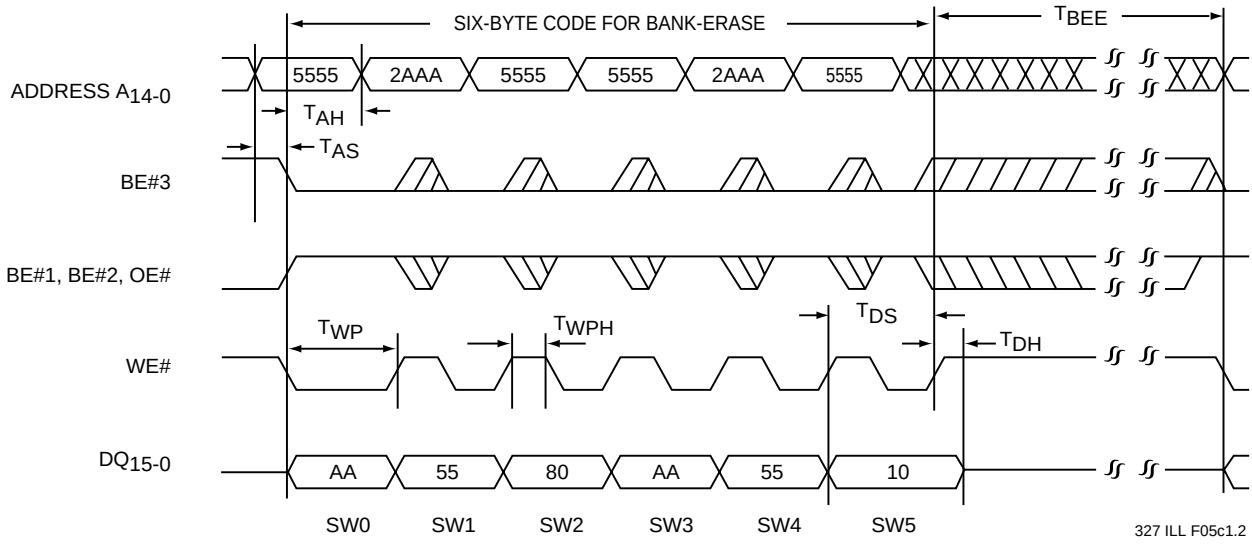


FIGURE 19: E2 BANK, BANK-ERASE TIMING DIAGRAM

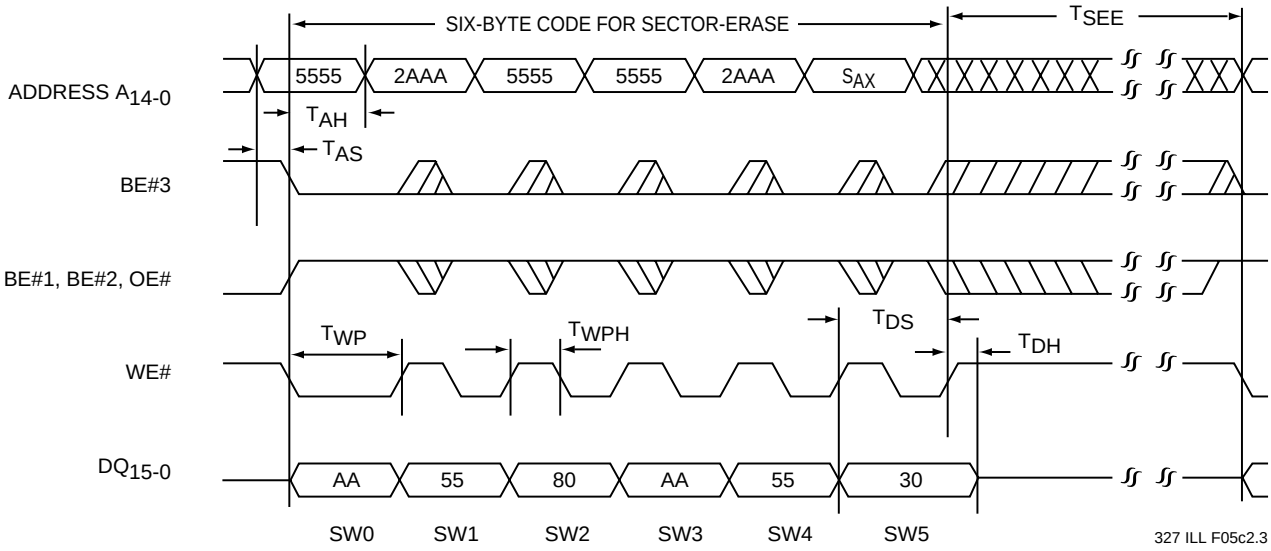


FIGURE 20: E2 BANK, SECTOR-ERASE TIMING DIAGRAM

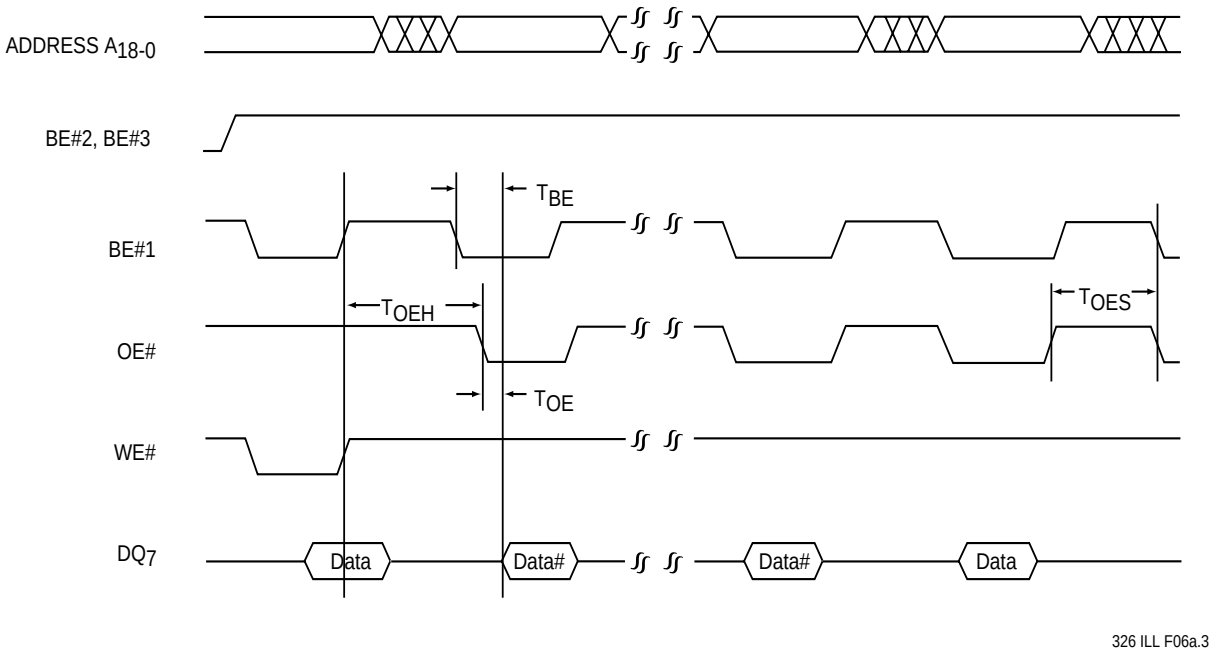


FIGURE 21: FLASH BANK 1, DATA# POLLING TIMING DIAGRAM

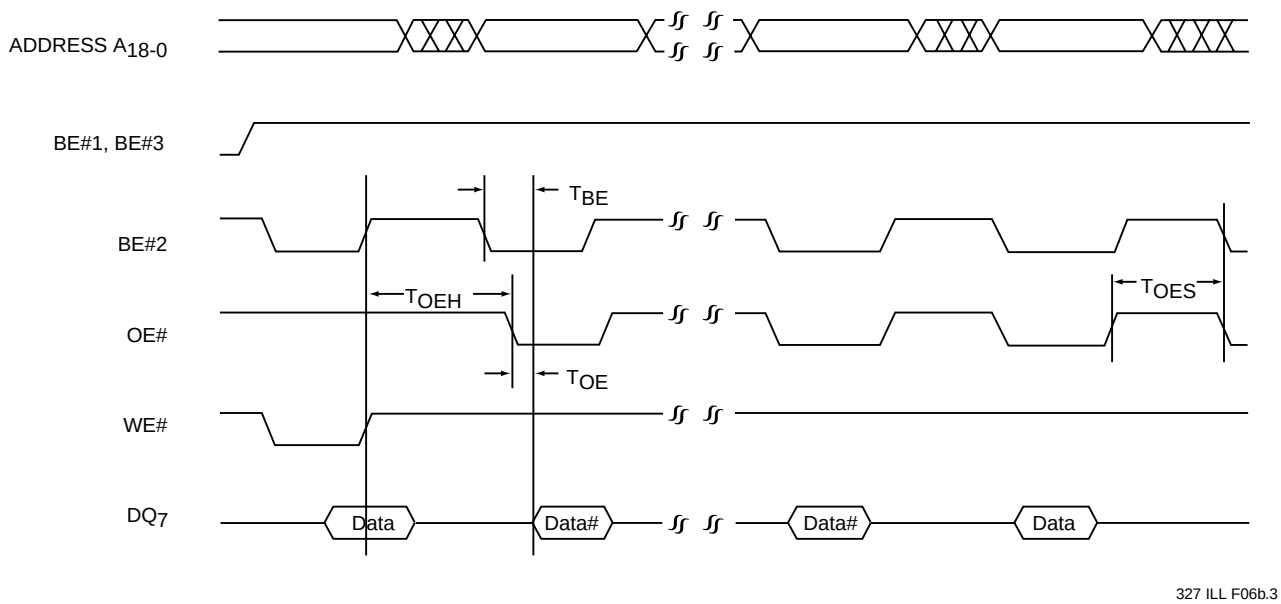


FIGURE 22: FLASH BANK 2, DATA# POLLING TIMING DIAGRAM

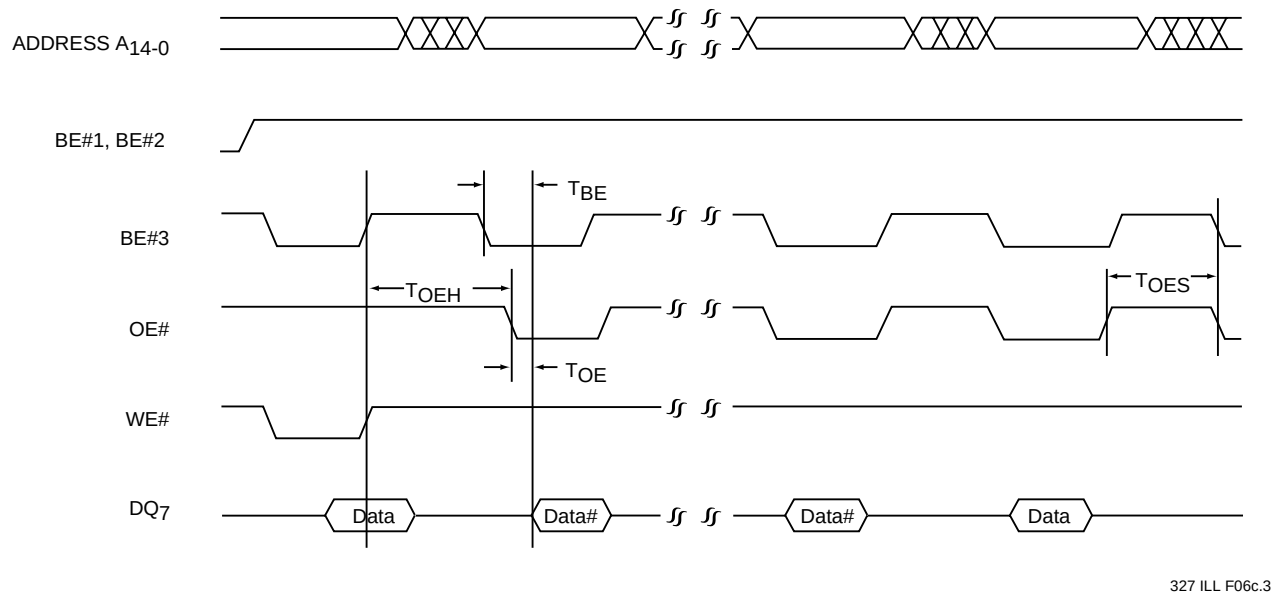


FIGURE 23: E2 BANK, DATA# POLLING TIMING DIAGRAM

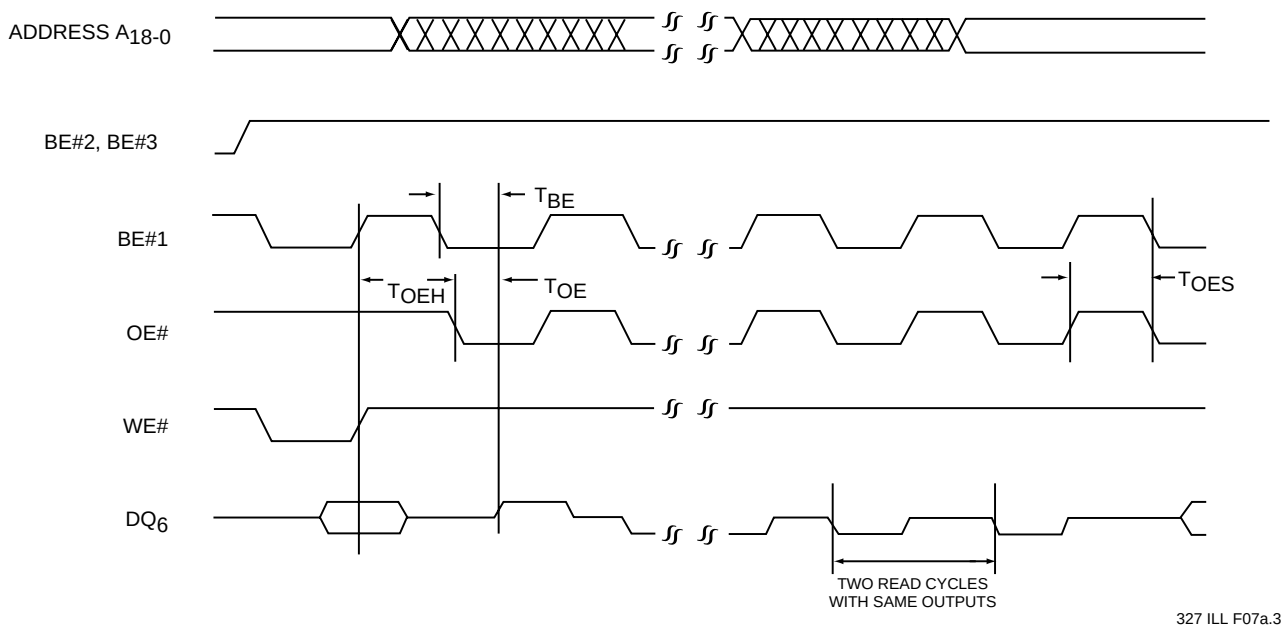


FIGURE 24: FLASH BANK 1, TOGGLE BIT TIMING DIAGRAM

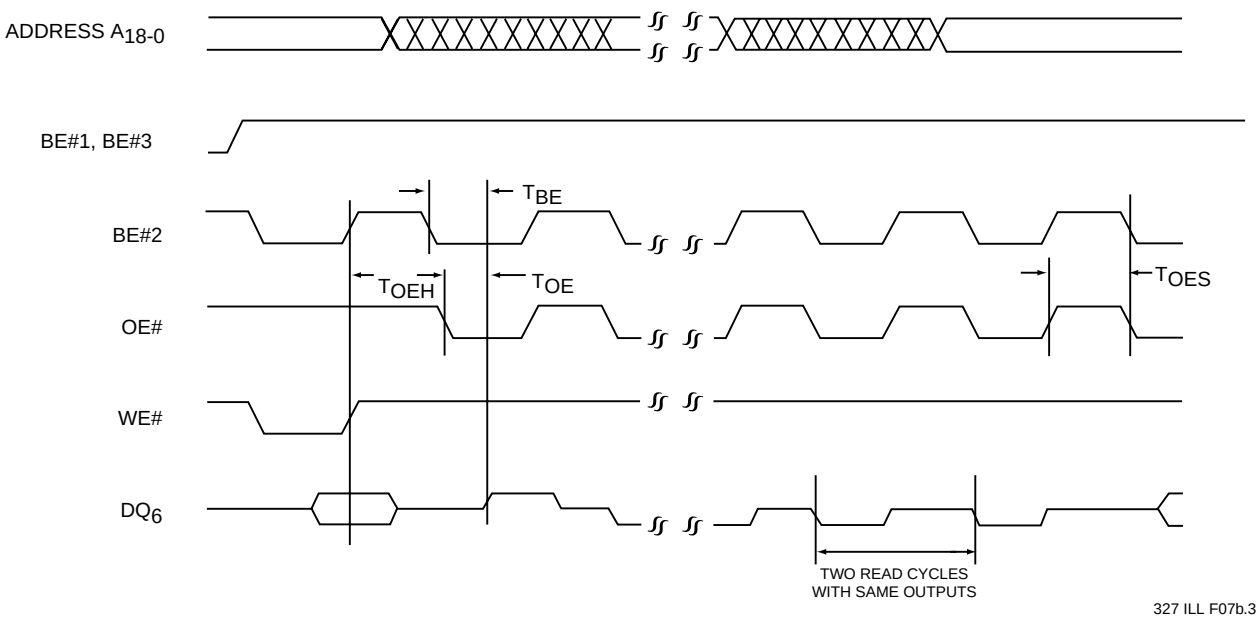


FIGURE 25: FLASH BANK 2, TOGGLE BIT TIMING DIAGRAM

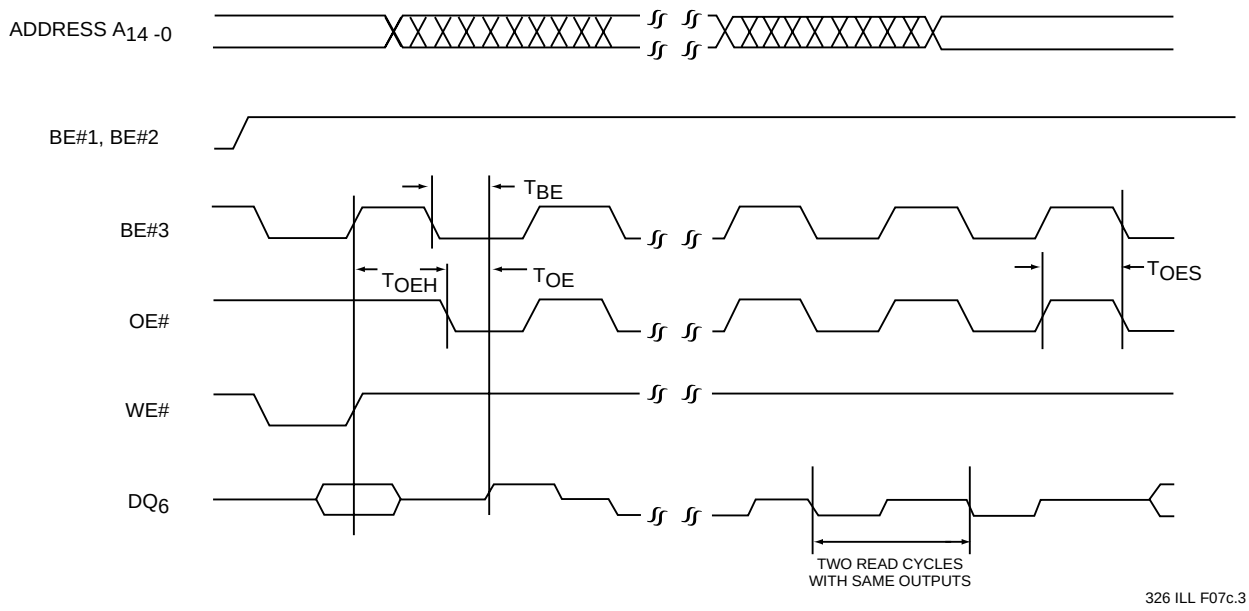


FIGURE 26: E² BANK, TOGGLE BIT TIMING DIAGRAM

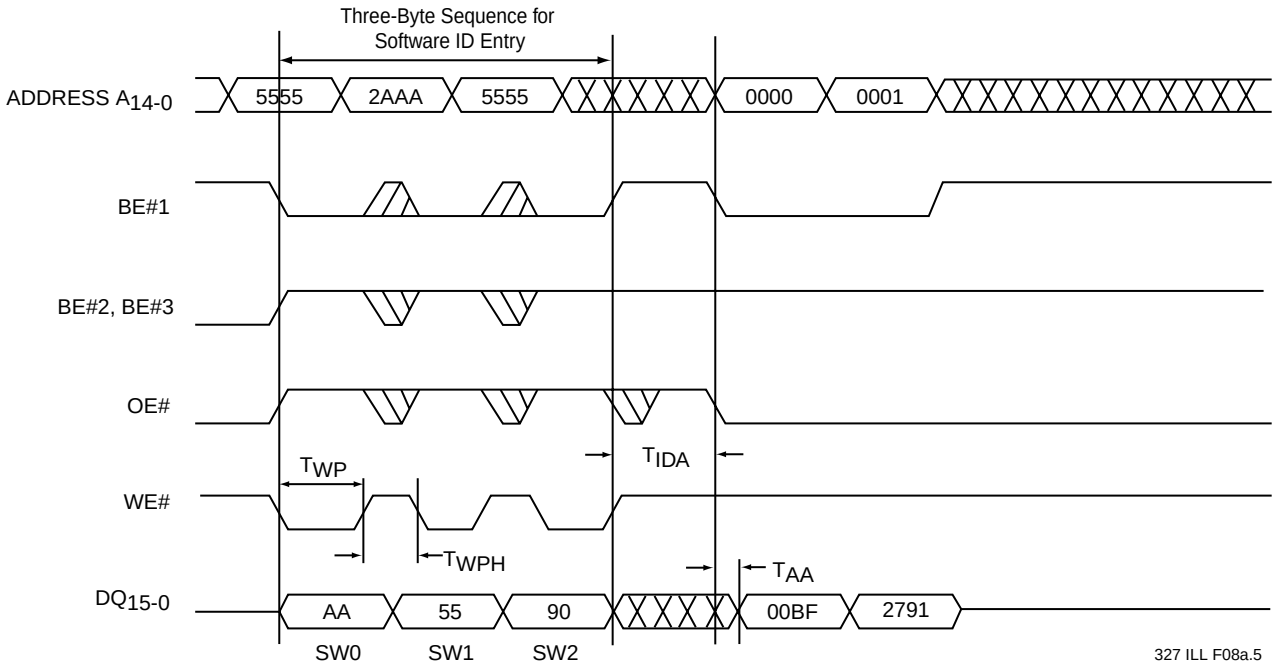


FIGURE 27: FLASH BANK 1, SOFTWARE ID ENTRY AND READ

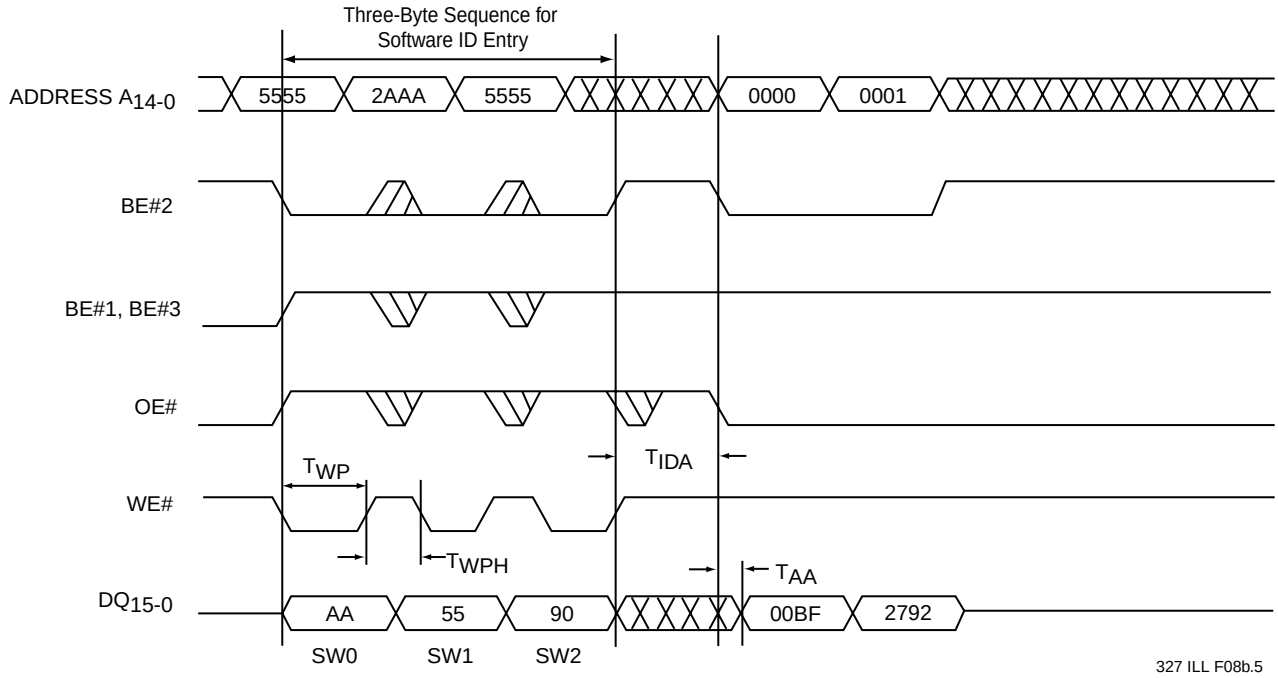


FIGURE 28: FLASH BANK 2, SOFTWARE ID ENTRY AND READ

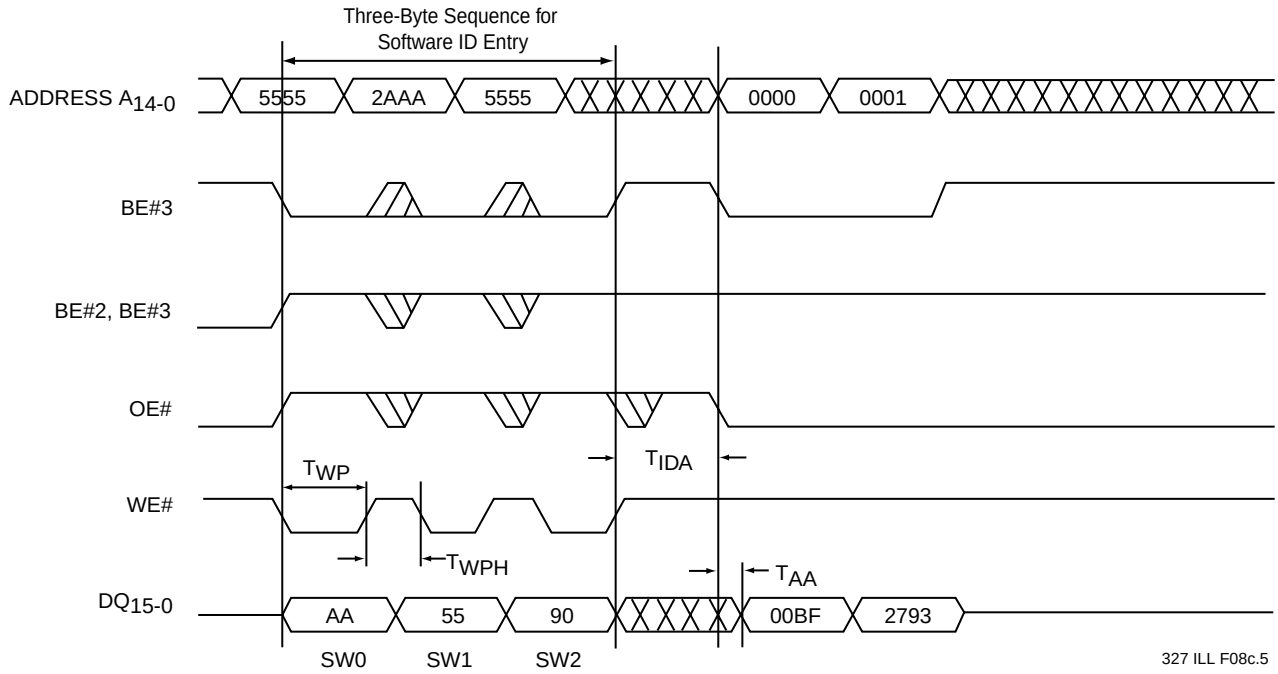


FIGURE 29: E^2 BANK, SOFTWARE ID ENTRY AND READ

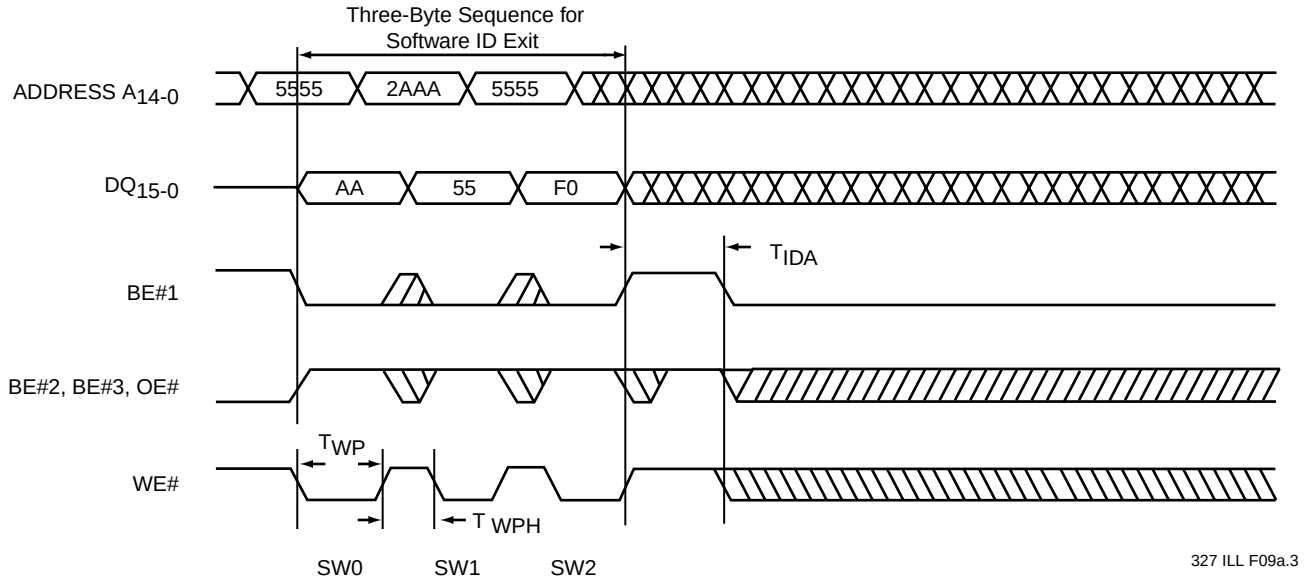


FIGURE 30: FLASH BANK 1, SOFTWARE ID EXIT

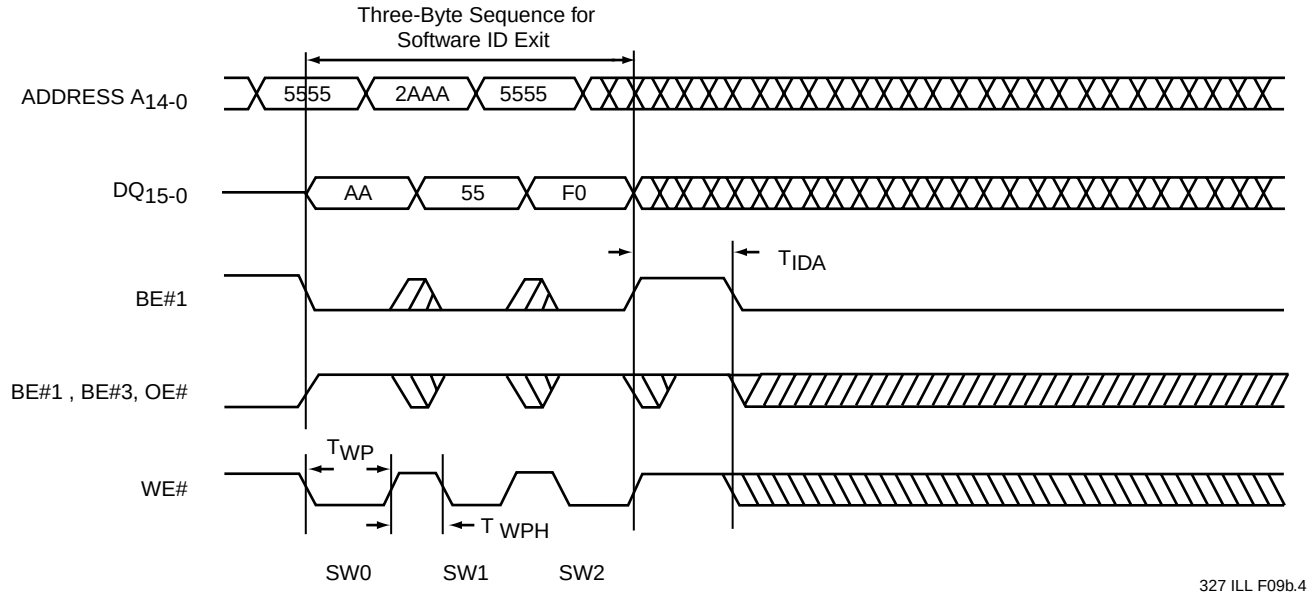


FIGURE 31: FLASH BANK 2, SOFTWARE ID EXIT

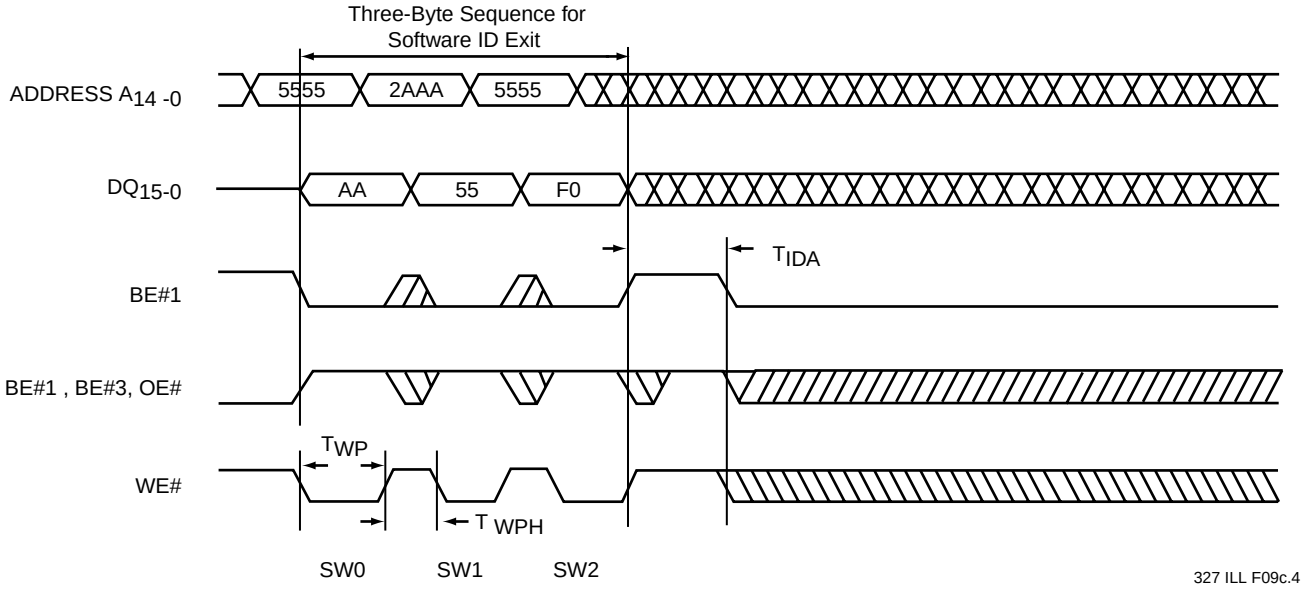


FIGURE 32: E² BANK, SOFTWARE ID EXIT

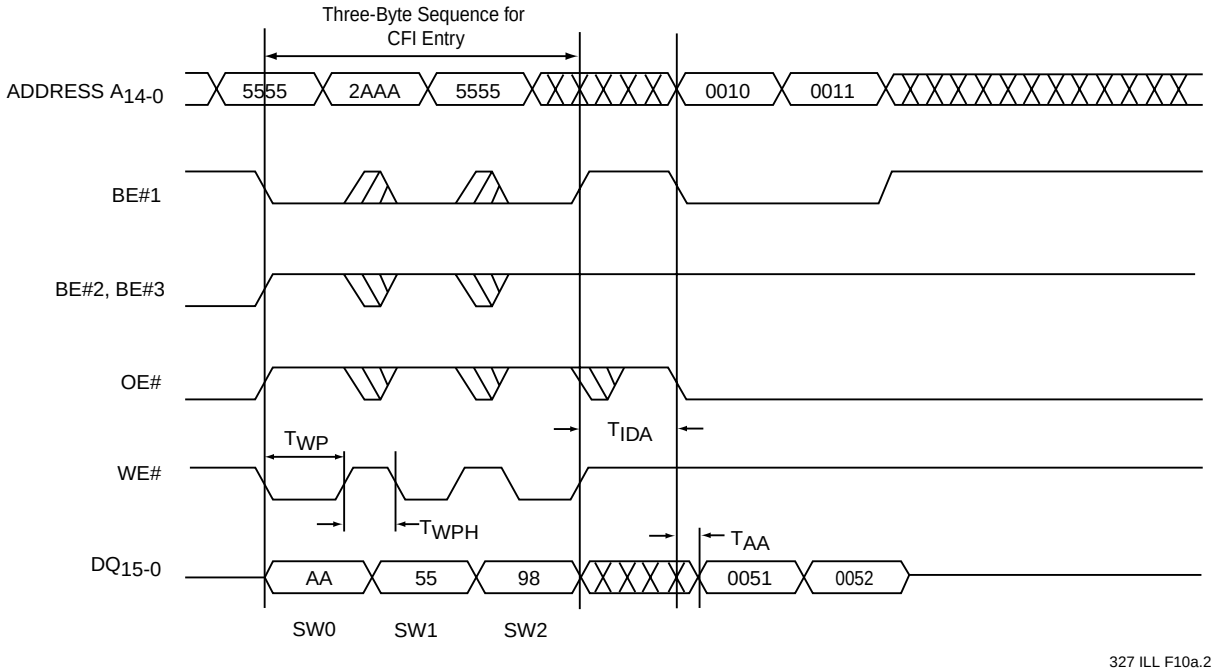


FIGURE 33: FLASH BANK 1, CFI ENTRY AND READ

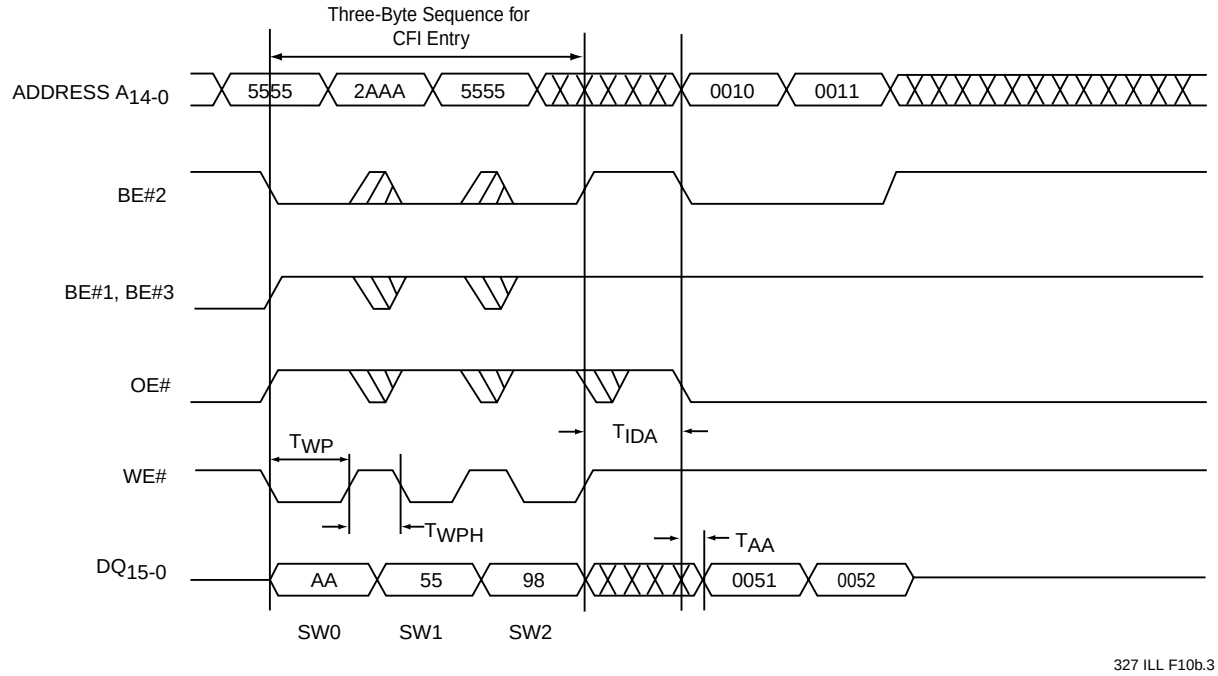


FIGURE 34: FLASH BANK 2, CFI ENTRY AND READ

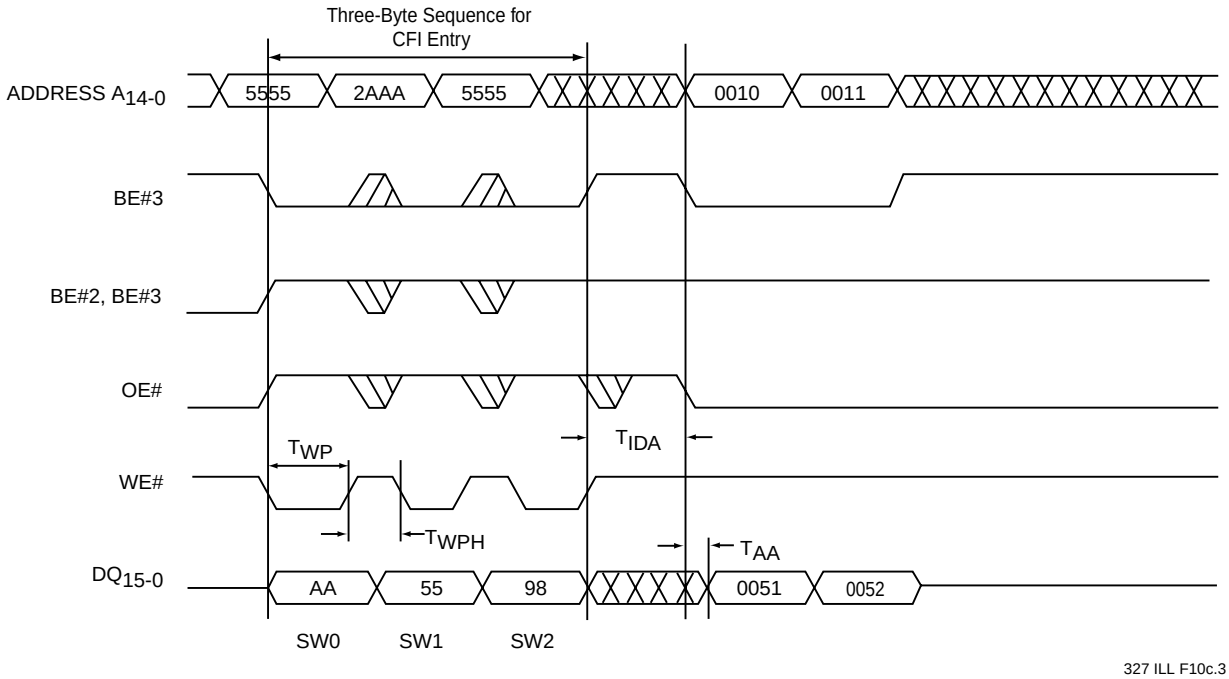


FIGURE 35: E2 BANK, CFI ENTRY AND READ

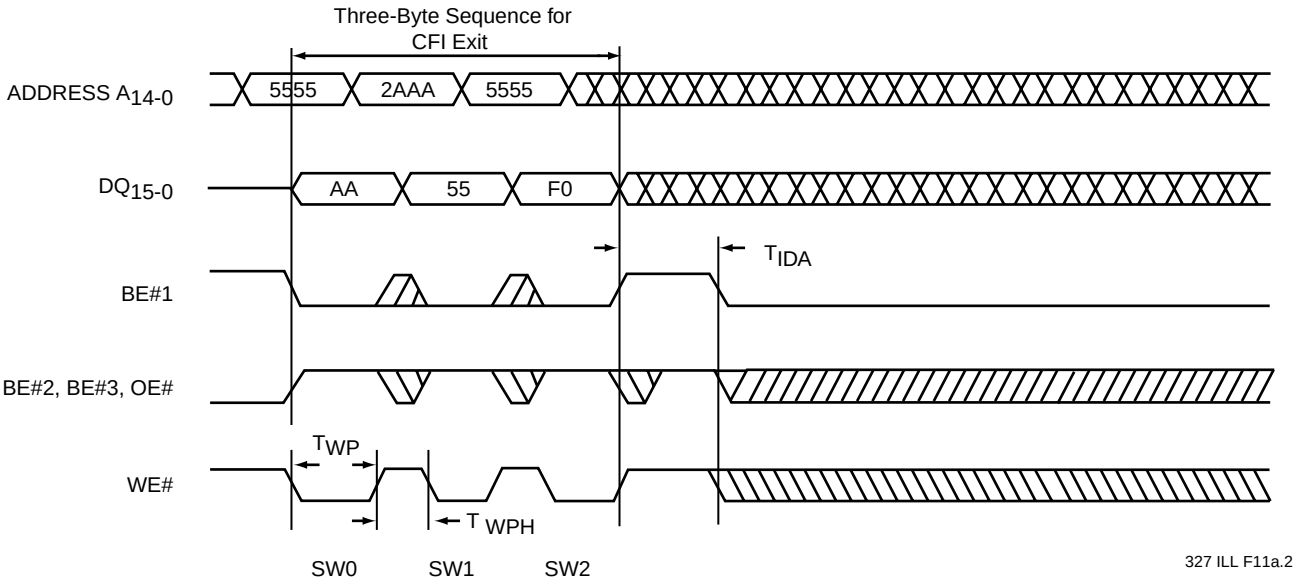


FIGURE 36: FLASH BANK 1, CFI EXIT

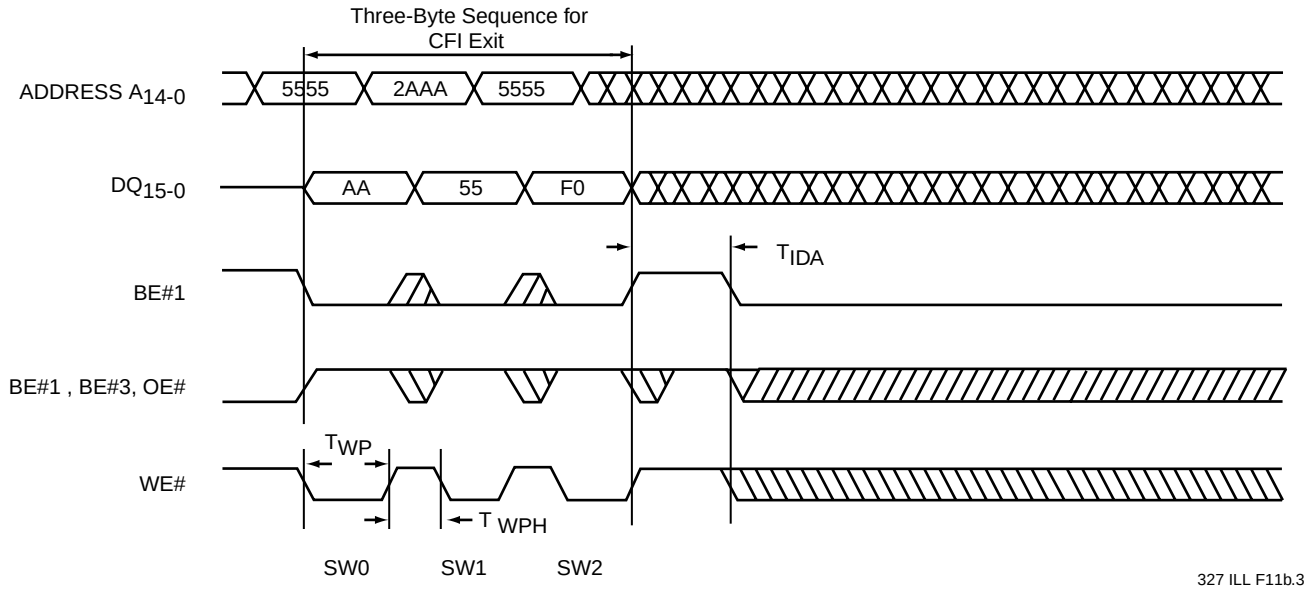


FIGURE 37: FLASH BANK 2, CFI EXIT

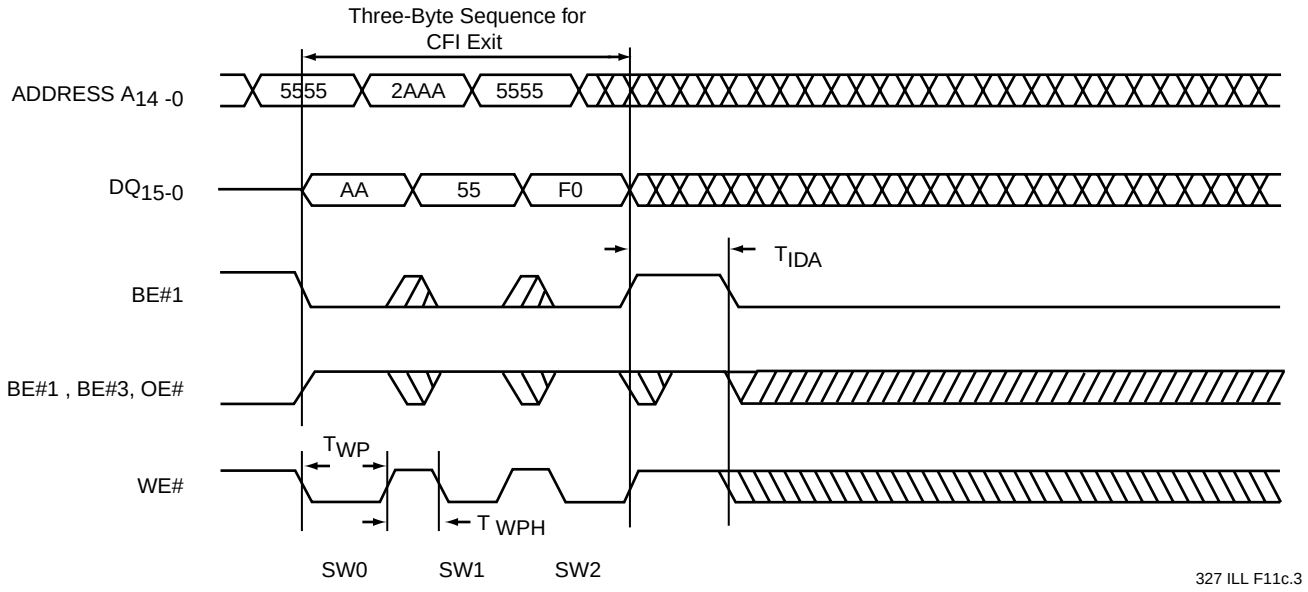


FIGURE 38: E² BANK, CFI EXIT

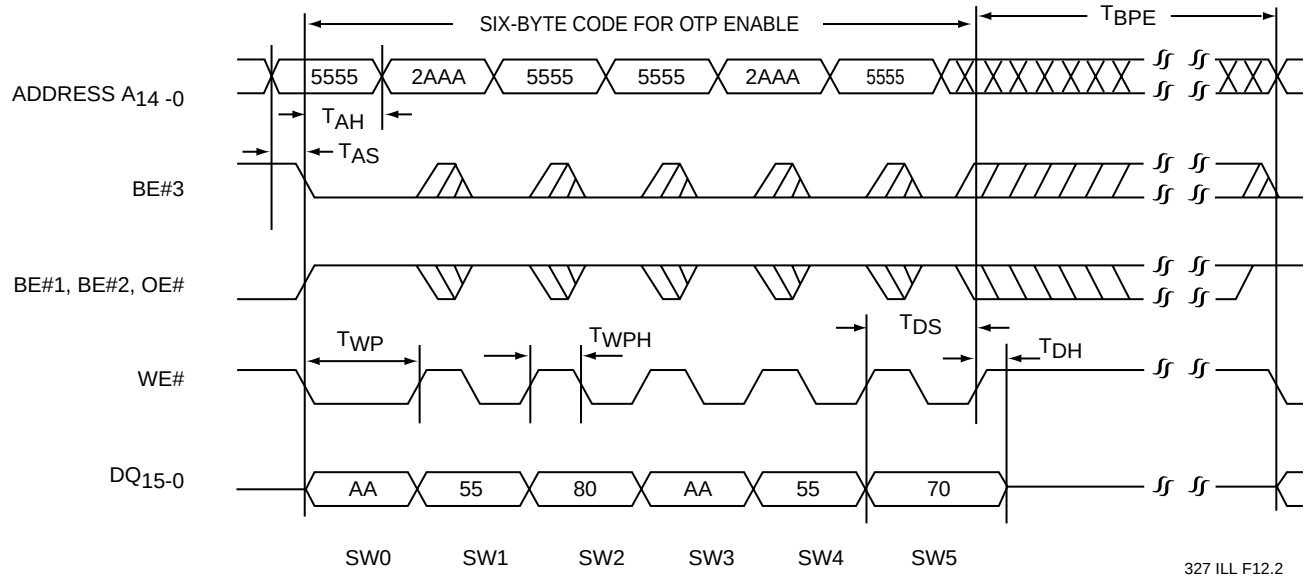


FIGURE 39: E² BANK, OTP ENABLE

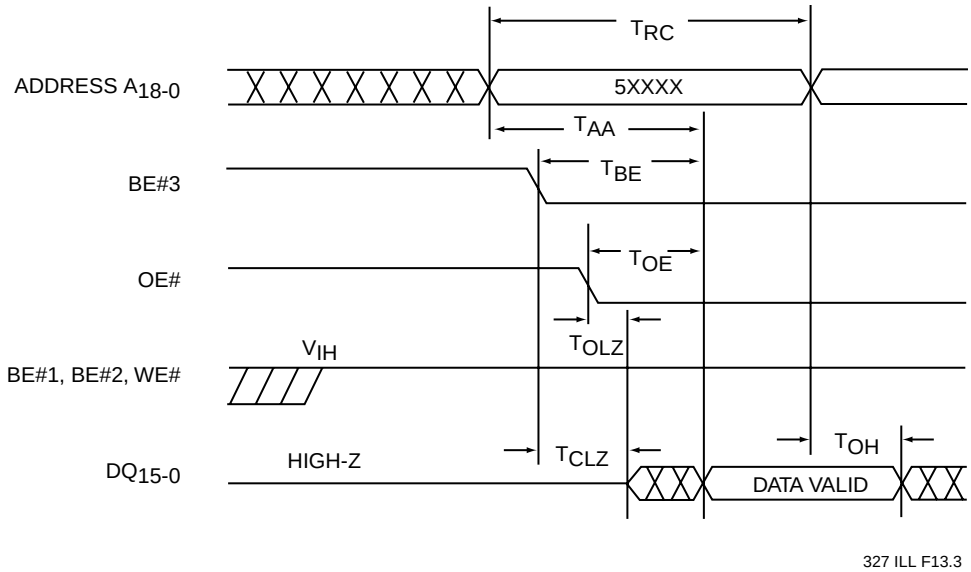


FIGURE 40: WRITE OPERATION STATUS READ

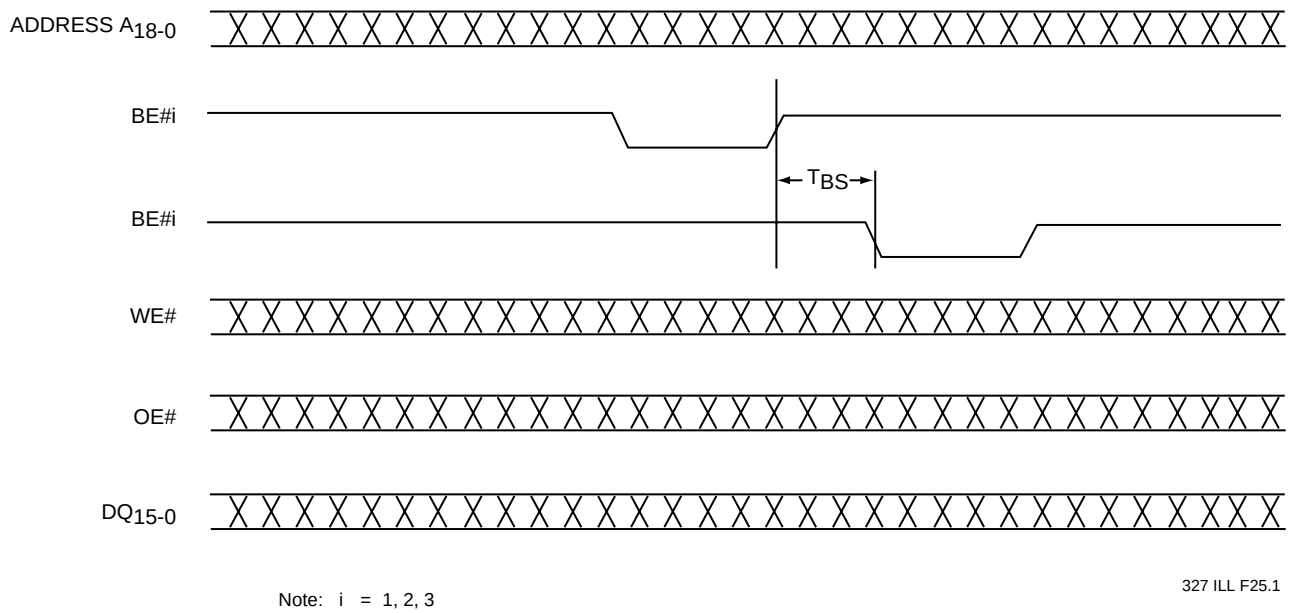
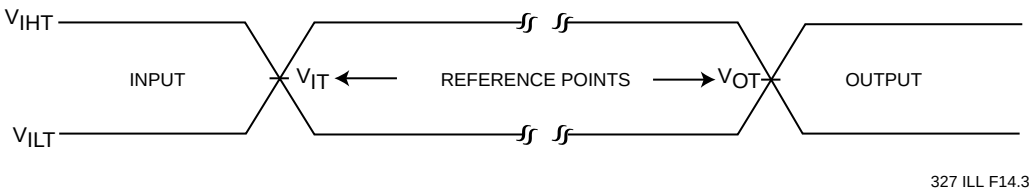


FIGURE 41: TIMING DIAGRAM TO ALTERNATE BETWEEN EACH MEMORY BANK



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 42: AC INPUT/OUTPUT REFERENCE WAVEFORMS

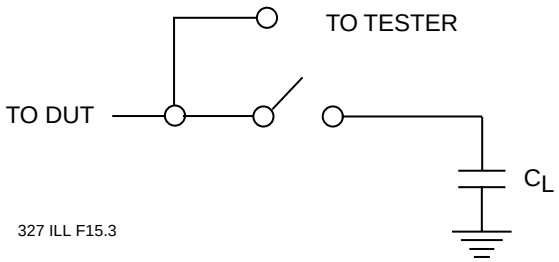


FIGURE 43: A TEST LOAD EXAMPLE

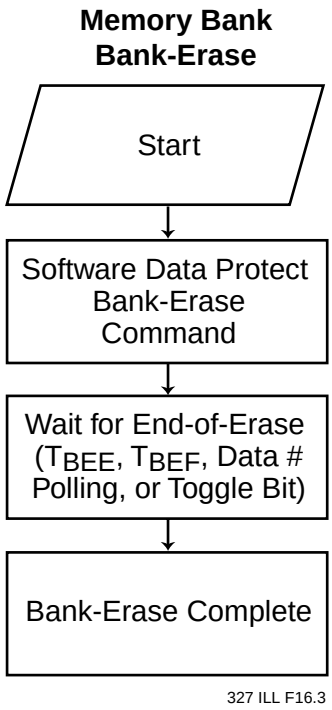


FIGURE 44: BANK-ERASE FLOWCHART

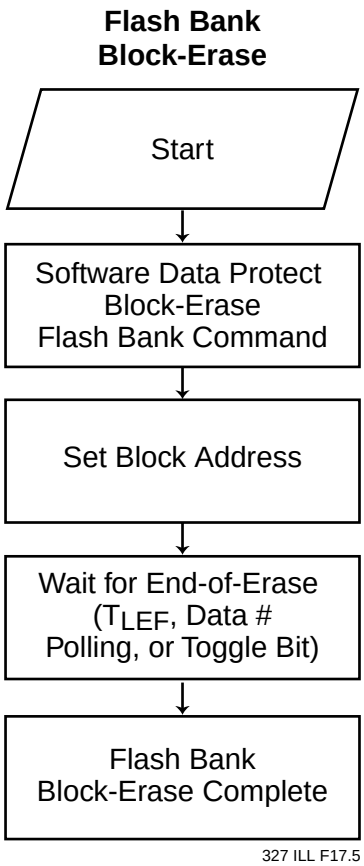


FIGURE 45: FLASH BANK BLOCK-ERASE FLOWCHART

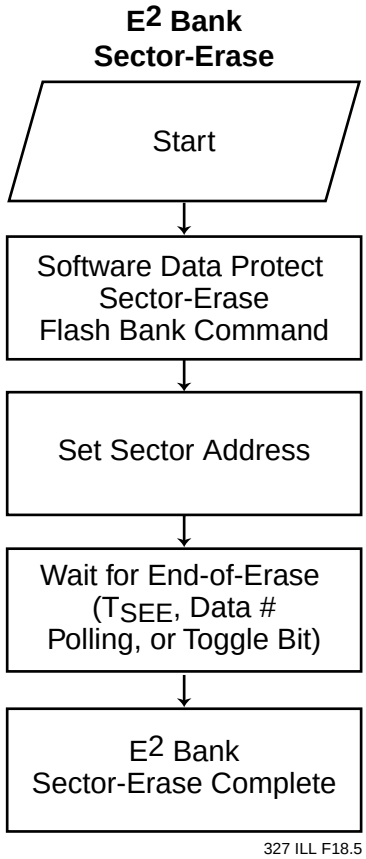


FIGURE 46: E^2 BANK SECTOR-ERASE FLOWCHART

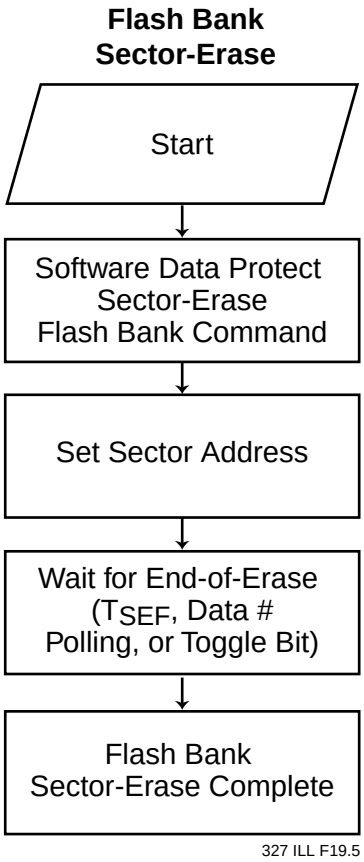


FIGURE 47: FLASH BANK SECTOR-ERASE FLOWCHART

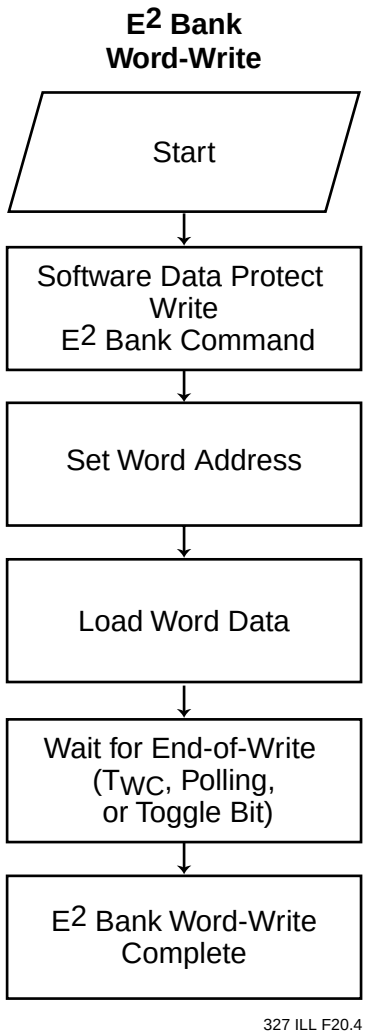


FIGURE 48: E2 BANK WORD-WRITE FLOWCHART

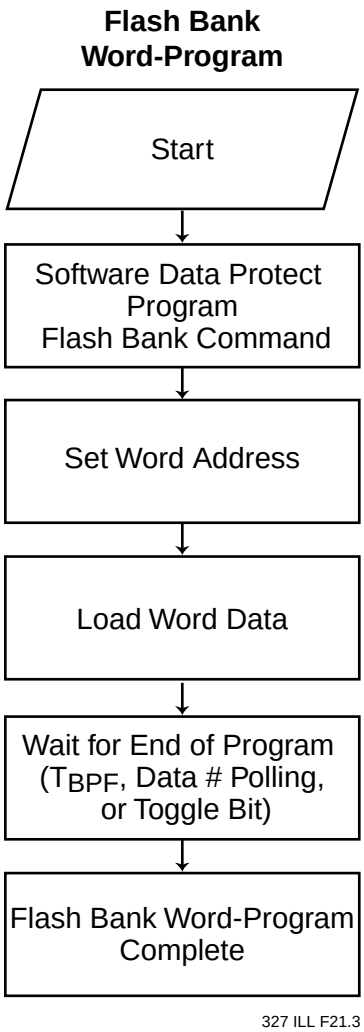


FIGURE 49: FLASH BANK WORD-PROGRAM FLOWCHART

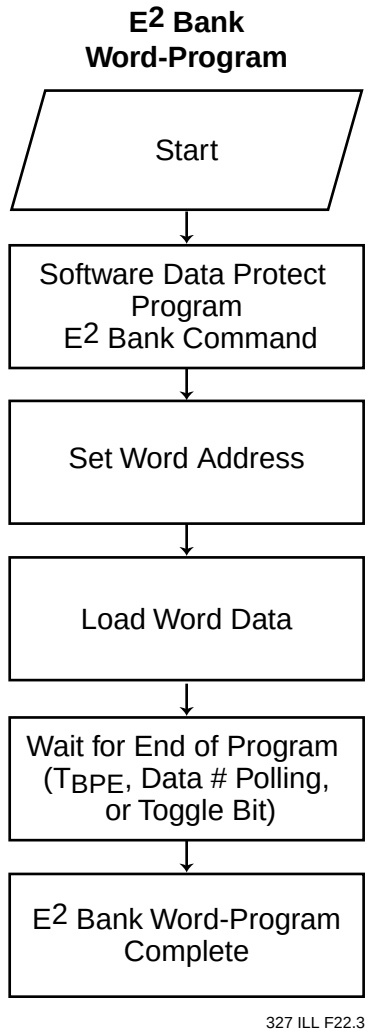


FIGURE 50: E^2 BANK WORD-PROGRAM FLOWCHART

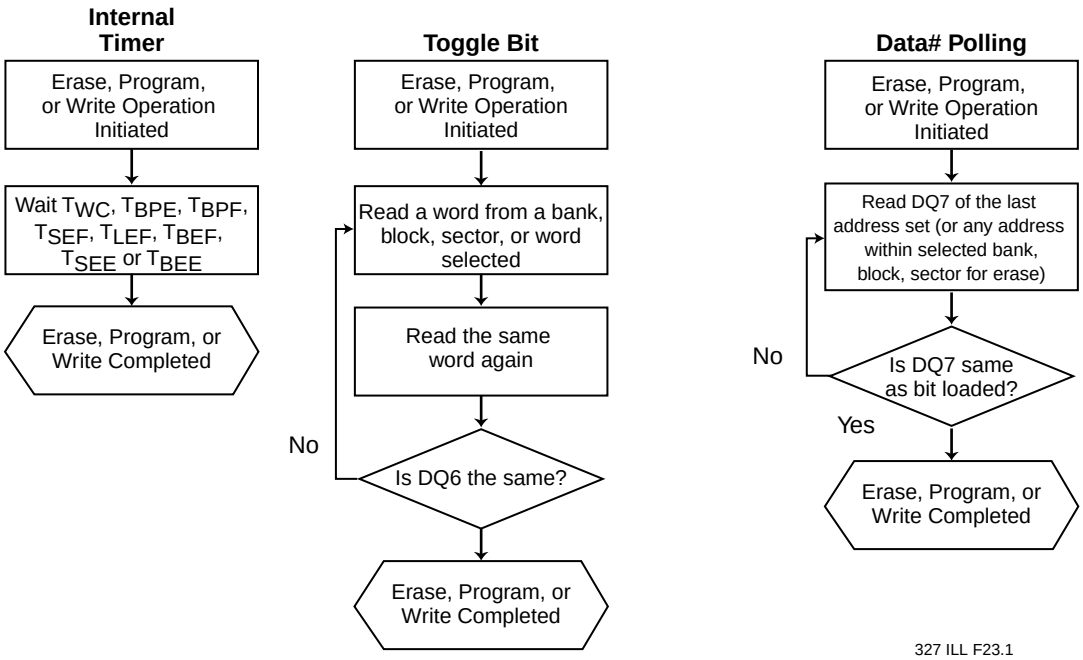


FIGURE 51: END-OF-WRITE, ERASE, OR PROGRAM WAIT OPTIONS FLOWCHART

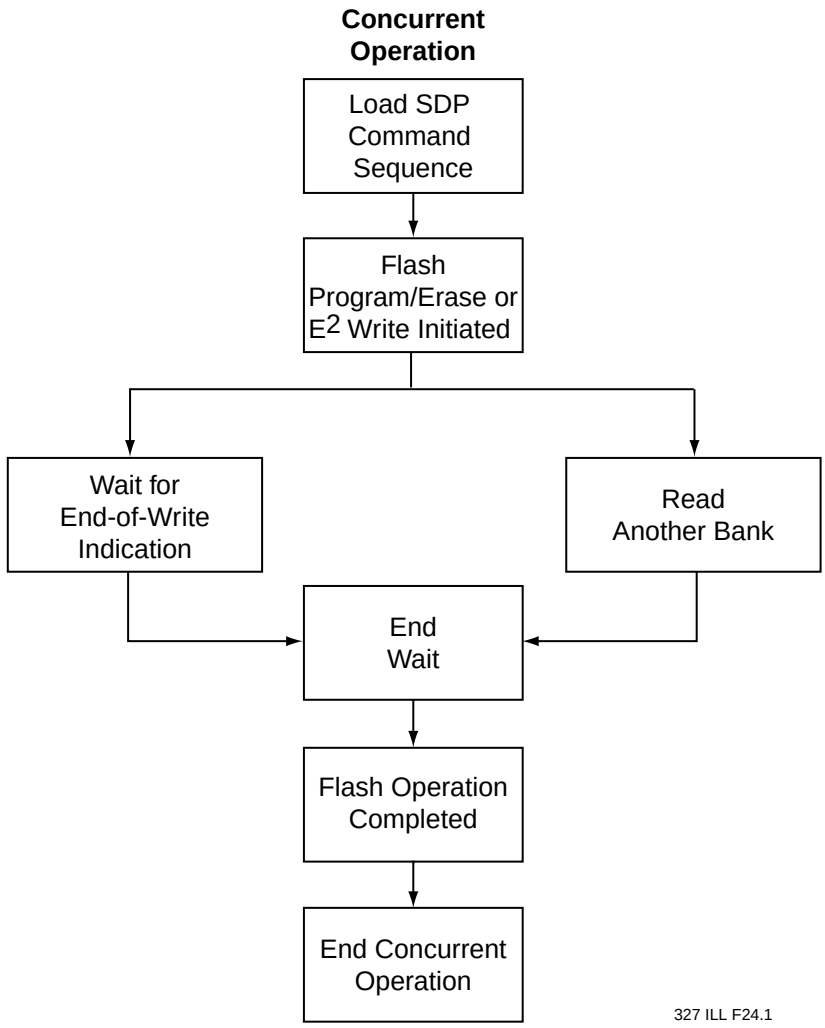
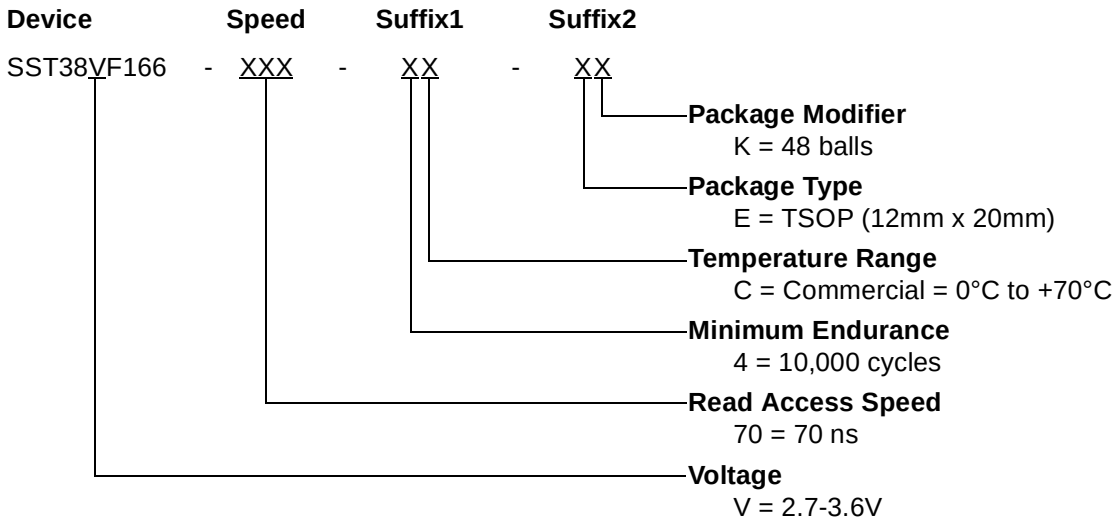


FIGURE 52: CONCURRENT OPERATION FLOWCHART

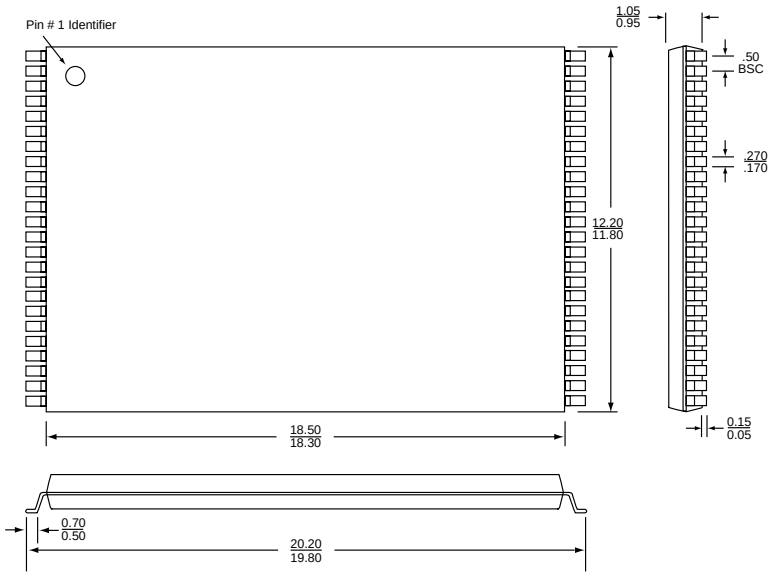


SST38VF166 Valid combinations

SST38VF166-70-4C-EK

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-142 DD dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 (±.05) mm.
4. Maximum allowable mold flash is 0.15mm at the package ends, and 0.25mm between leads.

48.TSOP-EK-ILL.5

48-PIN THIN SMALL OUTLINE PACKAGE (TSOP) 12MM X 20MM
SST PACKAGE CODE: EK