

Dual P-Channel 1.8-V (G-S) MOSFET

CHARACTERISTICS

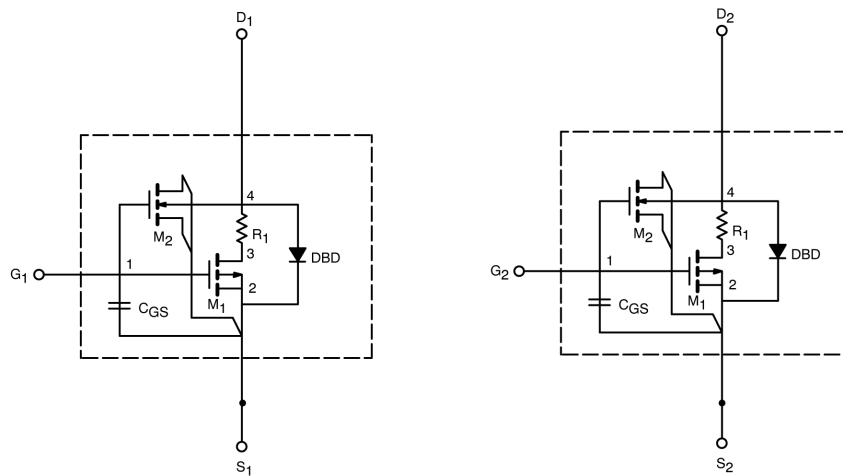
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model schematic is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device(s).

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model Si4965DY

Vishay Siliconix



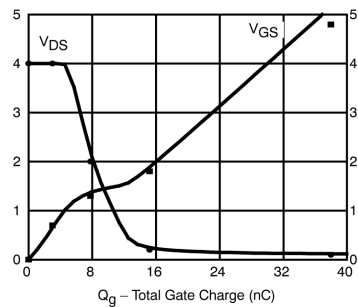
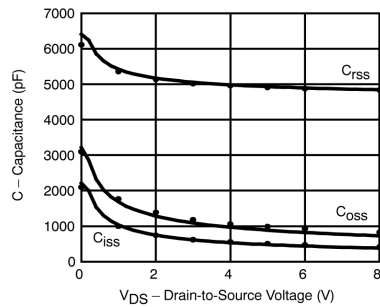
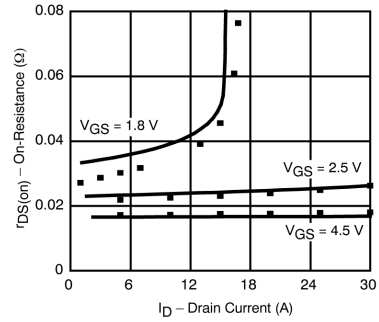
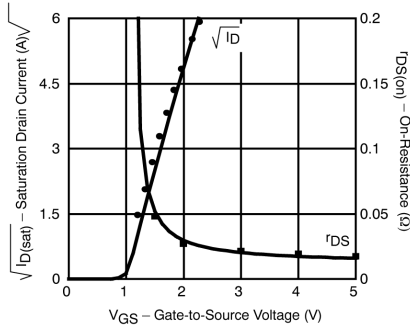
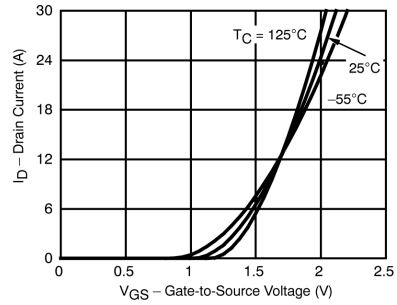
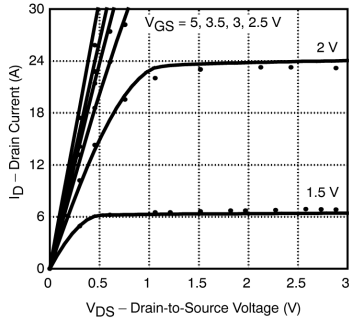
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Condition	Typical	Unit
Static				
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	0.82	V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ -5 V, V _{GS} = -4.5 V	213	A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -8 A	0.017	Ω
		V _{GS} = -2.5 V, I _D = -7 A	0.023	
		V _{GS} = -1.8 V, I _D = -5.8 A	0.035	
Forward Transconductance ^a	g _{fs}	V _{DS} = -5 V, I _D = -8 A	23	S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.7 A, V _{GS} = 0 V	0.79	V
Dynamic^b				
Total Gate Charge	Q _g	V _{DS} = -4 V, V _{GS} = -4.5 V, I _D = -8 A	35	nC
Gate-Source Charge	Q _{gs}		7.5	
Gate-Drain Charge	Q _{gd}		5	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -4 V, R _L = 4 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω	54	ns
Rise Time	t _r		31	
Turn-Off Delay Time	t _{d(off)}		167	
Fall Time	t _f		36	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -1.7 A, di/dt = 100 A/μs	57	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.