

Advance Information

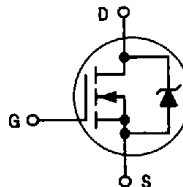
TMOS E-FET™

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

This advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

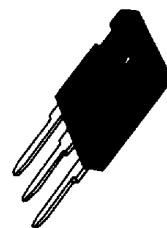
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature



MTW4N80E

Motorola Preferred Device

TMOS POWER FET
4.0 AMPERES
 $R_{DS(on)} = 3.00 \text{ OHM}$
800 VOLTS



CASE 340F-03
TO-247AE

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	800	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	800	Vdc
Gate-Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ $T_C = 25^\circ\text{C}$	I_D	4.0	Adc
— Continuous @ $T_C = 100^\circ\text{C}$	I_D	3.0	
— Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	25	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	150	Watts
Derate above 25°C		1.0	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 50 \text{ Vdc}$, $V_{GS} = 10 \text{ Vpk}$, $I_L = 10 \text{ Apk}$, $L = 10.4 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	83	mJ
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
— Junction to Ambient	$R_{\theta JA}$	40	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	$^\circ\text{C}$

This document contains information on a new product. Specifications and information are subject to change without notice

E-FET is a trademark of Motorola Inc

TMOS is a registered trademark of Motorola Inc

Preferred devices are Motorola recommended choices for future use and best overall value

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$) Temperature Coefficient (Positive)	BV_{DSS}	800	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 600\text{ Vdc}$, $V_{GS} = 0$) ($V_{DS} = 600\text{ Vdc}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)	I_{DSS}	—	—	250 1000	μA
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	—	100	nA

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$) Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	— 5.0	4.0 —	Vdc mV/ $^\circ\text{C}$
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.0\text{ A}$)	$R_{DS(on)}$	—	—	3.0	Ω
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$) ($I_D = 4.0\text{ A}$) ($I_D = 2.0\text{ A}$, $T_J = 125^\circ\text{C}$)	$V_{DS(on)}$	—	—	14 12	Vpk
Forward Transconductance ($V_{DS} = 15\text{ Vdc}$, $I_D = 2.0\text{ A}$)	g_{FS}	2.5	—	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\text{ Vdc}$, $V_{GS} = 0$, $f = 1.0\text{ MHz}$)	C_{iss}	—	1435	—	pF
Output Capacitance		C_{oss}	—	175	—	
Reverse Transfer Capacitance		C_{rss}	—	35	—	

SWITCHING CHARACTERISTICS*†

Turn-On Delay Time	$(V_{DD} = 300\text{ Vdc}$, $I_D = 4.0\text{ A}$, $V_{GS} = 10\text{ Vdc}$, $R_g = 9.1\ \Omega$)	$t_{d(on)}$	—	22	50	ns
Rise Time		t_r	—	29	75	
Turn-Off Delay Time		$t_{d(off)}$	—	65	150	
Fall Time		t_f	—	34	65	
Gate Charge	$(V_{DS} = 640\text{ Vdc}$, $I_D = 4.0\text{ A}$, $V_{GS} = 10\text{ Vdc}$)	Q_T	—	50	80	nC
		Q_1	—	8.0	—	
		Q_2	—	26	—	
		Q_3	—	30	—	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	$(I_S = 4.0\text{ A}$, $V_{GS} = 0$) $(I_S = 4.0\text{ A}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)	V_{SD}	—	1.3 1.2	1.5 —	Vdc
Reverse Recovery Time		$(I_S = 4.0\text{ A}$, $V_{GS} = 0$, $di_S/dt = 100\text{ A}/\mu\text{s}$)	t_{rr}	—	330	—
	t_a		—	220	—	
	t_b		—	110	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.3	—	μC

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)	L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_S	—	13	—	nH

*Pulse Test Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

† Switching characteristics are independent of operating junction temperature