DATA SHEET

PCF2103 family
LCD controllers/drivers

Product specification
File under Integrated Circuits, IC12

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Single-chip LCD controller/driver
- 2-line display of up to 12 characters + 120 icons, or 1-line display of up to 24 characters + 120 icons
- 5×7 character format plus cursor; 5×8 for kana (Japanese syllabary) and user defined symbols
- Icon mode: reduced current consumption while displaying icons only(1)
- Icon blink function
- On-chip:
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240, 5×8 characters
- Character generator RAM: 16, 5×8 characters; 3 characters used to drive 120 icons, 6 characters used if icon blink feature is used in application
- 4 or 8-bit parallel bus and 2-wire I^2C-bus interface
- CMOS compatible
- 18 row, 60 column outputs
- Mux rates 1 : 18 (for normal operation) and 1 : 2 (for icon-only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage range, $V_{DD} - V_{SS}$ = 1.8 to 5.5 V; chip may be driven with two battery cells
- Display supply voltage range, $V_{LCD} - V_{SS}$ = 2.2 to 6.5 V
- Very low current consumption (20 to 120 μA):
  - Icon mode: <25 μA
  - Power-down mode: <2.5 μA.

(1) Icon mode is used to save current. When only icons are displayed, a much lower operating voltage V_{LCD} can be used and the switching frequency of the LCD outputs is reduced. In most applications it is possible to use V_{DD} as V_{LCD}.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point-of-sale terminals.

3 GENERAL DESCRIPTION

The PCF2103 family is a low power CMOS LCD controller and driver, designed to drive a dot matrix LCD display of 2 line by 12 or 1 line by 24 characters with 5×8 dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2103 interfaces to most microcontrollers via a 4 or 8-bit bus or via the 2-wire I^2C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters. The letter 'X' in PCF2103X characterizes the built-in character set. Various character sets can be manufactured on request.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2103EU/2/F2	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

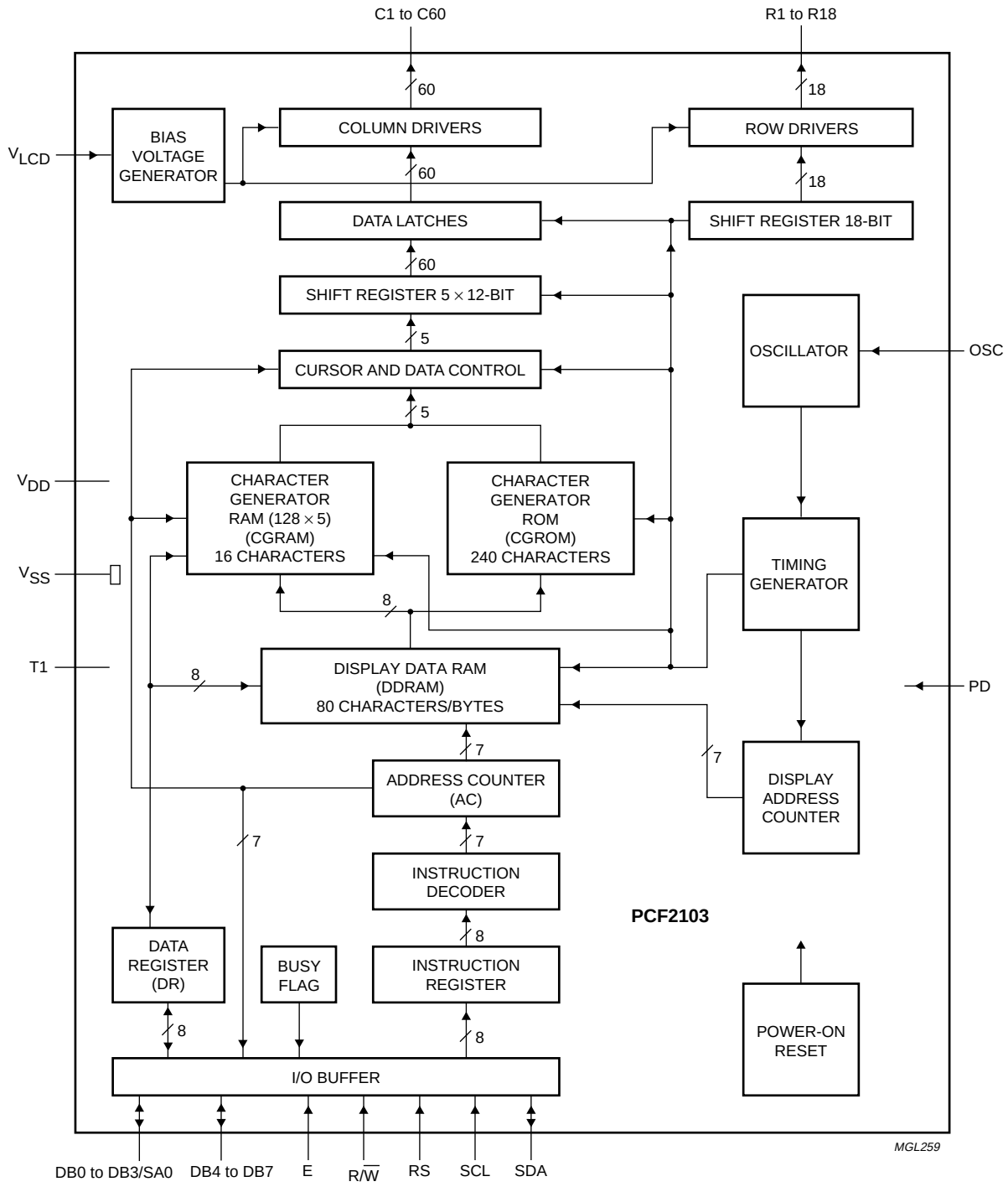


Fig.1 Block diagram.

6 PINNING

SYMBOL	DIE PAD	DESCRIPTION
V_{DD}	1	supply voltage
OSC	2	oscillator/external clock input
PD	3	power-down pad input
T1	4	test pad (connected to V_{SS})
V_{SS}	5	ground
V_{LCD}	6	V_{LCD} input; note 1
R9 to R16	7 to 14	LCD row driver outputs 9 to 16
R18	15	LCD row driver output 18
C60 to C1	16 to 23, 26 to 50, 53 to 77, 80, 81	LCD column driver outputs 60 to 1
R8 to R1	82 to 89	LCD row driver outputs 8 to 1
R17	90	LCD row driver output 17
SCL	91	I^2C-bus serial clock input
SDA	92	I^2C-bus serial data input/output
E	93	data bus clock input
RS	94	register select input
R/$\overline{W}$	95	read/write input
DB7	96	bit of bi-directional data bus
DB6	97	bit of bi-directional data bus
DB5	98	bit of bi-directional data bus
DB4	99	bit of bi-directional data bus
DB3/SA0	100	bit of bi-directional data bus/I^2C-bus address pin
DB2	101	bit of bi-directional data bus
DB1	102	bit of bi-directional data bus
DB0	103	bit of bi-directional data bus

Note

1. This is the voltage used for the generation of LCD bias levels.

Table 1 Pin functions; note 1

NAME	FUNCTION	DESCRIPTION
RS	register select	RS selects the register to be accessed for read and write; there is an internal pull-up on this pin RS = 0 selects the instruction register for write and the busy flag and address counter for read RS = 1 selects the data register for both read and write
R/$\overline{W}$	read/write	R/$\overline{W}$ selects either the read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation; there is an internal pull-up on this pin
E	data bus clock	pin E is set HIGH to signal the start of a read or write operation; data is clocked in or out of the chip on the negative edge of the clock
DB7 to DB0	data bus	the bi-directional, 3-state data bus transfers data between the system controller and the PCF2103; DB7 may be used as the busy flag, signalling that internal operations are not yet completed; in 4-bit operations the 4 higher order lines DB7 to DB4 are used; DB3 to DB0 must be left open-circuit; there is an internal pull-up on each of the data lines
C1 to C60	column driver outputs	these pins output the data for columns
R1 to R18	row driver outputs	these pins output the row select waveforms to the display; R17 and R18 drive the icons
V_{LCD}	LCD power supply	positive power supply for the liquid crystal display
OSC	oscillator	when the on-chip oscillator is used this pin must be connected to V_{DD}; an external clock signal, if used, is input at this pin
SCL	serial clock line	input for the I^2C-bus clock signal
SDA	serial data line	I/O for the I^2C-bus data line
SA0	address pin	the hardware sub-address line is used to program the device sub-address for two different PCF2103s on the same I^2C-bus
T1	test pad	must be connected to V_{SS}; not user accessible
PD	power-down pad	PD selects chip power-down mode; for normal operation PD = 0

Note

1. When the I^2C-bus is used, the parallel interface pin E must be defined as E = 0. In I^2C-bus read mode DB7 to DB0 should be connected to V_{DD} or left open-circuit.
   a) When the parallel bus is used, pins SCL and SDA must be connected to V_{SS} or V_{DD}; they may not be left unconnected.
   b) If the 4-bit interface is used without reading out from the PCF2103 (i.e. R/$\overline{W}$ is set permanently to logic 0), the unused ports DB0 to DB3 can either be set to V_{SS} or V_{DD} instead of leaving them open.

7 FUNCTIONAL DESCRIPTION

7.1 LCD bias voltage generator

The intermediate bias voltages for the LCD display are generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels and is given by the relationships given in Tables 2 and 3. Using a 5-level bias scheme for 1 : 18 maximum rate allows V_{LCD} <5 V for most LCD liquids.

Table 2 Optimum/maximum values for V_{OP} (off pixels start darkening; $V_{off} = V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.272	3.7	5.2 V
1 : 2	3	2.236	2.283	3.9 V

Table 3 Minimum values for V_{OP} (on pixels clearly visible; $V_{on} > V_{th}$)

MUX RATE	NUMBER OF LEVELS	V_{on}/V_{th}	V_{OP}/V_{th}	V_{OP} (typical; for V_{th} = 1.4 V)
1 : 18	5	1.12	3.2	4.6 V
1 : 2	3	1.2	1.5	2.1 V

7.2 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and pin OSC must be connected to V_{DD}.

7.3 External clock

If an external clock is to be used, it is input at the OSC pin. The resulting display frame frequency is given by

$$f_{frame} = \frac{f_{osc}}{3072}$$

Only in the power-down state is the clock allowed to be stopped (OSC connected to V_{SS}), otherwise the LCD is frozen in a DC state.

7.4 Power-on reset

The on-chip power-on reset block initializes the chip after power-on or power failure. This is a synchronous reset and requires 3 oscillator cycles to be executed. Afterwards, a clear display is initiated.

7.5 Power-down mode

The chip can be put into power-down mode where all static currents are switched off (no internal oscillator, no bias level generation, all LCD outputs are internally connected to V_{SS}) when PD = 1.

During power-down, the whole chip is being reset and will restart with a clear display after power-down. Therefore, the whole chip has to be initialized after a power-down as after an initial power-up.

7.6 Registers

The PCF2103 has two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes such as ‘display clear’ and ‘cursor shift’, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written from but not read by the system controller. The data register temporarily stores data to be read from the DDRAM and CGRAM. When reading, data from the DDRAM or CGRAM corresponding to the address in the instruction register is written to the data register prior to being read by the ‘read data’ instruction.

7.7 Busy flag

The busy flag indicates the internal status of the PCF2103. Logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output at pin DB7 when RS = 0 and R/$\overline{W}$ = 1. Instructions should only be written after checking that the busy flag is logic 0 or waiting for the required number of cycles.

7.8 Address Counter (AC)

The address counter assigns addresses to the DDRAM and CGRAM for reading and writing and is set by the commands 'set CGRAM address' and 'set DDRAM address'. After a read/write operation the address counter is automatically incremented or decremented by 1. The address counter contents are output to the bus (DB6 to DB0) when RS = 0 and R/$\overline{W}$ = 1.

7.9 Display Data RAM (DDRAM)

The DDRAM stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM. The basic RAM-to-display addressing scheme is shown in Fig.2. With no display shift the characters represented by the codes in the first 24 RAM locations starting at address 00 in line 1 are displayed. Figures 3 and 4 show the display mapping for right and left shift respectively.

When data is written to or read from the DDRAM wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together.
The address ranges and wrap-around operations for the various modes are shown in Table 4.

7.10 Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) generates 240 character patterns in 5×8 dot format from 8-bit character codes. Figure 6 shows the character set that is currently implemented.

7.11 Character Generator RAM (CGRAM)

Up to 16 user defined characters may be stored in the CGRAM. Some CGRAM characters (see Fig.14) are also used to drive icons (6 if icons blink and both icon rows are used in application; 3 if no blink but both icon rows are used in application; 0 if no icons are driven by the icon rows). The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Fig.6). Figure 7 shows the addressing principle for the CGRAM.

7.12 Cursor control circuit

The cursor control circuit generates the cursor (underline and/or cursor blink as shown in Fig.5) at the DDRAM address contained in the address counter. When the address counter contains the CGRAM address the cursor will be inhibited.

7.13 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

7.14 LCD row and column drivers

The PCF2103 contains 18 row and 60 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figures 8, 9 and 10 show typical waveforms. Unused outputs should be left unconnected.

Table 4 Address space and wrap-around operation

MODE	ADDRESS SPACE	READ/WRITE WRAP-AROUND(1)	DISPLAY SHIFT WRAP-AROUND(2)
1×24	00H to 4FH	4FH to 00H	4FH to 00H
2×12	00H to 27H; 40H to 67H	27H to 40H; 67H to 00H	27H to 00H; 67H to 40H

Notes

1. Moves to next line.
2. Stays within line.

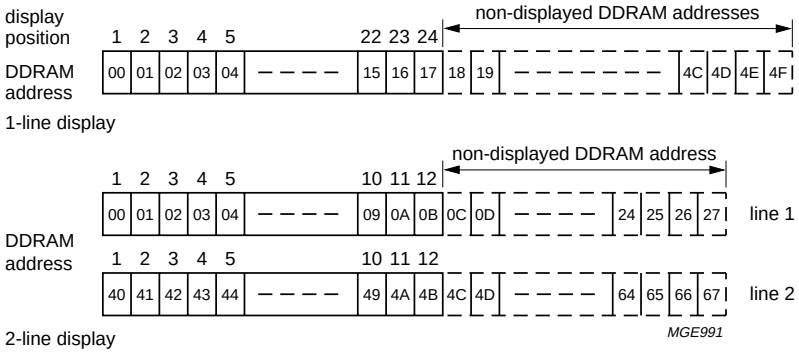


Fig.2 DDRAM-to-display mapping: no shift.

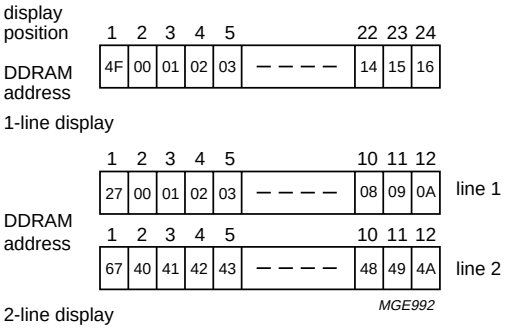


Fig.3 DDRAM-to-display mapping: right shift.

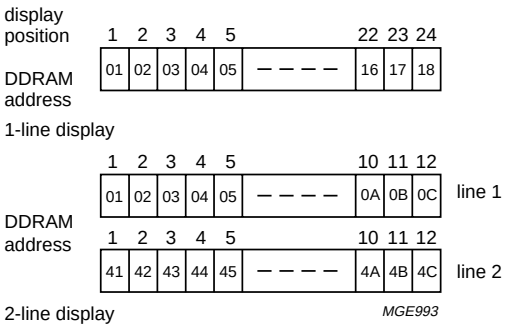
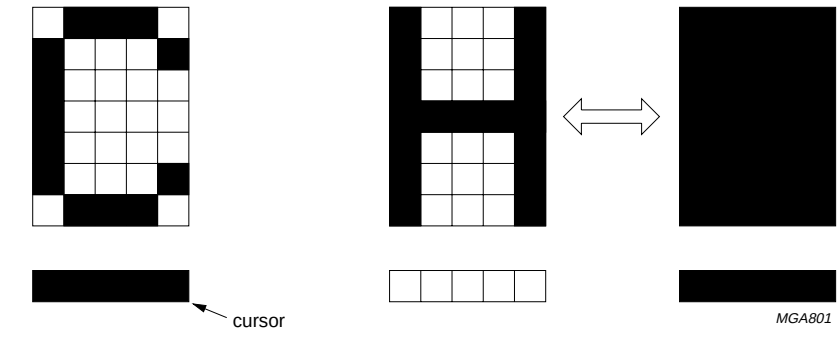


Fig.4 DDRAM-to-display mapping: left shift.



cursor display example blink display example

Fig.5 Cursor and blink display examples.

lower 4 bits \ upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 0000	1															
xxxx 0001	2															
xxxx 0010	3															
xxxx 0011	4															
xxxx 0100	5															
xxxx 0101	6															
xxxx 0110	7															
xxxx 0111	8															
xxxx 1000	9															
xxxx 1001	10															
xxxx 1010	11															
xxxx 1011	12															
xxxx 1100	13															
xxxx 1101	14															
xxxx 1110	15															
xxxx 1111	16															

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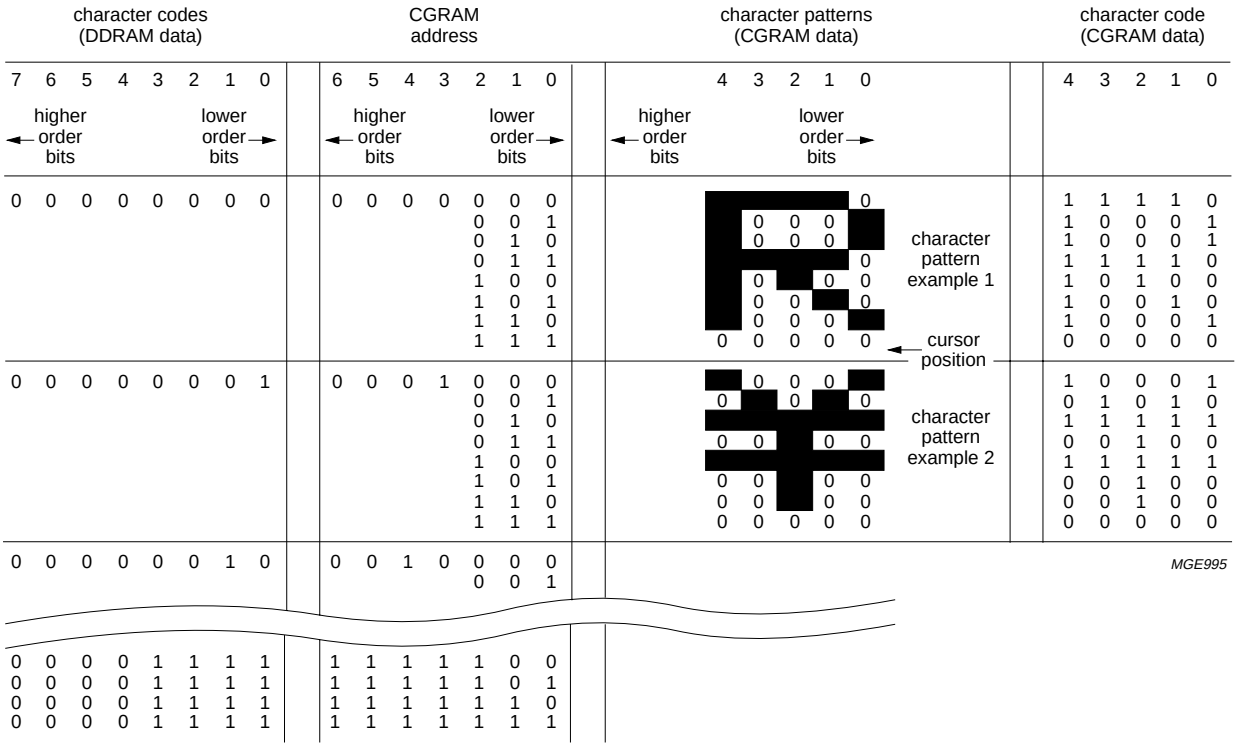
Fig.6 Character set ‘E’ in CGROM.



Character code bits 0 to 3 correspond to CGRAM address bits 3 to 6.

CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and display is performed by logical OR with the cursor. Data in the 8th position will appear in the cursor position.

Character pattern column positions correspond to CGRAM data bits 0 to 4, as shown in Fig.6.

As shown in Figs 6 and 7, CGRAM character patterns are selected when character code bits 4 to 7 are all logic 0. CGRAM data = logic 1 corresponds to selection for display.

Only bits 0 to 5 of the CGRAM address are set by the ‘set CGRAM address’ command. Bit 6 can be set using the ‘set DDRAM address’ command in the valid address range or by using the auto-increment feature during CGRAM write. All bits 0 to 6 can be read using the ‘read busy flag and address counter’ command; see Table 7.

Fig.7 Relationship between CGRAM addresses and data and display patterns.

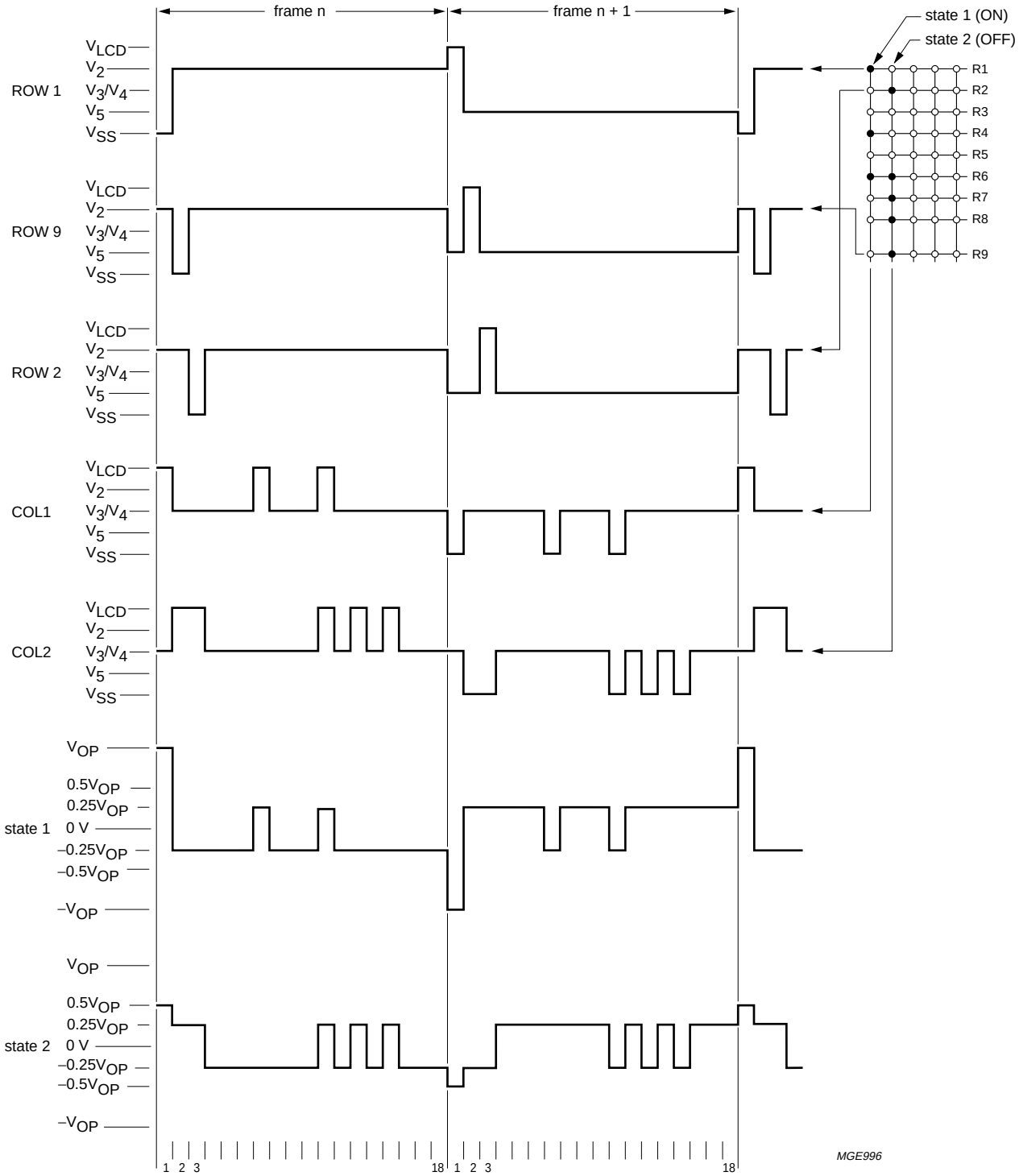


Fig.8 Typical LCD waveforms; character mode.

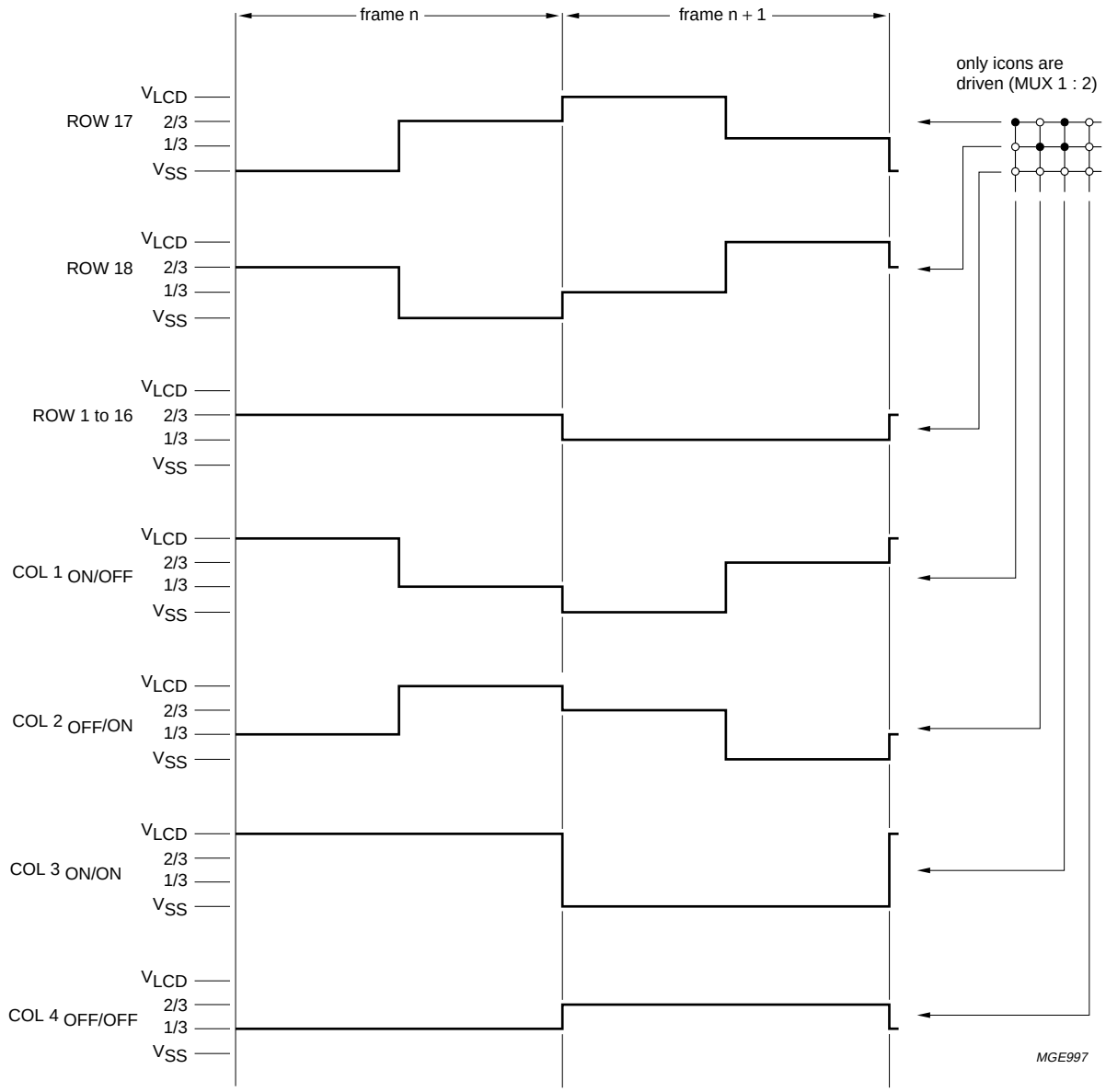
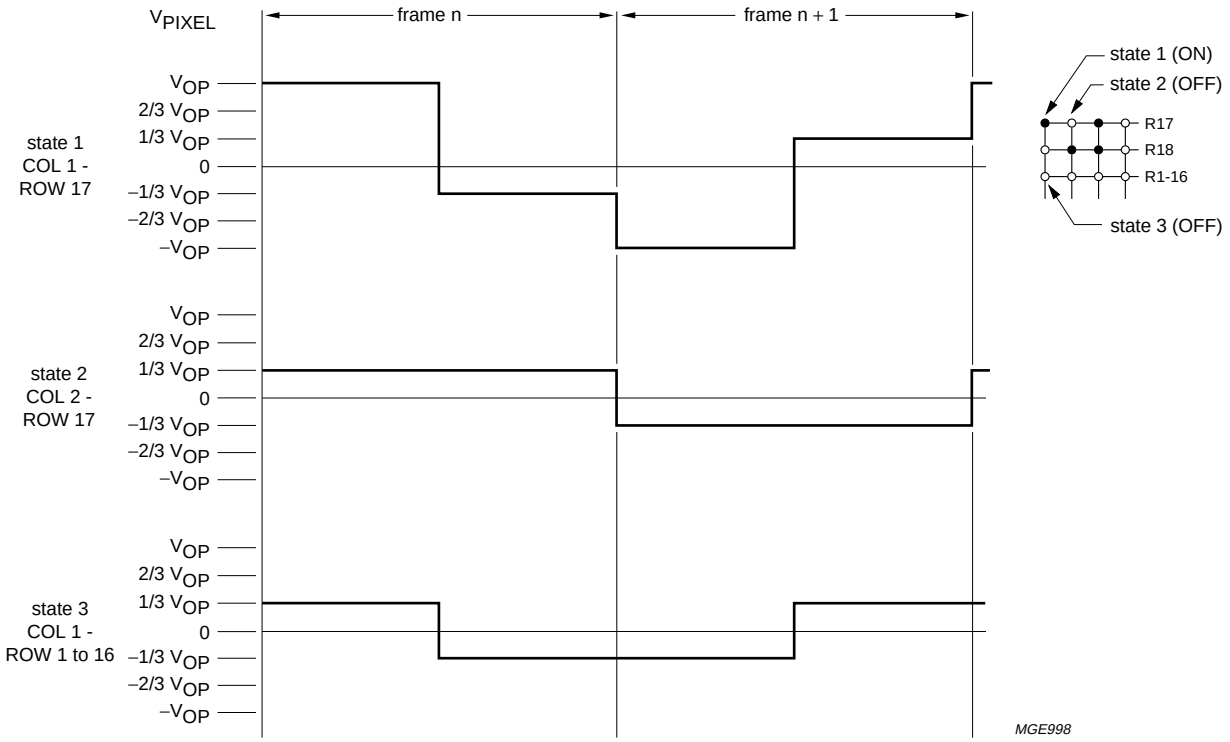


Fig.9 Mux 1 : 2 LCD waveforms; icon mode.



$V_{ON(rms)} = 0.745\ V_{OP}$.

$V_{OFF(rms)} = 0.333\ V_{OP}$.

$$D = \frac{V_{ON}}{V_{OFF}} = 2.23$$

Fig.10 Mux 1 : 2 LCD waveforms; icon mode.

7.15 Reset function

The PCF2103 automatically initializes (resets) when power is turned on. The reset executes a ‘clear display’ instruction, requiring 165 oscillator cycles. After the reset the chip has the state shown in Table 5.

Table 5 State after reset

STEP	INSTRUCTION	RESET STATE (BIT/REGISTER)	RESET STATE (DESCRIPTION)
1	clear display		
2	entry mode set	I/D = 1	+1 (increment)
		S = 0	no shift
3	display control	D = 0	display off
		C = 0	cursor off
		B = 0	cursor character blink off
4	function set	DL = 1	8-bit interface
		M = 0	1-line display
		H = 0	normal instruction set
5	default address pointer to DDRAM; the Busy Flag (BF) indicates the busy state (BF = 1) until initialization ends; the busy state lasts 2 ms; the chip may also be initialized by software; see Tables 16 and 17		
6	icon control	IM, IB = 00	icons/icon blink disabled
7	display/screen configuration	L, P, Q = 000	default configurations
8	I^2C-bus interface reset		

8 INSTRUCTIONS

Only two PCF2103 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the microcontroller. Before internal operation, control information is stored temporarily in these registers to allow interface to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs. The format for instructions when I^2C-bus control is used is shown in Table 6. The PCF2103 operation is controlled by the instructions given in Table 7 together with their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that:

1. Designate PCF2103 functions such as display format, data length, etc.
2. Set internal RAM addresses
3. Perform data transfer with internal RAM
4. Others.

In normal use, instructions that perform data transfer with internal RAM are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instruction other than the ‘read busy flag and address counter’ instruction will be executed. Because the busy flag is set to logic 1 while an instruction is being executed, the user should verify that the busy flag is at logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in Table 7. An instruction sent while the busy flag is logic 1 will not be executed.

Table 6 Instruction set for I^2C-bus commands

CONTROL BYTE								COMMAND BYTE								I^2C-BUS COMMANDS
Co	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	note 1

Note

1. R/$\overline{W}$ is set together with the slave address.

Table 7 Instruction set with parallel bus commands; note 1

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 0 or 1												
NOP	0	0	0	0	0	0	0	0	0	0	no operation	3
Function set	0	0	0	0	1	DL	0	M	0	H	sets interface Data Length (DL) and number of display lines (M); extended instruction set control (H)	3
Read busy flag and address counter	0	1	BF	AC							reads the Busy Flag (BF) indicating internal operating is being performed and reads address counter contents	0
Read data	1	1	read data								reads data from CGRAM or DDRAM	3
Write data	1	0	write data								writes data from CGRAM or DDRAM	3
H = 0												
Clear display	0	0	0	0	0	0	0	0	0	1	clears entire display and sets DDRAM address 0 in address counter	165
Return home	0	0	0	0	0	0	0	0	1	0	sets DDRAM address 0 in address counter; also returns shifted display to original position; DDRAM contents remain unchanged	3
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	sets cursor move direction and specifies shift of display; these operations are performed during data write and read	3
Display control	0	0	0	0	0	0	1	D	C	B	sets entire display on/off (D), cursor on/off (C) and blink of cursor position character (B); D = 0 (display off) puts chip into power-down mode	3
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	0	0	moves cursor and shifts display without changing DDRAM contents	3
Set CGRAM address	0	0	0	1	A_{CG}						sets CGRAM address; bit 6 is to be set by the command ‘set DDRAM address’; look at the description of the commands	3
Set DDRAM address	0	0	1	A_{DD}							sets DDRAM address	3

INSTRUCTION	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	REQUIRED CLOCK CYCLES
H = 1												
Reserved	0	0	0	0	0	0	0	0	0	1	do not use	–
Screen configuration	0	0	0	0	0	0	0	0	1	L	set screen configuration	3
Display configuration	0	0	0	0	0	0	0	1	P	Q	set display configuration	3
Icon control	0	0	0	0	0	0	1	IM	IB	0	set icon mode (IM), icon blink (IB)	3
Reserved	0	0	0	0	0	1	X	X	X	X	do not use	–
Reserved	0	0	0	1	X	X	X	X	X	X	do not use	–
Reserved	0	0	1	X	X	X	X	X	X	X	do not use	–

Note

1. X = don’t care.

Table 8 Specification of mnemonics used in Table 7

BIT	LOGIC 0	LOGIC 1
I/D	decrement	increment
S	display freeze	display shift
D	display off	display on
C	cursor off	cursor on
B	cursor character blink off: character at cursor position does not blink	cursor character blink on: character at cursor position blinks
S/C	cursor move	display shift
R/L	left shift	right shift
DL	4 bits	8 bits
H	use basic instruction set	use extended instruction set
L (ignored, if M = 1)	left/right screen: standard connection (as in PCF2114); 1st 12 characters of 24: columns are from 1 to 60; 2nd 12 characters of 24: columns are from 1 to 60	left/right screen: mirrored connection (as in PCF2116); 1st 12 characters of 24: columns are from 1 to 60; 2nd 12 characters of 24: columns are from 60 to 1
P	column data: left to right (as in PCF2116); column data is displayed from 1 to 60	column data: right to left; column data is displayed from 60 to 1
Q	row data: top to bottom (as in PCF2116); row data is displayed from 1 to 16 and icon row data is in 17 and 18	row data: bottom to top; row data is displayed from 16 to 1 and icon row data is in 18 and 17
IM	character mode; full display	icon mode; only icons displayed
IB	icon blink disabled	icon blink enabled
M	1-line by 24 display	2-line by 12 display
C_0	last control byte; see Table 6	another control byte follows after data/command

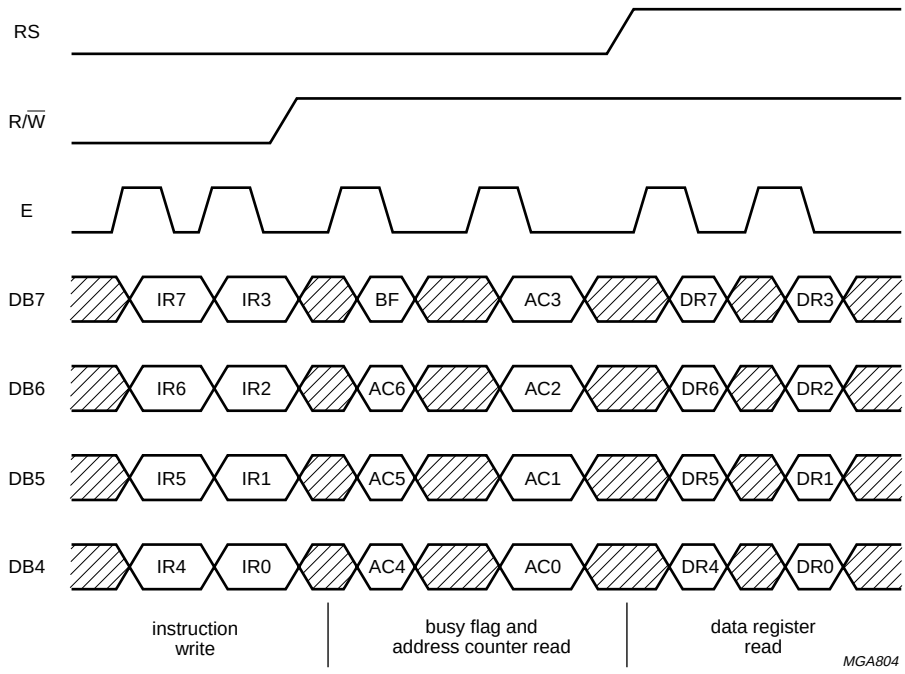
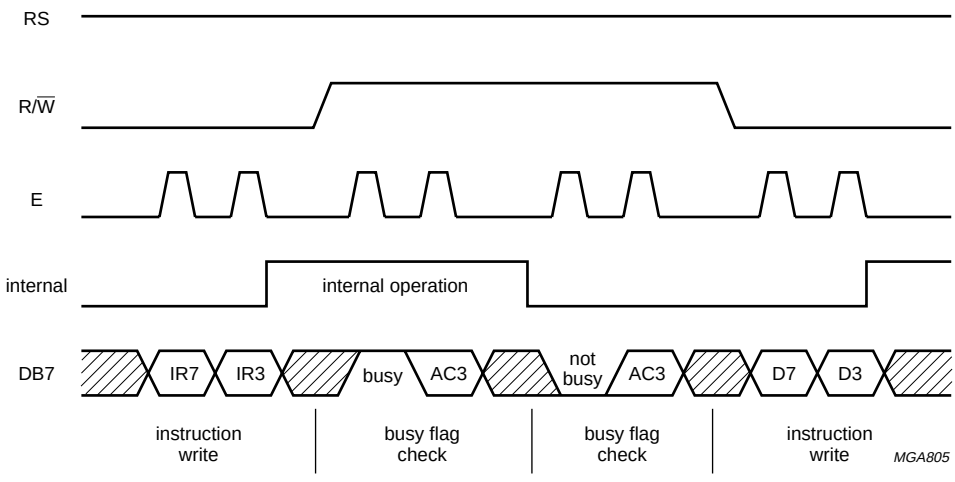


Fig.11 4-bit transfer example.



IR7 and IR3: instruction 7th and 3rd bit.
AC3: address counter 3rd bit.
D7 and D3: data 7th and 3rd bit.

Fig.12 An example of 4-bit data transfer timing sequence.

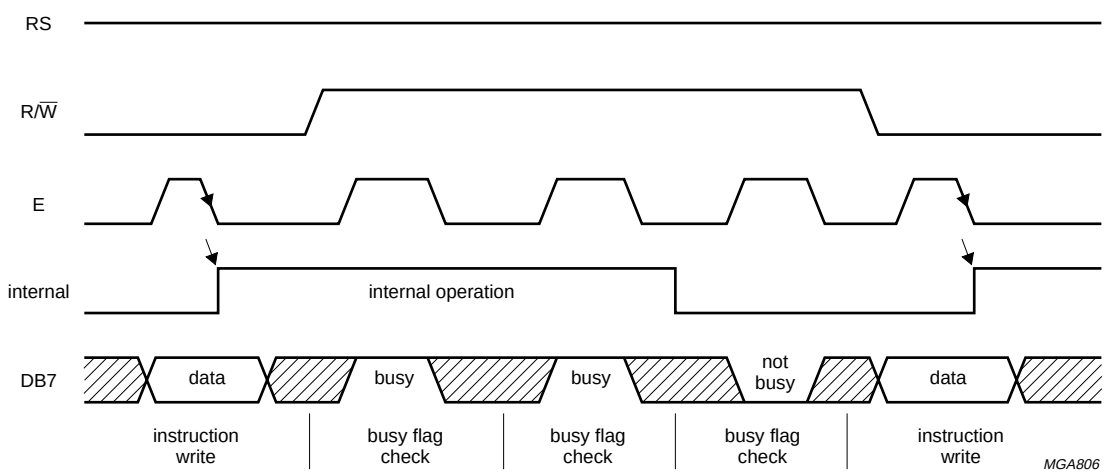


Fig.13 Example of busy flag checking timing sequence.

8.1 Clear display

'Clear display' writes character code 20H into all DDRAM addresses (the character pattern for character code 20H must be a blank pattern), sets the DDRAM address counter to logic 0 and returns display to its original position if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display. Sets entry mode I/D = 1 (increment mode). S of entry mode does not change.

The instruction 'clear display' requires extra execution time. This may be allowed by checking the Busy Flag (BF) or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

8.2 Return home

'Return home' sets the DDRAM address counter to logic 0 and returns display to its original position if it was shifted. DDRAM contents do not change. The cursor or blink position goes to the left of the first display line. I/D and S of entry mode do not change.

8.3 Entry mode set

8.3.1 I/D

When I/D = 1 (0) the DDRAM or CGRAM address increments (decrements) by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right when incremented and to the left when decremented. The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

8.3.2 S

When S = 1, the entire display shifts either to the right (I/D = 0) or to the left (I/D = 1) during a DDRAM write. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing into or reading out of the CGRAM. When S = 0 the display does not shift.

8.4 Display control (and partial power-down mode)

8.4.1 D

The display is on when D = 1 and off when D = 0. Display data in the DDRAM are not affected and can be displayed immediately by setting D to logic 1.

When the display is off (D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V_{SS}
- Bias generator is turned off.

3 oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at V_{SS}, afterwards OSC can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (OSC = V_{SS}).

To ensure I_{DD} < 2 μA the parallel bus pins DB7 to DB0 should be connected to V_{DD}; RS and R/$\overline{W}$ to V_{DD} or left open-circuit and PD to V_{DD}. Recovery from power-down mode: put PD back to logic 0, if necessary put OSC back to V_{DD} and send a 'display control' instruction with D = 1 to enable the display again.

8.4.2 C

The cursor is displayed when C = 1 and inhibited when C = 0. Even if the cursor disappears, the display functions I/D, etc. remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Fig.5).

8.4.3 B

The character indicated by the cursor blinks when B = 1. The cursor character blink is displayed by switching between display characters and all dots on with a period of approximately 1 s, with $f_{BLINK} = \frac{f_{osc}}{52224}$

The cursor underline and the cursor character blink can be set to display simultaneously.

8.5 Cursor or display shift

'Cursor/display shift' moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display. In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The Address Counter (AC) content does not change if the only action performed is shift display, but increments or decrements with the 'cursor shift'.

8.6 Function set

8.6.1 DL (PARALLEL MODE ONLY)

Sets interface data width. Data is sent or received in bytes (DB7 to DB0) when DL = 1 or in two nibbles (DB7 to DB4) when DL = 0. When 4-bit width is selected, data is transmitted in two cycles using the parallel bus. In a 4-bit application DB3 to DB0 should be left open-circuit (internal pull-ups). Hence in the first 'function set' instruction after power-on N and H are set to logic 1. A second 'function set' must then be sent (2 nibbles) to set N and H to their required values.

'Function set' from the I^2C-bus interface sets the DL bit to logic 1.

8.6.2 M

Chooses either 1-line by 24 display (M = 0) or 2-line by 12 display (M = 1).

8.6.3 H

When H = 0 the chip can be programmed via the standard 11 instruction codes used in the PCF2116 and other LCD controllers.

When H = 1 the extended range of instructions will be used. These are mainly for controlling the display configuration and the icons.

8.7 Set CGRAM address

'Set CGRAM address' sets bits 5 to 0 of the CGRAM address A_{CG} into the address counter (binary A[5] to A[0]). Data can then be written to or read from the CGRAM.

Attention: the CGRAM address uses the same address register as the DDRAM address and consists of 7 bits (binary A[6] to A[0]). With the 'set CGRAM address' command, only bits 5 down to 0 are set. Bit 6 can be set using the 'set DDRAM address' command first, or by using the auto-increment feature during CGRAM write.
All bits 6 to 0 can be read using the 'read busy flag and address counter' command.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write or read action).

8.8 Set DDRAM address

'Set DDRAM address' sets the DDRAM address A_{DD} into the address counter (binary A[6] to A[0]). Data can then be written to or read from the DDRAM.

8.9 Read busy flag and address counter

'Read busy flag and address counter' reads the Busy Flag (BF) and Address Counter (AC). BF = 1 indicates that an internal operation is in progress. The next instruction will not be executed until BF = 0, so BF should be checked before sending another instruction.

At the same time, the value of the address counter expressed in binary A[6] to A[0] is read out. The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous instruction.

8.10 Write data to CGRAM or DDRAM

'Write data' writes binary 8-bit data D[7] to D[0] to the CGRAM or the DDRAM.

Whether the CGRAM or DDRAM is to be written into is determined by the previous 'set CGRAM address' or 'set DDRAM address' command. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode. Only bits D[4] to D[0] of CGRAM data are valid, bits D[7] to D[5] are 'don't care'.

8.11 Read data from CGRAM or DDRAM

'Read data' reads binary 8-bit data D[7] to D[0] from the CGRAM or DDRAM.

The most recent 'set address' command determines whether the CGRAM or DDRAM is to be read.

The 'read data' instruction gates the content of the Data Register (DR) to the bus while pin E is HIGH. After pin E goes LOW again, internal operation increments (or decrements) the AC and stores RAM data corresponding to the new AC into the DR.

It should be noted that there are only three instructions that update the Data Register (DR). These are:

- 'set CGRAM address'
- 'set DDRAM address'
- 'read data' from CGRAM or DDRAM.

Other instructions (e.g. 'write data', 'cursor/display shift', 'clear display', 'return home') do not modify the data register content.

8.12 Extended function set instructions and features

8.12.1 NEW INSTRUCTIONS

H = 1 sets the chip into alternate instruction set mode.

8.12.2 ICON CONTROL

The PCF2103 can drive up to 120 icons. See Fig.14 for CGRAM to icon mapping.

8.12.3 IM

When IM = 0 the chip is in character mode. In character mode characters and icons are driven (mux 1 : 18).

When IM = 1 the chip is in icon mode. In icon mode only the icons are driven (mux 1 : 2).

8.12.4 IB

Icon blink control is independent of the cursor/character blink function.

When IB = 0 icon blink is disabled. Icon data is stored in CGRAM character 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons).

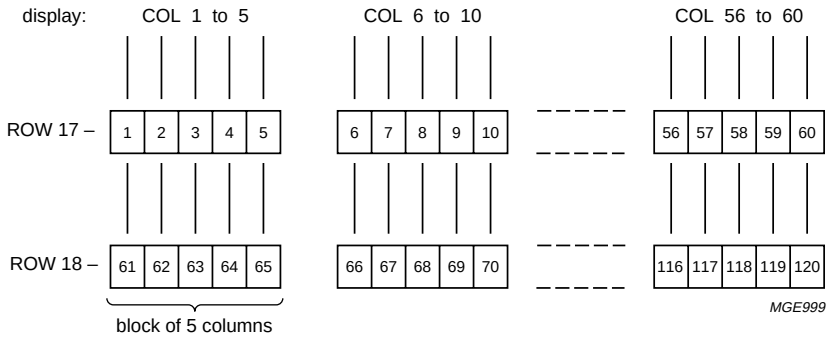
When IB = 1 icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 2 ($3 \times 8 \times 5 = 120$ bits for 120 icons). These bits also define the icon state when the icon blink is not used.

Icon states for the odd phase are stored in CGRAM character 4 to 6 (another 120 bits for the 120 icons). When icon blink is disabled CGRAM characters 4 to 6 may be used as normal CGRAM characters.

Table 9 Blink effect for icons and cursor character blink

PARAMETER	EVEN PHASE	ODD PHASE
Cursor underline	on	off
Cursor character blink	block (all on)	normal (display character)
Icons	state 1: CGRAM characters 0 to 2	state 2: CGRAM characters 4 to 6



icon no.	phase	ROW/COL	character codes	CGRAM address	CGRAM data	icon view
			7 6 5 4 3 2 1 0 MSB LSB	6 5 4 3 2 1 0 MSB LSB	4 3 2 1 0 MSB LSB	
1-5	even	17/1-5	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0	1 0 1 0 1	
6-10	even	17/6-10	0 0 0 0 0 0 0 0	0 0 0 0 0 0 1	0 1 0 1 0	
11-15	even	17/11-15	0 0 0 0 0 0 0 0	0 0 0 0 0 1 0	0 1 1 1 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
56-60	even	17/56-60	0 0 0 0 0 0 0 1	0 0 0 1 0 1 1	1 1 1 1 1	
61-65	even	18/1-5	0 0 0 0 0 0 0 1	0 0 0 1 1 0 0	1 1 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	even	18/56-60	0 0 0 0 0 0 1 0	0 0 1 0 1 1 1	1 1 1 0 1	
1-5	odd (blink)	17/1-5	0 0 0 0 0 1 0 0	0 1 0 0 0 0 0	0 0 0 0 0	
⋮	⋮	⋮	⋮	⋮	⋮	⋮
116-120	odd (blink)	18/56-60	0 0 0 0 0 1 1 0	0 1 1 0 0 1 1	0 0 1 1 0	

MGG001

CGRAM data bit = logic 1 turns the icon on, data bit = logic 0 turns the icon off.
Data in character codes 0 to 2 define the icon states when icon blink is disabled or during the even phase when icon blink is enabled.
Data in character codes 4 to 6 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled).

Fig.14 CGRAM-to-icon mapping.

8.12.5 SCREEN CONFIGURATION

The default value for L is logic 0. In the event of L = 0 the two halves of a split screen are connected in a standard way i.e. column 1/61, 2/62 to 60/120. In the event of L = 1 the two halves of a split screen are connected in a mirrored way i.e. column 1/120, 2/119 to 60/61. This allows single layer PCB or glass layout.

8.12.6 DISPLAY CONFIGURATION

The default value for P and Q is logic 0. P = 1 mirrors the column data whereas Q = 1 mirrors the row data.

8.12.7 REDUCING CURRENT CONSUMPTION

Reducing current consumption can be achieved by one of the options mentioned in Table 10.

Table 10 Reducing current consumption

ORIGINAL MODE	ALTERNATIVE MODE
Character mode	icon mode (control bit IM)
Display on	display off (control bit D)

9 INTERFACE TO MICROCONTROLLER

9.1 Parallel interface

The PCF2103 can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 data lines DB7 to DB0. Three further control lines E, RS and R/$\overline{W}$ are required; see Table 1.

In 4-bit mode data is transferred in two cycles of 4 bits each using pins DB7 to DB4 for transaction. The higher order bits (corresponding to DB7 to DB4 in 8-bit mode) are sent in the first cycle and the lower order bits (DB3 to DB0 in 8-bit mode) in the second. Data transfer is complete after two 4-bit data transfers. Note that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction. See Figs 11 to 14 for examples of bus protocol.

In 4-bit mode pins DB3 to DB0 must be left open-circuit. They are pulled up to V_{DD} internally.

9.2 I²C-bus interface

9.2.1 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a Serial Clock Line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

9.2.2 I²C-bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The I²C-bus configuration for the different PCF2103 read and write cycles is shown in Figs 20 to 21. The slow down feature of the I²C-bus protocol (receiver holds SCL low during internal operations) is not used in the PCF2103.

9.2.3 Definitions

- Transmitter: the device which sends the data to the bus
- Receiver: the device which receives the data from the bus
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronization: procedure to synchronize the clock signals of two or more devices.

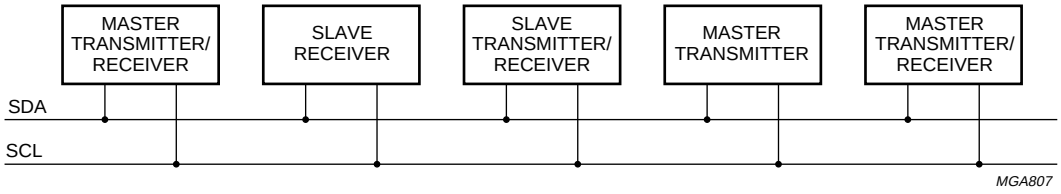


Fig.15 System configuration.

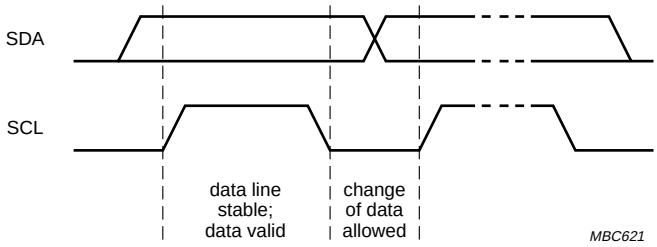


Fig.16 Bit transfer.

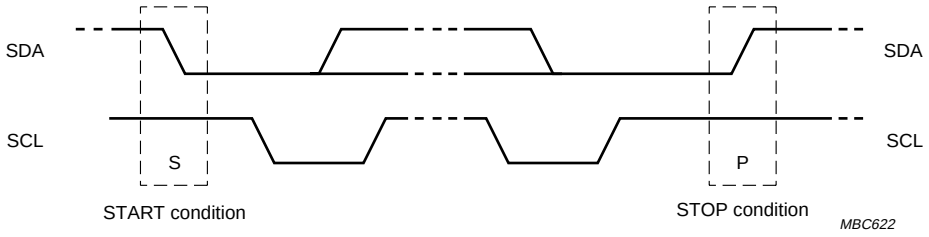


Fig.17 Definition of START and STOP conditions.

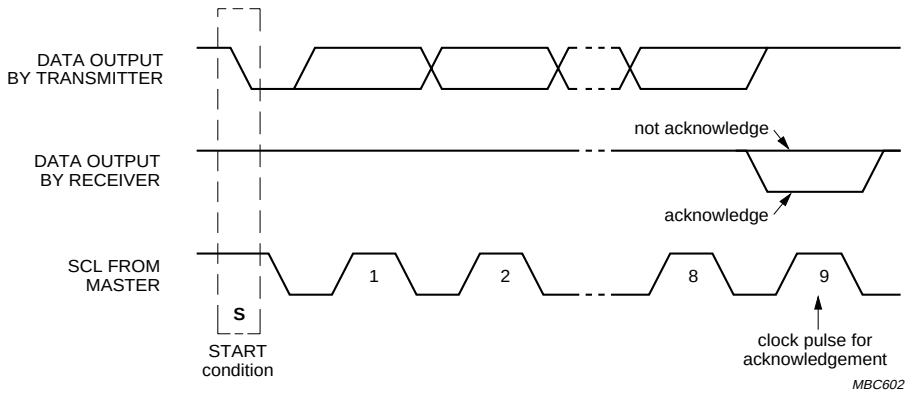


Fig.18 Acknowledgement on the I^2C-bus.

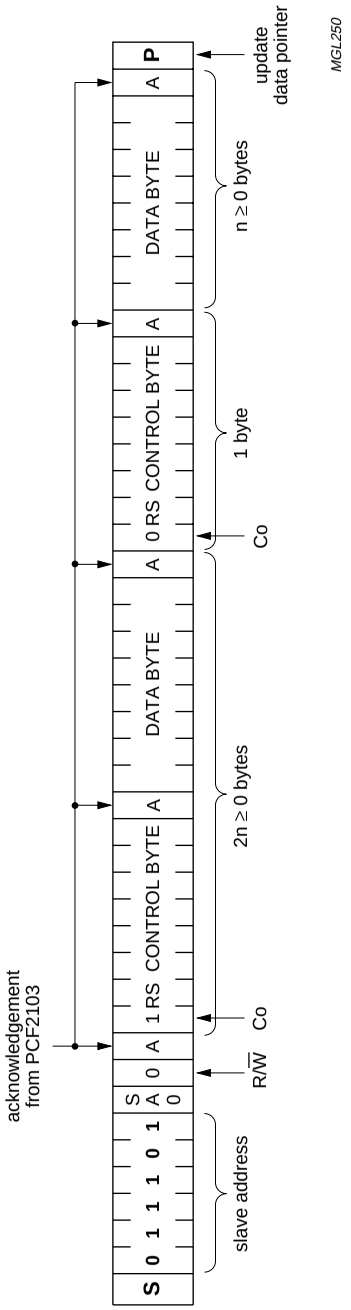
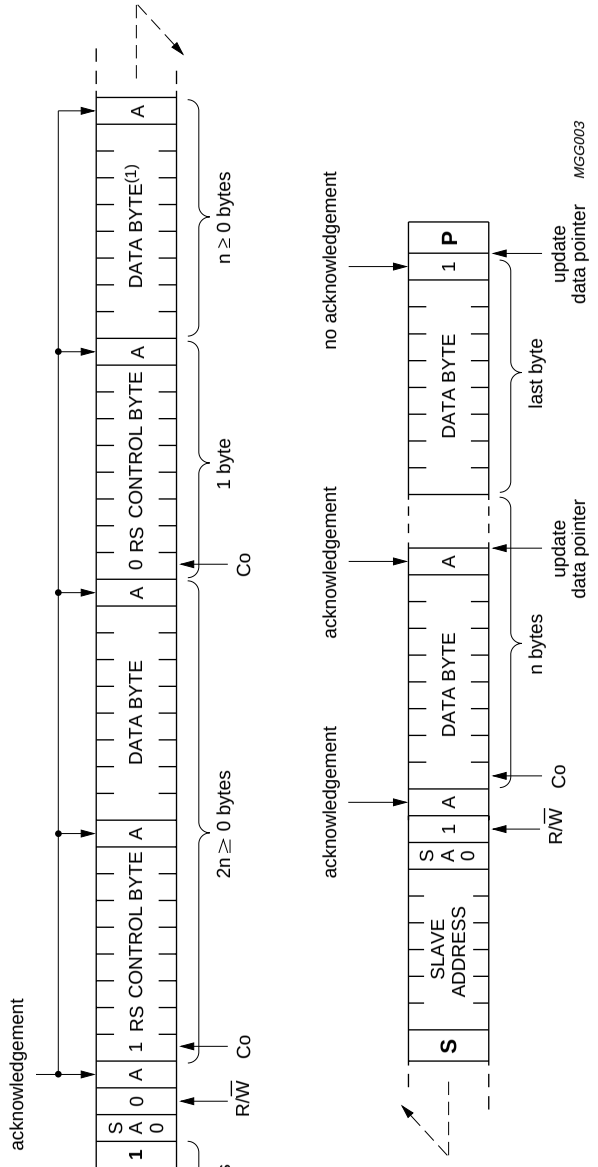


Fig.19 Master transmits to slave receiver; write mode.



(1) Last data byte is a dummy byte (may be omitted).

Fig.20 Master reads after setting word address; write word address, set RS; 'read data'.

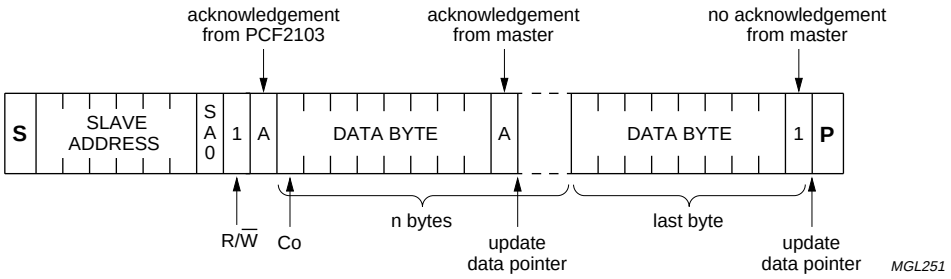


Fig.21 Master reads slave immediately after first byte; read mode (RS previously defined).

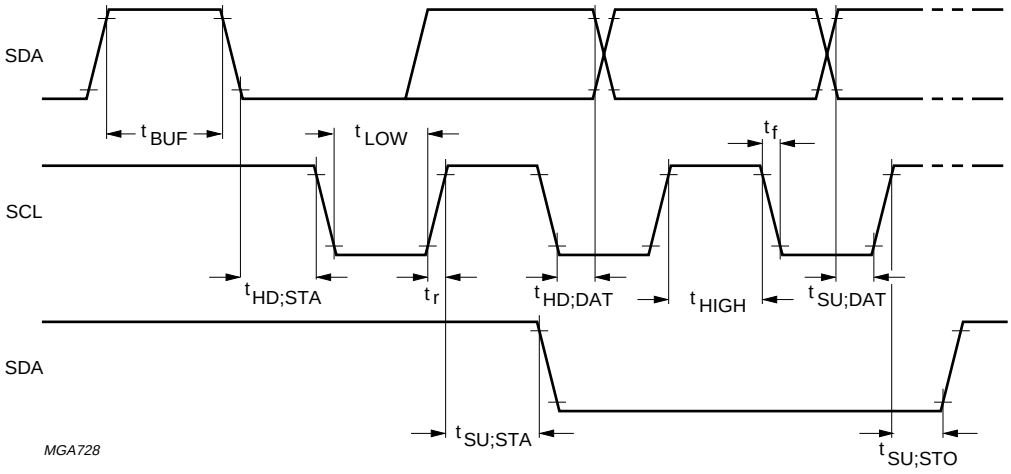


Fig.22 I^2C-bus timing diagram.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
V_{LCD}	LCD supply voltage	–0.5	+7.5	V
$V_{I(1)}$	input voltage on pins OSC, RS, R/$\overline{W}$, E and DB7 to DB0	–0.5	V_{DD} + 0.5	V
$V_{I(2)}$	input voltage on pins SCL and SDA	–0.5	+6.5	V
V_O	output voltage on pins R1 to R18, C1 to C60 and V_{LCD}	–0.5	V_{LCD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}, I_{SS} and I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	–50	+50	mA
P_{tot}	total power dissipation	–	400	mW
P/out	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

12 DC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 to 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		1.8	–	5.5	V
V_{LCD}	LCD supply voltage		2.2	–	6.5	V
I_{SS}	supply current	note 1	–	60	120	µA
		V_{DD} = 3 V; V_{LCD} = 5 V; notes 1 and 2	–	45	80	µA
		icon mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; notes 1 and 2	–	25	45	µA
		power-down mode; V_{DD} = 3 V; V_{LCD} = 2.5 V; DB7 to DB0, RS and R/$\overline{W}$ = 1; OSC = 0; PD = 1; note 1	–	2	6	µA
V_{POR}	power-on reset voltage	note 3	–	1.3	1.6	V
Logic						
V_{IL}	LOW-level input voltage on pins T1, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		0	–	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage on pins T1, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0		0.7V_{DD}	–	V_{DD}	V
$V_{IL(PD)}$	LOW-level input voltage on pin PD		0	–	0.2V_{DD}	V
$V_{IH(PD)}$	HIGH-level input voltage on pin PD		0.8V_{DD}	–	V_{DD}	V
$V_{IL(OSC)}$	LOW-level input voltage on pin OSC		0	–	V_{DD} – 1.5	V
$V_{IH(OSC)}$	HIGH-input voltage on pin OSC		V_{DD} – 0.1	–	V_{DD}	V
$I_{OL(DB)}$	LOW-level output current on pins DB7 to DB0	V_{OL} = 0.4 V; V_{DD} = 5 V	1.6	4	–	mA
$I_{OH(DB)}$	HIGH-level output current on pins DB7 to DB0	V_{OH} = 4 V; V_{DD} = 5 V	–1	–8	–	mA
I_{pu}	pull-up current on pins DB7 to DB0	V_I = V_{SS}	0.04	0.12	1	µA
I_L	leakage current on pins OSC, E, RS, R/$\overline{W}$, DB7 to DB0 and SA0	V_I = V_{DD} or V_{SS}	–1	–	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I^2C-bus						
SDA AND SCL						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	5.5	V
I_L	input leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	μA
C_i	input capacitance	note 4	–	–	10	pF
I_{OL}	LOW-level output current pin SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
LCD outputs						
$R_{o(ROW)}$	row output resistance on pins R1 to R18	note 5	–	10	30	kΩ
$R_{o(COL)}$	column output resistance on pins C1 to C60	note 5	–	15	40	kΩ
$V_{bias(tol)}$	bias tolerance on pins R1 to R18 and C1 to C60	note 6	–	20	130	mV

Notes

1. LCD outputs are open-circuit; inputs at V_{DD} or V_{SS}; bus inactive.
2. T_{amb} = 25 °C; f_{osc} = 200 kHz.
3. Resets all logic when $V_{DD} < V_{POR}$; 3 oscillator clock cycles required.
4. Tested on sample basis.
5. Resistance of output terminals (R1 to R18 and C1 to C60) with a load current of 20 μA; outputs measured one at a time.
6. LCD outputs open-circuit.

13 AC CHARACTERISTICS

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.2 – 6.5 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{fr(LCD)}$	LCD frame frequency (internal clock)	V_{DD} = 5.0 V	45	81	147	Hz
f_{osc}	oscillator frequency (not available at any pin)		140	250	450	kHz
$f_{osc(ext)}$	external clock frequency		140	–	450	kHz
t_{OSCST}	oscillator start-up time after PD going from logic 1 to logic 0		–	200	300	µs
Bus timing characteristics: parallel interface; note 1						
WRITE OPERATION (WRITING DATA FROM MICROCONTROLLER TO PCF2103); see Fig.23						
$T_{en(cy)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{su(D)}$	data set-up time		60	–	–	ns
$t_{h(D)}$	data hold time		25	–	–	ns
READ OPERATION (READING DATA FROM PCF2103 TO MICROCONTROLLER); see Fig.24						
$T_{en(cy)}$	enable cycle time		500	–	–	ns
$t_{W(en)}$	enable pulse width		220	–	–	ns
$t_{su(A)}$	address set-up time		50	–	–	ns
$t_{h(A)}$	address hold time		25	–	–	ns
$t_{d(D)}$	data delay time		–	–	150	ns
$t_{h(D)}$	data hold time		20	–	100	ns
Timing characteristics: I^2C-bus interface; note 1						
f_{SCL}	SCL clock frequency		–	–	400	kHz
t_{LOW}	SCL clock LOW period		1.3	–	–	µs
t_{HIGH}	SCL clock HIGH period		0.6	–	–	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
t_r	SCL and SDA rise time		–	–	300	ns
t_f	SCL and SDA fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Note

1. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

14 TIMING CHARACTERISTICS

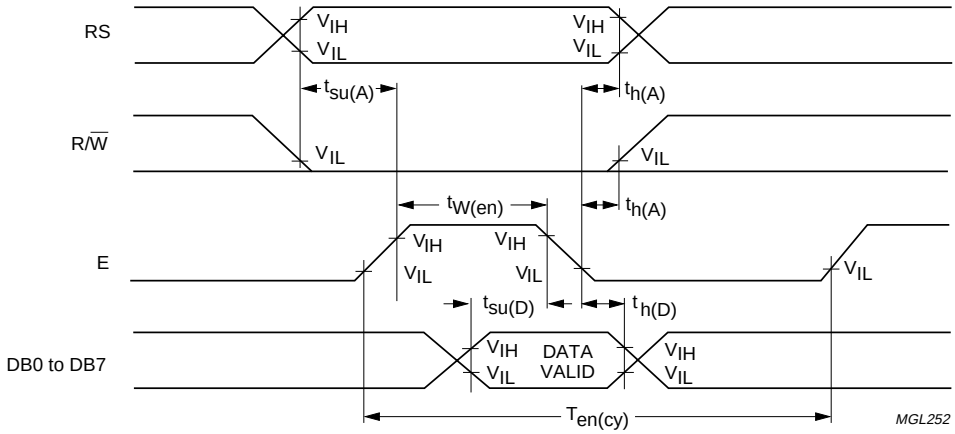


Fig.23 Parallel bus write operation sequence; writing data from microcontroller to PCF2103.

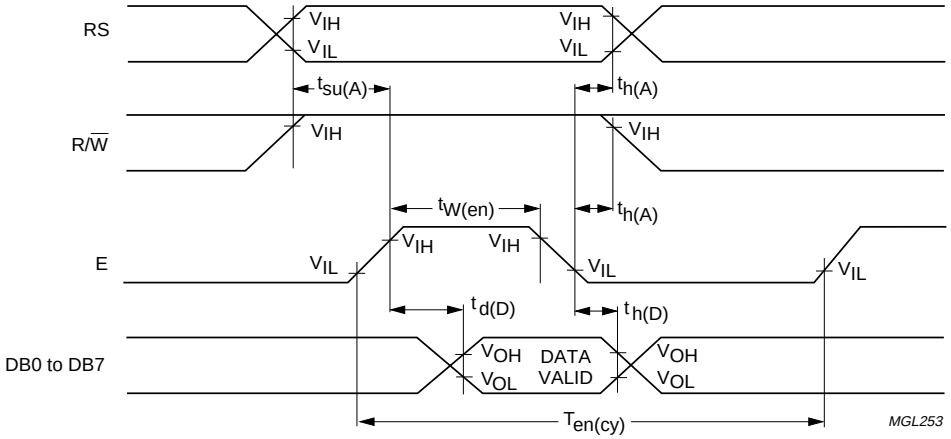


Fig.24 Parallel bus read operation sequence; reading data from PCF2103 to microcontroller.

15 APPLICATION INFORMATION

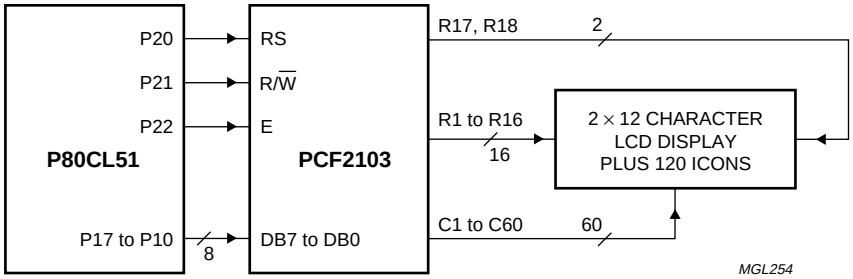


Fig.25 Direct connection to 8-bit microcontroller; 8-bit bus.

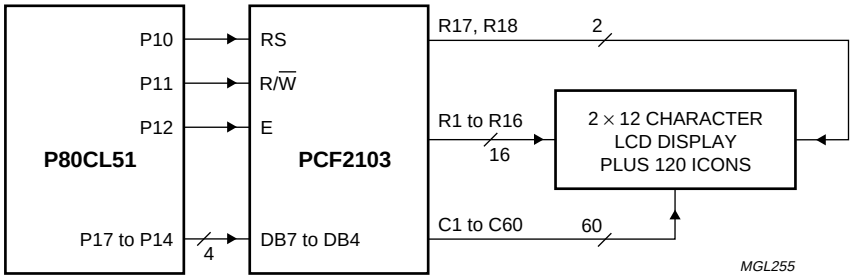


Fig.26 Direct connection to 8-bit microcontroller; 4-bit bus.

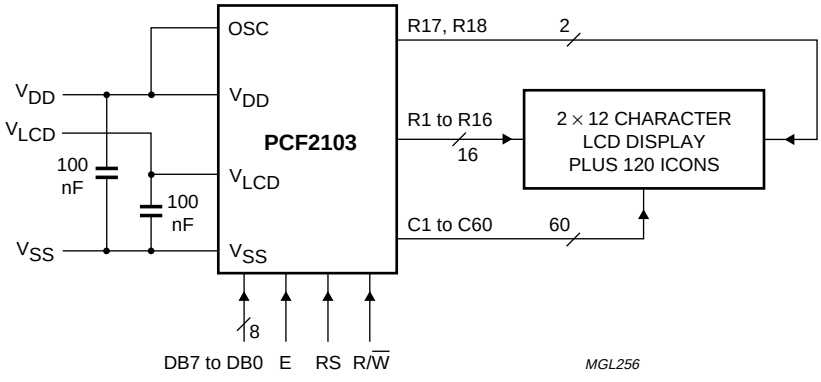


Fig.27 Application example using parallel interface.

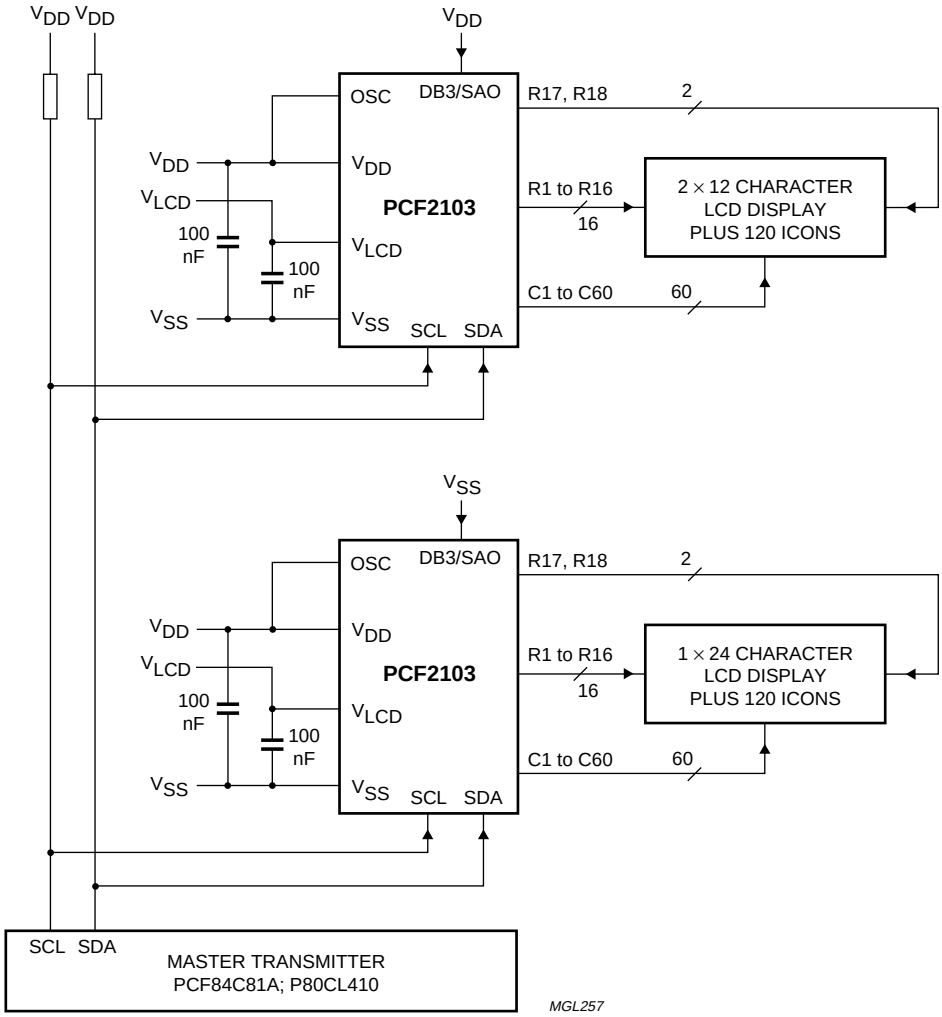


Fig.28 Application using I^2C-bus interface.

15.1 4-bit operation, 1-line display using internal reset

The program must set functions prior to 4-bit operation; Table 11 shows an example. When power is turned on, 8-bit operation is automatically selected and the PCF2103 attempts to perform the first write as an 8-bit operation. Since nothing is connected to DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see Table 11 step 3). Thus, DB4 to DB7 of the 'function set' are written twice.

15.2 8-bit operation, 1-line display using internal reset

Table 12 shows an example of a 1-line display in 8-bit operation. The PCF2103 functions must be set by the 'function set' instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays when combined with display shift operation.

Since the display shift operation changes display position only and DDRAM contents remain unchanged, display data entered first can be displayed when the 'return home' operation is performed.

15.3 8-bit operation, 2-line display

For a 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the eighth character is completed (see Table 6). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

15.4 I^2C-bus operation, 1-line display

A control byte is required with most commands (see Table 15).

Table 11 4-bit operation, 1-line display example; using internal reset

STEP	INSTRUCTION						DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset circuit)							initialized; no display appears
2	function set							
	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4		sets to 4-bit operation; in this instance operation is handled as 8-bit by initialization and only this instruction completes with one write
	0	0	0	0	1	0		
3	function set							
	0	0	0	0	1	0		sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$; 4-bit operation starts from this point and resetting is needed
	0	0	0	0	0	0		
4	display on/off control							
	0	0	0	0	0	0	_	turns on display and cursor; entire display is blank after initialization
	0	0	1	1	1	0		
5	entry mode set							
	0	0	0	0	0	0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DD/CGRAM; display is not shifted
	0	0	0	1	1	0		
6	'write data' to CGRAM/DDRAM							
	1	0	0	1	0	1	**P**_	writes 'P'; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
	1	0	0	0	0	0		

Table 12 8-bit operation, 1-line display example; using internal reset (character set ‘A’)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes ‘P’; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes ‘H’
7 to 11			
12	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes ‘S’
13	entry mode set 0 0 0 0 0 0 0 1 1 1	**PHILIPS**_	sets mode for display shift at the time of write
14	‘write data’ to CGRAM/DDRAM 1 0 0 0 1 0 0 0 0 0	**HILIPS** _	writes space
15	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**ILIPS M**_	writes ‘M’
16			

STEP	INSTRUCTION										DISPLAY	OPERATION
17	‘write data’ to CGRAM/DDRAM											
	1	0	0	1	0	0	1	1	1	1	**MICROKO_**	writes ‘O’
18	cursor/display shift											
	0	0	0	0	0	1	0	0	0	0	**MICROKO**	shifts only the cursor position to the left
19	cursor/display shift											
	0	0	0	0	0	1	0	0	0	0	**MICROKO**	shifts only the cursor position to the left
20	‘write data’ to CGRAM/DDRAM											
	1	0	0	1	0	0	0	0	1	1	**ICROKO**	writes ‘C’ correction; the display moves to the left
21	cursor/display shift											
	0	0	0	0	0	1	1	1	0	0	**MICROKO**	shifts the display and cursor to the right
22	cursor/display shift											
	0	0	0	0	0	1	0	1	0	0	**MICROCO_**	shifts only the cursor to the right
23	‘write data’ to CGRAM/DDRAM											
	1	0	0	1	0	0	1	1	0	1	**ICROCOM_**	writes ‘M’
24												
25	return home											
	0	0	0	0	0	0	0	0	1	0	**PHILIPS M**	returns both display and cursor to the original position (address 0)

Table 13 8-bit operation, 1-line display and icon example; using internal reset (character set ‘A’)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 0 0		sets to 8-bit operation, selects 1-line display
3	display mode on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted
5	set CGRAM address 0 0 0 1 0 0 0 0 0 0	_	sets the CGRAM address to position of character 0; the CGRAM is selected
6	‘write data’ to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon even phase; icons appear
7			
8	set CGRAM address 0 0 0 1 1 1 0 0 0 0	_	sets the CGRAM address to position of character 4; the CGRAM is selected
9	‘write data’ to CGRAM/DDRAM 1 0 0 0 0 0 1 0 1 0	_	writes data to CGRAM for icon odd phase
10			
11	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 1
12	icon control 0 0 0 0 0 0 1 0 1 0	_	icons blink
13	function set 0 0 0 0 1 1 0 0 0 1	_	sets H = 0

STEP	INSTRUCTION	DISPLAY	OPERATION
14	set DDRAM address 0 0 1 0 0 0 0 0 0 0		sets the DDRAM address to the first position; DDRAM is selected
15	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes ‘P’; the cursor is incremented by 1 and shifted to the right
16	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 0 0 0	**PH**_	writes ‘H’
17 to 20			
21	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS**	returns both display and cursor to the original position (address 0)

Table 14 8-bit operation, 2-line display example; using internal reset

STEP	INSTRUCTION	DISPLAY	OPERATION
1	power supply on (PCF2103 is initialized by the internal reset function)		initialized; no display appears
2	function set RS R/$\overline{W}$ DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 0 0		sets to 8-bit operation; selects 2-line display and voltage generator off
3	display on/off control 0 0 0 0 0 0 1 1 1 0	_	turns on display and cursor; entire display is blank after initialization
4	entry mode set 0 0 0 0 0 0 0 1 1 0	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted
5	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 0 0	**P**_	writes ‘P’; the DDRAM has already been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6 to 10		|	
11	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 1 0 0 1 1	**PHILIPS**_	writes ‘S’
12	set DDRAM address 0 0 1 1 0 0 0 0 0 0	**PHILIPS** _	sets DDRAM address to position the cursor at the head of the 2nd line
13	‘write data’ to CGRAM/ DDRAM 1 0 0 1 0 0 1 1 0 1	**PHILIPS** **M**_	writes ‘M’
14 to 19		|	

STEP	INSTRUCTION	DISPLAY	OPERATION
20	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 1 1	**PHILIPS** **MICROCO_**	writes ‘O’
21	‘write data’ to CGRAM/DDRAM 0 0 0 0 0 0 0 1 1 1	**PHILIPS** **MICROCO_**	sets mode for display shift at the time of write
22	‘write data’ to CGRAM/DDRAM 1 0 0 1 0 0 1 1 0 1	**HILIPS** **ICROCOM_**	writes ‘M’; display is shifted to the left; the first and second lines shift together
23			
24	return home 0 0 0 0 0 0 0 0 1 0	**PHILIPS** **MICROCOM**	returns both display and cursor to the original position (address 0)

Table 15 Example of I²C-bus operation; 1-line display (using internal reset, assuming SA0 = V_{SS}; note 1)

STEP	INSTRUCTION	DISPLAY	OPERATION
1	I²C-bus start		initialized; no display appears
2	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1		during the acknowledge cycle SDA will be pulled-down by the PCF2103
3	send a control byte for ‘function set’ Co RS 0 0 0 0 0 0 Ack 0 0 0 0 0 0 0 0 1		control byte sets RS for following data bytes
4	function set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 1 X 0 0 0 0 1		selects 1-line display; SCL pulse during acknowledge cycle starts execution of instruction
5	display on/off control DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 1 1 1 0 1	_	turns on display and cursor; entire display shows character 20H (blank in ASCII-like character sets)
6	entry mode set DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 1 1 0 1	_	sets mode to increment the address by 1 and to shift the cursor to the right at the time of write to the DDRAM or CGRAM; display is not shifted
7	I²C-bus start	_	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave address for write SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 0 1	_	
9	send a control byte for ‘write data’ Co RS 0 0 0 0 0 0 Ack 0 1 0 0 0 0 0 0 1	_	
10	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 0 0 1	 **P**_	writes ‘P’; the DDRAM has been selected at power-up; the cursor is incremented by 1 and shifted to the right

STEP	INSTRUCTION	DISPLAY	OPERATION
11	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 1	**PH_**	writes ‘H’
12 to 15		|	
16	‘write data’ to DDRAM DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 1 0 0 1 1 1	**PHILIPS_**	writes ‘S’
17	(optional I^2C-bus stop) I^2C-bus start + slave address for write (as step 8)	**PHILIPS_**	
18	control byte Co RS 0 0 0 0 0 0 Ack 1 0 0 0 0 0 0 0 1	**PHILIPS_**	
19	return home DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 0 0 0 0 0 1 0 1	**PHILIPS**	sets DDRAM address 0 in address counter (also returns shifted display to original position; DDRAM contents unchanged); this instruction does not update the Data Register (DR)
20	I^2C-bus start	**PHILIPS**	
21	slave address for read SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/$\overline{W}$ Ack 0 1 1 1 0 1 0 1 1	**PHILIPS**	during the acknowledge cycle the content of the DR is loaded into the internal I^2C-bus interface to be shifted out; in the previous instruction neither a ‘set address’ nor a ‘read data’ has been performed; therefore the content of the DR was unknown; R/$\overline{W}$ has to be set to logic 1 while still in I^2C-bus write mode
22	control byte for read Co RS 0 0 0 0 0 0 Ack 0 1 1 0 0 0 0 0 1	**PHILIPS**	DDRAM content will be read from following instructions

STEP	INSTRUCTION	DISPLAY	OPERATION
23	‘read data’: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack X X X X X X X X 0	**PHILIPS**	8 × SCL; content loaded into interface during previous acknowledge cycle is shifted out over SDA; MSB is DB7; during master acknowledge content of DDRAM address 01 is loaded into the I^2C-bus interface
24	‘read data’: 8 × SCL + master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 0 0	**PHILIPS**	8 × SCL; code of letter ‘H’ is read first; during master acknowledge code of ‘I’ is loaded into the I^2C-bus interface
25	‘read data’: 8 × SCL + no master acknowledge; note 2 DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack 0 1 0 0 1 0 0 1 1	**PHILIPS**	no master acknowledge; after the content of the I^2C-bus interface register is shifted out no internal action is performed; no new data is loaded to the interface register, Data Register (DR) is not updated, Address Counter (AC) is not incremented and cursor is not shifted
26	I^2C-bus stop	**PHILIPS**	

Notes

1. X = don’t care.
2. SDA is left at high-impedance by the microcontroller during the read acknowledge.

Table 16 Initialization by instruction, 8-bit interface (note 1)

STEP										DESCRIPTION
power-on or unknown state										
					↓					
wait 2 ms after V_{DD} rises above V_{POR}										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait 2 ms										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓					
wait more than 40 μs										
					↓					
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	BF cannot be checked before this instruction
0	0	0	0	1	1	X	X	X	X	function set (interface is 8 bits long)
					↓ ↓					BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 4)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	function set (interface is 8 bits long); specify the number of display lines
0	0	0	0	1	1	0	M	0	H	
0	0	0	0	0	0	1	0	0	0	display off
0	0	0	0	0	0	0	0	0	1	clear display
0	0	0	0	0	0	0	1	I/D	S	entry mode set
					↓					
Initialization ends										

Note

1. X = don’t care.

Table 17 Initialization by instruction, 4-bit interface; not applicable for I²C-bus operation

STEP						DESCRIPTION
Power-on or unknown state						
			↓			
Wait 2 ms after V_{DD} rises above V_{POR}						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			
Wait 2 ms						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			
Wait 40 μs						
			↓			
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	BF cannot be checked before this instruction
0	0	0	0	1	1	function set (interface is 8 bits long)
			↓			BF can be checked after the following instructions; when BF is not checked, the waiting time between instructions is the specified instruction time (see Table 4)
RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	function set (set interface to 4 bits long)
0	0	0	0	1	0	interface is 8 bits long
0	0	0	0	1	0	function set (interface is 4 bits long)
0	0	0	M	0	H	specify number of display lines
0	0	0	0	0	0	
0	0	1	0	0	0	display off
0	0	0	0	0	0	clear display
0	0	0	0	0	1	
0	0	0	0	0	0	entry mode set
0	0	0	1	I/D	S	
			↓			
Initialization ends						

16 BONDING PAD LOCATIONS

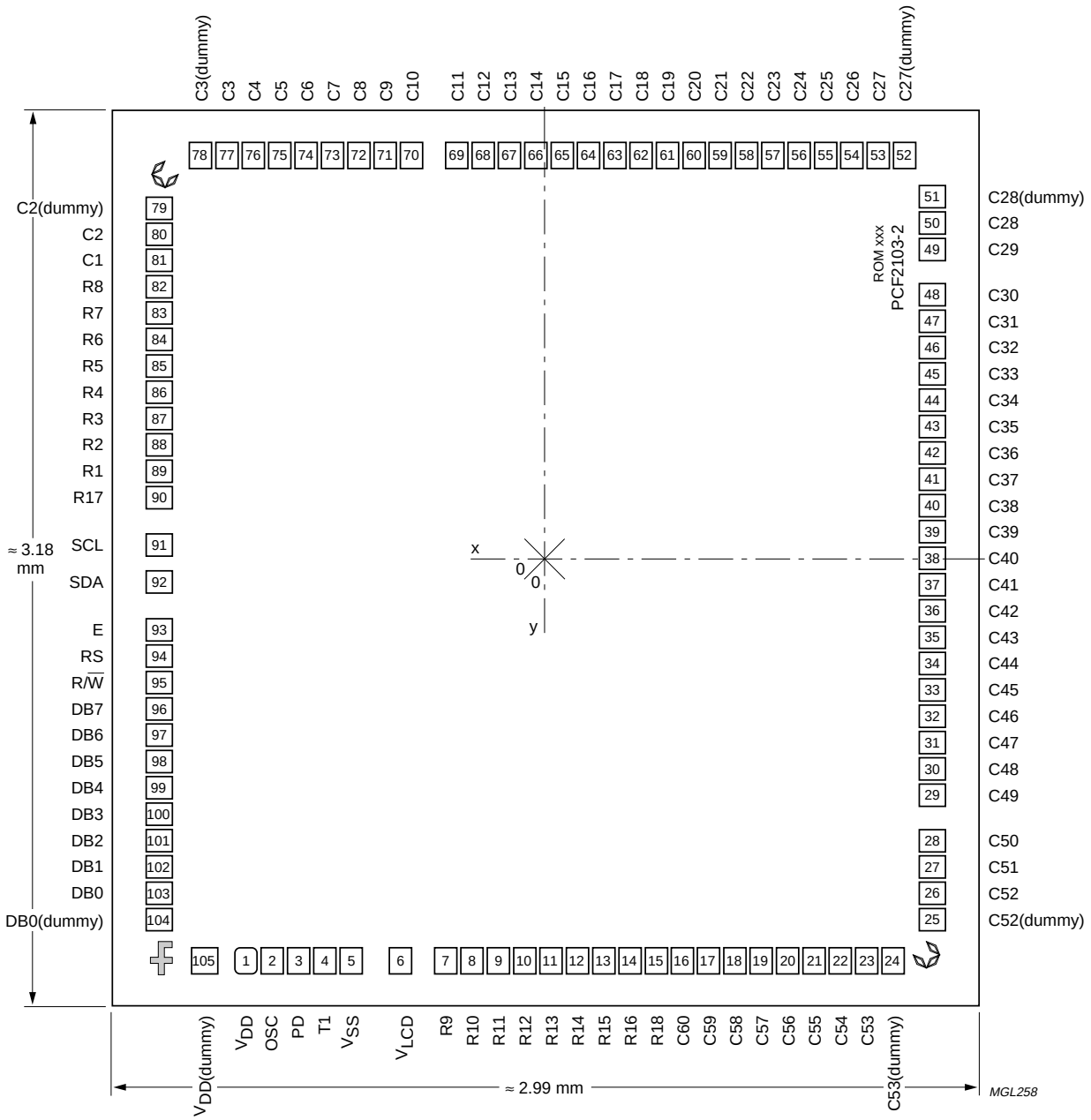


Fig.29 Bonding pad locations.

Table 18 Bonding pad locations (dimensions in μm). All x/y coordinates are referenced to centre of chip (see Fig.29)

SYMBOL	PAD	X	Y
V_{DD} (dummy)	105	−1228	−1414
V_{DD}	1	−1048	−1414
OSC	2	−958	−1414
PD	3	−868	−1414
T1	4	−778	−1414
V_{SS}	5	−688	−1414
V_{LCD}	6	−516	−1414
R9	7	−349	−1414
R10	8	−259	−1414
R11	9	−169	−1414
R12	10	−79	−1414
R13	11	11	−1414
R14	12	101	−1414
R15	13	191	−1414
R16	14	281	−1414
R18	15	371	−1414
C60	16	461	−1414
C59	17	551	−1414
C58	18	641	−1414
C57	19	731	−1414
C56	20	821	−1414
C55	21	911	−1414
C54	22	1001	−1414
C53	23	1091	−1414
C53 (dummy)	24	1181	−1414
C52 (dummy)	25	1344	−1254
C52	26	1344	−1164
C51	27	1344	−1074
C50	28	1344	−948
C49	29	1344	−812
C48	30	1344	−722
C47	31	1344	−632
C46	32	1344	−542
C45	33	1344	−452
C44	34	1344	−362
C43	35	1344	−272
C42	36	1344	−182
C41	37	1344	−92

SYMBOL	PAD	X	Y
C40	38	1344	−2
C39	39	1344	88
C38	40	1344	178
C37	41	1344	268
C36	42	1344	358
C35	43	1344	448
C34	44	1344	538
C33	45	1344	628
C32	46	1344	718
C31	47	1344	808
C30	48	1344	898
C29	49	1344	1070
C28	50	1344	1160
C28 (dummy)	51	1344	1250
C27 (dummy)	52	1262	1414
C27	53	1172	1414
C26	54	1082	1414
C25	55	992	1414
C24	56	902	1414
C23	57	805	1414
C22	58	715	1414
C21	59	625	1414
C20	60	535	1414
C19	61	445	1414
C18	62	355	1414
C17	63	265	1414
C16	64	175	1414
C15	65	85	1414
C14	66	−5	1414
C13	67	−95	1414
C12	68	−185	1414
C11	69	−275	1414
C10	70	−446	1414
C9	71	−536	1414
C8	72	−626	1414
C7	73	−716	1414
C6	74	−806	1414
C5	75	−896	1414

SYMBOL	PAD	X	Y
C4	76	−986	1414
C3	77	−1076	1414
C3 (dummy)	78	−1166	1414
C2 (dummy)	79	−1344	1303
C2	80	−1344	1213
C1	81	−1344	1123
R8	82	−1344	1033
R7	83	−1344	943
R6	84	−1344	853
R5	85	−1344	763
R4	86	−1344	673
R3	87	−1344	583
R2	88	−1344	493
R1	89	−1344	403
R17	90	−1344	313
SCL	91	−1344	131
SDA	92	−1344	−9
E	93	−1344	−195
RS	94	−1344	−289
RW	95	−1344	−382
DB7	96	−1344	−476
DB6	97	−1344	−572
DB5	98	−1344	−668
DB4	99	−1344	−765
DB3	100	−1344	−861
DB2	101	−1344	−957
DB1	102	−1344	−1054
DB0	103	−1344	−1150
DB0 (dummy)	104	−1344	−1240
Rec. Pat. C1		1335	−1405
Rec. Pat. C2		−1335	1405
Rec. Pat. F		−1340	−1397

Table 19 Bump specifications

PARAMETER	SPECIFICATION	UNIT
Bump variant	N	–
Type	galvanic; pure aurum	–
Bump width	60 ±6	µm
Bump length	90 ±6	µm
Bump height	17.5 ±5	µm
Height difference in one die	<2	µm
Convex deformation	<5	µm
Pad size; aluminium	80 × 100	µm
Passivation opening CBB	46 × 76	µm
Wafer thickness	380 ±25	µm
Minimum pitch	90	µm

17 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

18 LIFE SUPPORT APPLICATIONS

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