



CYPRESS SEMICONDUCTOR

T-46-23-14

CYM1465

512K x 8 SRAM Module

Features

- High-density 4-megabit SRAM module
- High-speed CMOS SRAMs
— Access time of 70 ns
- Low active power
— 605 mW (max.)
- JEDEC-compatible pinout
- 32-pin, 0.6-inch-wide DIP package
- TTL-compatible inputs and outputs
- Low profile
— Max. height of .27 inches
- Small PCB footprint
— 0.98 sq. in.

Functional Description

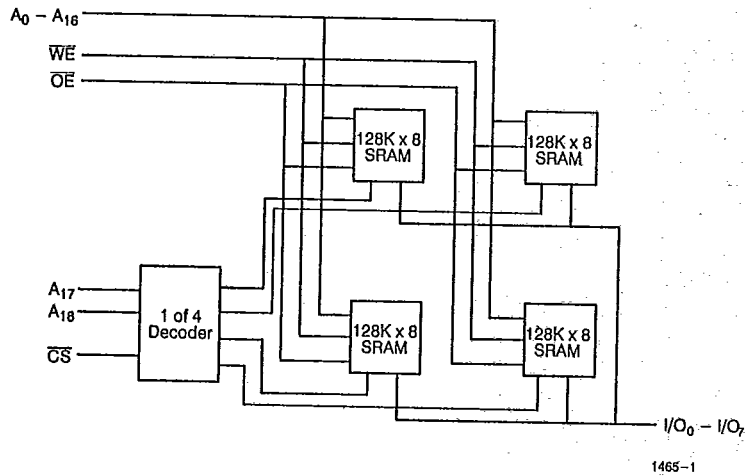
The CYM1465 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 128K x 8 RAMs mounted on a substrate with pins. A decoder is used to interpret the higher-order addresses (A_{17} and A_{18}) and to select one of the four RAMs. Two packaging options are offered: VSOP packages on FR4 substrate (PD), and SOIC packages on ceramic substrate (SD).

Writing to the module is accomplished when the chip select (\overline{CS}) and write enable (\overline{WE}) inputs are both LOW. Data on the

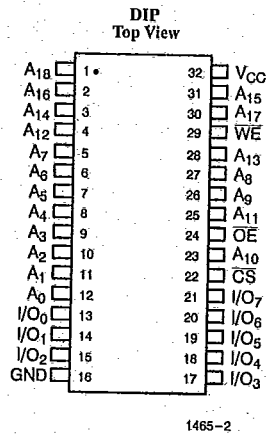
eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable (\overline{OE}) LOW while write enable remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

Logic Block Diagram



Pin Configuration



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Selection Guide

	1465-70	1465-85	1465-100	1465-120	1465-150
Maximum Access Time (ns)	70	85	100	120	150
Maximum Operating Current (mA)	110	110	110	110	110
Maximum Standby Current (mA)	12	12	12	12	12



Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature	- 55°C to +125°C
Ambient Temperature with Power Applied	-10°C to +85°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	- 40°C to + 85°C	5V ± 10%

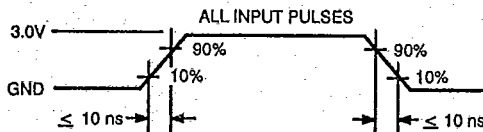
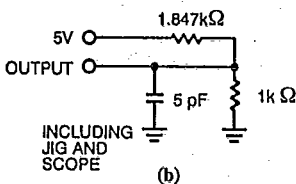
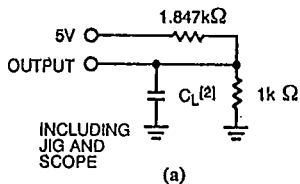
Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	1465		Units
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 1.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-20	+20	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, CS ≤ V _{IL}		110	mA
I _{SB1}	Automatic CS Power-Down Current	V _{CC} = Max., CS ≥ V _{IH} , Min. Duty Cycle = 100%		12	mA
I _{SB2}	Automatic CS Power-Down Current	V _{CC} = Max., CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	Standard Version	8	mA
			L Version	420	μA

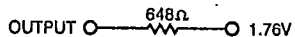
Capacitance⁽¹⁾

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	45	pF
C _{OUT}	Output Capacitance		45	pF

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT



1465-3

1465-4

Notes:

1. Tested on a sample basis.
2. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of

the specified I_{OL}/I_{OH} and 100-pF load capacitance for 85, 100, 120, and 150 ns speeds. C_L = 30 pF for 70 ns speed.



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Switching Characteristics Over the Operating Range^[2]

Parameters	Description	1465-70		1465-85		1465-100		1465-120		1465-150		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	70		85		100		120		150		ns
t _{AA}	Address to Data Valid		70		85		100		120		150	ns
t _{OHA}	Data Hold from Address Change	10		10		10		10		10		ns
t _{ACS}	CS LOW to Data Valid		70		85		100		120		150	ns
t _{DOE}	OE LOW to Data Valid		35		45		50		60		75	ns
t _{LZOE}	OE LOW to Low Z	5		5		5		5		5		ns
t _{HZOE}	OE HIGH to High Z ^[3]		25		30		35		45		55	ns
t _{LZCS}	CS LOW to Low Z	10		10		10		10		10		ns
t _{HZCS}	CS HIGH to High Z ^[3]		30		30		35		45		60	ns
WRITE CYCLE												
t _{WC}	Write Cycle Time	70		85		100		120		150		ns
t _{SCS}	CS LOW to Write End	65		75		90		100		115		ns
t _{AW}	Address Set-Up to Write End	65		75		90		100		110		ns
t _{HA}	Address Hold from Write End	0		5		5		5		5		ns
t _{SA}	Address Set-Up from Write Start	0		5		5		5		5		ns
t _{PWE}	WE Pulse Width	55		65		75		85		95		ns
t _{SD}	Data Set-Up to Write End	30		35		40		45		50		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z	5		5		5		5		5		ns
t _{HZWE}	WE LOW to High Z ^[3]		25		30		35		40		45	ns

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Data Retention Characteristics Over the Operating Range (L Version Only)

Parameters	Description	Test Conditions	Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
V _{DR}	V _{CC} for Retention Data	CS ≥ V _{CC} - 0.2V	2.0		2.0		V
I _{CCDR3}	Data Retention Current	V _{CC} = Max., CS ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V		50		150	μA
t _{CDR} ^[4]	Chip Deselect to Data Retention Time		0		0		ns
t _R ^[4]	Operation Recovery Time		5		5		ms

Notes:

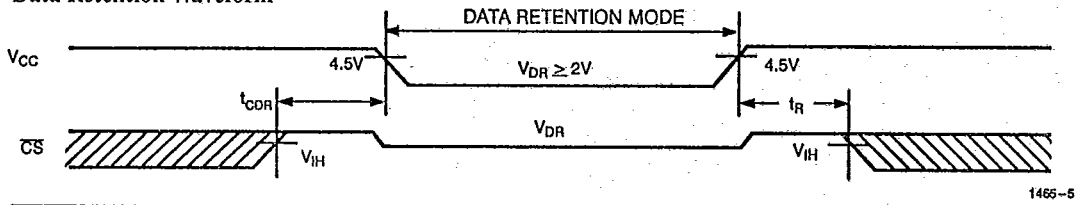
- CL = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- Guaranteed, not tested.
- WE is HIGH for the read cycle.
- Device is continuously selected, CS = VIL.
- Address valid prior to or coincident with CS transition LOW.
- The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- If CS goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.



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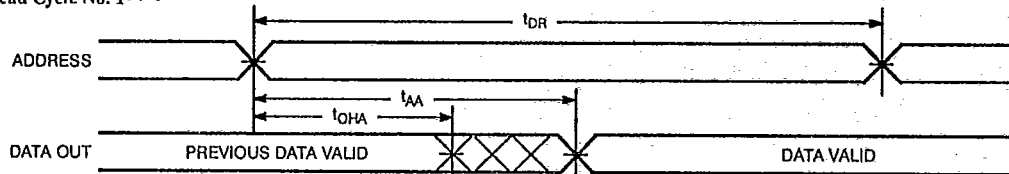
Data Retention Waveform



1465-5

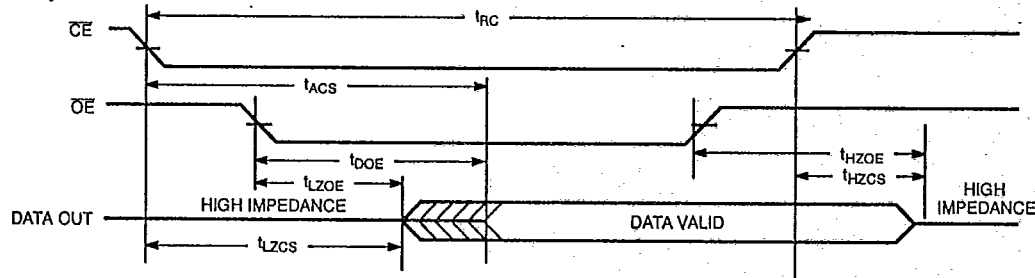
Switching Waveforms

Read Cycle No. 1^[5, 6]



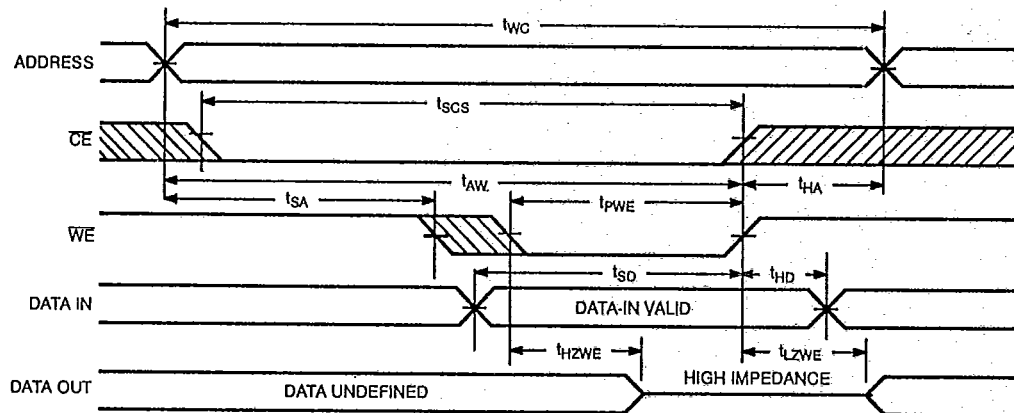
1465-6

Read Cycle No. 2^[5, 7]



1465-7

Write Cycle No. 1 (WE Controlled)^[8]



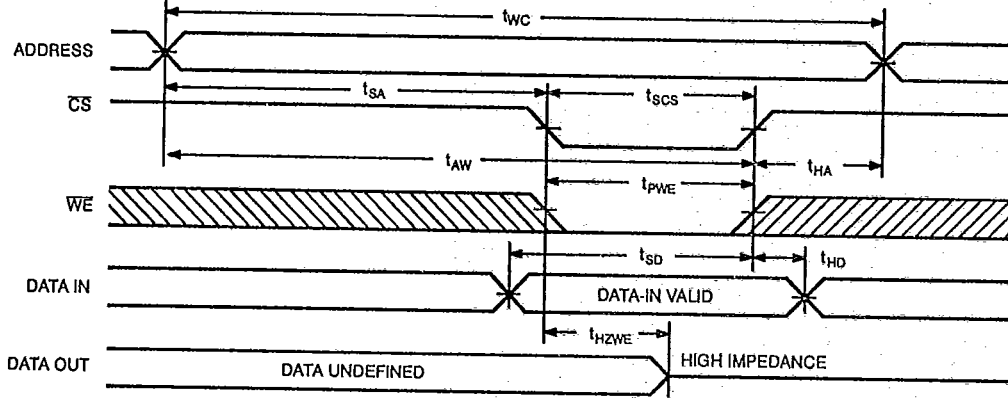
1465-8



CYM1465

Switching Waveforms (continued)^[8,9]

Write Cycle No. 2 (\overline{CS} Controlled)



1465-9

Truth Table

Inputs			Outputs	Mode
CS	WE	OE		
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
70	CYM1465PD-70C	PD03	Commercial
	CYM1465LPD-70C		
	CYM1465SSD-70C	SD01	
	CYM1465LSD-70C		
85	CYM1465PD-85C	PD03	Commercial
	CYM1465LPD-85C		
	CYM1465SSD-85C	SD01	
	CYM1465LSD-85C		
	CYM1465PD-85I	PD03	Industrial
	CYM1465LPD-85I		
	CYM1465SSD-85I	SD01	
	CYM1465LSD-85I		
100	CYM1465PD-100C	PD03	Commercial
	CYM1465LPD-100C		
	CYM1465SSD-100C	SD01	
	CYM1465LSD-100C		
	CYM1465PD-100I	PD03	Industrial
	CYM1465LPD-100I		

Speed (ns)	Ordering Code	Package Type	Operating Range
100	CYM1465SD-100I	SD01	Industrial
	CYM1465LSD-100I		
120	CYM1465PD-120C	PD03	Commercial
	CYM1465LPD-120C		
	CYM1465SSD-120C	SD01	
	CYM1465PD-120I	PD03	Industrial
	CYM1465LPD-120I		
	CYM1465LSD-120I	SD01	
150	CYM1465PD-150C	PD03	Commercial
	CYM1465LPD-150C		
	CYM1465LSD-150C	SD01	
	CYM1465PD-150I	PD03	Industrial
	CYM1465LPD-150I		
	CYM1465LSD-150I	SD01	



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