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## *Application Note*

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# INTERFACING COMPACT FLASH TO THE EP72XX



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## 1. INTRODUCTION

This application note describes a CompactFlash™ (CF) interface for the Cirrus Logic, Inc. EP72xx embedded processor family. Of the three types of interface standards defined by the CompactFlash Association, only true IDE is supported in this application note.

**NOTE:** You can find more information about the CF specification at <http://www.compactflash.org/index.htm> of the Compact Flash Association.

## 2. ABOUT COMPACTFLASH CARDS

CompactFlash™ (CF) storage cards provide the capability to easily transfer all types of digital information and software between the components of a Cirrus Logic embedded processor-based system. CF is a small form factor card standard that includes:

- CompactFlash FLASH data cards
- Magnetic disk cards
- I/O cards, including but not limited to:
  - Serial cards
  - Ethernet cards
  - Disk drive cards
  - Fax / modem cards
  - Wireless pager cards

## 3. DESCRIPTION OF CF INTERFACE

A design solution for creating a CF interface is shown in the schematic diagram in Figure 1.

All connections between the EP72xx and the CF Interface are buffered. This practice protects the EP72xx pins from “hot swapping” the card. The two 74LVX245 TTL devices buffer and control the data bus direction. The 74LVX244's provide buffering and could be replaced with other logic.

A P-Channel MOSFET device provides power to the CF device when the gate is low. This signal is provided by a EP72xx GPIO line, which should be normally high after a reset. The normal procedure is for the EP72xx to monitor one or both of the

CDn# pins. A low level signifies that the card is inserted and it is OK for the EP72xx to apply power. The CF device will go into True IDE mode when power is cycled and when ATASEL# is low.

The CF chip select lines are enabled by two GPIO pins from the EP72xx. The 74LVX245 buffers are enabled when either GPIO pin is de-asserted and qualified by nCS2. The CF IOR# and IOW# signals are qualified by the OR gates and by nMOE or nMWE. Since the CS lines from the EP72xx are de-asserted at the same time as nMOE and nMWE, this insures the CF timing is not violated. The CF specification requires that CS be de-asserted at least 20 ns after IOR# or IOW# is de-asserted.

The CF CS0# is the chip select for the Task File Registers, while CS1# is used to select the Alternate Status Register and the Device Control Register.

The CF RESET# is controlled by a GPIO signal from the EP72xx. It is not recommended that the EP72xx system reset be used, as it may be necessary for the host to toggle CF RESET under certain conditions. This is an active low signal.

The CF IOIS16# signal is asserted low by the CF device when it is expecting a 16-bit word data transfer cycle. All Task File operations occur in byte mode using D[7:0], while all data transfers are 16-bit using D[15:0]. Monitoring IOIS16# may not be necessary except for confirmation.

The CF address lines A[2:0] are used to select the one of eight registers in the Task File, while the remaining address lines should be grounded.

CF INTRQ is the active high Interrupt Request to the EP72xx.

CF DASP# is a no-connect. It is used as an input / output Disk Active / Slave Present signal in the Master/Slave handshake protocol, which is not used in this design.



• **Notes** •

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