GENERAL DESCRIPTION

The XRT86SH328 is an integrated VT/TU Mapper with 28 port T1/E1 Line Interface Units. The XRT86SH328 contains integrated DS1/E1/J1 Framers for performance monitoring.

The XRT86SH328 processes the Section, Line and Path overhead in the SONET/SDH data-stream. The processing of path overhead bytes within the STS-1s or TUG-3s include 64 bytes (of buffer) for storing the (Section Trace and Path Trace) messages. Path Overhead bytes can be accessed either by on-chip registers or a Serial Output Port.

Each of the 28 T1 or E1 Channels use an internal De-Synchronizer circuit with an internal pointer leak algorithm. This removes the jitter due to mapping and pointer adjustments from the T1 or E1 signals that are de-mapped from the incoming SONET/SDH data-stream. These De-Synchronizer circuits do not need any external clock references for its operation.

The Transmit Blocks permit flexible insertion of TOH and POH bytes via both Hardware and Software control.

The Receive Blocks receive a SONET STS-1 signals or an SDH STM-1 signal and performs the necessary Transport and Path Overhead Processing.

A PRBS Pattern Generator and Receiver is implemented within each of the 28 T1/E1 channels in order to implement and measure Bit-Error performance.

A general purpose Microprocessor Interface is included for control, configuration and monitoring.

FEATURES

- Provides mapping of up to 28 T1 streams as Asynchronous VT1.5 into an STS-1 SPE or TU-11 tributary unit into an STM-1/VC-3 or TUG-3 from STM-1/VC-4
- Supports 28 T1 streams M13 multiplexed into a serial DS3
- Supports 21 E1 streams M13 multiplexed into a serial DS3 (compliant with ITU-T G.747)
- 28 T1 Streams M13 Multiplexed into a DS3 and DS3 is asynchronously mapped into STS-1.
- 21 E1 Streams M13 Multiplexed into a DS3 (ITU-T G.747) and DS3 is asynchronously mapped into STS-1.
- Supports 21 E1 mapped as Asynchronous VT2 into an STS-1 SPE or TU-12 tributary units into STM-1/VC-3 or TUG-3 from a STM-1/VC-4.
- Supports TU cross-mapping function TU-12/VC-11/T1.
- Supports mixed mapping of VT-G/VT1.5 and VT-G/VT2.
- Supports mixed mapping of TUG-2/TU-11 and TUG-2/TU-12
- 28 VT1.5/TU-11 or 21 VT-2/TU-12 tributaries can be passed as transparent between SONET/SDH Telecom Bus on the line side and Clock and Data on the system side.
- Supports Unframed T1/E1 signals
- Supports DS1/E1 Performance Monitoring in both Egress and Ingress direction
- VC-11/VC-12 Tandem Connection Monitoring support
- Complies with the Category I Intrinsic Jitter Requirements for DS1 signals being de-mapped from SONET, per Telcordia GR-253-CORE
- Complies with the "Mapping Jitter Generation Specification" for DS1 and E1 signals being de-mapped from SDH, per ITU-T G.783
- Complies with the "Combined Jitter Generation Specification" for DS1 and E1 signals being de-mapped from SDH, per ITU-T G.783
- Line and Facility Loop-backs
- Each of the 28 T1/E1 Channels includes a PRBS Generator and Receiver.
- Each of the 28 VT-Mapper blocks are capable of generating BIP-2 and REI errors upon software command (for diagnostic purposes).
- ·The Transmit and Receive DS3 Framer blocks support both the M13(M23) and the C-bit Parity Framing formats.
- Integrated 28 T1/E1/J1 Short-Haul Line Interface Units
- IEEE 1149.1 Standard Boundary Scan
- Low Power: 1.8V Power Supply for Core Logic; 3.3V Power Supply for I/O
- General Purpose Microprocessor Interface

APPLICATIONS

- Channelized and Unchannelized DS3 applications
- T1/E1 Terminals
- SONET/SDH ADM

FIGURE 1. BLOCK DIAGRAM OF THE XRT86SH328

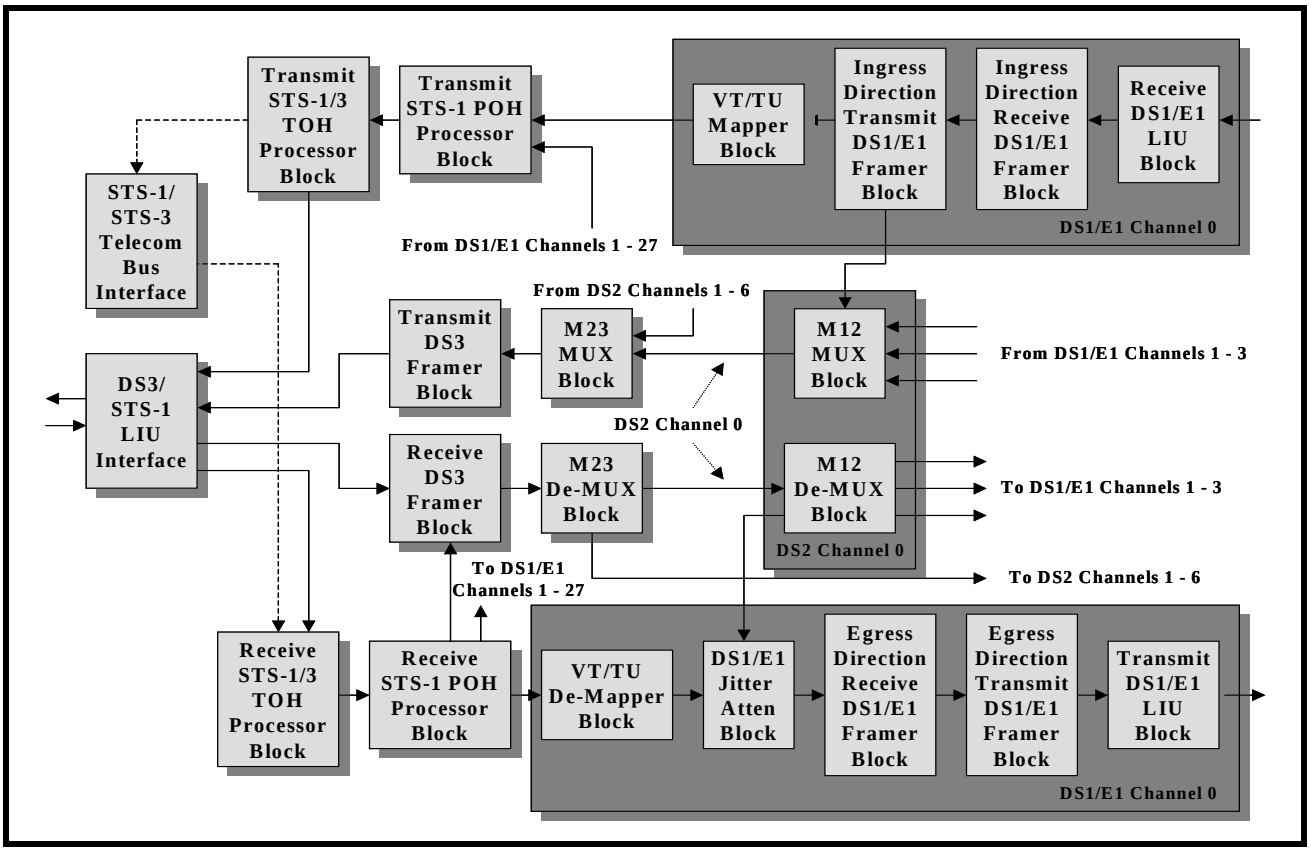
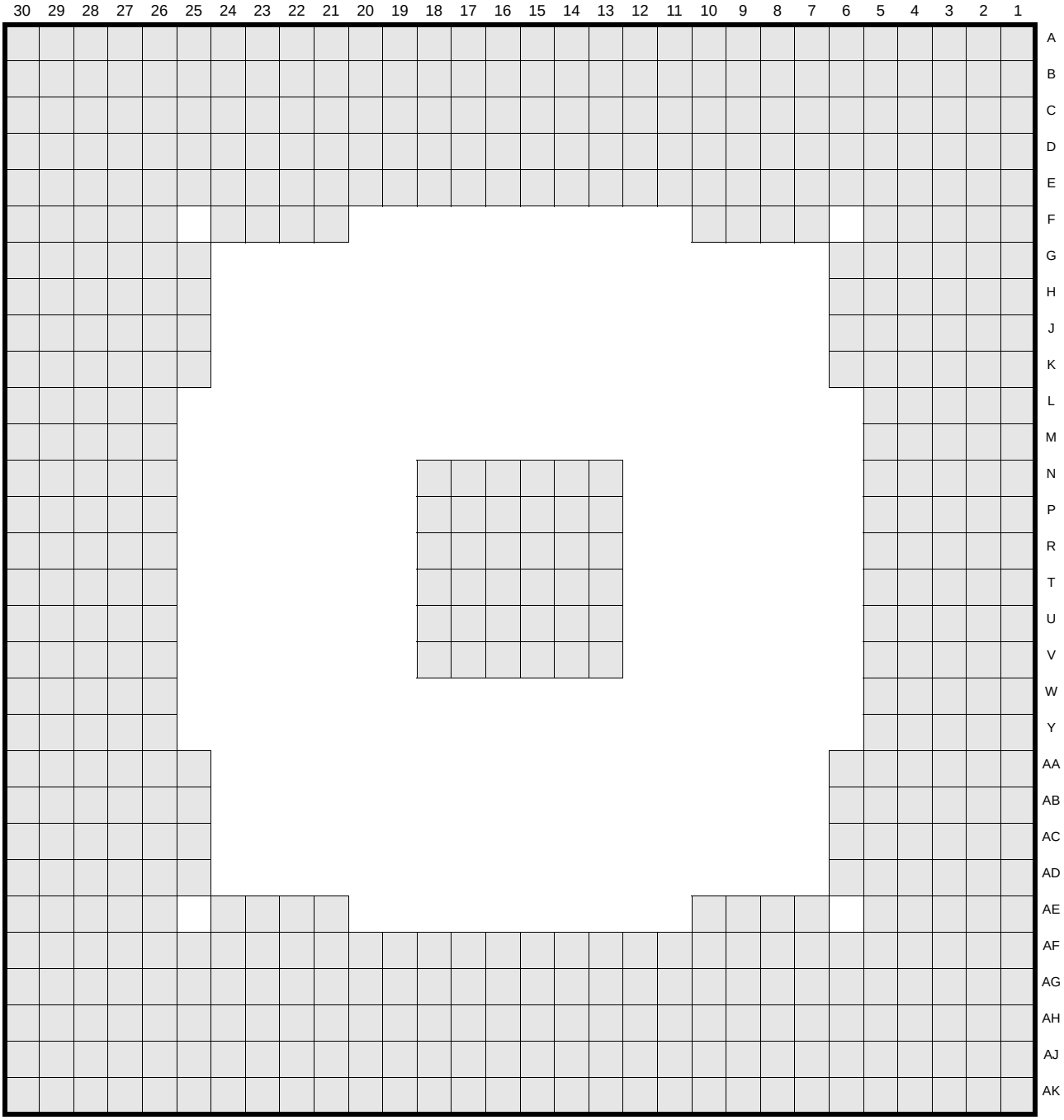


TABLE 1: ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT86SH328IB	568 Ball BGA	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT86SH328 (BOTTOM VIEW)



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1.0 REGISTER MAP & DESCRIPTION FOR THE XRT86SH328 28-CHANNEL DS1/E1 FRAMER/LIU WITH DS3 MUX AND VT-MAPPER IC - SONET APPLICATIONS

1.1 REGISTER MAP OF THE XRT86SH328

TABLE 2: OPERATION CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0000	Operation Control Register - Byte 3	R/W	0x00
0x0001	Operation Control Register - Byte 2	R/W	0x00
0x0002	Reserved		
0x0003	Operation Control Register - Byte 0	R/W	0x00
0x0004	Device ID Register	R/O	0x50
0x0005	Revision ID Register	R/O	0x01
0x0006 - 0x000A	Reserved		
0x000B	Operation Interrupt Status Register - Byte 0	RUR	0x00
0x000C - 0x000E	Reserved		
0x000F	Operation Interrupt Enable Register - Byte 0	R/W	0x00
0x0010 - 0x0011	Reserved		
0x0012	Operation Block - Interrupt Status Register - Byte 1	R/O	0x00
0x0013	Operation Block - Interrupt Status Register - Byte 0	R/O	0x00
0x0014 - 0x0015	Reserved		
0x0016	Operation Block - Interrupt Enable Register - Byte 1	R/W	0x00
0x0017	Operation Block - Interrupt Enable Register - Byte 0	R/W	0x00
0x0018 - 0x001A	Reserved		
0x001B	Operation Block - Mode Control Register - Byte 0	R/W	0x00
0x001C - 0x001E	Reserved		
0x001F	Operation Block - Loop-back Control Register - Byte 0	R/W	0x00
0x0020 - 0x0033	Reserved		
0x0034	Operation Block - Telecom Bus Control Register - Byte 3	R/W	0x00
0x0035	Operation Block - Telecom Bus Control Register - Byte 2	R/W	0x00
0x0036	Operation Block - Telecom Bus Control Register - Byte 1	R/W	0x00
0x0037	Operation Block - Telecom Bus Control Register - Byte 0	R/W	0x00
0x0038 - 0x003B	Reserved		
0x003C	Operation Block - Interface Control Register	RUR & R/W	0x00
0x003D - 0x0046	Reserved		
0x0047	Operation Block - General Purpose Input/Output Register - Byte 0	R/W	0x00

TABLE 2: OPERATION CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0048 - 0x004A	Reserved		
0x004B	Operation Block - General Purpose Input/Output Direction Register - Byte 0	RW	0x00
0x004C - 0x004E	Reserved		
0x004F	Operation Block - Operation I/O Control Register	R/W	0x00
0x0050	Operation Block - Channel Interrupt Indication Register - VT Slot[27:24]	R/O	0x00
0x0051	Operation Block - Channel Interrupt Indicator Register - VT Slot[23:16]	R/O	0x00
0x0052	Operation Block - Channel Interrupt Indicator Register - VT Slot[15:8]	R/O	0x00
0x0053	Operation Block - Channel Interrupt Indicator Register - VT Slot[7:0]	R/O	0x00
0x0054	Operation Block - Channel Interrupt Indicator Register - M13 Slot[27:24]	R/O	0x00
0x0055	Operation Block - Channel Interrupt Indicator Register - M13 Slot[23:16]	R/O	0x00
0x0056	Operation Block - Channel Interrupt Indicator Register - M13 Slot[15:8]	R/O	0x00
0x0057	Operation Block - Channel Interrupt Indicator Register - M13 Slot[7:0]	R/O	0x00
0x0058	Operation Block - Channel Interrupt Indicator Register - DS1E1 LIU Slot[27:24]	R/O	0x00
0x0059	Operation Block - Channel Interrupt Indicator Register - DS1E1 LIU Slot[23:16]	R/O	0x00
0x005A	Operation Block - Channel Interrupt Indicator Register - DS1E1 LIU Slot[15:8]	R/O	0x00
0x005B	Operation Block - Channel Interrupt Indicator Register - DS1E1 LIU Slot[7:0]	R/O	0x00
0x005C	Operation Block - Channel Interrupt Indicator Register - VT-Mapper Slot[27:24]	R/O	0x00
0x005D	Operation Block - Channel Interrupt Indicator Register - VT-Mapper Slot[23:16]	R/O	0x00
0x005E	Channel Interrupt Indication Register - VT-Mapper Slot[15:8]	R/O	0x00
0x005F	Channel Interrupt Indication Register - VT-Mapper Slot[7:0]	R/O	0x00
0x0060 - 0x00FF	Reserved		

TABLE 3: LIU COMMON CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0100	LIU Common Control Register - 0	R/W	0x00
0x0101	LIU Common Control Register - 1	R/W	0x00
0x0102	LIU Common Control Register - 2	R/W	0x00

TABLE 3: LIU COMMON CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0103	LIU Common Control Register - Global Channel Interrupt Status Register - Channels [6:0]	RUR	0x00
0x0104	LIU Common Control Register - Global Channel Interrupt Status Register - Channels [13:7]	RUR	0x00
0x0105	LIU Common Control Register - Global Channel Interrupt Status Register - Channels [20:14]	RUR	0x00
0x0106	LIU Common Control Register - Global Channel Interrupt Status Register - Channels [27:21]	RUR	0x00
0x0107 - 0x01FF	Reserved		

TABLE 4: RECEIVE STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0200 - 0x0201	Reserved		
0x0202	Receive STS-1/STS-3 Transport - Control Register - Byte 1	R/W	0x00
0x0203	Receive STS-1/STS-3 Transport - Control Register - Byte 0	R/W	0x00
0x0204 - 0x0205	Reserved	R/O	0x00
0x0206	Receive STS-1/STS-3 Transport - Status Register - Byte 1	R/O	0x00
0x0207	Receive STS-1/STS-3 Transport - Status Register - Byte 0	R/O	0x00
0x0208	Reserved		
0x0209	Receive STS-1/STS-3 Transport - Interrupt Status Register - Byte 2	RUR	0x00
0x020A	Receive STS-1/STS-3 Transport - Interrupt Status Register - Byte 1	RUR	0x00
0x020B	Receive STS-1/STS-3 Transport - Interrupt Status Register - Byte 0	RUR	0x00
0x020C	Reserved		
0x020D	Receive STS-1/STS-3 Transport - Interrupt Enable Register - Byte 2	R/W	0x00
0x020E	Receive STS-1/STS-3 Transport - Interrupt Enable Register - Byte 1	R/W	0x00
0x020F	Receive STS-1/STS-3 Transport - Interrupt Enable Register - Byte 0	R/W	0x00
0x0210	Receive STS-1/STS-3 Transport - Receive B1 Byte Error Count Register - Byte 3	RUR	0x00
0x0211	Receive STS-1/STS-3 Transport - Receive B1 Byte Error Count Register - Byte 2	RUR	0x00
0x0212	Receive STS-1/STS-3 Transport - Receive B1 Byte Error Count Register - Byte 1	RUR	0x00
0x0213	Receive STS-1/STS-3 Transport - Receive B1 Byte Error Count Register - Byte 0	RUR	0x00

TABLE 4: RECEIVE STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0214	Receive STS-1/STS-3 Transport - Receive B2 Byte Error Count Register - Byte 3	RUR	0x00
0x0215	Receive STS-1/STS-3 Transport - Receive B2 Byte Error Count Register - Byte 2	RUR	0x00
0x0216	Receive STS-1/STS-3 Transport - Receive B2 Byte Error Count Register - Byte 1	RUR	0x00
0x0217	Receive STS-1/STS-3 Transport - Receive B2 Byte Error Count Register - Byte 0	RUR	0x00
0x0218	Receive STS-1/STS-3 Transport - Receive REI-L Event Count Register - Byte 3	RUR	0x00
0x0219	Receive STS-1/STS-3 Transport - Receive REI-L Event Count Register - Byte 2	RUR	0x00
0x021A	Receive STS-1/STS-3 Transport - Receive REI-L Event Count Register - Byte 1	RUR	0x00
0x021B	Receive STS-1/STS-3 Transport - Receive REI-L Event Count Register - Byte 0	RUR	0x00
0x021C - 0x021E	Reserved		
0x021F	Receive STS-1/STS-3 Transport - Receive K1 Byte Value Register	R/O	0x00
0x0220 - 0x0222	Reserved		
0x0223	Receive STS-1/STS-3 Transport - Receive K2 Byte Value Register	R/O	0x00
0x0224 -0x0226	Reserved		
0x0227	Receive STS-1/STS-3 Transport - Receive S1 Byte Value Register	R/O	0x00
0x0228 - 0x022A	Reserved		
0x022B	Receive STS-1/STS-3 Transport - Receive In-Sync Threshold Register	R/W	0x00
0x022C - 0x022D	Reserved		
0x022E	Receive STS-1/STS-3 Transport - Receive LOS Threshold Register - MSB	R/W	0x00
0x022F	Receive STS-1/STS-3 Transport - Receive LOS Threshold Register - LSB	R/W	0x00
0x0230	Reserved		
0x0231	Receive STS-1/STS-3 Transport - Receive SF Defect Declare Monitor Interval Register - Byte 2	R/W	0x00
0x0232	Receive STS-1/STS-3 Transport - Receive SF Defect Declare Monitor Interval Register - Byte 1	R/W	0x00
0x0233	Receive STS-1/STS-3 Transport - Receive SF Defect Declare Monitor Interval Register - Byte 0	R/W	0x00
0x0234 - 0x0235	Reserved		
0x0236	Receive STS-1/STS-3 Transport - Receive SF Defect Set Threshold Register - Byte 1	R/W	0x00

TABLE 4: RECEIVE STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0237	Receive STS-1/STS-3 Transport - Receive SF Defect Set Threshold Register - Byte 0	R/W	0x00
0x0238 - 0x0239	Reserved		
0x023A	Receive STS-1/STS-3 Transport - Receive SF Defect Clear Threshold Register - Byte 1	R/W	0x00
0x023B	Receive STS-1/STS-3 Transport - Receive SF Defect Clear Threshold Register - Byte 0	R/W	0x00
0x023C	Reserved		
0x023D	Receive STS-1/STS-3 Transport - Receive SD Defect Declare Monitor Interval - Byte 2	R/W	0x00
0x023E	Receive STS-1/STS-3 Transport - Receive SD Defect Declare Monitor Interval - Byte 1	R/W	0x00
0x023F	Receive STS-1/STS-3 Transport - Receive SD Defect Declare Monitor Interval - Byte 0	R/W	0x00
0x0240 - 0x0241	Reserved		
0x0242	Receive STS-1/STS-3 Transport - Receive SD Defect Set Threshold Register - Byte 1	R/W	0x00
0x0243	Receive STS-1/STS-3 Transport - Receive SD Defect Set Threshold Register - Byte 0	R/W	0x00
0x0244 - 0x0245	Reserved		
0x0246	Receive STS-1/STS-3 Transport - Receive SD Defect Clear Threshold Register - Byte 1	R/W	0x00
0x0247	Receive STS-1/STS-3 Transport - Receive SD Defect Clear Threshold Register - Byte 0	R/W	0x00
0x0248 - 0x024A	Reserved		
0x024B	Receive STS-1/STS-3 Transport - SEF Force Register	R/W	0x00
0x024C -0x024E	Reserved		
0x024F	Receive STS-1/STS-3 Transport - Receive J0 Byte/Section Trace Message Control Register	R/W	0x00
0x0250 - 0x0251	Reserved		
0x0252	Receive STS-1/STS-3 Transport - Receive SD Defect Error Burst Tolerance Register - Byte 1	R/W	0x00
0x0253	Receive STS-1/STS-3 Transport - Receive SD Defect Error Burst Tolerance Register - Byte 0	R/W	0x00
0x0254 - 0x0255	Reserved		
0x0256	Receive STS-1/STS-3 Transport - Receive SF Defect Error Burst Tolerance Register - Byte 1	R/W	0x00

TABLE 4: RECEIVE STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0257	Receive STS-1/STS-3 Transport - Receive SF Defect Error Burst Tolerance Register - Byte 0	R/W	0x00
0x0258	Reserved		
0x0259	Receive STS-1/STS-3 Transport - Receive SD Defect Clear Monitor Interval - Byte 2	R/W	0x00
0x025A	Receive STS-1/STS-3 Transport - Receive SD Defect Clear Monitor Interval - Byte 1	R/W	0x00
0x025B	Receive STS-1/STS-3 Transport - Receive SD Defect Clear Monitor Interval - Byte 0	R/W	0x00
0x025C	Reserved		
0x025D	Receive STS-1/STS-3 Transport - Receive SF Defect Clear Monitor Interval - Byte 2	R/W	0x00
0x025E	Receive STS-1/STS-3 Transport - Receive SF Defect Clear Monitor Interval - Byte 1	R/W	0x00
0x025F	Receive STS-1/STS-3 Transport - Receive SF Defect Clear Monitor Interval - Byte 0	R/W	0x00
0x0260 - 0x0262	Reserved		
0x0263	Receive STS-1/STS-3 Transport - Auto AIS Control Register	R/W	0x00
0x0264 - 0x0266	Reserved		
0x0267	Receive STS-1/STS-3 Transport - Serial Port Control Register	R/W	0x00
0x0268 - 0x026A	Reserved		
0x026B	Receive STS-1/STS-3 Transport - Auto AIS (in Downstream T1/E1) Register	R/W	0x00
0x026C - 0x026D	Reserved		
0x026E	Receive STS-1/STS-3 Transport - A1, A2 Byte Error Count Register - Byte 1	RUR	0x00
0x026F	Receive STS-1/STS-3 Transport - A1, A2 Byte Error Count Register - Byte 0	RUR	0x00
0x0270 - 0x0279	Reserved		
0x027A	Receive STS-1/STS-3 Transport - Receive TOH Capture Buffer - Indirect Address Register - Byte 1	W	0x00
0x027B	Receive STS-1/STS-3 Transport - Receive TOH Capture Buffer - Indirect Address Register - Byte 0	W	0x00
0x027C	Receive STS-1/STS-3 Transport - Receive TOH Capture Buffer - Indirect Data Register - Byte 3	W	0x00
0x027D	Receive STS-1/STS-3 Transport - Receive TOH Capture Buffer - Indirect Data Register - Byte 2	W	0x00

TABLE 4: RECEIVE STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x027E	Receive STS-1/STS-3 Transport - Receive TOH Capture Buffer - Indirect Data Register - Byte 1	W	0x00
0x027F	Receive STS-1/STS-3 Transport - Receive TOH Capture Buffer - Indirect Data Register - Byte 0	W	0x00
0x0280	Reserved		

TABLE 5: RECEIVE STS-1/STS-3 POH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0281	Receive STS-1/STS-3 Path - Receive Control Register - Byte 2	R/W	0x00
0x0282	Reserved		
0x0283	Receive STS-1/STS-3 Path - Receive Control Register - Byte 0	R/W	0x00
0x0284 - 0x0285	Reserved		
0x0286	Receive STS-1/STS-3 Path - Receive Status Register - Byte 1	R/O	0x00
0x0287	Receive STS-1/STS-3 Path - Receive Status Register - Byte 0	R/O	0x00
0x0288	Reserved		
0x0289	Receive STS-1/STS-3 Path - Receive Interrupt Status Register - Byte 2	RUR	0x00
0x028A	Receive STS-1/STS-3 Path - Receive Interrupt Status Register - Byte 1	RUR	0x00
0x028B	Receive STS-1/STS-3 Path - Receive Interrupt Status Register - Byte 0	RUR	0x00
0x028C	Reserved		
0x028D	Receive STS-1/STS-3 Path - Receive Interrupt Enable Register - Byte 2	R/W	0x00
0x028E	Receive STS-1/STS-3 Path - Receive Interrupt Enable Register - Byte 1	R/W	0x00
0x028F	Receive STS-1/STS-3 Path - Receive Interrupt Enable Register - Byte 0	R/W	0x00
0x0290 - 0x0292	Reserved		
0x0293	Receive STS-1/STS-3 Path - Receive RDI-P Register	R/O & R/W	0x00
0x0294 - 0x295	Reserved		
0x0296	Receive STS-1/STS-3 Path - Receive C2 (Path Label) Byte Accepted Register	R/O	0xFF
0x0297	Receive STS-1/STS-3 Path - Receive C2 (Path Label) Byte Expected Register	R/W	0xFF
0x0298	Receive STS-1/STS-3 Path - Receive B3 Byte Error Count Register - Byte 3	RUR	0x00
0x0299	Receive STS-1/STS-3 Path - Receive B3 Byte Error Count Register - Byte 2	RUR	0x00
0x029A	Receive STS-1/STS-3 Path - Receive B3 Byte Error Count Register - Byte 1	RUR	0x00

TABLE 5: RECEIVE STS-1/STS-3 POH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x029B	Receive STS-1/STS-3 Path - Receive B3 Byte Error Count Register - Byte 0	RUR	0x00
0x029C	Receive STS-1/STS-3 Path - Receive REI-P Event Count Register - Byte 3	RUR	0x00
0x029D	Receive STS-1/STS-3 Path - Receive REI-P Event Count Register - Byte 2	RUR	0x00
0x029E	Receive STS-1/STS-3 Path - Receive REI-P Event Count Register - Byte 1	RUR	0x00
0x029F	Receive STS-1/STS-3 Path - Receive REI-P Event Count Register - Byte 0	RUR	0x00
0x02A0 - 0x02A2	Reserved		
0x02A3	Receive STS-1/STS-3 Path - Receive J1 Byte/Path Trace Message Control Register	R/W	0x00
0x02A4 - 0x02A5	Reserved		
0x02A6	Receive STS-1/STS-3 - Receive Pointer Value Register - Byte 1	R/O	0x00
0x02A7	Receive STS-1/STS-3 - Receive Pointer Value Register - Byte 0	R/O	0x00
0x02A8 - 0x02AA	Reserved		
0x02AB	Receive STS-1/STS-3 - Receive LOP-C Status Register	R/O	0x00
0x02AC - 0x02B2	Reserved		
0x02B3	Receive STS-1/STS-3 - Receive AIS-C Status Register	R/O	0x00
0x02B4 - 0x02B8	Reserved		
0x02B9	Receive STS-1/STS-3 - Receive Auto AIS - C2 Byte Value Register	R/W	0x00
0x02BA	Receive STS-1/STS-3 - Receive Auto AIS - C2 Byte Control Register	R/W	0x00
0x02BB	Receive STS-1/STS-3 - Receive Auto AIS Control Register	R/W	0x00
0x02BC - 0x02BE	Reserved		
0x02BF	Receive STS-1/STS-3 - Receive Serial Port Control Register	R/W	0x00
0x02C0 -0x02C2	Reserved		
0x02C3	Receive STS-1/STS-3 - Auto AIS (in Downstream T1/E1) Register	R/W	0x00
0x02C4	Receive STS-1/STS-3 - Receive Negative Pointer Adjustment Count Register - Byte 1	RUR	0x00
0x02C5	Receive STS-1/STS-3 - Receive Negative Pointer Adjustment Count Register - Byte 0	RUR	0x00
0x02C6	Receive STS-1/STS-3 - Receive Positive Pointer Adjustment Count Register - Byte 1	RUR	0x00
0x02C7	Receive STS-1/STS-3 - Receive Positive Pointer Adjustment Count Register - Byte 0	RUR	0x00
0x02C8 - 0x02D2	Reserved		
0x02D3	Receive STS-1/STS-3 - Receive J1 Byte Value Register	R/O	0x00
0x02D4 - 0x02D6	Reserved		

TABLE 5: RECEIVE STS-1/STS-3 POH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x02D7	Receive STS-1/STS-3 - Receive B3 Byte Value Register	R/O	0x00
0x02D8 - 0x02DA	Reserved		
0x02DB	Receive STS-1/STS-3 - Receive C2 Byte Value Register	R/O	0x00
0x02DC - 0x02DE	Reserved		
0x02DF	Receive STS-1/STS-3 - Receive G1 Byte Value Register	R/O	0x00
0x02E0 - 0x02E2	Reserved		
0x02E3	Receive STS-1/STS-3 - Receive F2 Byte Value Register	R/O	0x00
0x02E4 - 0x02E6	Reserved		
0x02E7	Receive STS-1/STS-3 - Receive H4 Byte Value Register	R/O	0x00
0x02E8 - 0x02EA	Reserved		
0x02EB	Receive STS-1/STS-3 - Receive Z3 Byte Value Register	R/O	0x00
0x02EC - 0x02EE	Reserved		
0x02EF	Receive STS-1/STS-3 - Receive Z4 Byte Value Register	R/O	0x00
0x02F0 - 0x02F2	Reserved		
0x02F3	Receive STS-1/STS-3 - Receive Z5 Byte Value Register	R/O	0x00
0x02F4 - 0x02FF	Reserved		

TABLE 6: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SECTION TRACE MESSAGE BUFFER

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0300 - 0x033F	Receive STS-1/STS-3 Transport - Receive Section Trace Message Buffer	R/O	0x00
0x0340 - 0x03FF	Reserved	R/O	0x00

TABLE 7: RECEIVE STS-1/STS-3 PATH - RECEIVE PATH TRACE MESSAGE BUFFER

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0400 - 0x043F	Receive STS-1/STS-3 Path - Receive Path Trace Message Buffer	R/O	0x00
0x0440 - 0x0580	Reserved	R/O	0x00

TABLE 8: RECEIVE TU-3 POH PROCESSOR BLOCK REGISTERS (SDH/TUG-3 APPLICATIONS ONLY)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0581	Receive TU-3 Path - Receive Control Register - Byte 2	R/W	0x00
0x0582	Reserved		

TABLE 8: RECEIVE TU-3 POH PROCESSOR BLOCK REGISTERS (SDH/TUG-3 APPLICATIONS ONLY)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0583	Receive TU-3 Path - Receive Control Register - Byte 0	R/W	0x00
0x0584 - 0x0585	Reserved		
0x0586	Receive TU-3 Path - Receive Status Register - Byte 1	R/O	0x00
0x0587	Receive TU-3 Path - Receive Status Register - Byte 0	R/O	0x00
0x0588	Reserved		
0x0589	Receive TU-3 Path - Receive Interrupt Status Register - Byte 2	RUR	0x00
0x058A	Receive TU-3 Path - Receive Interrupt Status Register - Byte 1	RUR	0x00
0x058B	Receive TU-3 Path - Receive Interrupt Status Register - Byte 0	RUR	0x00
0x058C	Reserved		
0x058D	Receive TU-3 Path - Receive Interrupt Enable Register - Byte 2	R/W	0x00
0x058E	Receive TU-3 Path - Receive Interrupt Enable Register - Byte 1	R/W	0x00
0x058F	Receive TU-3 Path - Receive Interrupt Enable Register - Byte 0	R/W	0x00
0x0590 - 0x0592	Reserved		
0x0593	Receive TU-3 Path - Receive RDI-P Register	R/O & R/W	0x00
0x0594 - 0x0595	Reserved		
0x0596	Receive TU-3 Path - Receive C2 (Path Label) Byte Accepted Register	R/O	0xFF
0x0597	Receive TU-3 Path - Receive C2 (Path Label) Byte Expected Register	R/W	0xFF
0x0598	Receive TU-3 Path - Receive B3 Byte Error Count Register - Byte 3	RUR	0x00
0x0599	Receive TU-3 Path - Receive B3 Byte Error Count Register - Byte 2	RUR	0x00
0x059A	Receive TU-3 Path - Receive B3 Byte Error Count Register - Byte 1	RUR	0x00
0x059B	Receive TU-3 Path - Receive B3 Byte Error Count Register - Byte 0	RUR	0x00
0x059C	Receive TU-3 Path - Receive REI-P Event Count Register - Byte 3	RUR	0x00
0x059D	Receive TU-3 Path - Receive REI-P Event Count Register - Byte 2	RUR	0x00
0x059E	Receive TU-3 Path - Receive REI-P Event Count Register - Byte 1	RUR	0x00
0x059F	Receive TU-3 Path - Receive REI-P Event Count Register - Byte 0	RUR	0x00
0x05A0 - 0x05A2	Reserved		
0x05A3	Receive TU-3 Path - Receive J1 Byte/Path Trace Message Control Register	R/W	0x00
0x05A4 - 0x05A5	Reserved		
0x05A6	Receive TU-3 Path - Receive Pointer Value Register - Byte 1	R/O	0x00
0x05A7	Receive TU-3 Path - Receive Pointer Value Register - Byte 0		
0x05A8 - 0x05AA	Reserved		
0x05AB	Receive TU-3 Path - Receive LOP-C Status Register	R/O	0x00

TABLE 8: RECEIVE TU-3 POH PROCESSOR BLOCK REGISTERS (SDH/TUG-3 APPLICATIONS ONLY)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x05AC - 0x05B2	Reserved		
0x05B3	Receive TU-3 Path - Receive AIS-C Status Register	R/O	0x00
0x05B4 - 0x05B8	Reserved		
0x05B9	Receive TU-3 Path - Receive Auto AIS - C2 Byte Value Register	R/W	0x00
0x05BA	Receive TU-3 Path - Receive Auto AIS - C2 Byte Control Register	R/W	0x00
0x05BB	Receive TU-3 Path - Receive Auto AIS Control Register	R/W	0x00
0x05BC - 0x05BE	Reserved		
0x05BF	Receive TU-3 Path - Receive Serial Port Control Register	R/W	0x00
0x05C0 - 0x05C2	Reserved		
0x05C3	Receive TU-3 Path - Auto AIS (in Downstream T1/E1) Register	R/W	0x00
0x05C4	Receive TU-3 Path - Receive Negative Pointer Adjustment Count Register - Byte 1	RUR	0x00
0x05C5	Receive TU-3 Path - Receive Negative Pointer Adjustment Count Register - Byte 0	RUR	0x00
0x05C6	Receive TU-3 Path - Receive Positive Pointer Adjustment Count Register - Byte 1	RUR	0x00
0x05C7	Receive TU-3 Path - Receive Positive Pointer Adjustment Count Register - Byte 0	RUR	0x00
0x05C8 - 0x05D2	Reserved		
0x05D3	Receive TU-3 Path - Receive J1 Byte Value Register	R/O	0x00
0x05D4 - 0x05D6	Reserved		
0x05D7	Receive TU-3 Path - Receive B3 Byte Value Register	R/O	0x00
0x05D8 - 0x05DA	Reserved		
0x05DB	Receive TU-3 Path - Receive C2 Byte Value Register	R/O	0x00
0x05DC - 0x05DE	Reserved		
0x05DF	Receive TU-3 Path - Receive G1 Byte Value Register	R/O	0x00
0x05E0 - 0x05E2	Reserved		
0x05E3	Receive TU-3 Path - Receive F2 Byte Value Register	R/O	0x00
0x05E4 - 0x05E6	Reserved		
0x05E7	Receive TU-3 Path - Receive H4 Byte Value Register	R/O	0x00
0x05E8 - 0x05EA	Reserved		
0x05EB	Receive TU-3 Path - Receive Z3 Byte Value Register	R/O	0x00
0x05EC - 0x05EE	Reserved		
0x05EF	Receive TU-3 Path - Receive Z4 Byte Value Register	R/O	0x00

TABLE 8: RECEIVE TU-3 POH PROCESSOR BLOCK REGISTERS (SDH/TUG-3 APPLICATIONS ONLY)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x05F0 - 0x05F2	Reserved		
0x05F3	Receive TU-3 Path - Receive Z5 Byte Value Register	R/O	0x00
0x05F4 - 0x05FF	Reserved		

TABLE 9: RECEIVE TU-3 POH PROCESSOR BLOCK - RECEIVE PATH TRACE MESSAGE BUFFER (SDH/TUG-3 APPLICATIONS ONLY)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0600 - 0x063F	Receive TU-3 POH Processor Block - Receive Path Trace Message Buffer	R/O	0x00
0x0640 - 0x06FF	Reserved		

TABLE 10: TRANSMIT STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0700	Transmit STS-1/STS-3 Transport - Transmit Control Register - Byte 3	R/W	0x00
0x0701	Transmit STS-1/STS-3 Transport - Transmit Control Register - Byte 2	R/W	0x00
0x0702	Transmit STS-1/STS-3 Transport - Transmit Control Register - Byte 1	R/W	0x00
0x0703	Transmit STS-1/STS-3 Transport - Transmit Control Register - Byte 0	R/W	0x00
0x0704 - 0x0715	Reserved		
0x0716	Transmit STS-1/STS-3 Transport - Transmit A1 Byte Error Mask Register - Byte 1	R/W	0x00
0x0717	Transmit STS-1/STS-3 Transport - Transmit A1 Byte Error Mask Register - Byte 0	R/W	0x00
0x0718 - 0x071D	Reserved		
0x071E	Transmit STS-1/STS-3 Transport - Transmit A2 Byte Error Mask Register - Byte 1	R/W	0x00
0x071F	Transmit STS-1/STS-3 Transport - Transmit A2 Byte Error Mask Register - Byte 0	R/W	0x00
0x0720 - 0x0722	Reserved		
0x0723	Transmit STS-1/STS-3 Transport - Transmit B1 Byte Error Mask Register	R/W	0x00
0x0724 - 0x0725			
0x0726	Transmit STS-1/STS-3 Transport - Transmit B2 Byte Error Mask Register - Byte 1	R/W	0x00
0x0727	Transmit STS-1/STS-3 Transport - Transmit B2 Byte Error Mask Register - Byte 0	R/W	0x00
0x0728 - 0x072A	Reserved		

TABLE 10: TRANSMIT STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x072B	Transmit STS-1/STS-3 Transport - Transmit B2 Byte Bit Error Mask Register	R/W	0x00
0x072C - 0x072D	Reserved		
0x072E	Transmit STS-1/STS-3 Transport - Transmit K1 Byte Value Register	R/W	0x00
0x072F	Transmit STS-1/STS-3 Transport - Transmit K2 Byte Value Register	R/W	0x00
0x0730 - 0x0732	Reserved		
0x0733	Transmit STS-1/STS-3 Transport - Transmit RDI-L Control Register	R/W	0x00
0x0734	Transmit STS-1/STS-3 Transport - Transmit M0/M1 Byte Control Register	R/W	0x00
0x0735	Reserved		
0x0736	Transmit STS-1/STS-3 Transport - Transmit M0/M1 Byte Pointer Register	R/W	0x00
0x0737	Transmit STS-1/STS-3 Transport - Transmit M0/M1 Byte Value Register	R/W	0x00
0x0738	Transmit STS-1/STS-3 Transport - Transmit S1 Byte Control Register	R/W	0x00
0x0739	Reserved		
0x073A	Transmit STS-1STS-3 Transport - Transmit S1 Pointer Register	R/W	0x00
0x073B	Transmit STS-1/STS-3 Transport - Transmit S1 Byte Value Register	R/W	0x00
0x073C	Transmit STS-1/STS-3 Transport - Transmit F1 Byte Control Register	R/W	0x00
0x073D	Reserved		
0x073E	Transmit STS-1/STS-3 Transport - Transmit F1 Byte Pointer Register	R/W	0x00
0x073F	Transmit STS-1/STS-3 Transport - Transmit F1 Byte Value Register	R/W	0x00
0x0740	Transmit STS-1/STS-3 Transport - Transmit E1 Byte Control Register	R/W	0x00
0x0741	Reserved		
0x0742	Transmit STS-1/STS-3 Transport - Transmit E1 Pointer Register	R/W	0x00
0x0743	Transmit STS-1/STS-3 Transport - Transmit E1 Byte Value Register	R/W	0x00
0x0744	Transmit STS-1/STS-3 Transport - Transmit E2 Byte Control Register	R/W	0x00
0x0745	Reserved		
0x0746	Transmit STS-1/STS-3 Transport - Transmit E2 Byte Pointer Register	R/W	0x00
0x0747	Transmit STS-1/STS-3 Transport - Transmit E2 Byte Value Register	R/W	0x00
0x0748 - 0x074A	Reserved		
0x074B	Transmit STS-1/STS-3 Transport - Transmit J0 Byte Value Register	R/W	0x00
0x074C -0x074E	Reserved		
0x074F	Transmit STS-1/STS-3 Transport - Transmit J0 Byte/Section Trace Message Control Register	R/W	0x00
0x0750 - 0x0780	Reserved		

TABLE 11: TRANSMIT STS-1/STS-3 POH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0781	Transmit STS-1/STS-3 Path - Transmit Path Control Register - Byte 2	R/W	0x00
0x0782	Transmit STS-1/STS-3 Path - Transmit Path Control Register - Byte 1	R/W	0x00
0x0783	Transmit STS-1/STS-3 Path - Transmit Path Control Register - Byte 0	R/W	0x00
0x0784 - 0x0792	Reserved		
0x0793	Transmit STS-1/STS-3 Path - Transmit J1 Byte Value Register	R/W	0x00
0x0794 - 0x0796	Reserved		
0x0796	Transmit STS-1/STS-3 Path - Transmit B3 Byte Pass Thru Register	R/W	0x00
0x0797	Transmit STS-1/STS-3 Path - Transmit B3 Byte Mask Register	R/W	0x00
0x0798 - 0x079A	Reserved		
0x079B	Transmit STS-1/STS-3 Path - Transmit C2 Byte Value Register	R/W	0x00
0x079C - 0x079E	Reserved		
0x079F	Transmit STS-1/STS-3 Path - Transmit G1 Byte Value Register	R/W	0x00
0x07A0 - 0x07A2	Reserved		
0x07A3	Transmit STS-1/STS-3 Path - Transmit F2 Byte Value Register	R/W	0x00
0x07A4 - 0x07A6	Reserved		
0x07A7	Transmit STS-1/STS-3 Path - Transmit H4 Byte Value Register	R/W	0x00
0x07A8 - 0x07AA	Reserved		
0x07AB	Transmit STS-1/STS-3 Path - Transmit Z3 Byte Value Register	R/W	0x00
0x07AC - 0x07AE	Reserved		
0x07AF	Transmit STS-1/STS-3 Path - Transmit Z4 Byte Value Register	R/W	0x00
0x07B0 - 0x07B2	Reserved		
0x07B3	Transmit STS-1/STS-3 Path - Transmit Z5 Byte Value Register	R/W	0x00
0x07B4 - 0x07B6	Reserved		
0x07B7	Transmit STS-1/STS-3 Path - Transmit Control Register - Byte 0	R/W	0x00
0x07B8 - 0x07BA	Reserved		
0x07BB	Transmit STS-1/STS-3 Path - Transmit J1 Byte/Path Trace Message Control Register	R/W	0x00
0x07BC - 0x07BE	Reserved		
0x07BF	Transmit STS-1/STS-3 Path - Transmit Arbitrary Pointer (H1 Byte) Value Register	R/W	0x00
0x07C0 - 0x07C2	Reserved		
0x07C3	Transmit STS-1/STS-3 Path - Transmit Arbitrary Pointer (H2 Byte) Value Register	R/W	0x00

TABLE 11: TRANSMIT STS-1/STS-3 POH PROCESSOR BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x07C4 - 0x07C5	Reserved		
0x07C6	Transmit STS-1/STS-3 Path - Current Pointer Value Register - High-Byte	R/O	0x02
0x07C7	Transmit STS-1/STS-3 Path - Current Pointer Value Register - Low-Byte	R/O	0x0A
0x07C8	Reserved		
0x07C9	Transmit STS-1/STS-3 Path - Transmit RDI-P Control Register - Byte 2	R/W	0x00
0x07CA	Transmit STS-1/STS-3 Path - Transmit RDI-P Control Register - Byte 1	R/W	0x00
0x07CB	Transmit STS-1/STS-3 Path - Transmit RDI-P Control Register - Byte 0	R/W	0x00
0x07CA - 0x07CE	Reserved		
0x07CF	Transmit STS-1/STS-3 Path - Transmit Path Serial Port Control Register	R/W	0x00
0x07D0	Transmit STS-1/STS-3 - Transmit Negative Pointer Adjustment Count Register - Byte 1	RUR	0x00
0x07D1	Transmit STS-1/STS-3 - Transmit Negative Pointer Adjustment Count Register - Byte 0	RUR	0x00
0x07D2	Transmit STS-1/STS-3 - Transmit Positive Pointer Adjustment Count Register - Byte 1	RUR	0x00
0x07D3	Transmit STS-1/STS-3 - Transmit Positive Pointer Adjustment Count Register - Byte 0	RUR	0x00
0x07D4 - 0x07FF	Reserved		

TABLE 12: TRANSMIT STS-1/STS-3 TOH PROCESSOR BLOCK - TRANSMIT PATH TRACE MESSAGE BUFFER

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0800 - 0x083F	Transmit STS-1/STS-3 Transport - Transmit Section Trace Message Buffer	R/W	0x00
0x0840 - 0x08FF	Reserved		

TABLE 13: TRANSMIT STS-1/STS-3 POH PROCESSOR BLOCK - TRANSMIT PATH TRACE MESSAGE BUFFER

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0900 - 0x093F	Transmit STS-1/STS-3 Path - Transmit Path Trace Message Buffer	R/W	0x00
0x0940 - 0x0A80	Reserved	R/O	0x00

TABLE 14: TRANSMIT TU-3 POH PROCESSOR BLOCK REGISTERS (SDH/TUG-3 APPLICATIONS ONLY)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0A81	Transmit TU-3 Path - Transmit Path Control Register - Byte 2	R/W	0x00
0x0A82	Transmit TU-3 Path - Transmit Path Control Register - Byte 1	R/W	0x00
0x0A83	Transmit TU-3 Path - Transmit Path Control Register - Byte 0	R/W	0x00
0x0A84 -0x0A92	Reserved		
0x0A93	Transmit TU-3 Path - Transmit J1 Byte Value Register	R/W	0x00
0x0A94 - 0x0A95	Reserved		
0x0A96	Transmit TU-3 Path - Transmit B3 Byte Pass Thru Register	R/W	0x00
0x0A97	Transmit TU-3 Path - Transmit B3 Byte Mask Register	R/W	0x00
0x0A98 - 0x0A9A	Reserved		
0x0A9B	Transmit TU-3 Path - Transmit C2 Byte Value Register	R/W	0x00
0x0A9C - 0x0A9E	Reserved		
0x0A9F	Transmit TU-3 Path - Transmit G1 Byte Value Register	R/W	0x00
0x0AA0 - 0x0AA2	Reserved		
0x0AA3	Transmit TU-3 Path - Transmit F2 Byte Value Register	R/W	0x00
0x0AA4 - 0x0AA6	Reserved		
0x0AA7	Transmit TU-3 Path - Transmit H4 Byte Value Register	R/W	0x00
0x0AA8 - 0x0AAA	Reserved		
0x0AAB	Transmit TU-3 Path - Transmit Z3 Byte Value Register	R/W	0x00
0x0AAC - 0x0AAE	Reserved		
0x0AAF	Transmit TU-3 Path - Transmit Z4 Byte Value Register	R/W	0x00
0x0AB0 - 0x0AB2	Reserved		
0x0AB3	Transmit TU-3 Path - Transmit Z5 Byte Value Register	R/W	0x00
0x0AB4 - 0x0AB6	Reserved		
0x0AB7	Transmit TU-3 Path - Transmit Control Register - Byte 0	R/W	0x00
0x0AB8 - 0x0ABA	Reserved		
0x0ABB	Transmit TU-3 Path - Transmit J1 Byte/Path Trace Message Control Register	R/W	0x00
0x0ABC - 0x0ABE	Reserved		
0x0ABF	Transmit TU-3 Path - Transmit Arbitrary Pointer (H1 Byte) Value Register	R/W	0x00
0x0AC0 -0x0AC2	Reserved		
0x0AC3	Transmit TU-3 Path - Transmit Arbitrary Pointer (H2 Byte) Value Register	R/W	0x00
0x0AC4 - 0x0AC5	Reserved		

TABLE 14: TRANSMIT TU-3 POH PROCESSOR BLOCK REGISTERS (SDH/TUG-3 APPLICATIONS ONLY)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0AC6	Transmit TU-3 Path - Current Pointer Value Register - High Byte	R/O	0x02
0x0AC7	Transmit TU-3 Path - Current Pointer Value Register - Low Byte	R/O	0x0A
0x0AC8	Reserved		
0x0AC9	Transmit TU-3 Path - Transmit RDI-P Control Register - Byte 2	R/W	0x00
0x0ACA	Transmit TU-3 Path - Transmit RDI-P Control Register - Byte 1	R/W	0x00
0x0ACB	Transmit TU-3 Path - Transmit RDI-P Control Register - Byte 0	R/W	0x00
0x0ACC - 0x0ACE	Reserved		
0x0ACF	Transmit TU-3 Path - Transmit Path Serial Port Control Register	R/W	0x00
0x0AD0	Transmit TU-3 Path - Transmit Negative Pointer Adjustment Count Register - Byte 1	RUR	0x00
0x0AD1	Transmit TU-3 Path - Transmit Negative Pointer Adjustment Count Register - Byte 0	RUR	0x00
0x0AD2	Transmit TU-3 Path - Transmit Positive Pointer Adjustment Count Register - Byte 1	RUR	0x00
0x0AD3	Transmit TU-3 Path - Transmit Positive Pointer Adjustment Count Register - Byte 0	RUR	0x00
0x0AD4 - 0xAFF	Reserved	R/O	0x00

TABLE 15: TRANSMIT TU-3 POH PROCESSOR BLOCK - TRANSMIT PATH TRACE MESSAGE BUFFER

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0B00 - 0x0B3F	Transmit TU-3 POH Processor Block - Transmit Path Trace Message Buffer	R/W	0x00
0x0B40 - 0x0BFF	Reserved	R/O	0x00

TABLE 16: VT MAPPER CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0C00 - 0x0C02	Reserved		
0x0C03	Global Control - VT Mapper Control Block - VT Mapper Block Level Control Register	R/W	0x00
0x0C04 - 0x0C05	Reserved		
0x0C06	Global Control - VT Mapper Control Block - Composite Status Register	R/O	0x00
0x0C07	Global Control - VT Mapper Control Block - Composite Status Register	R/O	0x00
0x0C08 - 0x0C09	Reserved		

TABLE 16: VT MAPPER CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0C0A	Global Control - VT Mapper Control Block - Composite Interrupt Enable Register	R/W	0x00
0x0C0B	Global Control - VT Mapper Control Block - Composite Interrupt Enable Register	R/W	0x00
0x0C0C - 0x0C0D	Reserved		
0x0C0E	Global Control - VT Mapper Control Block - Test Pattern Control Register - Byte 1	R/W & R/O	0x00
0x0C0F	Global Control - VT Mapper Control Block - Test Pattern Control Register - Byte 0	R/O	0x00
0x0C10 - 0x0C11	Reserved		
0x0C12	Global Control - VT Mapper Control Block - Test Pattern Drop Register - Byte 1	R/W	0x00
0x0C13	Global Control - VT Mapper Control Block - Test Pattern Drop Register - Byte 0	R/W	0x00
0x0C14 - 0x0C15	Reserved		
0x0C16	Global Control - VT Mapper Control Block - Test Pattern Detector Error Register - Upper Byte	RUR	0x00
0x0C17	Global Control - VT Mapper Control Block - Test Pattern Detector Error Register - Lower Byte	RUR	0x00
0x0C18 - 0x0C19	Reserved		
0x0C1A	Global Control - VT Mapper Control Block - Transmit Tributary Size Select Register - Byte 1	R/W	0x00
0x0C1B	Global Control - VT Mapper Control Block - Transmit Tributary Size Select Register - Byte 0	R/W	0x00
0x0C1C - 0x0C1D	Reserved		
0x0C1E	Global Control - VT Mapper Control Block - Receive Tributary Size Select Register - Byte 1	R/W	0x00
0x0C1F	Global Control - VT Mapper Control Block - Receive Tributary Size Select Register - Byte 0	R/W	0x00
0x0C20 - 0x0D01	Reserved		

TABLE 17: DS3 MAPPER CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0D02	DS3 Mapper Block - Control Register - Byte 1	R/W	0x03
0x0D03	DS3 Mapper Block - Control Register - Byte 0	R/W	0x00
0x0D04 - 0x0D05	Reserved		
0x0D06	DS3 Mapper Block - Receive Mapper Status Register - Byte 1	R/O	0x03

TABLE 17: DS3 MAPPER CONTROL REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0D07	DS3 Mapper Block - Receive Mapper Status Register - Byte 0	R/O	0x00
0x0D08 - 0x0D0A	Reserved		
0x0D0B	DS3 Mapper Block - Receive Mapper Interrupt Status Register - Byte 0	RUR	0x00
0x0D0C - 0x0D0D	Reserved		
0x0D0E	DS3 Mapper Block - Receive Mapper Interrupt Enable Register - Byte 0	R/W	0x00
0x0D0F - 0x0D20	Reserved		
0x0D21	Pointer Justification Status Register - Byte 2	R/O	0x00
0x0D22	Pointer Justification Status Register - Byte 1	R/O	0x00
0x0D23	Pointer Justification Status Register - Byte 0	R/O	0x00
0x0D24 - 0x0D25	Reserved		
0x0D26	Pointer Justification Jitter Control Register - Byte 1	R/W	0xC0
0x0D27	Pointer Justification Jitter Control Register - Byte 0	R/W	0x80
0x0D28 - 0x0DFF	Reserved		

TABLE 18: DS3 FRAMER AND M13 MUX BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0E00	DS3 Framer and M13 MUX Block - Operating Mode Register	R/W	0x23
0x0E01	DS3 Framer and M13 MUX Block - I/O Control Register	R/W	0xC0
0x0E02 - 0x0E03	Reserved		
0x0E04	DS3 Framer and M13 MUX Block - Block Interrupt Enable Register	R/W	0x00
0x0E05	DS3 Framer and M13 MUX Block - Block Interrupt Status Register	R/O	0x00
0x0E06	Reserved	R/W	0x00
0x0E07	DS3 Framer and M13 MUX Block - M23 Configuration Register	R/W	0x00
0x0E08	DS3 Framer and M13 MUX Block - M23 Transmit DS2 AIS Register	R/W	0x00
0x0E09	DS3 Framer and M13 MUX Block - M23 DS2 Loop-back Request Register	R/W	0x00
0x0E0A	DS3 Framer and M13 MUX Block - M23 Loop-back Activation Register	R/W	0x00
0x0E0B	DS3 Framer and M13 MUX Block - M23 MUX Force DS2 AIS Command Register	R/W	0x00
0x0E0C	DS3 Framer and M13 MUX Block - DS3 Test Register # 1	R/W	0x00
0x0E0D	Reserved	R/O	0x00
0x0E0E	DS3 Framer and M13 MUX Block - DS3 Test Register # 2	R/W	0x00

TABLE 18: DS3 FRAMER AND M13 MUX BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0E10	DS3 Framer and M13 MUX Block - Receive DS3 Configuration & Status Register	R/W	0x10
0x0E11	DS3 Framer and M13 MUX Block - Receive DS3 Status Register	R/W	0x00
0x0E12	DS3 Framer and M13 MUX Block - Receive DS3 Interrupt Enable Register	R/W	0x00
0x0E13	DS3 Framer and M13 MUX Block - Receive DS3 Interrupt Status Register	RUR	0x00
0x0E14	DS3 Framer and M13 MUX Block - Receive DS3 Sync Detect Register	R/W	0x00
0x0E15	Reserved	R/O	0x00
0x0E16	S3 Framer and M13 MUX Block - Receive DS3 FEAC Register	R/O	0x7E
0x0E17	DS3 Framer and M13 MUX Block - Receive DS3 FEAC Interrupt Enable/Status Register	R/W	0x00
0x0E18	DS3 Framer and M13 MUX Block - Receive DS3 LAPD Control Register	R/W	0x00
0x0E19	DS3 Framer and M13 MUX Block - Receive DS3 LAPD Status Register	R/W	0x00
0x0E1A	M12 DS2 # 1 Configuration Register	R/W	0x00
0x0E1B	DS3 Framer and M13 MUX Block - M12 Configuration Register - DS2 Channel # 2	R/W	0x00
0x0E1C	DS3 Framer and M13 MUX Block - M12 Configuration Register - DS2 Channel # 3	R/W	0x00
0x0E1D	DS3 Framer and M13 MUX Block - M12 Configuration Register - DS2 Channel # 4	R/W	0x00
0x0E1E	DS3 Framer and M13 MUX Block - M12 Configuration Register - DS2 Channel # 5	R/W	0x00
0x0E1F	DS3 Framer and M13 MUX Block - M12 Configuration Register - DS2 Channel # 6	R/W	0x00
0x0E20	DS3 Framer and M13 MUX Block - M12 Configuration Register - DS2 Channel # 7	R/W	0x00
0x0E21	DS3 Framer and M13 MUX Block - M12 De-MUX Force DS1/E1 AIS Register - DS2 # Channel 1	R/W	0x00
0x0E22	DS3 Framer and M13 MUX Block - M12 DS2 # 2 AIS Register	R/W	0x00
0x0E23	DS3 Framer and M13 MUX Block - M12 DS2 # 3 AIS Register	R/W	0x00
0x0E24	DS3 Framer and M13 MUX Block - M12 DS2 # 4 AIS Register	R/W	0x00
0x0E25	DS3 Framer and M13 MUX Block - M12 DS2 # 5 AIS Register	R/W	0x00
0x0E26	DS3 Framer and M13 MUX Block - M12 DS2 # 6 AIS Register	R/W	0x00
0x0E27	DS3 Framer and M13 MUX Block - M12 DS2 # 7 AIS Register	R/W	0x00
0x0E28	M12 DS2 # 1 Loop-back Request Register	R/W	0x00
0x0E29	M12 DS2 # 2 Loop- back Request Register	R/W	0x00
0x0E2A	M12 DS2 # 3 Loop-back Request Register	R/W	0x00

TABLE 18: DS3 FRAMER AND M13 MUX BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0E2B	M12 DS2 # 4 Loop-back Request Register	R/W	0x00
0x0E2C	M12 DS2 # 5 Loop-back Request Register	R/W	0x00
0x0E2D	M12 DS2 # 6 Loop-back Request Register	R/W	0x00
0x0E2E	M12 DS2 # 7 Loop-back Request Register	R/W	0x00
0x0E2F	Reserved	R/O	0x00
0x0E30	Transmit DS3 Configuration Register	R/W	0x00
0x0E31	Transmit DS3 FEAC Configuration & Status Register	R/W	0x00
0x0E32	Transmit DS3 FEAC Register	R/W	0x7E
0x0E33	Transmit DS3 LAPD Configuration Register	R/W	0x00
0x0E34	Transmit DS3 LAPD Status/Interrupt Register	R/W	0x00
0x0E35	Transmit DS3 M-Bit Mask Register	R/W	0x00
0x0E36	Transmit DS3 F-Bit Mask Register # 1	R/W	0x00
0x0E37	Transmit DS3 F-Bit Mask Register # 2	R/W	0x00
0x0E38	Transmit DS3 F-Bit Mask Register # 3	R/W	0x00
0x0E39	Transmit DS3 F-Bit Mask Register # 4	R/W	0x00
0x0E3A	M12 DS2 # 1 Framer Configuration Register	R/W	0x00
0x0E3B	M12 DS2 # 2 Framer Configuration Register	R/W	0x00
0x0E3C	M12 DS2 # 3 Framer Configuration Register	R/W	0x00
0x0E3D	M12 DS2 # 4 Framer Configuration Register	R/W	0x00
0x0E3E	M12 DS2 # 5 Framer Configuration Register	R/W	0x00
0x0E3F	M12 DS2 # 6 Framer Configuration Register	R/W	0x00
0x0E40	M12 DS2 # 7 Framer Configuration Register	R/W	0x00
0x0E41 - 0x0E4B	Reserved	R/O	0x00
0x0E4C	Transmit DS3 Pattern Register	R/W	0x00
0x0E4D	Auto T1/E1 AIS upon DS3 Defect Condition Register	R/W	0x00
0x0E4E	PMON EXZ Event Count Register - MSB	RUR	0x00
0x0E4F	PMON EXZ Event Count Register - LSB	RUR	0x00
0x0E50	PMON LCV Event Count Register - MSB	RUR	0x00
0x0E51	PMON LCV Event Count Register - LSB	RUR	0x00
0x0E52	PMON Framing Bit Error Count Register - MSB	RUR	0x00
0x0E53	PMON Framing Bit Error Count Register - LSB	RUR	0x00
0x0E54	PMON P-Bit Error Count Register - MSB	RUR	0x00

TABLE 18: DS3 FRAMER AND M13 MUX BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0E55	PMON P-Bit Error Count Register - LSB	RUR	0x00
0x0E56	PMON FEBE Count Register - MSB	RUR	0x00
0x0E57	PMON FEBE Count Register - LSB	RUR	0x00
0x0E58	PMON CP-Bit Error Count Register - MSB	RUR	0x00
0x0E59	PMON CP-Bit Error Count Register - LSB	RUR	0x00
0x0E5A	PMON DS2 # 1 Framing Bit Error Count Register	RUR	0x00
0x0E5B	PMON DS2 # 2 Framing Bit Error Count Register	RUR	0x00
0x0E5C	PMON DS2 # 3 Framing Bit Error Count Register	RUR	0x00
0x0E5D	PMON DS2 # 4 Framing Bit Error Count Register	RUR	0x00
0x0E5E	PMON DS2 # 5 Framing Bit Error Count Register	RUR	0x00
0x0E5F	PMON DS2 # 6 Framing Bit Error Count Register	RUR	0x00
0x0E60	PMON DS2 # 7 Framing Bit Error Count Register	RUR	0x00
0x0E61	PMON G.747 # 1 Parity Bit Error Count Register	RUR	0x00
0x0E62	PMON G.747 # 2 Parity Bit Error Count Register	RUR	0x00
0x0E63	PMON G.747 # 3 Parity Bit Error Count Register	RUR	0x00
0x0E64	PMON G.747 # 4 Parity Bit Error Count Register	RUR	0x00
0x0E65	PMON G.747 # 5 Parity Bit Error Count Register	RUR	0x00
0x0E66	PMON G.747 # 6 Parity Bit Error Count Register	RUR	0x00
0x0E67	PMON G.747 # 7 Parity Bit Error Count Register	RUR	0x00
0x0E68	PRBS Bit Error Count Register - MSB	RUR	0x00
0x0E69	PRBS Bit Error Count Register - LSB	RUR	0x00
0x0E6A - 0x0E6C	Reserved		
0x0E6D	One Second Error Status Register	R/O	0x00
0x0E6E	LCV One Second Accumulator Register - MSB	R/O	0x00
0x0E6F	LCV One Second Accumulator Register - LSB	R/O	0x00
0x0E70	Frame Parity Error One Second Accumulator Register - MSB	R/O	0x00
0x0E71	Frame Parity Error One Second Accumulator Register - LSB	R/O	0x00
0x0E72	CP Bit Error One Second Accumulator Register - MSB	R/O	0x00
0x0E73	CP Bit Error One Second Accumulator Register - LSB	R/O	0x00
0x0E74 - 0x0E7F	Reserved	R/O	0x00
0x0E80	Line Interface Drive Register	R/W	0x00
0x0E81	Line Interface Scan Register	R/W	0x00

TABLE 18: DS3 FRAMER AND M13 MUX BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0E82	Reserved	R/O	0x00
0x0E83	Transmit DS3 LAPD Byte Count Register	R/W	0x00
0x0E84	Receive DS3 LAPD Byte Count Register	R/O	0x00
0x0E85 - 0x0E8F	Reserved		
0x0E90	M23 Receive DS2 Loop-back Request Interrupt Enable Register	R/W	0x00
0x0E91	M23 Receive DS2 Loop-back Request Interrupt Status Register	RUR	0x00
0x0E92	M23 Receive DS2 Loop-back Request Status Register	R/O	0x00
0x0E93	M12 DS2 # 1 Loop-back Interrupt/Interrupt Enable Register	R/W, RUR	0x00
0x0E94	M12 DS2 # 1 Loop-back Status Register	R/O	0x00
0x0E95	M12 DS2 # 2 Loop-back Interrupt/Interrupt Enable Register	R/W, RUR	0x00
0x0E96	M12 DS2 # 2 Loop-back Status Register	R/O	0x00
0x0E97	M12 DS2 # 3 Loop-back Interrupt/Interrupt Enable Register	R/W, RUR	0x00
0x0E98	M12 DS2 # 3 Loop-back Status Register	R/O	0x00
0x0E99	M12 DS2 # 4 Loop-back Interrupt/Interrupt Enable Register	R/W, RUR	0x00
0x0E9A	M12 DS2 # 4 Loop-back Status Register	R/O	0x00
0x0E9B	M12 DS2 # 5 Loop-back Interrupt/Interrupt Enable Register	R/W, RUR	0x00
0x0E9C	M12 DS2 # 5 Loop-back Status Register	R/O	0x00
0x0E9D	M12 DS2 # 6 Loop-back Interrupt/Interrupt Enable Register	R/W, RUR	0x00
0x0E9E	M12 DS2 # 6 Loop-back Status Register	R/O	0x00
0x0E9F	M12 DS2 # 7 Loop-back Interrupt/Interrupt Enable Register	R/W, RUR	0x00
0x0EA0	M12 DS2 # 7 Loop-back Status Register	R/O	0x00
0x0EA1	DS2 # 1 Framer Interrupt Enable Register	R/W	0x00
0x0EA2	DS2 # 1 Framer Interrupt Status Register	RUR	0x00
0x0EA3	DS2 # 1 Framer Status Register	R/O	0x00
0x0EA4	DS2 # 2 Framer Interrupt Enable Register	R/W	0x00
0x0EA5	DS2 # 2 Framer Interrupt Status Register	RUR	0x00
0x0EA6	DS2 # 2 Framer Status Register	R/O	0x00
0x0EA7	DS2 # 3 Framer Interrupt Enable Register	R/W	0x00
0x0EA8	DS2 # 3 Framer Interrupt Status Register	RUR	0x00
0x0EA9	DS2 # 3 Framer Status Register	R/O	0x00
0x0EAA	DS2 # 4 Framer Interrupt Enable Register	R/W	0x00
0x0EAB	DS2 # 4 Framer Interrupt Status Register	RUR	0x00

TABLE 18: DS3 FRAMER AND M13 MUX BLOCK REGISTERS

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0x0EAC	DS2 # 4 Framer Status Register	R/O	0x00
0x0EAD	DS2 # 5 Framer Interrupt Enable Register	R/W	0x00
0x0EAE	DS2 # 5 Framer Interrupt Status Register	RUR	0x00
0x0EAF	DS2 # 5 Framer Status Register	R/O	0x00
0x0EB0	DS2 # 6 Framer Interrupt Enable Register	R/W	0x00
0x0EB1	DS2 # 6 Framer Interrupt Status Register	RUR	0x00
0x0EB2	DS2 # 6 Framer Status Register	R/O	0x00
0x0EB3	DS2 # 7 Framer Interrupt Enable Register	R/W	0x00
0x0EB4	DS2 # 7 Framer Interrupt Status Register	RUR	0x00
0x0EB5	DS2 # 7 Framer Status Register	R/O	0x00
0x0EB6 -0x0EB7	Reserved		
0x0EB8	M13 DeMUX External Alarm Enable Register	R/W	0x00
0x0EB9 - 0x0EBF	Reserved		
0x0EC0	LAPD Memory Indirect Address Register	R/W	0x00
0x0EC1	LAPD Memory Indirect Data Register	R/W	0x00
0x0EC2 - 0x0FFF	Reserved	R/O	0x00

TABLE 19: T1/E1 LIU CHANNEL CONTROL REGISTERS (WHERE N RANGES FROM 0X01 TO 0X1D)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN000	T1/E1 LIU Register - Byte 0 - Channel 0	R/W	0x00
0xN001	LIU Channel Control Register - Byte 1 - Channel 0	R/W	0x00
0xN002	LIU Channel Control Register - Byte 2 - Channel 0	R/W	0x00
0xN003	LIU Channel Control Register - Byte 3 - Channel 0	R/W	0x00
0xN004	LIU Channel Control Register - Byte 4 - Channel 0	R/W	0x00
0xN005	LIU Channel Control Register - Byte 5 - Channel 0	R/W	0x00
0xN006	LIU Channel Control Register - Byte 6 - Channel 0	R/W	0x00
0xN007	LIU Channel Control Register - Byte 7 - Channel 0	R/W	0x00
0xN008	LIU Channel Control Register - Byte 8 - Channel 0	R/W	0x00
0xN009	LIU Channel Control Register - Byte 9 - Channel 0	R/W	0x00
0xN00A	LIU Channel Control Register - Byte 10 - Channel 0	R/W	0x00
0xN00B	LIU Channel Control Register - Byte 11 - Channel 0	R/W	0x00
0xN00C	LIU Channel Control Register - Byte 12 - Channel 0	R/W	0x00

TABLE 19: T1/E1 LIU CHANNEL CONTROL REGISTERS (WHERE N RANGES FROM 0X01 TO 0X1D)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN00D	LIU Channel Control Register - Byte 13 - Channel 0	R/W	0x00
0xN00E	LIU Channel Control Register - Byte 14 - Channel 0	R/W	0x00
0xN00F	LIU Channel Control Register - Byte 15 - Channel 0	R/W	0x00
0xN010	LIU Channel Control Register - Byte 16 - Channel 0	R/W	0x00
0xN011	LIU Channel Control Register - Byte 17 - Channel 0	R/W	0x00
0xN012 - 0xN0FF	Reserved		

TABLE 20: T1/E1 FRAMER BLOCK CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN100	Clock Select Register	R/W	0x00
0xN101	Line Interface Control Register	R/W	0x00
0xN102 - 0N106	Reserved	RUR	
0xN107	Framing Select Register	R/W	0x00
0xN108	Alarm Generation Register	R/W	0x00
0xN109	Synchronization Mux Register	R/W	0x00
0xN10A	Transmit Signaling and Data Link Select Register	R/W	0x00
0xN10B	Framing Control Register	R/W	0x00
0xN10C	Receive Signaling Data Link Select Register	R/W	0x00
0xN10D	Receive Signaling Change Register - 0Framing Control Register (E1 Applications Only)	R/W	0x00
0xN10E	Receive Signaling Change Register - 1	R/W	0x00
0xN10F	Receive Signaling Change Register - 2	R/W	0x00
0xN110	Reserved		
0xN111	Receive National Bits Register (E1 Applications Only)	R/W	0x00
0xN112	Receive Extra Bits (E1 Applications)Receive In-Sync Register (T1 Applications)	R/W	0x00
0xN113	Data Link control Register	R/W	0x00
0xN114	Transmit Data Link Byte Count Register	R/W	0x00
0xN115	Receive Data Link Byte Count Register	R/W	0x00
0xN116 - 0xN117	Reserved		
0x1118	DMA 0 Write Configuration Register	R/W	0x00
0x1119	DMA 1 Read Configuration Register	R/W	0x00

TABLE 20: T1/E1 FRAMER BLOCK CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN11A	Reserved		
0xN11B	LAPD Channel Select Register (T1 Applications)	R/W	0x00
0xN11C	Customer Installation Alarm Generation Register	R/W	0x00
0xN11D	Transmit Performance Report Control Register	R/W	0x00
0xN11E - 0xN11	Reserved		
0xN120	Transmit Interface Control Register	R/W	0x00
0xN121	DS1/E1 Test Register - 2	R/W	0x00
0xN122	Receive Interface Control Register	R/W	0x00
0xN123	DS1/E1 Test Register - 1	R/W	0x00
0xN124	Loop Back Code Control Register - Code 0	R/W	0x00
0xN125	Transmit Loop Back Code Control Register	R/W	0x00
0xN126	Receive Loop Back Code Activation Control Register - Code 0	R/W	0x00
0xN127	Receive Loop Back Code Deactivation Control Register - Code 0	R/W	0x00
0xN129	Receive DS1 External Alarm Enable Register	R/W	0x00
0xN12A	Loop-Back Code Control Register - Code 1	R/W	0x00
0xN12B	Receive Loop Back Code Activation Control Register - Code 1	R/W	0x00
0xN12C	Receive Loop Back Code Deactivation Control Register - Code 1	R/W	0x00
0xN12D	Loop-back Code Control Register - Code 2	R/W	0x00
0xN12E	Receive Loop-back Activation Code Control Register - Code 2	R/W	0x00
0xN12F	Receive Loop-back Deactivation Code Control Register - Code 2	R/W	0x00
0xN130	Transmit Sa Select Register (E1 Applications Only)	R/W	0x00
0xN131	Transmit Sa Auto Control Register - Byte 1 (E1 Applications Only)	R/W	0x00
0xN132	Transmit Sa Auto Control Register - Byte 2 (E1 Applications Only)	R/W	0x00
0xN133	Transmit Sa4 Register (E1 Applications Only)	R/W	0x00
0xN134	Transmit Sa5 Register (E1 Applications Only)	R/W	0x00
0xN135	Transmit Sa6 Register (E1 Applications Only)	R/W	0x00
0xN136	Transmit Sa7 Register (E1 Applications Only)	R/W	0x00
0xN137	Transmit Sa8 Register (E1 Applications Only)	R/W	0x00
0xN138 - 0xN13A	Reserved		
0xN13B	Receive Sa4 Register (E1 Applications Only)	R/W	0x00
0xN13C	Receive Sa5 Register (E1 Applications Only)	R/W	0x00
0xN13D	Receive Sa6 Register (E1 Applications Only)	R/W	0x00

TABLE 20: T1/E1 FRAMER BLOCK CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN13E	Receive Sa7 Register (E1 Applications Only)	R/W	0x00
0xN13F	Receive Sa8 Register (E1 Applications Only)	R/W	0x00
0xN140 - 0xN142	Reserved		
0xN142	Transmit SPRM Control Register	R/W	0x00
0xN143 - 0xN2FF	Reserved		

TABLE 21: TRANSMIT CHANNEL CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN300	Transmit Channel Control Register - Channel 0	R/W	0x00
0xN301	Transmit Channel Control Register - Channel 1	R/W	0x00
0xN302	Transmit Channel Control Register - Channel 2	R/W	0x00
0xN303	Transmit Channel Control Register - Channel 3	R/W	0x00
0xN304	Transmit Channel Control Register - Channel 4	R/W	0x00
0xN305	Transmit Channel Control Register - Channel 5	R/W	0x00
0xN306	Transmit Channel Control Register - Channel 6	R/W	0x00
0xN307	Transmit Channel Control Register - Channel 7	R/W	0x00
0xN308	Transmit Channel Control Register - Channel 8	R/W	0x00
0xN309	Transmit Channel Control Register - Channel 9	R/W	0x00
0xN30A	Transmit Channel Control Register - Channel 10	R/W	0x00
0xN30B	Transmit Channel Control Register - Channel 11	R/W	0x00
0xN30C	Transmit Channel Control Register - Channel 12	R/W	0x00
0xN30D	Transmit Channel Control Register - Channel 13	R/W	0x00
0xN30E	Transmit Channel Control Register - Channel 14	R/W	0x00
0xN30F	Transmit Channel Control Register - Channel 15	R/W	0x00
0xN310	Transmit Channel Control Register - Channel 16	R/W	0x00
0xN311	Transmit Channel Control Register - Channel 17	R/W	0x00
0xN312	Transmit Channel Control Register - Channel 18	R/W	0x00
0xN313	Transmit Channel Control Register - Channel 19	R/W	0x00
0xN314	Transmit Channel Control Register - Channel 20	R/W	0x00
0xN315	Transmit Channel Control Register - Channel 21	R/W	0x00
0xN316	Transmit Channel Control Register - Channel 22	R/W	0x00
0xN317	Transmit Channel Control Register - Channel 23	R/W	0x00

TABLE 21: TRANSMIT CHANNEL CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN318	Transmit Channel Control Register - Channel 24 (E1 Applications Only)	R/W	0x00
0xN319	Transmit Channel Control Register - Channel 25 (E1 Applications Only)	R/W	0x00
0xN31A	Transmit Channel Control Register - Channel 26 (E1 Applications Only)	R/W	0x00
0xN31B	Transmit Channel Control Register - Channel 27 (E1 Applications Only)	R/W	0x00
0xN31C	Transmit Channel Control Register - Channel 28 (E1 Applications Only)	R/W	0x00
0xN31D	Transmit Channel Control Register - Channel 29 (E1 Applications Only)	R/W	0x00
0xN31E	Transmit Channel Control Register - Channel 30 (E1 Applications Only)	R/W	0x00
0xN31F	Transmit Channel Control Register - Channel 31 (E1 Applications Only)	R/W	0x00
0xN320	User (IDLE) Code Register - Channel 0	R/W	0x00
0xN321	User (IDLE) Code Register - Channel 1	R/W	0x00
0xN322	User (IDLE) Code Register - Channel 2	R/W	0x00
0xN323	User (IDLE) Code Register - Channel 3	R/W	0x00
0xN324	User (IDLE) Code Register - Channel 4	R/W	0x00
0xN325	User (IDLE) Code Register - Channel 5	R/W	0x00
0xN326	User (IDLE) Code Register - Channel 6	R/W	0x00
0xN327	User (IDLE) Code Register - Channel 7	R/W	0x00
0xN328	User (IDLE) Code Register - Channel 8	R/W	0x00
0xN329	User (IDLE) Code Register - Channel 9	R/W	0x00
0xN32A	User (IDLE) Code Register - Channel 10	R/W	0x00
0xN32B	User (IDLE) Code Register - Channel 11	R/W	0x00
0xN32C	User (IDLE) Code Register - Channel 12	R/W	0x00
0xN32D	User (IDLE) Code Register - Channel 13	R/W	0x00
0xN32E	User (IDLE) Code Register - Channel 14	R/W	0x00
0xN32F	User (IDLE) Code Register - Channel 15	R/W	0x00
0xN330	User (IDLE) Code Register - Channel 16	R/W	0x00
0xN331	User (IDLE) Code Register - Channel 17	R/W	0x00
0xN332	User (IDLE) Code Register - Channel 18	R/W	0x00
0xN333	User (IDLE) Code Register - Channel 19	R/W	0x00
0xN334	User (IDLE) Code Register - Channel 20	R/W	0x00
0xN335	User (IDLE) Code Register - Channel 21	R/W	0x00
0xN336	User (IDLE) Code Register - Channel 22	R/W	0x00
0xN337	User (IDLE) Code Register - Channel 23	R/W	0x00

TABLE 21: TRANSMIT CHANNEL CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN338	User (IDLE) Code Register - Channel 24 (E1 Applications Only)	R/W	0x00
0xN339	User (IDLE) Code Register - Channel 25 (E1 Applications Only)	R/W	0x00
0xN33A	User (IDLE) Code Register - Channel 26 (E1 Applications Only)	R/W	0x00
0xN33B	User (IDLE) Code Register - Channel 27 (E1 Applications Only)	R/W	0x00
0xN33C	User (IDLE) Code Register - Channel 28 (E1 Applications Only)	R/W	0x00
0xN33D	User (IDLE) Code Register - Channel 29 (E1 Applications Only)	R/W	0x00
0xN33E	User (IDLE) Code Register - Channel 30 (E1 Applications Only)	R/W	0x00
0xN33F	User (IDLE) Code Register - Channel 31 (E1 Applications Only)	R/W	0x00
0xN340	Transmit Signaling Control Register - Channel 0	R/W	0x00
0xN341	Transmit Signaling Control Register - Channel 1	R/W	0x00
0xN342	Transmit Signaling Control Register - Channel 2	R/W	0x00
0xN343	Transmit Signaling Control Register - Channel 3	R/W	0x00
0xN344	Transmit Signaling Control Register - Channel 4	R/W	0x00
0xN345	Transmit Signaling Control Register - Channel 5	R/W	0x00
0xN346	Transmit Signaling Control Register - Channel 6	R/W	0x00
0xN347	Transmit Signaling Control Register - Channel 7	R/W	0x00
0xN348	Transmit Signaling Control Register - Channel 8	R/W	0x00
0xN349	Transmit Signaling Control Register - Channel 9	R/W	0x00
0xN34A	Transmit Signaling Control Register - Channel 10	R/W	0x00
0xN34B	Transmit Signaling Control Register - Channel 11	R/W	0x00
0xN34C	Transmit Signaling Control Register - Channel 12	R/W	0x00
0xN34D	Transmit Signaling Control Register - Channel 13	R/W	0x00
0xN34E	Transmit Signaling Control Register - Channel 14	R/W	0x00
0xN34F	Transmit Signaling Control Register - Channel 15	R/W	0x00
0xN350	Transmit Signaling Control Register - Channel 16	R/W	0x00
0xN351	Transmit Signaling Control Register - Channel 17	R/W	0x00
0xN352	Transmit Signaling Control Register - Channel 18	R/W	0x00
0xN353	Transmit Signaling Control Register - Channel 19	R/W	0x00
0xN354	Transmit Signaling Control Register - Channel 20	R/W	0x00
0xN355	Transmit Signaling Control Register - Channel 21	R/W	0x00
0xN356	Transmit Signaling Control Register - Channel 22	R/W	0x00
0xN357	Transmit Signaling Control Register - Channel 23	R/W	0x00

TABLE 21: TRANSMIT CHANNEL CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN358	Transmit Signaling Control Register - Channel 24 (E1 Applications Only)	R/W	0x00
0xN359	Transmit Signaling Control Register - Channel 25 (E1 Applications Only)	R/W	0x00
0xN35A	Transmit Signaling Control Register - Channel 26 (E1 Applications Only)	R/W	0x00
0xN35B	Transmit Signaling Control Register - Channel 27 (E1 Applications Only)	R/W	0x00
0xN35C	Transmit Signaling Control Register - Channel 28 (E1 Applications Only)	R/W	0x00
0xN35D	Transmit Signaling Control Register - Channel 29 (E1 Applications Only)	R/W	0x00
0xN35E	Transmit Signaling Control Register - Channel 30 (E1 Applications Only)	R/W	0x00
0xN35F	Transmit Signaling Control Register - Channel 31 (E1 Applications Only)	R/W	0x00
0xN360	Receive Channel Control Register - Channel 0	R/W	0x00
0xN361	Receive Channel Control Register - Channel 1	R/W	0x00
0xN362	Receive Channel Control Register - Channel 2	R/W	0x00
0xN363	Receive Channel Control Register - Channel 3	R/W	0x00
0xN364	Receive Channel Control Register - Channel 4	R/W	0x00
0xN365	Receive Channel Control Register - Channel 5	R/W	0x00
0xN366	Receive Channel Control Register - Channel 6	R/W	0x00
0xN367	Receive Channel Control Register - Channel 7	R/W	0x00
0xN368	Receive Channel Control Register - Channel 8	R/W	0x00
0xN369	Receive Channel Control Register - Channel 9	R/W	0x00
0xN36A	Receive Channel Control Register - Channel 10	R/W	0x00
0xN36B	Receive Channel Control Register - Channel 11	R/W	0x00
0xN36C	Receive Channel Control Register - Channel 12	R/W	0x00
0xN36D	Receive Channel Control Register - Channel 13	R/W	0x00
0xN36E	Receive Channel Control Register - Channel 14	R/W	0x00
0xN36F	Receive Channel Control Register - Channel 15	R/W	0x00
0xN370	Receive Channel Control Register - Channel 16	R/W	0x00
0xN371	Receive Channel Control Register - Channel 17	R/W	0x00
0xN372	Receive Channel Control Register - Channel 18	R/W	0x00
0xN373	Receive Channel Control Register - Channel 19	R/W	0x00
0xN374	Receive Channel Control Register - Channel 20	R/W	0x00
0xN375	Receive Channel Control Register - Channel 21	R/W	0x00
0xN376	Receive Channel Control Register - Channel 22	R/W	0x00
0xN377	Receive Channel Control Register - Channel 23	R/W	0x00

TABLE 21: TRANSMIT CHANNEL CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN378	Receive Channel Control Register - Channel 24	R/W	0x00
0xN379	Receive Channel Control Register - Channel 25	R/W	0x00
0xN37A	Receive Channel Control Register - Channel 26	R/W	0x00
0xN37B	Receive Channel Control Register - Channel 27	R/W	0x00
0xN37C	Receive Channel Control Register - Channel 28	R/W	0x00
0xN37D	Receive Channel Control Register - Channel 29	R/W	0x00
0xN37E	Receive Channel Control Register - Channel 30	R/W	0x00
0xN37F	Receive Channel Control Register - Channel 31	R/W	0x00
0xN380	Receive User Code Register - Channel 0	R/W	0x00
0xN381	Receive User Code Register - Channel 1	R/W	0x00
0xN382	Receive User Code Register - Channel 2	R/W	0x00
0xN383	Receive User Code Register - Channel 3	R/W	0x00
0xN384	Receive User Code Register - Channel 4	R/W	0x00
0xN385	Receive User Code Register - Channel 5	R/W	0x00
0xN386	Receive User Code Register - Channel 6	R/W	0x00
0xN387	Receive User Code Register - Channel 7	R/W	0x00
0xN388	Receive User Code Register - Channel 8	R/W	0x00
0xN389	Receive User Code Register - Channel 9	R/W	0x00
0xN38A	Receive User Code Register - Channel 10	R/W	0x00
0xN38B	Receive User Code Register - Channel 11	R/W	0x00
0xN38C	Receive User Code Register - Channel 12	R/W	0x00
0xN38D	Receive User Code Register - Channel 13	R/W	0x00
0xN38E	Receive User Code Register - Channel 14	R/W	0x00
0xN38F	Receive User Code Register - Channel 15	R/W	0x00
0xN390	Receive User Code Register - Channel 16	R/W	0x00
0xN391	Receive User Code Register - Channel 17	R/W	0x00
0xN392	Receive User Code Register - Channel 18	R/W	0x00
0xN393	Receive User Code Register - Channel 19	R/W	0x00
0xN394	Receive User Code Register - Channel 20	R/W	0x00
0xN395	Receive User Code Register - Channel 21	R/W	0x00
0xN396	Receive User Code Register - Channel 22	R/W	0x00
0xN397	Receive User Code Register - Channel 23	R/W	0x00

TABLE 21: TRANSMIT CHANNEL CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN398	Receive User Code Register - Channel 24	R/W	0x00
0xN399	Receive User Code Register - Channel 25	R/W	0x00
0xN39A	Receive User Code Register - Channel 26	R/W	0x00
0xN39B	Receive User Code Register - Channel 27	R/W	0x00
0xN39C	Receive User Code Register - Channel 28	R/W	0x00
0xN39D	Receive User Code Register - Channel 29	R/W	0x00
0xN39E	Receive User Code Register - Channel 30	R/W	0x00
0xN39F	Receive User Code Register - Channel 31	R/W	0x00
0xN3A0	Receive Signaling Control Register - Channel 0	R/W	0x00
0xN3A1	Receive Signaling Control Register - Channel 1	R/W	0x00
0xN3A2	Receive Signaling Control Register - Channel 2	R/W	0x00
0xN3A3	Receive Signaling Control Register - Channel 3	R/W	0x00
0xN3A4	Receive Signaling Control Register - Channel 4	R/W	0x00
0xN3A5	Receive Signaling Control Register - Channel 5	R/W	0x00
0xN3A6	Receive Signaling Control Register - Channel 6	R/W	0x00
0xN3A7	Receive Signaling Control Register - Channel 7	R/W	0x00
0xN3A8	Receive Signaling Control Register - Channel 8	R/W	0x00
0xN3A9	Receive Signaling Control Register - Channel 9	R/W	0x00
0xN3AA	Receive Signaling Control Register - Channel 10	R/W	0x00
0xN3AB	Receive Signaling Control Register - Channel 11	R/W	0x00
0xN3AC	Receive Signaling Control Register - Channel 12	R/W	0x00
0xN3AD	Receive Signaling Control Register - Channel 13	R/W	0x00
0xN3AE	Receive Signaling Control Register - Channel 14	R/W	0x00
0xN3AF	Receive Signaling Control Register - Channel 15	R/W	0x00
0xN3B0	Receive Signaling Control Register - Channel 16	R/W	0x00
0xN3B1	Receive Signaling Control Register - Channel 17	R/W	0x00
0xN3B2	Receive Signaling Control Register - Channel 18	R/W	0x00
0xN3B3	Receive Signaling Control Register - Channel 19	R/W	0x00
0xN3B4	Receive Signaling Control Register - Channel 20	R/W	0x00
0xN3B5	Receive Signaling Control Register - Channel 21	R/W	0x00
0xN3B6	Receive Signaling Control Register - Channel 22	R/W	0x00
0xN3B7	Receive Signaling Control Register - Channel 23	R/W	0x00

TABLE 21: TRANSMIT CHANNEL CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN3B8	Receive Signaling Control Register - Channel 24	R/W	0x00
0xN3B9	Receive Signaling Control Register - Channel 25	R/W	0x00
0xN3BA	Receive Signaling Control Register - Channel 26	R/W	0x00
0xN3BB	Receive Signaling Control Register - Channel 27	R/W	0x00
0xN3BC	Receive Signaling Control Register - Channel 28	R/W	0x00
0xN3BD	Receive Signaling Control Register - Channel 29	R/W	0x00
0xN3BE	Receive Signaling Control Register - Channel 30	R/W	0x00
0xN3BF	Receive Signaling Control Register - Channel 31	R/W	0x00
0xN3C0	Receive Substitution Signaling Register - Channel 0	R/W	0x00
0xN3C1	Receive Substitution Signaling Register - Channel 1	R/W	0x00
0xN3C2	Receive Substitution Signaling Register - Channel 2	R/W	0x00
0xN3C3	Receive Substitution Signaling Register - Channel 3	R/W	0x00
0xN3C4	Receive Substitution Signaling Register - Channel 4	R/W	0x00
0xN3C5	Receive Substitution Signaling Register - Channel 5	R/W	0x00
0xN3C6	Receive Substitution Signaling Register - Channel 6	R/W	0x00
0xN3C7	Receive Substitution Signaling Register - Channel 7	R/W	0x00
0xN3C8	Receive Substitution Signaling Register - Channel 8	R/W	0x00
0xN3C9	Receive Substitution Signaling Register - Channel 9	R/W	0x00
0xN3CA	Receive Substitution Signaling Register - Channel 10	R/W	0x00
0xN3CB	Receive Substitution Signaling Register - Channel 11	R/W	0x00
0xN3CC	Receive Substitution Signaling Register - Channel 12	R/W	0x00
0xN3CD	Receive Substitution Signaling Register - Channel 13	R/W	0x00
0xN3CE	Receive Substitution Signaling Register - Channel 14	R/W	0x00
0xN3CF	Receive Substitution Signaling Register - Channel 15	R/W	0x00
0xN3D0	Receive Substitution Signaling Register - Channel 16	R/W	0x00
0xN3D1	Receive Substitution Signaling Register - Channel 17	R/W	0x00
0xN3D2	Receive Substitution Signaling Register - Channel 18	R/W	0x00
0xN3D3	Receive Substitution Signaling Register - Channel 19	R/W	0x00
0xN3D4	Receive Substitution Signaling Register - Channel 20	R/W	0x00
0xN3D5	Receive Substitution Signaling Register - Channel 21	R/W	0x00
0xN3D6	Receive Substitution Signaling Register - Channel 22	R/W	0x00
0xN3D7	Receive Substitution Signaling Register - Channel 23	R/W	0x00

TABLE 21: TRANSMIT CHANNEL CONTROL REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN3D8 - 0xN3FF	Reserved		
0xN400 - 0xN4FF	Reserved	R/O	0x00

TABLE 22: RECEIVE SIGNALING REGISTER ARRAY REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN500	Receive Signaling Register Array - Channel 0	R/O	0x00
0xN501	Receive Signaling Register Array - Channel 1	R/O	0x00
0xN502	Receive Signaling Register Array - Channel 2	R/O	0x00
0xN503	Receive Signaling Register Array - Channel 3	R/O	0x00
0xN504	Receive Signaling Register Array - Channel 4	R/O	0x00
0xN505	Receive Signaling Register Array - Channel 5	R/O	0x00
0xN506	Receive Signaling Register Array - Channel 6	R/O	0x00
0xN507	Receive Signaling Register Array - Channel 7	R/O	0x00
0xN508	Receive Signaling Register Array - Channel 8	R/O	0x00
0xN509	Receive Signaling Register Array - Channel 9	R/O	0x00
0xN50A	Receive Signaling Register Array - Channel 10	R/O	0x00
0xN50B	Receive Signaling Register Array - Channel 11	R/O	0x00
0xN50C	Receive Signaling Register Array - Channel 12	R/O	0x00
0xN50D	Receive Signaling Register Array - Channel 13	R/O	0x00
0xN50E	Receive Signaling Register Array - Channel 14	R/O	0x00
0xN50F	Receive Signaling Register Array - Channel 15	R/O	0x00
0xN510	Receive Signaling Register Array - Channel 16	R/O	0x00
0xN511	Receive Signaling Register Array - Channel 17	R/O	0x00
0xN512	Receive Signaling Register Array - Channel 18	R/O	0x00
0xN513	Receive Signaling Register Array - Channel 19	R/O	0x00
0xN514	Receive Signaling Register Array - Channel 20	R/O	0x00
0xN515	Receive Signaling Register Array - Channel 21	R/O	0x00
0xN516	Receive Signaling Register Array - Channel 22	R/O	0x00
0xN517	Receive Signaling Register Array - Channel 23	R/O	0x00
0xN518	Receive Signaling Register Array - Channel 24	R/O	0x00

TABLE 22: RECEIVE SIGNALING REGISTER ARRAY REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN519	Receive Signaling Register Array - Channel 25	R/O	0x00
0xN51A	Receive Signaling Register Array - Channel 26	R/O	0x00
0xN51B	Receive Signaling Register Array - Channel 27	R/O	0x00
0xN51C	Receive Signaling Register Array - Channel 28	R/O	0x00
0xN51D	Receive Signaling Register Array - Channel 29	R/O	0x00
0xN51E	Receive Signaling Register Array - Channel 30	R/O	0x00
0xN51F	Receive Signaling Register Array - Channel 31	R/O	0x00
0xN520 - 0xN59F	Reserved		
0xN5A0	Receive Signaling Control Registers - Channel 0	R/W	0x00
0xN5A1	Receive Signaling Control Registers - Channel 1	R/W	0x00
0xN5A2	Receive Signaling Control Registers - Channel 2	R/W	0x00
0xN5A3	Receive Signaling Control Registers - Channel 3	R/W	0x00
0xN5A4	Receive Signaling Control Registers - Channel 4	R/W	0x00
0xN5A5	Receive Signaling Control Registers - Channel 5	R/W	0x00
0xN5A6	Receive Signaling Control Registers - Channel 6	R/W	0x00
0xN5A7	Receive Signaling Control Registers - Channel 7	R/W	0x00
0xN5A8	Receive Signaling Control Registers - Channel 8	R/W	0x00
0xN5A9	Receive Signaling Control Registers - Channel 9	R/W	0x00
0xN5AA	Receive Signaling Control Registers - Channel 10	R/W	0x00
0xN5AB	Receive Signaling Control Registers - Channel 11	R/W	0x00
0xN5AC	Receive Signaling Control Registers - Channel 12	R/W	0x00
0xN5AD	Receive Signaling Control Registers - Channel 13	R/W	0x00
0xN5AE	Receive Signaling Control Registers - Channel 14	R/W	0x00
0xN5AF	Receive Signaling Control Registers - Channel 15	R/W	0x00
0xN5B0	Receive Signaling Control Registers - Channel 16	R/W	0x00
0xN5B1	Receive Signaling Control Registers - Channel 17	R/W	0x00
0xN5B2	Receive Signaling Control Registers - Channel 18	R/W	0x00
0xN5B3	Receive Signaling Control Registers - Channel 19	R/W	0x00
0xN5B4	Receive Signaling Control Registers - Channel 20	R/W	0x00
0xN5B5	Receive Signaling Control Registers - Channel 21	R/W	0x00
0xN5B6	Receive Signaling Control Registers - Channel 22	R/W	0x00
0xN5B7	Receive Signaling Control Registers - Channel 23	R/W	0x00

TABLE 22: RECEIVE SIGNALING REGISTER ARRAY REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN5B8 - 0xN5FF	Reserved		
0xN600 - 0xN640	LAPD Buffer 0 Control Register (64-Bytes)	R/W	0x00
0xN700 - 0xN740	LAPD Buffer 1 Control Register (64-Bytes)	R/W	0x00
0xN741 - 0xN8FF	Reserved		

TABLE 23: T1/E1 PERFORMANCE MONITOR REGISTER (WHERE N RANGES VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xN900	T1 Receive Line Code Violation Count Register (MSB)	RUR	0x00
0xN901	T1 Receive Line Code Violation Count Register (LSB)	RUR	0x00
0xN902	T1/E1 Receive Frame Alignment Error Count Register - MSB	RUR	0x00
0xN903	T1/E1 Receive Frame Alignment Error Count Register (LSB)	RUR	0x00
0xN904	T1/E1 Receive Severely Erred Frame Count Register	RUR	0x00
0xN905	T1/E1 Receive Synchronization Bit Error Count Register - MSB	RUR	0x00
0xN906	T1/E1 Receive Synchronization Bit Error Count Register - LSB	RUR	0x00
0xN907	T1/E1 Receive FEBE Event Count Register - MSB	RUR	0x00
0xN908	T1/E1 Receive FEBE Event Count Register - LSB	RUR	0x00
0xN909	T1/E1 Receive Slip Event Count Register	RUR	0x00
0xN90A	T1/E1 Receive Loss of Frame Count Register	RUR	0x00
0xN90B	T1/E1 Receive Change of Frame Count Register	RUR	0x00
0xN90C	LAPD Frame Check Sequence Error Count Register	RUR	0x00
0xN90D	T1/E1 PRBS Bit Error Count Register - MSB	RUR	0x00
0xN90E	T1/E1 PRBS Bit Error Count Register - LSB	RUR	0x00
0xN90F	T1/E1 Transmit Slip Event Count Register	RUR	0x00
0xN910 - 0xNAFF	Reserved		

TABLE 24: T1/E1 FRAMER BLOCK INTERRUPT REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xNB00	T1/E1 Framer Block Interrupt Enable Register	R/W	0x00
0xNB01	T1/E1 Framer Block Interrupt Status Register	R/O	0x00
0xNB02	Alarm and Error Status Register	RUR	0x00
0xNB03	Alarm and Error Interrupt Enable Register	R/W	0x00

TABLE 24: T1/E1 FRAMER BLOCK INTERRUPT REGISTERS (WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xNB04	Framer Interrupt Enable Register	R/W	0x00
0xNB05	Framer Interrupt Status Register	RUR	0x00
0xNB06	Data Link Interrupt Status Register	RUR	0x00
0xNB07	Data Link Interrupt Enable Register		
0xNB0A	Receive Loop Back Code Interrupt & Status Register - Code 0	R/W	0x00
0xNB0B	Receive Loop Back Code Interrupt Enable Register - Code 0	R/W	0x00
0xNB0C - 0xNB0D	Reserved		
0xNB0E	Excessive Zero Interrupt Status Register	RUR	0x00
0xNB0F	Excessive Zero Interrupt Enable Register	RUR	0x00
0xNB10	Receive Sa Interrupt Enable Register (E1 Applications)SS7 Interrupt Status Register - LAPD # 1 (T1 Applications)	R/W	0x00
0xNB11	Receive Sa Interrupt Enable Register (E1 Applications)SS7 Interrupt Enable Register - LAPD # 1 (T1 Applications)	R/W	0x00
0xNB12 - 0xNB13	Reserved		
0xNB14	Receive Loop-back Code Interrupt Status Register - Code 1	RUR	v0x00
OxNB15	Receive Loop-back Code Interrupt Enable Register - Code 1	R/W	0x00v
0xNB16 - 0xNB17	Reserved		
0xNB18	SS7 Interrupt Status Register - LAPD # 2 (T1 Applications)	R/W	0x00
0xNB19	SS7 Interrupt Enable Register - LAPD # 2 (T1 Applications)	R/W	
0xNB1A	Receive Loop-back Code Interrupt Status Register - Code 2	RUR	0x00
0xNB1B	Receive Loop-back Code Interrupt Enable Register - Code 2	R/W	0x00
0xNB1C - 0xNB27	Reserved		
0xNB28	SS7 Interrupt Status Register - LAPD # 3 (T1 Applications)	R/W	0x00
0xNB29	SS7 Interrupt Enable Register - LAPD # 3 (T1 Applicaions)	R/W	0x00
0xNB30 - 0xNB3F	Reserved		
0xNB40	Customer Installation Alarm Status Register	RUR	0x00
0xNB41	Customer Installation Alarm Interrupt Enable Register	R/W	0x00
0xNB42 - 0xNCFF	Reserved	R/O	0x00

TABLE 25: VT MAPPER REGISTER (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xND00 - 0xND41	Reserved		
0xND42	Channel Control - VT Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register - Byte 1	R/O & R/W	0x00
0xND43	Channel Control - VT-Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register - Byte 0	R/W	0x00
0xND44	Channel Control - VT-De-Mapper Block - Egress Direction - DS1/E1 Drop Control Register - Byte 3	R/W	0x00
0xND45	Channel Control - VT-De-Mapper Block - Egress Direction - DS1/E1 Drop Control Register - Byte 2	R/W	0x00
0xND46	Channel Control - VT-De-Mapper Block - Egress Direction - DS1/E1 Drop Control Register - Byte 1	R/O	0x10
0xND47	Channel Control - VT De-Mapper Block - Egress Direction - DS1/E1 Drop Control Register - Byte 0	R/O & R/W	0x00
0xND48 - 0xND49	Reserved		
0xND4A	Channel Control - VT De-Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 1	RUR	0x00
0xND4B	Channel Control - VT De-Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 0	RUR	0x00
0xND4C - 0xND4D	Reserved		
0xND4E	Channel Control - VT De-Mapper Block - Egress Direction - REI-V Event Count Register - Byte 1	RUR	0x00
0xND4F	Channel Control - VT-De-Mapper Block - Egress Direction - REI-V Event Count Register - Byte 0	RUR	0x00
0xND50 - 0xND52	Reserved		
0xND53	Channel Control - VT-De-Mapper Block - Egress Direction - Receive APS Register - Byte 0	R/W	0x00
0xND54 - 0xND55	Reserved		
0xND56	Channel Control - VT-Mapper Block - Ingress Direction - Transmit APS Register - Byte 1	R/W	0x00
0xND57	Channel Control - VT-Mapper Block - Ingress Direction - Transmit APS/K4 Register - Byte 0	R/W	0x00
0xND58 - 0xND62	Reserved		
0xND63	Channel Control - VT-De-Mapper Block- Egress Direction - J2 Byte Status Register - Byte 0	R/O	0x00
0xND64	Channel Control - VT-De-Mapper Block - Egress Direction - Composite Status Register - Byte 1	RUR	0x00
0xND65	Channel Control - VT-De-Mapper Block - Egress Direction -Composite Status Register - Byte 0	RUR	0x00

TABLE 25: VT MAPPER REGISTER (WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

ADDRESS LOCATION	REGISTER NAME	TYPE	DEFAULT VALUE
0xND66	Reserved	RUR	0x00
0xND67	Channel Control - VT-De-Mapper Block - Egress Direction - Interrupt Status Register - Byte 0	RUR	0x00
0xND68	Channel Control - VT-De-Mapper Block - Egress Direction - Interrupt Enable Register	R/W	0x00
0xND69	Channel Control - VT-De-Mapper - Block - Egress Direction - Interrupt Enable Register	R/W	0x00
0xND6A	Reserved	R/W	0x00
0xND6B	Channel Control - VT-De-Mapper Block - Egress Direction -Interrupt Enable Register - Byte 0	R/W	0x00
0xND6C - 0xND70	Reserved		
0xND71	Channel Control - VT-De-Mapper Block - Egress Direction - VT Path Trace Buffer Control Register	R/W	0x00
0xND72	Channel Control - VT-De-Mapper Block - Egress Direction - Auto AIS Control Register - Byte 1	R/W	0x00
0xND73	Channel Control VT De-Mapper Block - Egress Direction - Auto AIS Control Register - Byte 0	R/W	0x00
0xND74 - 0xND75	Reserved		
0xND76	Channel Control - VT-Mapper Block - Ingress Direction - Transmit J2 Byte Value Register	R/W	0x00
0xND77	Channel Control - VT Mapper Block - Ingress Direction - Transmit N2 Byte Value Register	R/W	0x00

2.0 REGISTER DESCRIPTIONS

the remainder of this document use register descriptions with the folowing format:

8-BIT register table

TABLE 26: OPERATION CONTROL REGISTER - BYTE 3 (ADDRESS = 0X0000)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT descriptions

BIT 7 - Bit name

Bit Description

- 0 - Logic LOW condition
- 1 - Logic HIGH condition

NOTE: *Speial notes*

BIT [6:0] - Bit name

2.1 OPERATION CONTROL REGISTERS

TABLE 27: OPERATION CONTROL REGISTER - BYTE 3 (ADDRESS = 0X0000)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Ingress Direction Add-Drop Interface Enable	Egress Direction Add-Drop Interface Enable	Parallel Interface Enable	Mode_Select[3:0]			
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Unused

BIT6 - Ingress Direction Add-Drop Interface Enable:

This READ/WRITE bit-field is used to either enable or disable the Ingress Direction Add-Drop Interface.

If the Ingress Direction Add-Drop Interface is enabled, then the Ingress Direction Drop Port will drop out the entire traffic (of all 28 channels in the Ingress Direction) via the IG_TE1RxDATA[7:0] output pins. Additionally, the user can add in of the 28 DS1 or 21 E1 Ingress Direction signals via the Ingress Direction Add Port.

- 0 - Disables the Ingress Direction Add-Drop Interface.
- 1 - Enables the Ingress Direction Add-Drop Interface.

NOTE: *This feature is only available if the XRT86SH328 has been configured to operate in either of the following modes.·*

- The VT-Mapper Mode (w/ T1/E1 Framing)
- The M13 MUX Mode (w/ T1/E1 Framing)
- The M13 MUX to STS-1/STS-3 Mode
- The Transmux Mode

BIT 5 - Egress Direction Add-Drop Interface Enable:

This READ/WRITE bit-field is used to either enable or disable the Egress Direction Add-Drop Interface.

If the user enables the Egress Direction Add-Drop Interface, then the Egress Direction Drop Port will drop out the entire traffic (of all 28 channels in the Egress Direction) via the EG_TE1RxDATA[7:0] output pins. Additionally, the user can add in any of the 28 DS1 or 21 E1 Egress Direction signals via the Egress Direction Add Interface.

- 0 - Disables the Egress Direction Add-Drop Interface.
- 1 - Enables the Egress Direction Add-Drop Interface.

NOTE: *This feature is only available if the XRT86SH328 has been configured to operate in either of the following modes.*

- The VT-Mapper Mode (w/ T1/E1 Framing)
- The M13 MUX Mode (w/ T1/E1 Framing)
- The M13 MUX to STS-1/STS-3 Mode
- The Transmux Mode

BIT 4 - Parallel Interface Enable

NOTE: *This bit-field is only valid if the XRT86SH328 has been configured to operate in the 28-Channel DS1/E1 Framer & LIU Mode.*

BIT[3:0] - Mode Select Bits[3:0]:

These four READ/WRITE bit-fields are used to select the mode that the XRT86SH328 will operate in, as shown in the table below below.

Mode Select Bits

MODE_SELECT[3:0]	RESULTING MODE OF OPERATION
0000	VT-Mapper Mode (w/ T1/E1 Framing)
0001	M13 MUX Mode (w/ T1/E1 Framing
0010	M13 MUX to STS-1/STS-3 Mode
0011	Reserved
0100	28 Channel T1/E1 Framer & LIU Mode
0101	Transmux Mode (w/ T1/E1 Framing)
0110 & 0111	Reserved
1000	VT-Mapper Mode (w T1/E1 Framers by-passed)
1001	M13 MUX Mode (w/ T1/E1 Framers by-passed)
1010	M13 MUX to STS-1/STS-3 Mode (w/ T1/E1 Framers by-passed)
1011	Reserved
1100	28 Channel T1/E1 LIU Mode
1101	Transmux Mode (w/ T1/E1 Framers by-passed)

TABLE 28: OPERATION CONTROL REGISTER - BYTE 2 (ADDRESS = 0X0001)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Interrupt Write Clear/RUR	Enable Interrupt Clear	Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Unused

Please set to 0 for normal operation.

BIT 2 - Interrupt Write to Clear/RUR

This READ/WRITE bit-field is used to configure all of the Source-Level Interrupt Status bits (within the XRT86SH328) to either be Write to Clear (WTC) or Reset-upon-Read (RUR) bits.

- 0 - Configures all Source-Level Interrupt Status register bits to function as Reset-upon-Read (RUR).
- 1 - Configures all Source-Level Interrupt Status register bits to function as Write-to-Clear (WTC)

BIT 1 - Enable Interrupt Clear

This READ/WRITE bit-field is used to configure the XRT94L43 to automatically disable all interrupts that are activated.

- 0 - Configures the chip to NOT automatically disable any Interrupts following their activation.
- 1 - Configures the chip to automatically disable all Interrupts following their activation.

BIT 0 - Interrupt Enable

This READ/WRITE bit-field is used to configure the XRT94L43 to generate interrupt requests to the Microprocessor.

- 0 - Configures the chip to NOT generate interrupt to the Microprocessor.

All interrupts are disabled and the Microprocessor must poll the register bits.

- 1 - Configures the chip to generate interrupts to the Microprocessor.

NOTE: To operate the XRT986SH328 in an Interrupt-Driven Manner, this bit-field must be set to a logic 1.

TABLE 29: OPERATION CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0003)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Receive Clock Detect	Reserved		Burst Enable	Reserved		SWRESET
R/W	R/W	R/O	R/O	R/W	R/O	R/O	R/W
0	1	0	0	0	0	0	0

BIT7 - Reserved

BIT6 - Receive Clock Detect

This READ/WRITE bit-field is used to enable or disable the Receive Clock Detect feature. If this feature is enabled, then the Receive STS-1/STS-3 circuitry will check for the existence of the 6.48MHz or 19.44MHz clock signal (through the Receive STS-1/STS-3 Telecom Bus Interface). If none of these clock signals are present, then the Receive STS-1/STS-3 TOH Processor block and each of the 1 (or 3) Receive SONET POH Processor block circuitry will automatically switch over and use the 19.44MHz clock signal that is applied to the Tx19_51MHz input pin (Ball R3) as there timing source.

- 0 - Disables the Receive Clock Detect feature.
- 1 - Enables the Receive Clock Detect feature.

BIT [5:4] = Reserved

BIT 3 - Burst Enable

This READ/WRITE bit-field is used to either enable or disable Burst Mode operation within the Microprocessor Interface.

- 0 - Disables Burst Mode operation.
- 1 - Enables Burst Mode operation

BIT 2 - BIT 1 - Reserved

BIT 0 - SWReset - SONET Block

This READ/WRITE bit-field is used to command a software reset to the SONET/SDH block. If a software reset to the SONET/SDH blocks is invoked, then all of the internal state machines will be reset to their default conditions and each of the following blocks will undergo a re-frame operation.

- The Receive STS-1/3 TOH Processor block
- Each of the three (3) Receive SONET POH Processor blocks
- Each of the three (3) VT Mapper Blocks

A 0 to 1 transition, within this bit-field commands this Software Reset.

NOTE: This Software Reset does not reset the command registers to their default state. This can only be achieved by executing a Hardware RESET (e.g., by pulling the RESET_L input pin LOW).*

TABLE 30: DEVICE ID VALUE REGISTER - BYTE 3 (ADDRESS = 0X0004)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device ID Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	0	1	0	0	0	0

BIT [7:0] - Device ID Value

This READ-ONLY bit-field is set to the value 0x50 and is used's software code to uniquely identify this device as being the XRT86SH328.

TABLE 31: REVISION NUMBER VALUE REGISTER - BYTE 2 (ADDRESS = 0X0005)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Revision Number Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	1

BIT [7:0] - Revision Number Value

This READ-ONLY bit-field is set to the value that corresponds to its revision number. Revision A silicon will be set to the value 0x01. This register is uses software code to uniquely identify the revision number of this device

TABLE 32: OPERATION INTERRUPT STATUS REGISTER - BYTE 0 (ADDRESS = 0X000B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							TB Parity Error Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR/WTC
0	0	0	0	0	0	0	0

BIT [7:1] - Unused

Please set to 0 for normal operation

BIT 0 - Telecom Bus Parity Error Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of 51.84/155.52Mbps Telecom Bus - Parity Error interrupt has occurred since the last read of this register bit.

- 0 - Indicates that the Detection of 51.84/155.52Mbps Telecom Bus - Parity Error interrupt has NOT occurred since the last read of this register bit.
- 1 - Indicates that the Detection of 51.84/155.52Mbps Telecom Bus - Parity Error interrupt has occurred since the last of this register bit.

NOTE: *This register bit is only active if the XRT86SH328 has been configured to operate in the Telecom Bus Mode.*

TABLE 33: OPERATION INTERRUPT ENABLE REGISTER - BYTE 0 (ADDRESS = 0X000F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Telecom BusParity Error Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Unused

Please set to 0 for normal operation

BIT 0 - Telecom Bus Parity Error Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of 51.84/155.52Mbps Telecom Bus - Parity Error interrupt.

- 0 - Disables the Detection of 51.84/155.52Mbps Telecom Bus - Parity Error interrupt.
- 1 - Enables the Detection of 51.84/155.52Mbps Telecom Bus - Parity Error interrupt.NOTE: This register bit is only active if the XRT86SH328 has been configured to operate in the Telecom Bus Mode.

TABLE 34: OPERATION BLOCK INTERRUPT STATUS REGISTER - BYTE 1 (ADDRESS = 0X0012)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Op Control Block Interrupt Status	DS3 Mapper Block Interrupt Status	VT Mapper Block Interrupt Status	DS1/E1 Framer/LIU Block (VT Side) Interrupt Status	DS1/E1 Framer/LIU Block (M13 Side) Interrupt Status	DS3/E3 Framer Block nterrupt Status	Receive Line Interface Block Interrupt Status	Transmit Line Interface Block Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Operation Control Block Interrupt Status

This READ-ONLY bit-field indicates whether or not an Operation Control Block-related Interrupt is awaiting service.

- 0 - No Operation Control Block Interrupts are awaiting service.
- 1 - At least one Operation Control Block Interrupt is awaiting service.

BIT 6- DS3 Mapper Block Interrupt Status

This READ-ONLY bit-field indicates whether or not a Mapper Block-related Interrupt is awaiting service.

- 0 - No Mapper Block interrupt is awaiting service.
- 1 - At least one Mapper Block Interrupt is awaiting service.

BIT 5 - VT Mapper Block Interrupt Status

This READ-ONLY bit-field indicates whether or not a VT-Mapper block interrupt is awaiting service.

- 0 - Indicates that no VT Mapper block interrupt is awaiting service.
- 1 - Indicates that at least one VT Mapper block interrupt is awaiting service.

BIT 4 - DS1/E1 Framer/LIU Block (VT Side) Interrupt Status

This READ-ONLY bit-field indicates whether or not a DS1/E1 Framer/LIU Block (on the VT Side) Interrupt is awaiting service.

- 0 - Indicates that no DS1/E1 Framer Block (VT Side) interrupt is awaiting service.
- 1 - At least one DS1/E1 Framer/LIU Block (VT Side) interrupt is awaiting service.

BIT 3 - DS1/E1 Framer/LIU Block (M13 Side) Interrupt Status

This READ-ONLY bit-field indicates whether or not a DS1/E1 Framer/LIU Block (M13 Side) Interrupt is awaiting service.

- 0 - No DS1/E1 Framer/LIU Block (M13 Side) interrupt is awaiting service.
- 1 - At least one DS1/E1 Framer/LIU (M13 Side) interrupt is awaiting service.

BIT 2 - DS3/E3 Framer Block Interrupt Status

This READ-ONLY bit-field indicates whether or not a DS3/E3 Framer Block interrupt is awaiting service.

- 0 - No DS3/E3 Framer block interrupt is awaiting service.
- 1 - At least one DS3/E3 Framer block interrupt is awaiting service.

BIT 1:0 - Unused

TABLE 35: OPERATION BLOCK INTERRUPT STATUS REGISTER - BYTE 0 (ADDRESS = 0X0013)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Receive STS-1/STS-3 TOH Block Interrupt Status	Receive STS-1/STS-3 POH Block Interrupt Status	Unused		External Interrupt Status # 1	Unused	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT 6 - Receive STS-1/ST3-3TOH Processor Block Interrupt Status

This READ-ONLY bit-field indicates whether or not a Receive STS-1/STS-3 TOH Processor Block interrupt is awaiting service.

- 0 - No Receive STS-1/STS-3 TOH Processor Block Interrupt is awaiting service.
- 1 - At least one Receive STS-1/STS-3 TOH Processor Block interrupt is awaiting service.

BIT 5 - Receive STS-1/STS-3 POH Processor Block Interrupt Status

This READ-ONLY bit-field indicates whether or not a Receive STS-1/STS-3 POH Processor Block interrupt is awaiting service.

- 0 - No Receive STS-1/STS-3 POH Processor Block Interrupt is awaiting service.
- 1 - At least one Receive STS-1/STS-3 POH Processor Block Interrupt is awaiting service.

BIT [4:3] - Unused

BIT 2 - External Interrupt Input Pin # 1 - Interrupt Status

This READ-ONLY bit-field indicates whether or not an External Interrupt Input Pin # 1 Interrupt is awaiting service, as described below.

- 0 - No External Interrupt Input Pin # 1 Interrupt is awaiting service.
- 1 - The External Interrupt Input Pin # 1 Interrupt is awaiting service.

NOTE: *If this interrupt is enabled, then the XRT86SH328 will generate this interrupt anytime that the EXT_INT_1 Input pin (Ball T5) has been driven to the logic HIGH level.*

BIT [1:0] - Unused

TABLE 36: OPERATION BLOCK INTERRUPT ENABLE REGISTER - BYTE 1 (ADDRESS = 0X0016)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Op Control Block Interrupt Enable	DS3Mapper Block Interrupt Enable	VT Mapper Block Interrupt Enable	DS1/E1 Framer/LIU Block (VT Side) Interrupt Enable	DS1/E1 Framer/LIU Block (M13 Side) Interrupt Enable	DS3Framer Block nterrupt Enable	Unused	
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Operation Control Block Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Operation Control Block for interrupt generation. If a 0 is written to this register bit and if the Operation Control Block (for interrupt generation) is disabled, then all Operation Control Block interrupts will be disabled for interrupt generation.

If a 1 is written to this register bit, the individual Operation Control Block interrupt(s) at the Source Level will still need

to be enabled in order to enable that particular interrupt

- .0 - Disable all Operation Control Block interrupts within the device.
- 1 - Enables the Operation Control Block at the Block-Level for interrupt generation

BIT 6 - DS3 Mapper Block Interrupt Enable

This READ/WRITE bit is used to either enable or disable the DS3 Mapper Block for interrupt generation. If a 0 is written to this register bit and if the DS3 Mapper Block (for interrupt generation) is disabled, then all DS3 Mapper Block interrupts will be disabled for interrupt generation.

If a 1is written to this register bit, the individual DS3 Mapper Block interrupt(s) at the Source Levelwill still need to be enabled in order to enable that particular interrupt.

- 0 - Disable all DS3 Mapper Block interrupts within the device.
- 1 - Enables the DS3 Mapper Block interrupts at the Block-Level

BIT 5 - VT Mapper Block Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the VT-Mapper Block for interrupt generation. If the user writes a 0 into this register bit and disables the VT Mapper Block (for interrupt generation) then all VT-Mapper Block interrupts will be disabled for interrupt generation.

If the user writes a 1 into this register bit, the user will still need to enable the individual VT-Mapper Block Interrupt(s) at the Source Level in order to enable that particular interrupt.

- 0 - Disables all VT Mapper Block Interrupts within the device.
- 1 - Enables the VT Mapper Block Interrupts at the Block-Level

BIT 4- DS1/E1 Framer/LIU Block (VT Side) Interrupt Enable

This READ/WRITE bit is used to either enable or disable the DS1/E1 Framer/LIU Block (on the VT Side) for interrupt generation.

If the user writes a 0 to this register bit and disables the DS1/E1 Framer/LIU Block (on the VT Side) for interrupt generation, then all DS1/E1 Framer/LIU Block interrupts will be disabled for interrupt generation.

If the user writes a 1 to this register bit, the user will still need to enable the individual DS1/E1 Framer/LIU Block interrupt(s) at the Source Level in order to enable that particular interrupt.

- 0 - Disable all DS1/E1 Framer/LIU Block interrupts within the device.
- 1 - Enables the DS1/E1 Framer/LIU Block at the Block-Level.

BIT 3 - DS1/E1 Framer/LIU Block (M13 Side) Interrupt Enable

This READ/WRITE bit is used to either enable or disable the DS1/E1 Framer/LIU Block (on the M13 Side) for interrupt generation.

If the user writes a 0 to this register bit and disables the DS1/E1 Framer/LIU Block (for interrupt generation), then all DS1/E1 Framer/LIU Block interrupts will be disabled for interrupt generation.

If the user writes a 1 to this register bit, the user will still need to enable the individual DS1/E1 Framer/LIU Block interrupt(s) at the Source Level in order to enable that particular interrupt.

- 0 - Disable all DS1/E1 Framer/LIU Block interrupts within the device,
- 1 - Enables the DS1/E1 Framer/LIU Block interrupts at the Block-Level.

BIT 2 - DS3 Framer Block Interrupt Enable

This READ/WRITE bit is used to either enable or disable the DS3 Framer Block for interrupt generation.

If the user writes a 0 to this register bit and disables the DS3 Framer Block (for interrupt generation), then all DS3 Framer Block interrupts will be disabled for interrupt generation. If the user writes a 1 to this register bit, the user will still need to enable the individual DS3 Framer Block interrupt(s) at the Source Level in order to enable that particular interrupt.

- 0 - Disable all DS3 Framer Block interrupts within the device.
- 1 - Enables the DS3 Framer Block at the Block-Level.

BIT [1:0] - Unused

TABLE 37: OPERATION BLOCK INTERRUPT ENABLE REGISTER - BYTE 0 (ADDRESS = 0X0017)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Receive STS-1/STS-3 TOHBlock Interrupt Enable	Receive STS-1 POH Block Interrupt Enable	Unused		External Interrupt Enable # 1	Unused	
R/O	R/W	R/W	R/O	R/O	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT 6 - Receive STS-1/STS-3 TOH Processor Block Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Receive STS-1/STS-3 TOH Processor Block for interrupt generation.

If the user writes a 0 to this register bit and disables the Receive STS-1/STS-3 TOH Processor Block (for interrupt generation), then all Receive STS-1/STS-3 TOH Processor Block interrupts will be disabled for interrupt generation.

If the user writes a 1 to this register bit, the user will still need to enable the individual Receive STS-1/STS-3 TOH Processor Block interrupt(s) at the Source Level in order to enable that particular interrupt.

- 0 - Disables all Receive STS-1/STS-3 TOH Processor Block interrupts within the device.
- 1 - Enables the Receive STS-1/STS-3 TOH Processor Block at the Block Level for interrupt generation.

BIT 5 - Receive STS-1/STS-3 POH Processor Block Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Receive STS-1/STS-3 POH Processor Block for interrupt generation.

If the user writes a 0 into this register bit and disables the Receive STS-1/STS-3 POH Processor Block (for interrupt generation), then all Receive STS-1/STS-3 Processor Block interrupts will be disabled for interrupt generation.

If the user writes a 1 to this register bit, then the user will still need to enable the individual Receive STS-1/STS-3 POH Processor Block Interrupt(s) at the Source Level in order to enable that particular interrupt.

- 0 - Disables all Receive STS-1/STS-3 POH Processor Block Interrupts within the device.
- 1 - Enables the Receive STS-1/STS-3 POH Processor Block at the Block Level for interrupt generation.

BIT [4:3] - Unused

BIT 2 - External Interrupt Input Pin # 1 - Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the External Interrupt Pin # 1 Interrupt.

If this interrupt is enabled, then the XRT86SH328 will generate an interrupt anytime that the EXT_INT_1 input pin (Ball T5) has been driven to the logic HIGH level.

- 0 - Disables the External Interrupt Input # 1 Interrupt
- 1 - Enables the External Interrupt Input # 1 Interrupt.

BIT [1:0] - Unused

TABLE 38: MODE CONTROL REGISTER - BYTE 0 (ADDRESS = 0X001B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
T1/E1 De-Sync Disable	STS-1/STS-3 & DS3 Share Serial Interface	Additional T1/E1 Framers Enabled	Unused				AU-3/TUG_3*
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - T1/E1 De-Sync Disable

This READ/WRITE bit-field is used to either enable or disable the T1/E1 De-Sync Circuitry within the XRT86SH328.

- 0 - Enables the T1/E1 De-Sync Circuitry.
- 1 - Disables the T1/E1 De-Sync Circuitry.

BIT 6 - STS-1/STS-3 and DS3 Share Serial Interface

This READ/WRITE bit-field is used to configure the DS3 and STS-1/STS-3 circuitry to either share the same Serial Interface or not. To operate the XRT86SH328 in the Transmux mode, then the user must configure the DS3 and STS-1/STS-3 circuitry to NOT share the same Serial Interface.

- 0 - Configures the STS-1/STS-3 and DS3 circuitry to NOT share the same Serial Interface.
- 1 - Configures the STS-1/STS-3 and DS3 circuitry to Share the same Serial Interface.

BIT 5 - Additional T1/E1 Framer Enabled

This READ/WRITE bit-field is used to either enable or disable the M13 T1/E1 Framers.

If the user enables these additional T1/E1 Framers, then the XRT86SH328 will be able to perform full-blown performance monitoring in both the Ingress and Egress Directions

.If the user disables the M13 T1/E1 Framers, then the user will only be able to perform full-block performance monitoring on the Ingress Direction T1/E1 signals.

- 0 - Disables the M13 T1/E1 Framer blocks.
- 1 - Enables the M13 T1/E1 Framer blocks.

NOTE: *This bit-field is only active if the XRT86SH328 has been configured to operate in the 28-Channel Clear-Channel T1/E1 Framer Mode.*

BIT [4:1] - Unused

BIT 0 - AU-3/TUG-3 Mode Select:

This READ/WRITE bit-field is used to configure the XRT86SH328 to operate in either the AU-3 or the TUG-3 Mapping Mode.

- 0 - Configures the XRT86SH328 to operate in the TUG-3 Mode.
- 1 - Configures the XRT86SH328 to operate in the AU-3 Mode.

NOTE: *This register bit is only active if the XRT86SH328 has been configured to operate in the SDH Mode.*

TABLE 39: LOOP-BACK CONTROL REGISTER - BYTE 0 (ADDRESS = 0X001F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Loop-back[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4]- Unused

BIT [3:0] - Loop-back Mode[3:0]

These four READ/WRITE bits-fields are used to configure the XRT86SH328 to operate in a variety of loop-back modes, as is tabulated below.

Loop Back Modes

LOOP-BACK[3:0]	RESULTING LOOP-BACK MODE
0000	**Normal Mode (e.g., No Loop-back Mode)**
0001	**Remote Line Loop-back** In this mode, all data that is received by the Receive STS-1/STS-3 Serial Interface will be routed to the Transmit STS-1/STS-3 Serial Interface.
0010	**Local Transport Loop-back** In this mode, all data that is being output via the Transmit STS-1/STS-3 TOH Processor block will also be routed to the Receive STS-1/STS-3 TOH Processor block.
0011	**Local Path Loop-back** In this mode, all data that is output by the Transmit STS-1/STS-3 POH Processor block (e.g., towards the Transmit STS-1/STS-3 TOH Processor block) will be routed to the Receive STS-1/STS-3 POH Processor block.
0100 - 1111	**Reserved - Do Not Use**

TABLE 40: STS-1/STS-3 TELECOM BUS CONTROL REGISTER - BYTE 3 (ADDRESS = 0X0034)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HRSYNC_Delay[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit STS-1/STS-3 Telecom Bus - Sync Delay - Upper Byte

The Transmit STS-1/STS-3 Telecom Bus can be configured to alignment its transmission of SONET/SDH frames with 8kHz pulses being applied to the TxSBFP_IN_OUT input pin.

The user is expected to apply a pulse (with the period of either a 6.48MHz or a 19.44MHz clock signal) at a rate of 8kHz to the TxSBFP_IN_OUT input (pin number P5). The Transmit STS-1/STS-3 Telecom Bus will align its transmission of the very first byte of a new STS-1/STS-3 frame, with a pulse at this input pin.

These READ/WRITE bit-fields (along with that within the STS-1/STS-3 Telecom Bus Control Register - Byte 2) are used to specify the amount of delay (in terms of either 6.48MHz or 19.44MHz clock periods) that will exist between the rising edge of TxSBFP_IN_OUT and the transmission of the very first byte, within a given STS-1/STS-3 frame via the Transmit STS-1/STS-3 Telecom Bus.

- 0x0000 - Configures each of the Transmit STS-1/STS-3 Telecom Bus Interfaces to transmit the very first byte of a new STS-1/STS-3 frame, upon detection of the rising edge of the TxSBFP_IN_OUT.
- 0x0001 - Configures each of the Transmit STS-1/STS-3 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STS-1/STS-3 frame, by one 6.48MHz or 19.44MHz clock period, and so on.

NOTE: *This register is only active if the STS-1/STS-3 Telecom Bus Interface is enabled.*

TABLE 41: STS-1/STS-3 TELECOM BUS CONTROL REGISTER - BYTE 2 (ADDRESS = 0X0035)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HRSYNC_Delay[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit STS-1/STS-3 Telecom Bus - Sync Delay - Lower Byte

The Transmit STS-1/STS-3 Telecom Bus is aligned to the TxSBFP_IN_OUT input pin. The user is expected to apply a pulse (with the period of either a 6.48MHz or a 19.44MHz clock signal) at a rate of 8kHz to the TxSBFP_IN_OUT input (pin number P5). The Transmit STS-1/STS-3 Telecom Bus will align its transmission of the very first byte of a new STS-1/STS-3 frame, with a pulse at this input pin.

These READ/WRITE bit-fields (along with that within the STS-1/STS-3 Telecom Bus Control Register - Byte 3) are used to specify the amount of delay (in terms of either a 6.48MHz or a 19.44MHz clock periods) that will exist between the rising edge of TxSBFP_IN_OUT and the transmission of the very first byte, within a given STS-1/STS-3 frame via the Transmit STS-1/STS-3 Telecom Bus.

- 0x0000 - Configures each of the Transmit STS-1/STS-3 Telecom Bus Interfaces to transmit the very first byte of a new STS-1/STS-3 frame, upon detection of the rising edge of the TxSBFP_IN_OUT. S
- 0x0001 - Configures each of the Transmit STS-1/STS-3 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STS-1/STS-3 frame, by one 6.48MHz or 19.44MHz clock period, and so on.

NOTE: *This register is only active if the STS-1/STS-3 Telecom Bus Interface is enabled.*

TABLE 42: STS-3/STS-1/STS-3 TELECOM BUS CONTROL REGISTER - BYTE 1 (ADDRESS = 0X0036)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Set Telecom Bus to STS-1/STS-3 Mode	Fractional Bandwidth Enable	Slot_0 Master	Slot[1:0]		Telecom Bus Parity Include V1 Signal	Framing Pulse Enable	Telecom Bus - V1 Signal Support Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Set Telecom Bus to STS-1/STS-3 Mode:

This READ/WRITE bit-field is used to configure the STS-1/STS-3 Telecom Bus Interface to operate at either the STS-1/STS-3 or STS-3 rates.

- .0 - Configures the Telecom Bus Interface to operate at the STS-3/STS-1/STS-3 rate. In this case, the Telecom Bus Interface will operate at a rate of 19.44MHz.
- 1 - Configures the Telecom Bus Interface to operate at the STS-1/STS-3 rate. In this case, the Telecom Bus Interface will operate with a clock rate of 6.48MHz.

NOTE: *This bit-field is only active if the XRT86SH328 has been configured to transmit/receive data (on the high-speed side) via the Telecom Bus Interface.*

BIT 6 - Fractional Bandwidth Enable:

If the XRT86SH328 is configured to transmit/receive data via the Telecom Bus Interface as STS-3/STS-1/STS-3 rates, then this READ/WRITE bit-field can be used to configure the XRT86SH328 to operate in the Fractional Bandwidth Mode.

If the XRT86SH328 is configured to operate in the Fractional Bandwidth Mode, then it will only fill in the STS-1/STS-3 time-slot data (within this outbound STS-3/STS-1 or STS-3 Data-stream) that pertains to this particular XRT86SH328. The XRT86SH328 will tri-state the Transmit STS-1/STS-3 Telecom bus interface coincident to whenever the other STS-1/STS-3 time-slot data would ordinarily be output via the STS-3/STS-1/STS-3 Telecom Bus Interface.

If the XRT86SH328 is NOT configured to operate in the Fractional Bandwidth Mode, then it will fill in the STS-1/STS-3 time-slot data (within this outbound STS-3/STS-1/STS-3 data-stream) that pertains to this particular XRT86SH328. The XRT86SH328 will automatically set the bytes (within all of the remaining STS-1/STS-3 time-slots) to 0x00 as it outputs this STS-3/STS-1/STS-3 data-stream via the Transmit STS-3/STS-1/STS-3 Telecom Bus Interface.

- 0 - Configures the XRT86SH328 to NOT operate in the Fractional Bandwidth Mode.
- 1 - Configures the XRT86SH328 to operate in the Fractional Bandwidth Mode.

NOTES:

1. *If the user wishes to design in three (3) XRT86SH328s (into his/her system) such that they are sharing the same STS-3/STS-1/STS-3 Telecom Bus, then the user must set this bit-field to 1.*

2. This bit-field is only active if the Telecom Bus Interface has been configured to operate in the STS-3/STS-1/STS-3 Mode.

BIT 5 - Slot Master Designate

This READ/WRITE bit-field is used to designate a given XRT86SH328 as being the Slot Master. If the user designates a given XRT86SH328 has being the Slot Master, then this device will be responsible for sourcing the B1 byte, the REI-L and RDI-L indicators (within the outbound STS-3/STS-1/STS-3 data-stream). Additionally, if a given XRT86SH328 has been designated as the Slot Master, then it will be responsible for generating an 8kHz signal via its TxSBFP_IN_OUT input/output pin.

If a given XRT86SH328 is NOT configured to function as the Slot Master, then its TxSBFP_IN_OUT input/output pin will function as an input pin

- 0 - Configures this particular XRT86SH328 to NOT be the Slot Master.
- 1 - Configures this particular XRT86SH328 to function as the Slot Master.

NOTES:

1. This bit-field is only value if (1) the Telecom Bus Interface is configured to operate in the STS-3/STS-1/STS-3 Mode.

2. The XRT86SH328 has been configured to operate in the Fractional Bandwidth Mode.

3. This particular XRT86SH328 has been assigned the STS-1/STS-3 Time Slot of [0, 0].

BIT [4:3] STS-1/STS-3 Time Slot Assignment:

This READ/WRITE bit-field is used to specify which STS-1/STS-3 Time-slot that the XRT86SH328 will fill-in, if it has been configured to operate in the Fractional Bandwidth Mode.

- Valid values to write into these bit-fields are: [0, 0], [0, 1], and [1, 0].

NOTES:

1. These bit-fields are only active if (1) the Telecom Bus Interface has been configured to operate in the STS-3/STS-1/STS-3 Mode, and (2) if the user has configured the XRT86SH328 to operate in the Fractional Bandwidth Mode.

2. If a given XRT86SH328 has been designed into a given STS-3/STS-1/STS-3 application (which involves a total of three XRT86SH328s), for the XRT86SH328 (which has been designated as the Slot Master), the user MUST set these bit-fields to [0, 0].

BIT2 - Telecom Bus Parity Include V1 Signal

BIT 1 - Telecom Bus Interface - Frame Pulse Mode:

This READ/WRITE bit-field is used to configure the STS-1/STS-3 Telecom Bus Interface to operate in the Frame Pulse Mode. If the STS-1/STS-3 Telecom Bus Interface is configured to operate in the Frame Pulse Mode, then all of the following will be true.

- The TxA_C1J1V1_FP output pin will only pulse high coincident to whenever the XRT86SH328 outputs the very first byte of a given STS-1/STS-3 frame via the Transmit STS-1/STS-3 Telecom Bus Interface - Output Data Bus (TxA_D[7:0]).
- The RxD_C1J1V1_FP input pin will accept a pulse, coincident to whenever the very first byte of the incoming STS-1/STS-3 frame is being placed on the Receive STS-1/STS-3 Telecom Bus Interface - Input Data Bus (RxD_D[7:0]).

If the STS-1/STS-3 Telecom Bus Interface is NOT configured to operate in the Frame Pulse Mode, then the Telecom Bus Interface will perform as configured in Bits 0 (Telecom Bus - V1 Signal Support Enable) within this register, and Bit 3 (Telecom Bus J1 Only) within the STS-3/STS-1/STS-3 Telecom Bus Control Register - Byte 0.0 - Configures the STS-1/STS-3 Telecom Bus Interface to NOT operate in the Frame Pulse Mode.1 - Configures the STS-1/STS-3 Telecom Bus Interface to operate in the Frame Pulse Mode.

BIT - 0 - Transmit STS-1/STS-3 Telecom Bus - V1 Pulse Enable:

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 Telecom Bus Interface to pulse the TxA_C1J1V1_FP output pin HIGH coincident to whenever the XRT86SH328 outputs a V1 byte via the Transmit STS-1/STS-3 Telecom Bus Interface - Output Data Bus (TxA_D[7:0]).

- 0 - Configures the Transmit STS-1/STS-3 Telecom Bus Interface to NOT denote the V1 byte via the TxA_C1J1V1_FP output pin.
- 1 - Configures the Transmit STS-1/STS-3 Telecom Bus Interface to denote the V1 byte via the TxA_C1J1V1_FP output pin.

NOTE: This register bit is only active if the XRT86SH328 has been configured to VT/TU map T1/E1 data into SONET/SDH.

TABLE 43: STS-3/STS-1/STS-3 TELECOM BUS CONTROL REGISTER - BYTE 1 (ADDRESS = 0X0036)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Set Telecom Bus to STS-1/STS-3 Mode	Fractional Bandwidth Enable	Slot_0 Master	Slot[1:0]		Telecom Bus Parity Include V1 Signal	Framing Pulse Enable	Telecom Bus - V1 Signa Support Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Set Telecom Bus to STS-1/STS-3 Mode

This READ/WRITE bit-field is used to configure the STS-1/STS-3 Telecom Bus Interface to operate at either the STS-1/STS-3 or STS-3 rates.

- 0 - Configures the Telecom Bus Interface to operate at the STS-3/STS-3 rate.

In this case, the Telecom Bus Interface will operate at a rate of 19.44MHz.

- 1 - Configures the Telecom Bus Interface to operate at the STS-1/STS-3 rate. In this case, the Telecom Bus Interface will operate with a clock rate of 6.48MHz.

NOTE: This bit-field is only active if the XRT86SH328 has been configured to transmit/receive data (on the high-speed side) via the Telecom Bus Interface.

BIT 6 - Fractional Bandwidth Enable

If the XRT86SH328 is configured to transmit/receive data via the Telecom Bus Interface as STS-3/STS-1/STS-3 rates, then this READ/WRITE bit-field is used to configure the XRT86SH328 to operate in the Fractional Bandwidth Mode.

If the user configures the XRT86SH328 to operate in the Fractional Bandwidth Mode, then it will only fill in the STS-1/STS-3 time-slot data (within this outbound STS-3/STS-1/STS-3 data-stream) that pertains to this particular XRT86SH328. The XRT86SH328 will tri-state the Transmit STS-1/STS-3 Telecom bus interface coincident to whenever the other STS-1/STS-3 time-slot data would ordinarily be output via the STS-3/STS-1/STS-3 Telecom Bus Interface.

If the user configures the XRT86SH328 to NOT operate in the Fractional Bandwidth Mode, then it will fill in the STS-1/STS-3 time-slot data (within this outbound STS-3/STS-1/STS-3 data-stream) that pertains to this particular XRT86SH328. The XRT86SH328 will automatically set the bytes (within all of the remaining STS-1/STS-3 time-slots) to 0x00 as it outputs this STS-3/STS-1/STS-3 data-stream via the Transmit STS-3/STS-1/STS-3 Telecom Bus Interface.

- 0 - Configures the XRT86SH328 to NOT operate in the Fractional Bandwidth Mode.
- 1 - Configures the XRT86SH328 to operate in the Fractional Bandwidth Mode.

NOTES:

1. *To design in three (3) XRT86SH328s (into the users system) such that they are sharing the same STS-3/STS-1/STS-3 Telecom Bus, then the user must set this bit-field to 1.*
2. *This bit-field is only active if the Telecom Bus Interface has been configured to operate in the STS-3/STS-1/STS-3 Mode.*

BIT 5 - Slot 0 Master Designate

This READ/WRITE bit-field is used to designate a given XRT86SH328 as being the Slot Master. If the user designates a given XRT86SH328 has being the Slot Master, then this device will be responsible for sourcing the B1 byte, the REI-L and RDI-L indicators (within the outbound STS-3/STS-1/STS-3 data-stream). Additionally, if a given XRT86SH328 has been designated as the Slot Master, then it will be responsible for generating an 8kHz signal via its TxSBFP_IN_OUT input/output pin.

If a given XRT86SH328 is NOT configured to function as the Slot Master, then its TxSBFP_IN_OUT input/output pin will function as an input pin.

- 0 - Configures this particular XRT86SH328 to NOT be the Slot Master.

- 1 - Configures this particular XRT86SH328 to function as the Slot Master.

NOTES:

1. This bit-field is only value if (1) the Telecom Bus Interface is configured to operate in the STS-3/STS-1/STS-3 Mode.

2. The XRT86SH328 has been configured to operate in the Fractional Bandwidth Mode.

3. This particular XRT86SH328 has been assigned the STS-1/STS-3 Time Slot of [0, 0].

BIT [4:3] - STS-1/STS-3 Time Slot Assignmen

This READ/WRITE bit-field is used to specify which STS-1/STS-3 Time-slot that the XRT86SH328 will fill-in, if it has been configured to operate in the Fractional Bandwidth Mode.

Valid values to write into these bit-fields are: [0, 0], [0, 1], and [1, 0].

NOTES:

1. These bit-fields are only active if (1) the Telecom Bus Interface has been configured to operate in the STS-3/STS-1/STS-3 Mode, and (2) if the user has configured the XRT86SH328 to operate in the Fractional Bandwidth Mode.2.

2. If a given XRT86SH328 has been designed into a given STS-3/STS-1/STS-3 application (which involves a total of three XRT86SH328s), for the XRT86SH328 (which has been designated as the Slot Master), the user MUST set these bit-fields to [0, 0].

BIT 2 - Telecom Bus Parity Include V1 Signal

BIT 1 - .Telecom Bus Interface - Frame Pulse Mode

This READ/WRITE bit-field is used to configure the STS-1/STS-3 Telecom Bus Interface to operate in the Frame Pulse Mode. If the user configures the STS-1/STS-3 Telecom Bus Interface to operate in the Frame Pulse Mode, then all of the following will be true.

- The TxA_C1J1V1_FP output pin will only pulse high coincident to whenever the XRT86SH328 outputs the very first byte of a given STS-1/STS-3 frame via the Transmit STS-1/STS-3 Telecom Bus Interface - Output Data Bus (TxA_D[7:0])
- The RxD_C1J1V1_FP input pin will accept a pulse, coincident to whenever the very first byte of the incoming STS-1/STS-3 frame is being placed on the Receive STS-1/STS-3 Telecom Bus Interface - Input Data Bus (RxD_D[7:0]).

If the user does NOT configure the STS-1/STS-3 Telecom Bus Interface to operate in the Frame Pulse Mode, then the Telecom Bus Interface will perform as configured in Bits 0 (Telecom Bus - V1 Signal Support Enable) within this register, and BIT 3 (Telecom Bus J1 Only) within the STS-3/STS-1/STS-3 Telecom Bus Control Register - Byte 0.

- 0 - Configures the STS-1/STS-3 Telecom Bus Interface to NOT operate in the Frame Pulse Mode
- 1 - Configures the STS-1/STS-3 Telecom Bus Interface to operate in the Frame Pulse Mode

BIT 0 - Transmit STS-1/STS-3 Telecom Bus - V1 Pulse Enable

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 Telecom Bus Interface to pulse the TxA_C1J1V1_FP output pin HIGH coincident to whenever the XRT86SH328 outputs a V1 byte via the Transmit STS-1/STS-3 Telecom Bus Interface - Output Data Bus (TxA_D[7:0])

- .0 - Configures the Transmit STS-1/STS-3 Telecom Bus Interface to NOT denote the V1 byte via the TxA_C1J1V1_FP output pin.
- 1 - Configures the Transmit STS-1/STS-3 Telecom Bus Interface to denote the V1 byte via the TxA_C1J1V1_FP output pin.

NOTE: *This register bit is only active if the XRT86SH328 has been configured to VT/TU map T1/E1 data into SONET/SDH.*

TABLE 44: STS-3/STS-1/STS-3 TELECOM BUS CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0037)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Telecom Bus ON	Telecom Bus Disable	Unused	Telecom Bus Parity Type	Telecom Bus J1 Only	Telecom Bus Parity Odd	Telecom Bus Parity Enable	Rephase STS-1
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

BIT 7 - Telecom Bus Enable

This READ/WRITE is used to either enable or disable the 51.84/155.52Mbps Telecom Bus Interface.

- 0 - Telecom Bus Interface is Disabled:STS-1/STS-3 data will output via the STS-1/STS-3 Serial Interface.
- 1 - Telecom Bus Interface is Enabled:In this selection, both the Transmit and Receive STS-1/STS-3 Telecom Bus Interfaces will be enabled.

BIT 6 - Telecom Bus Tri-state

This READ/WRITE bit-field is used to tri-state the Telecom Bus Interface.

- 0 - Telecom Bus Interface is NOT tri-stated.
- 1 - Telecom Bus Interface is tri-stated.

NOTE: *This READ/WRITE bit-field is ignored if the STS-1/STS- 3 Transmit and Receive STS-1/STS-3 Telecom Bus Interfaces are disabled.*

BIT 5 - Unused

BIT 4- Telecom Bus Parity Type

This READ/WRITE bit-field is used to define the parameters, over which Telecom Bus parity will be computed.

- 0 - Parity is computed/verified over the Transmit STS-1/STS-3 and Receive Telecom Bus - data bus pins (e.g., TXA_D[7:0] and RXD_D[7:0]).If the user implements this selection, then the following will happen.
  a. The Transmit STS-1/STS-3 Telecom Bus Interface will compute and output parity (via the TXA_DP output pin) based upon and coincident with the data being output via the TXA_D[7:0] output pins.
  b. The STS-1/STS-3 Receive Telecom Bus Interface will compute and verify the parity data (which is input via the RXD_DP input pin) based upon the data which is being input (and latched) via the RXD_D[7:0] input pins.
- 1 - Parity is computed/verified over the Transmit STS-1/STS-3 and Receive Telecom Bus - data bus pins (e.g., TXA_D[7:0] and RXD_D[7:0]), the C1J1 and PL input/output pins.
- If the user implements this selection, then the following will happen.
  a. The Transmit STS-1/STS-3 Telecom Bus Interface will compute and output parity (via the TXA_DP output) based upon and coincident with (1) the data being output via the TXA_D[7:0] output pins, (2) the state of the TXA_PL output pin, and (3) the state of the TXA_C1J1 output pin.
  b. The Receive STS-1/STS-3 Telecom Bus Interface will compute and verify the parity data (which is input via the RXD_DP input pin) based upon (1) the data which is being input (and latched) via the RXD_D[7:0] input pins, (2) the state of the RXD_PL input pin, and (3) the state of the RXD_C1J1 input pin.

NOTES:

1. *This bit-field is disabled if the STS-1/STS-3 Telecom Bus is disabled.*
2. *The user can configure the STS-1/STS-3 Telecom Bus to compute with either even or odd parity, by writing the appropriate data into BIT 2 (Telecom Bus Parity - Odd), within this register.*

BIT 3 - Telecom Bus - J1 Indicator Only:

This READ/WRITE bit-field is used to configure how the Transmit STS-1/STS-3 and Receive Telecom Bus interface handles the TXA_C1J1 and RXD_C1J1 signals, as described below.

- 0 - C1 and J1 Bytes

This selection configures the following.

a. The Transmit STS-1/STS-3 Telecom Bus to pulse the TXA_C1J1V1_FP output coincident to whenever the C1 and J1 bytes are being output via the TXA_D[7:0] output pins.

b. The STS-1/STS-3 Receive Telecom Bus will expect the RXD_C1J1V1_FP input to pulse high coincident to whenever the C1 and J1 bytes are being sampled via the RXD_D[7:0] input pins.

- 1 - J1 Bytes Only

This selection configures the following.

a. The Transmit STS-1/STS-3 Telecom Bus Interface to only pulse the TXA_C1J1V1_FP output pin coincident to whenever the J1 byte is being output via the TXA_D[7:0] output pins.

NOTE: *The TXA_C1J1V1_FP output pin will NOT be pulsed high whenever the C1 byte is being output via the TXA_D[7:0] output pins.*

b. The STS-1/STS-3 Receive Telecom Bus Interface will expect the RXD_C1J1V1_FP input to only pulse high coincident to whenever the J1 byte is being sampled via the RXD_D[7:0] input pins.

NOTE: *The RXD_C1J1V1_FP input pin will NOT be pulsed high whenever the C1 byte is being input via the RXD_D[7:0] input pins*

BIT 2 - Telecom Bus Parity - ODD Parity Select:

This READ/WRITE bit-field is used to configure the STS-1/STS-3 Telecom Bus Interface to do the following.

a. In the Transmit (Drop) DirectionThe STS-1/STS-3 Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) TxD_D[7:0] output pins, or (2) TxD_D[7:0] output pins, the states of the TxD_PL and TxD_C1J1 output pins (depending upon user setting for BIT 3).

b. In the Receive (Add) DirectionReceive STS-1/STS-3 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) RxA_D[7:0] input pins, or (2) RxA_D[7:0] input pins, the states of the RxA_PL and RxA_C1J1 input pins (depending upon user setting for BIT 3).

- 0 - Configures Transmit (Drop) Telecom Bus to compute EVEN parity and configures the Receive (Add) Telecom Bus to verify EVEN parity.

- 1 - Configures Transmit (Drop) Telecom Bus to compute ODD parity and configures the Receive (Add) Telecom Bus to verify ODD parity.

BIT 1 - Telecom Bus Parity Enable

This READ/WRITE bit-field is used to either enable or disable parity calculation and placement via the TxA_DP output pin. This bit field also is used to enable or disable parity verification by the Receive Telecom Bus.

- 0 - Disables Parity Calculation (on the Transmit Telecom Bus) and Disables Parity Verification (on the Receive Telecom Bus.

- 1 - Enables Parity Calculation and Verification

BIT 0 - Telecom Bus - Rephase Enable

This READ/WRITE bit-field is used to configure the Receive STS-1/STS-3 Telecom Bus to operate in either the Rephase ON or Rephase OFF Modes.

If the user configures the Receive STS-1/STS-3 Telecom Bus Interface to operate on the Rephase ON Mode, then the Receive STS-1/STS-3/STS-1/STS-3 TOH/POH Processor blocks will internally compute the Pointer Bytes, based upon the data that it receives via the RxD_D[7:0] input pins.

If the user configures the Receive STS-1/STS-3 Telecom Bus Interface to operate in the Rephase OFF Mode, then the Receive STS-1/STS-3/STS-1/STS-3 TOH/POH Processor blocks will NOT internally compute the Pointer Bytes, based upon the data that it receives via the RxD_D[7:0] input pins. In this case, the Voyager device will rely upon the signaling via the Telecom Bus Interface pins (e.g., via the RxD_PL and RxD_C1J1V1_FP pins) in order to compute these pointer bytes.

NOTE: *If the Receive STS-1/STS-3 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the RxD_C1J1V1_FP input pin), then this feature is unnecessary.*

- 0 - Configures the Telecom Bus Interface to operate in the Rephase OFF Mode.

- 1 - Configures the Telecom Bus Interface to operate in the Rephase ON Mode.

TABLE 45: OPERATION BLOCK - INTERFACE CONTROL REGISTER (ADDRESS = 0X003C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Telecom Bus Parity Error Interrupt Status	Unused			Telecom Bus Parity Error Interrupt Enable
R/O	R/O	R/O	RUR	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT 4- Telecom Bus Interface - Detection of Parity Error Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Receive STS-1/STS-3 Telecom Bus Interface has detected a parity error within the incoming STS-1/STS-3 data-stream since the last read of this register, as described below.

- 0 - Indicates that the Receive STS-1/STS-3 Telecom Bus Interface has NOT detected a parity error since the last read of this register.
- 1 - Indicates that the Receive STS-1/STS-3 Telecom Bus Interface has detected a parity error (and has generated the Detection of Parity Error interrupt) since the last read of this register.

NOTE: *This register bit-field is only active if the XRT86SH328 has been configured to exchange STS-1/STS-3 data via the Telecom Bus Interface.*

BIT [3:1] - Unused

BIT 0 - Telecom Bus Interface - Detection of Parity Error Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Receive STS-1/STS-3 Telecom Bus Interface - Detection of Parity Error interrupt. If this interrupt is enabled, then the Receive STS-1/STS-3 Telecom Bus Interface will generate this interrupt anytime it detects a parity error within the incoming STS-1/STS-3 data-stream.

- 0 - Disables the Receive STS-1/STS-3 Telecom Bus Interface - Detection of Parity Error interrupt.
- 1 - Enables the Receive STS-1/STS-3 Telecom Bus Interface - Detection of Parity Error interrupt.

TABLE 46: OPERATION GENERAL PURPOSE INPUT/OUTPUT REGISTER - BYTE 0 (ADDRESS = 0X0047)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits [7:0] - General Purpose Input/Output Pin # 7 thru 0

The function of this READ/WRITE bit-field depends upon whether the GPIO_[7:0] pins are configured to be an input or an output pin.

If GPIO_[7:0] is configured to be an input pin:

These register bits operates as a READ-ONLY bit-fields that reflects the state of the GPIO_[7:0] input pins.

If the GPIO_[7:0] input pins are pulled to a logic HIGH, then this register bit will be set to 1. Conversely, if the GPIO_7 input pin is pulled to a logic LOW, then this register bit will be set to 0.

If GPIO_[7:0] is configured to be an output pin

Tthe user can control the logic level of GPIO_[7:0] by writing the appropriate value into these bit-fields.

- 0 - Causes the GPIO_[7:0] output pins to be driven LOW.
- 1 - Causes the GPIO_[7:0] output pins to be driven HIGH.

TABLE 47: OPERATION GENERAL PURPOSE INPUT/OUTPUT DIRECTION REGISTER 0 (ADDRESS = 0X004B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIO_DIR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - GPIO_[7:0] Direction Select

These READ/WRITE bit-fields are used to configure the GPIO_[7:0] pins to function as either input or output pins.

- 0 - Configures GPIO_[7:0] to function as input pins.
- 1 - Configures GPIO_[7:0] to function as output pins.

TABLE 48: OPERATION I/O CONTROL REGISTER (ADDRESS = 0X004F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			RxCLK_Select[4:0]				
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT [4:0] - Recovered T1/E1 Clock Select[4:0]

These READ/WRITE bit-fields are used to select any one of 28 T1 or 21 E1 Recovered Clock signals, and do either of the following.· Output a replica of this selected clock signal via the RCLKOUT output pins.· Synthesize a 19.44MHz clock signal (from this selected Recovered T1/E1 Clock) and output this signal via the RCLKOUT output pin.

The relationship between the contents within these bit-fields and the selected channel is tabulated below.

Bit Field Contents

RXCLK_SELECT[4:0]	SELECTED CHANNEL	COMMENT
00000	NONE	RCLKOUT pin is tri-stated
00001	Channel 0	
00010	Channel 1	
00011	Channel 2	
00100	Channel 3	
00101	Channel 4	
00110	Channel 5	
00111	Channel 6	
01000	Channel 7	
01001	Channel 8	
01010	Channel 9	
01011	Channel 10	

Bit Field Contents

RXCLK_SELECT[4:0]	SELECTED CHANNEL	COMMENT
01100	Channel 11	
01101	Channel 12	
01110	Channel 13	
01111	Channel 14	
10000	Channel 15	
10001	Channel 16	
10010	Channel 17	
10011	Channel 18	
10100	Channel 19	
10101	Channel 20	
10110	Channel 21	
10111	Channel 22	
11000	Channel 23	
11001	Channel 24	
11010	Channel 25	
11011	Channel 26	
11100	Channel 27	
11101	NONE	RCLKOUT is an Input pin
11110	NONE	RCLKOUT is an Input Pin
11111	NONE	RCLKOUT is an Input Pin

TABLE 49: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 FRAMER (VT SIDE) BLOCK - BYTE 3 (ADDRESS = 0X0050)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1/E1 Framer VT-Side Channel 27	DS1/E1 Framer VT-Side Channel 26	DS1/E1 Framer VT-Side Channel 25	DS1/E1 Framer VT-Side Channel 24
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:4]- Unused

BIT [3:0] - DS1/E1 Framer Block (VT Side) Channels 27, 26, 25 & 24

These READ-ONLY bit-fields indicate whether or not the DS1/E1 Framer block (on the VT Side) associated with Channel [27:24] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 Framer block sassociated with Channel [27:24] (on the VT Side) does NOT have a

pending interrupt request.

- 1 - Indicates that the DS1/E1 Framer blocks associated with Channel [27:24] (on the VT side) DOES have a pending interrupt request.

TABLE 50: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 FRAMER (VT SIDE) BLOCK - BYTE 3 (ADDRESS = 0X0051)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 Framer VT-Side Channel 23	DS1/E1 Framer VT-Side Channel 22	DS1/E1 Framer VT-Side Channel 21	DS1/E1 Framer VT-Side Channel 20	DS1/E1 Framer VT-Side Channel 19	DS1/E1 Framer VT-Side Channel 18	DS1/E1 Framer VT-Side Channel 17	DS1/E1 Framer VT-Side Channel 16
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - DS1/E1 Framer Block (VT Side) Channels [23:16]

These READ-ONLY bit-field indicates whether or not the DS1/E1 Framer block (on the VT Side) associated with Channel [23:16] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 Framer blocks associated with Channel [23:16] (on the VT Side) does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 Framer blocks associated with Channel [23:16] (on the VT side) DOES have a pending interrupt request.

TABLE 51: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 FRAMER (VT SIDE) BLOCK - BYTE 3 (ADDRESS = 0X0052)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 Framer VT-Side Channel 15	DS1/E1 Framer VT-Side Channel 14	DS1/E1 Framer VT-Side Channel 13	DS1/E1 Framer VT-Side Channel 12	DS1/E1 Framer VT-Side Channel 11	DS1/E1 Framer VT-Side Channel 10	DS1/E1 Framer VT-Side Channel 9	DS1/E1 Framer VT-Side Channel 8
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - DS1/E1 Framer Block (VT Side) Channels [15:8]

These READ-ONLY bit-field indicates whether or not the DS1/E1 Framer block (on the VT Side) associated with Channel [15:8] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 Framer blocks associated with Channel [15:8] (on the VT Side) does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 Framer blocks associated with Channel [15:8] (on the VT side) DOES have a pending interrupt request.

TABLE 52: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 FRAMER (VT SIDE) BLOCK - BYTE 3 (ADDRESS = 0X0053)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 Framer VT-Side Channel 7	DS1/E1 Framer VT-Side Channel 6	DS1/E1 Framer VT-Side Channel 5	DS1/E1 Framer VT-Side Channel 4	DS1/E1 Framer VT-Side Channel 3	DS1/E1 Framer VT-Side Channel 2	DS1/E1 Framer VT-Side Channel 1	DS1/E1 Framer VT-Side Channel 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - DS1/E1 Framer Block (VT Side) Channels [7:0]

These READ-ONLY bit-field indicates whether or not the DS1/E1 Framer block (on the VT Side) associated with Channel [7:0] has a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 Framer blocks associated with Channel [7:0] (on the VT Side) does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 Framer blocks associated with Channel [7:0] (on the VT side) DOES have a pending interrupt request.

TABLE 53: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 FRAMER (M13 SIDE) BLOCK - BYTE 3 (ADDRESS = 0X0054)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1/E1 Framer M13-Side Channel 27	DS1/E1 Framer M13-Side Channel 26	DS1/E1 Framer M13-Side Channel 25	DS1/E1 Framer M13-Side Channel 24
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - BIT 4 - Unused

BIT [3:0] - DS1/E1 Framer Block (M13 Side) Channels [27:24]

These READ-ONLY bit-field indicate whether or not the DS1/E1 Framer block (on the M13 Side) associated with Channel [27:24] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 Framer block associated with Channel [27:24] (on the M13 Side) does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 Framer block associated with Channel [27:24] (on the M13 side) DOES have a pending interrupt request.

TABLE 54: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 FRAMER (M13 SIDE) BLOCK - BYTE 3 (ADDRESS = 0X0055)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 Framer M13-Side Channel 23	DS1/E1 Framer M13-Side Channel 22	DS1/E1 Framer M13-Side Channel 21	DS1/E1 Framer M13-Side Channel 20	DS1/E1 Framer M13-Side Channel 19	DS1/E1 Framer M13-Side Channel 18	DS1/E1 Framer M13-Side Channel 17	DS1/E1 Framer M13-Side Channel 16
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - DS1/E1 Framer Block (M13 Side) Channel [23:16]

These READ-ONLY bit-fields indicates whether or not the DS1/E1 Framer block (on the M13 Side) associated with Channel [23:16] has a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 Framer block associated with Channel [23:16] (on the M13 Side) does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 Framer block associated with Channel [23:16] (on the M13 side) DOES have a pending interrupt request.

TABLE 55: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 FRAMER (M13 SIDE) BLOCK - BYTE 3 (ADDRESS = 0X0056)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 Framer M13-Side Channel 15	DS1/E1 Framer M13-Side Channel 14	DS1/E1 Framer M13-Side Channel 13	DS1/E1 Framer M13-Side Channel 12	DS1/E1 Framer M13-Side Channel 11	DS1/E1 Framer M13-Side Channel 10	DS1/E1 Framer M13-Side Channel 9	DS1/E1 Framer M13-Side Channel 8
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - DS1/E1 Framer Block (M13 Side) Channels [15:8]

These READ-ONLY bit-fields indicate whether or not the DS1/E1 Framer block (on the M13 Side) associated with Channels [15:8] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 Framer block associated with Channel [15:8] (on the M13 Side) does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 Framer block associated with Channel [15:8] (on the M13 side) DOES have a pending interrupt request.

TABLE 56: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 FRAMER (M13 SIDE) BLOCK - BYTE 3 (ADDRESS = 0X0057)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 Framer M13-Side Chan-nel 7	DS1/E1 Framer M13-Side Chan-nel 6	DS1/E1 Framer M13-Side Chan-nel 5	DS1/E1 Framer M13-Side Chan-nel 4	DS1/E1 Framer M13-Side Chan-nel 3	DS1/E1 Framer M13-Side Chan-nel 2	DS1/E1 Framer M13-Side Chan-nel 1	DS1/E1 Framer M13-Side Chan-nel 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - DS1/E1 Framer Block (M13 Side) Channels [7:0]

These READ-ONLY bit-fields indicate whether or not the DS1/E1 Framer block (on the M13 Side) associated with Channels [7:0] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 Framer block associated with Channel [7:0] (on the M13 Side) does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 Framer block associated with Channel [7:0] (on the M13 side) DOES have a pending interrupt request.

TABLE 57: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 LIU BLOCK - BYTE 3 (ADDRESS = 0X0058)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				DS1/E1 LIU Channel 27	DS1/E1 LIU Channel 26	DS1/E1 LIU Channel 25	DS1/E1 LIU Channel 24
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT [3:0] - DS1/E1 LIU Block Channels [27:24]

These READ-ONLY bit-fields indicate whether or not the DS1/E1 LIU block associated with Channels [27:24] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 LIU block associated with Channel [27:24] does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 LIU block associated with Channel [27:24] DOES have a pending interrupt request.

TABLE 58: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 LIU BLOCK - BYTE 3 (ADDRESS = 0X0059)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 LIU Channel 23	DS1/E1 LIU Channel 22	DS1/E1 LIU Channel 21	DS1/E1 LIU Channel 20	DS1/E1 LIU Channel 19	DS1/E1 LIU Channel 18	DS1/E1 LIU Channel 17	DS1/E1 LIU Channel 16
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit[7:0] - DS1/E1 LIU Block Channels [23:16]

These READ-ONLY bit-fields indicate whether or not the DS1/E1 LIU block associated with Channels [23:16] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 LIU block associated with Channel [23:16] does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 LIU block associated with Channel [23:16] DOES have a pending interrupt request.

TABLE 59: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 LIU BLOCK - BYTE 3 (ADDRESS = 0X005A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 LIU Channel 15	DS1/E1 LIU Channel 14	DS1/E1 LIU Channel 13	DS1/E1 LIU Channel 12	DS1/E1 LIU Channel 11	DS1/E1 LIU Channel 10	DS1/E1 LIU Channel 9	DS1/E1 LIU Channel 8
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit [7:0] - DS1/E1 LIU Block Channel [15:8]

These READ-ONLY bit-fields indicate whether or not the DS1/E1 LIU block associated with Channels [15:8] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 LIU block associated with Channel [15:8] does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 LIU block associated with Channel [15:8] DOES have a pending interrupt request.

TABLE 60: CHANNEL INTERRUPT INDICATION REGISTER - DS1/E1 LIU BLOCK - BYTE 3 (ADDRESS = 0X005B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 LIU Channel 7	DS1/E1 LIU Channel 6	DS1/E1 LIU Channel 5	DS1/E1 LIU Channel 4	DS1/E1 LIU Channel 3	DS1/E1 LIU Channel 2	DS1/E1 LIU Channel 1	DS1/E1 LIU Channel 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - DS1/E1 LIU Block Channels [7:0]

These READ-ONLY bit-fields indicate whether or not the DS1/E1 LIU block associated with Channels [7:0] have a pending Interrupt Request.

- 0 - Indicates that the DS1/E1 LIU block associated with Channel [7:0] does NOT have a pending interrupt request.
- 1 - Indicates that the DS1/E1 LIU block associated with Channel [7:0] DOES have a pending interrupt request.

TABLE 61: CHANNEL INTERRUPT INDICATION REGISTER - VT-MAPPER BLOCK - BYTE 3 (ADDRESS = 0X005C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				VT Mapper Block Channel 27	VT Mapper Block Channel 26	VT Mapper Block Channel 25	VT Mapper Block Channel 24
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

Bit [3:0] - VT-Mapper Block Channels [27:24]

These READ-ONLY bit-fields indicate whether or not the VT-Mapper block associated with Channels [27:24] have a pending Interrupt Request.

- 0 - Indicates that the VT-Mapper block associated with Channel [27:24] does NOT have a pending interrupt request.
- 1 - Indicates that the VT-Mapper block associated with Channel [27:24] DOES have a pending interrupt request.

TABLE 62: CHANNEL INTERRUPT INDICATION REGISTER - VT-MAPPER BLOCK - BYTE 3 (ADDRESS = 0X005D)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT-Mapper Channel 23	VT-Mapper Channel 22	VT-Mapper Channel 21	VT-Mapper Channel 20	VT-Mapper Channel 19	VT-Mapper Channel 18	VT-Mapper Channel 17	VT-Mapper Channel 16
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - VT-Mapper Block Channels [23:16]

These READ-ONLY bit-fields indicate whether or not the VT-Mapper block associated with Channels [23:16] have a pending Interrupt Request.

- 0 - Indicates that the VT-Mapper block associated with Channel [23:16] does NOT have a pending interrupt request.
- 1 - Indicates that the VT-Mapper block associated with Channel [23:16] DOES have a pending interrupt request.

TABLE 63: CHANNEL INTERRUPT INDICATION REGISTER - VT-MAPPER BLOCK - BYTE 3 (ADDRESS = 0X005E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT-Mapper Channel 15	VT-Mapper Channel 14	VT-Mapper Channel 13	VT-Mapper Channel 12	VT-Mapper Channel 11	VT-Mapper Channel 10	VT-Mapper Channel 9	VT-Mapper Channel 8
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - VT-Mapper Block Channels [15:8]

These READ-ONLY bit-fields indicate whether or not the VT-Mapper block associated with Channels [15:8] have a pending Interrupt Request.

- 0 - Indicates that the VT-Mapper block associated with Channel [15:8] does NOT have a pending interrupt request.
- 1 - Indicates that the VT-Mapper block associated with Channel [15:8] DOES have a pending interrupt request.

TABLE 64: CHANNEL INTERRUPT INDICATION REGISTER - VT-MAPPER BLOCK - BYTE 3 (ADDRESS = 0X005F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT-Mapper Channel 7	VT-Mapper Channel 6	VT-Mapper Channel 5	VT-Mapper Channel 4	VT-Mapper Channel 3	VT-Mapper Channel 2	VT-Mapper Channel 1	VT-Mapper Channel 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit[7:0] - VT-Mapper Block Channels [7:0]

These READ-ONLY bit-fields indicate whether or not the VT-Mapper block associated with Channels [7:0] have a pending Interrupt Request.

- 0 - Indicates that the VT-Mapper block associated with Channel [7:0] does NOT have a pending interrupt request.
- 1 - Indicates that the VT-Mapper block associated with Channel [7:0] DOES have a pending interrupt request.

2.2 LIU COMMON CONTROL REGISTERS

TABLE 65: LIU COMMON CONTROL REGISTER 0 (ADDRESS = 0X0100)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	ATAOS	Reserved				TCLKCNTL	LIU Soft-ware RESET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved:

BIT 6 - ATAOS: Automatic Transmit All Ones Upon RLOS Condition

If ATAOS is selected, an all ones pattern will be transmitted on any channel that experiences an RLOS condition. If an RLOS condition does not occur, TAOS will remain inactive.

0 = Disabled

1 = Enabled

Bits [5:2] - Reserved:

BIT 1 - TCLKCNTL

If TCLKCNTL is selected, and if the transmit clock to the DS-1 framer is missing, Low, or High, then the transmitter outputs to the line interface will send an All Ones Signal.

0 = Disabled

1 = Enabled

BIT 0 - LIU Software RESET:

Writing a 1 to this bit for more than 10µS initiates a device reset for all internal circuits except the microprocessor register bits. To reset the registers to their default setting, use the Hardware Reset pin (See the pin description for more details)

0 = Disabled

1 = Enabled

TABLE 66: LIU COMMON CONTROL REGISTER 1 (ADDRESS = 0X0101)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVB_OF	PLL19_Dis	Reserved	Slicer Level Select[1:0]	RXMUTE	EXLOS	ICT	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Line Code Violation / Counter Overflow Monitor Select

This bit is used to select the monitoring activity between the LCV and the counter overflow status. When the 16-bit LCV counter saturates, the counter overflow condition is activated. By default, the LCV activity is monitored by bit D4 in register 0xN005, where N is equal to the channel number.

- 0 - Monitoring LCV
- 1 - Monitoring the counter overflow status

BIT 6 - PLL 19.44MHz Disable

This bit is used in conjunction with the DS-1/E1 recovered clock to synchronize to a 19.44MHz clock source. If this bit is set High, one of the 28 channel recovered line clocks, or an external line clock and be used to provide this synchronization.

- 0 - Disabled
- 1 - Enabled

BIT 5 - Reserved

BIT [4:3] - Slicer Level Select

These bits are to used to select the amplitude level that is used by the receive line interface to determine whether the input data is High or Low.

00 - 50%

01 - 45%

10 - 55%

11 - 68%

BIT 2 - RxMUTE

This bit is used to force the receive DS-1/E1 signals Low to prevent chattering any time that the DS-1/E1 receiver inputs at Rtip/Rring experience an RLOS condition.

- 0 - Disabled
- 1 - Enabled

BIT 1 - EXLOS

The number of zeros required to declare a Digital Loss of Signal is extended to 4,096.

- 0 - Normal RLOS operation
- 1 - EXLOS enabled

BIT 0 - In Circuit Testing

For Internal use only. This bit should be set to Low.

TABLE 67: LIU COMMON CONTROL REGISTER 2 (ADDRESS = 0X0102)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				CLKSEL[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Reserved

BIT [3:0] - Input Clock Selection

These bits are used to select the frequency of the input clock source to the PLL. Any state not listed is reserved.

0000 = 2.048 MHz

0001 = 1.544 MHz

1000 = 4.096 MHz

1001 = 3.088 MHz

1010 = 8.192 MHz

1011 = 6.176 MHz

1100 = 16.384 MHz

1101 = 12.352 MHz

1110 = 2.048 MHz

1111 = 1.544 MHz

TABLE 68: LIU COMMON CONTROL REGISTER 3 (ADDRESS = 0X0103)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global Interrupt Status Channel 6	DS1/E1 LIU Global Interrupt Status Channel 5	DS1/E1 LIU Global Interrupt Status Channel 4	DS1/E1 LIU Global Interrupt Status Channel 3	DS1/E1 LIU Global Interrupt Status Channel 2	DS1/E1 LIU Global Interrupt Status Channel 1	DS1/E1 LIU Global Interrupt Status Channel 0
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 0 to 6

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 69: LIU COMMON CONTROL REGISTER 4 (ADDRESS = 0X0104)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global nterrupt Status Channel 13	DS1/E1 LIU Global nterrupt Status Channel 12	DS1/E1 LIU Global nterrupt Status Channel 11	DS1/E1 LIU Global nterrupt Status Channel 10	DS1/E1 LIU Global nterrupt Status Channel 9	DS1/E1 LIU Global nterrupt Status Channel 8	DS1/E1 LIU Global nterrupt Status Channel 7
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 7 to 13

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 70: LIU COMMON CONTROL REGISTER 5 (ADDRESS = 0X0105)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global nterrupt Status Channel 20	DS1/E1 LIU Global nterrupt Status Channel 19	DS1/E1 LIU Global nterrupt Status Channel 18	DS1/E1 LIU Global nterrupt Status Channel 17	DS1/E1 LIU Global nterrupt Status Channel 16	DS1/E1 LIU Global nterrupt Status Channel 15	DS1/E1 LIU Global nterrupt Status Channel 14
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 14 to 20

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 71: LIU COMMON CONTROL REGISTER 6 (ADDRESS = 0X0106)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global Interrupt Status Channel 27	DS1/E1 LIU Global Interrupt Status Channel 26	DS1/E1 LIU Global Interrupt Status Channel 25	DS1/E1 LIU Global Interrupt Status Channel 24	DS1/E1 LIU Global Interrupt Status Channel 23	DS1/E1 LIU Global Interrupt Status Channel 22	DS1/E1 LIU Global Interrupt Status Channel 21
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 21 to 27

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register

is read back, these bit fields will automatically return Low.

2.3 RECEIVE STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

The register map for the Receive STS-1/STS-3 TOH Processor block is presented in the Table below. Additionally, a detailed description of each of the Receive STS-1/STS-3 TOH Processor Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328, with the Receive STS-1/STS-3 TOH Processor Block highlighted is presented below in Figure 3.

FIGURE 3. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WITH THE RECEIVE STS-1/STS-3 TOH PROCESSOR BLOCK HIGHLIGHTED

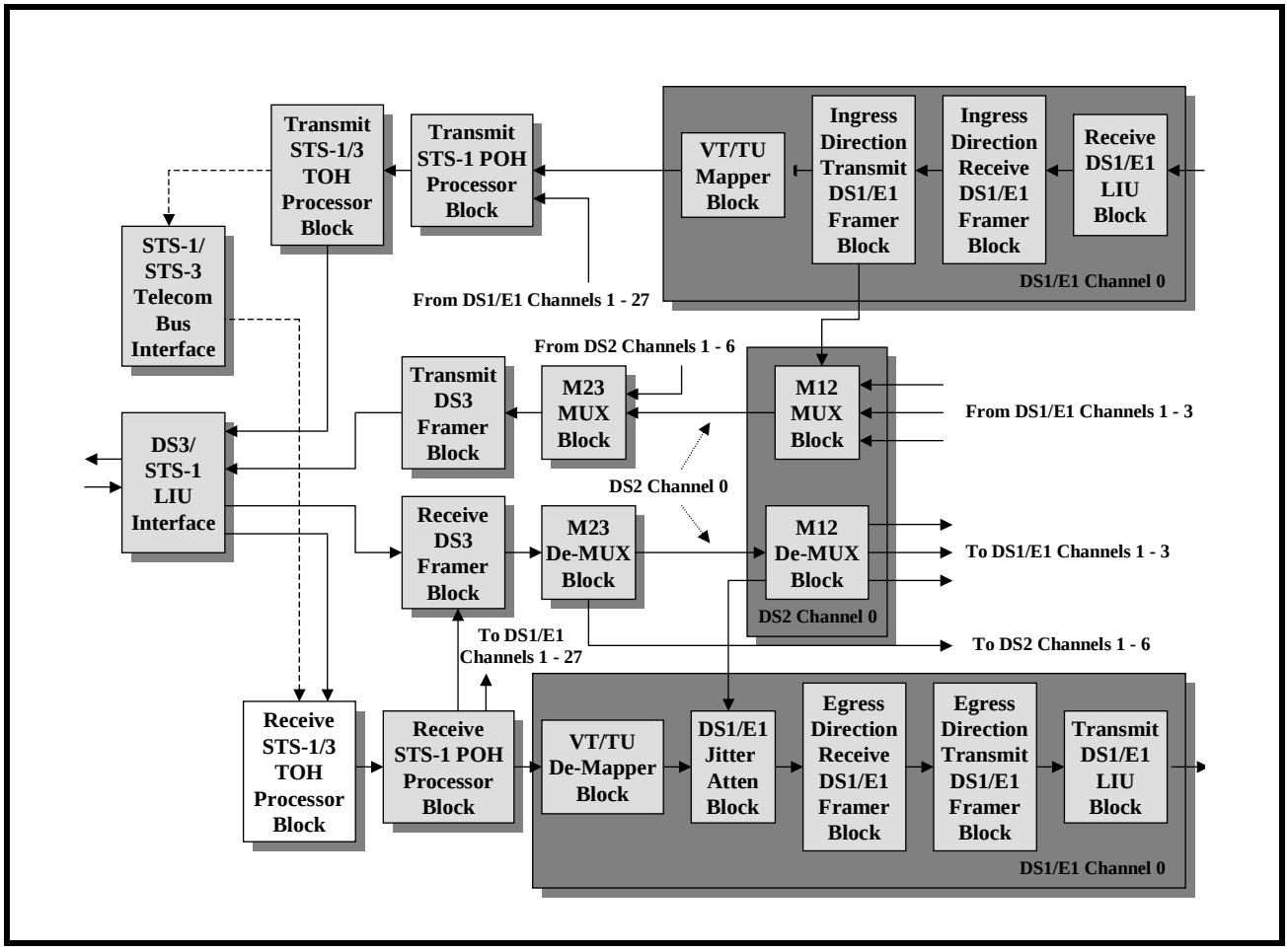


TABLE 72: RECEIVE STS-1/STS-3 TRANSPORT CONTROL REGISTER - BYTE 1 (ADDRESS LOCATION = 0X0202)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Sync on B1	Unused	No OH Extract
R/O	R/O	R/O	R/O	R/O	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Unused

BIT 2 - Sync on B1

BIT 1 - Unused

BIT 0 - No Overhead Data Extract

TABLE 73: RECEIVE STS-1/STS-3 TRANSPORT CONTROL REGISTER - BYTE 0 (ADDRESS LOCATION = 0X0203)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	SF Defect Condition Detect Enable	SD Defect Condition Detect Enable	Descramble-Disable	Unused	REI-LError Type	B2 ErrorType	B1 Error Type
R/O	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT 6 - Signal Failure (SF) Defect Condition Detect Enable

This READ/WRITE bit-field is used to enable or disable SF Defect Detection and Declaration by the Receive STS-1/STS-3 TOH Processor block.

- 0 - Configures the Receive STS-1/STS-3 TOH Processor block to NOT declare nor clear the SF defect condition per the user-specified SF defect declaration and clearance criteria.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to declare and clear the SF defect condition per the user-specified SF defect declaration and clearance criteria.

BIT 5 - Signal Degrade (SD) Defect Condition Detect Enable

This READ/WRITE bit-field is used to enable or disable SD Detection and Declaration by the Receive STS-1/STS-3 TOH Processor block.

- 0 - Configures the Receive STS-1/STS-3 TOH Processor block to NOT declare nor clear the SD defect condition per the user-specified SD defect declaration and clearance criteria.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to declare and clear the SD defect condition per the user-specified SD defect declaration and clearance criteria.

BIT 4 - De-Scramble Disable

This READ/WRITE bit-field is used to either enable or disable de-scrambling by the Receive STS-1/STS-3 TOH Processor block, associated with channel N.

- 0 - De-Scrambling is enabled.
- 1 - De-Scrambling is disabled.

BIT 3 - Unused

BIT 2 - REI-L Error Type

This READ/WRITE bit-field is used to specify how the Receive STS-1/STS-3 TOH Processor block will count (or tally) REI-L events, for Performance Monitoring purposes. The user can configure the Receive STS-1/STS-3 TOH Processor block to increment REI-L events on either a per-bit or per-frame basis.

If the user configures the Receive STS-1/STS-3 TOH Processor block to increment REI-L events on a per-bit basis, then it will incrememt the Receive STS-1/STS-3 Transport REI-L Error Count register by the value of the lower nibble within the M0/M1 byte of the incoming STS-1/STS-3 data-stream.

If the user configures the Receive STS-1/STS-3 TOH Processor block to increment REI-L events on a per-frame basis, then it will increment the Receive STS-1/STS-3 Transport REI-L Error Count register each time it receives an STS-1/STS-3 or STS-3 frame, in which the lower nibble of the M0/M1 byte is set to a non-zero value.

- 0 - Configures the Receive STS-1/STS-3 TOH Processor block to count or tally REI-L events on a per-bit basis.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to count or tally REI-L events on a per-frame basis.

BIT 1 - B2 Error Type

This READ/WRITE bit-field is used to specify how the Receive STS-1/STS-3 TOH Processor block will count (or tally) B2 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-1/STS-3 TOH Processor block to increment B2 byte errors on either a per-bit or a per-frame basis.

If the user configures the Receive STS-1/STS-3 TOH Processor block to increment B2 byte errors on a per-bit basis, then it will increment the Receive Transport B2 Byte Error Count register by the number of bits (within the B2 byte value) that is in error.

If the user configures the Receive STS-1/STS-3 TOH Processor block to increment B2 byte errors on a per-frame basis, then it will increment the Receive Transport B2 Byte Error Count register each time it receives an STS-1/STS-3 frame that contains an erred B2 byte.

- 0 - Configures the Receive STS-1/STS-3 TOH Processor block to count B2 byte errors on a per-bit basis.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to count B2 byte errors on a per-frame basis.

BIT 0 - B1 Error Type

This READ/WRITE bit-field is used to specify how the Receive STS-1/STS-3 TOH Processor block will count (or tally) B1 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-1/STS-3 TOH Processor block to increment B1 byte errors on either a per-bit or per-frame basis.

If the user configures the Receive STS-1/STS-3 TOH Processor block to increment B1 byte errors on a per-bit basis, then it will increment the Receive Transport B1 Byte Error Count register by the number of bits (within the B1 byte value) that is in error.

If the user configures the Receive STS-1/STS-3 TOH Processor block to increment B1 byte errors on a per-frame basis, then it will increment the Receive Transport B1 Byte Error Count Register each time it receives an STS-1/STS-3 frame that contains an erred B1 byte.

- 0 - Configures the Receive STS-1/STS-3 TOH Processor block to count B1 byte errors on a per-bit basis.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to count B1 byte errors on a per-frame basis.

TABLE 74: RECEIVE STS-1/STS-3 TRANSPORT STATUS REGISTER - BYTE 1 (ADDRESS LOCATION= 0X0206)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Section Trace Message (J0) Mismatch Defect Declared	Section Trace Message (J0) Unstable Defect Declared	AIS-L Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:3] - Unused

BIT 2 - Section Trace Message Mismatch Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the Section Trace Mismatch defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the Section Trace Message Mismatch defect condition, whenever it accepts a Section Trace Message (via the J0 byte, within the incoming STS-1/STS-3 data-stream) that differs from the Expected Section Trace Message.

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the Section Trace Message Mismatch Defect Condition.
- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the Section Trace Message Mismatch Defect Condition.

BIT 1 - Section Trace Message Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the Section Trace Message Unstable Defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the Section Trace Message Unstable defect condition, whenever the "Section Trace Message Unstable" counter reaches the value 8. The Receive STS-1/STS-3 TOH Processor block will increment the "Section Trace Message Unstable" counter for each time that it receives a Section Trace message that differs from the "Expected Section Trace Message". The Receive STS-1/STS-3 TOH Processor block will clear the "Section Trace Message Unstable" counter to "0" whenever it has received a given Section Trace Message 3 (or 5) consecutive times

NOTE: *The Receive STS-1/STS-3 TOH Processor block will clear the "Section Trace Message Unstable" defect condition whenever it receives a given Section Trace Message 3 (or 5) consecutive times".*

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the Section Trace

Message Unstable defect condition.

- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the Section Trace Message Unstable defect condition

BIT 0 - AIS-L Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the AIS-L (Line AIS) defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the AIS-L defect condition within the incoming STS-1/STS-3data stream if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) are set to the value [1, 1, 1] for five consecutive STS-1/STS-3frames.

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the AIS-L defect condition.
- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the AIS-L defect condition.

TABLE 75: RECEIVE STS-1/STS-3 TRANSPORT STATUS REGISTER - BYTE 0 (ADDRESS LOCATION = 0X0207)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDI-L Defect Declared	S1 Byte Unstable Defect Declared	K1, K2 Byte Unstable Defect Declared	SF Defect Declared	SD Defect Declared	LOFDefect Detected	SEFDefect Declared	LOSDefect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - RDI-L Defect Declared Indicator

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is detecting the RDI-L (Line-Remote Defect Indicator) defect condition, within the incoming STS-1/STS-3 signal. The Receive STS-1/STS-3 TOH Processor block will declare the RDI-L defect condition whenever bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the 1, 1, 0 pattern in 5 consecutive incoming STS-1/STS-3 or STS-3 frames.

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the AIS-L defect condition.
- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the AIS-L defect condition..

BIT 6 - S1 Byte Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the S1 Byte Unstable defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the S1 Byte Unstable defect condition whenever the S1 Byte Unstable Counter reaches the value 32. The Receive STS-1/STS-3 TOH Processor block will increment the "S1 Byte Unstable Counter" each time that the it receives an STS-1/STS-3 or STS-3 frame that contains an S1 byte that differs from the previously received S1 byte. The Receive STS-1/STS-3 TOH Processor block will clear the "S1 Byte Unstable Counter" to "0" when the same S1 byte is received for 8 consecutive STS-1/STS-3 frames.

NOTE: *The Receive STS-1/STS-3 TOH Processor block will clear the "S1 Byte Unstable" defect whenever it receives a given S1 byte, in 8 consecutive STS-1/STS-3 frames.*

1. 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the S1 Byte Unstable Defect Condition.
1. 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the S1 Byte Unstable Defect Condition.

BIT 5 - K1, K2 Byte Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the K1, K2 Byte Unstable defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the K1, K2 Byte Unstable defect condition whenever it fails to receive the same set of K1, K2 bytes, in 12 consecutive incoming STS-1/STS-3 frames. The Receive STS-1/STS-3 TOH Processor block will clear the "K1, K2 Byte Unstable" defect whenever it has received a given set of K1, K2 byte values within three consecutive incoming STS-1/STS-3 frames.

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the "K1, K2 Byte

Unstable Defect" Condition.

- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the "K1, K2 Byte Unstable Defect" Condition.

BIT 4 - SF (Signal Failure) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the SF defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the SF defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain user-specified B2 Byte Error threshold.

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the SF Defect condition.

This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SF Defect Declaration" threshold.

- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the SF Defect condition.

This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SF Defect Declaration" threshold

BIT 3 - SD (Signal Degrade) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the SD defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the SD defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain user-specified B2 Byte Error threshold.

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the SD Defect condition.

This bit is set to 0 when the number of B2 errors (accumulated over a given interval of time) does not exceed the SD Declaration threshold.

- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the SD Defect condition.

This bit is set to 1 when the number of B2 errors (accumulated over a given interval of time) does exceed the SD Defect Declaration threshold.

BIT 2 - LOF (Loss of Frame) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the LOF defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the LOF defect condition if it has been declaring the SEF condition for 24 consecutive STS-1/STS-3 frame periods. Once the Receive STS-1/STS-3 TOH Processor block has declared the LOF defect condition, then the Receive STS-1/STS-3 TOH Processor block will clear the LOF defect if it has not been declaring the SEF condition for 3ms (or 24 consecutive STS-1/STS-3 frame periods).

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the LOF defect condition.
- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the LOF defect condition.

BIT 1 - SEF (Severely Errored Frame) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the SEF defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the SEF defect condition if it detects Framing Alignment byte errors in four consecutive STS-1/STS-3 frames. Once the Receive TOH Processor block declares the SEF defect condition, the Receive STS-1/STS-3 TOH Processor block will then clear the SEF defect condition if it detects two consecutive STS-1/STS-3 frames with un-erred framing alignment bytes. If the Receive TOH Processor block declares the SEF defect condition for 24 consecutive STS-1/STS-3 frame periods, then it will declare the LOF defect condition.

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the SEF defect condition.
- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the SEF defect condition.

BIT 0 - LOS (Loss of Signal) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the LOS (Loss of Signal) defect condition. The Receive STS-1/STS-3 TOH Processor block will declare the LOS defect condition if it detects LOS_THRESHOLD[15:0] consecutive All Zero bytes in the incoming STS-1/STS-3 data stream.

NOTE: *The user can set the LOS_THRESHOLD[15:0] value by writing the appropriate data into the Receive STS-1/STS-3 Transport - LOS Threshold Value Register (Address Location= 0x022E and 0x022F).*

- 0 - Indicates that the Receive STS-1/STS-3 TOH Processor block is NOT currently declaring the LOS defect condition.
- 1 - Indicates that the Receive STS-1/STS-3 TOH Processor block is currently declaring the LOS defect condition.

TABLE 76: RECEIVE STS-1/STS-3 TRANSPORT INTERRUPT STATUS REGISTER - BYTE 2 (ADDRESS LOCATION= 0X0209)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-LDefect Condition Interrupt Status	Change of RDI-L Defect Condition Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7: 2] - Unused

BIT 1 - Change of AIS-L (Line AIS) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of AIS-L Defect Condition interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following occurrences.· Whenever the Receive STS-1/STS-3 TOH Processor block declares the AIS-L defect condition.· Whenever the Receive STS-1/STS-3 TOH Processor block clears the AIS-L defect condition.

- 0 - Indicates that the Change of AIS-L Defect Condition interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change of AIS-L Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the current state of the AIS-L defect condition by reading the contents of BIT 0 (AIS-L Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 1 (Address Location= 0x0206).*

BIT 0 - Change of RDI-L (Line - Remote Defect Indicator) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of RDI-L Defect Condition interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following occurrences.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the RDI-L defect condition.·
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the RDI-L defect condition.

- 0 - Indicates that the Change of RDI-L Defect Condition interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change of RDI-L Defect Condition interrupt has occurred since the last read of this register.Note:

NOTE: *The user can obtain the current state of the RDI-L defect condition by reading out the state of BIT7 (RDI-L Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 0 (Address Location= 0x0207).*

TABLE 77: RECEIVE STS-1/STS-3 TRANSPORT INTERRUPT STATUS REGISTER - BYTE 1 (ADDRESS LOCATION= 0X020A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 ByteInterrupt Status	Change in S1 Byte UnstableDefect ConditionInterrupt Status	Change in Section Trace Message Unstable Defect Condition Interrupt Status	New Section Trace Message Interrupt Status	Change in Section Trace Message MismatchDefect Declared Interrupt Status	Unused	Change in K1, K2 Byte Unstable Defect Condtion Interrupt Status	NEW K1K2 Byte Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - New S1 Byte Value Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New S1 Byte Value Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate the New S1 Byte Value Interrupt, anytime it has accepted a new S1 byte, from the incoming STS-1/STS-3 data-stream.

- 0 - Indicates that the New S1 Byte Value Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New S1 Byte Value interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the value for this most recently accepted value of the S1 byte by reading the Receive STS-1/STS-3 Transport S1 Byte Value register (Address Location= 0x0227).*

BIT 6 - Change in S1 Byte Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in S1 Byte Unstable Defect Condition Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the S1 Byte Unstable defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the S1 Byte Unstable defect condition.

- 0 - Indicates that the Change in S1 Byte Unstable Defect Condition Interrupt has occurred since the last read of this register.
- 1 - Indicates that the Change in S1 Byte Unstable Defect Condition Interrupt has not occurred since the last read of this register.

NOTE: *The user can obtain the current S1 Byte Unstable Defect condition by reading the contents of BIT6 (S1 Byte Unstable Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 5 - Change in Section Trace Message Unstable Defect condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in Section Trace Message Unstable defect condition interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the Section Trace Message Unstable defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clear the Section Trace Message Unstable defect condition.

- Indicates that the Change in Section Trace Message Unstable defect condition interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change in Section Trace Message Unstable defect condition interrupt has occurred since the last read of this register.

BIT 4 - New Section Trace Message Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New Section Trace Message interrupt has occurred since

the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt anytime it has accepted a new Section Trace Message within the incoming STS-1/STS-3 data-stream.

- 0 - Indicates that the New Section Trace Message Interrupt has not occurred since the last read of this register.
- 1 - Indicates that the New Section Trace Message Interrupt has occurred since the last read of this register.

NOTE: *The user can read out the contents of the Receive Section Trace Message Buffer, which is located at Address Locations 0x0400 through 0x04FF).*

BIT 3 - Change in Section Trace Message Mismatch Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in Section Trace Mismatch Defect Condition interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.· Whenever the Receive STS-1/STS-3 TOH Processor block declares the Section Trace Message Mismatch defect condition· Whenever the Receive STS-1/STS-3 TOH Processor block clears the Section Trace Mismatch defect condition.

- 0 - Indicates that the Change in Section Trace Message Mismatch Defect Condition interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change in Section Trace Message Mismatch Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether the Section Trace Message Mismatch condition is currently cleared or declared by reading the state of BIT 2 (Section Trace Message Mismatch Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 1 (Address Location= 0x0206).*

BIT 2 - Unused

BIT 1 - Change in K1, K2 Byte Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in K1, K2 Byte Unstable Defect Condition interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the K1, K2 Byte Unstable Defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the K1, K2 Byte Unstable Defect condition.

- 0 - Indicates that the Change of K1, K2 Byte Unstable Defect Condition interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of K1, K2 Byte Unstable Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether the K1, K2 Byte Unstable Defect Condition is currently being declared or cleared by reading out the contents of BIT 5 (K1, K2 Byte Unstable Defect Declared), within the Receive STS-1/STS-3 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 0 - New K1, K2 Byte Value Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New K1, K2 Byte Value Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt whenever its has accepted a new set of K1, K2 byte values from the incoming STS-1/STS-3 data-stream

- 0 - Indicates that the New K1, K2 Byte Value Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New K1, K2 Byte Value Interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the contents of the new K1 byte by reading out the contents of the Receive STS-1/STS-3 Transport K1 Byte Value Register (Address Location= 0xN11F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the Receive STS-1/STS-3 Transport K2 Byte Value Register (Address Location= 0x0223).*

TABLE 78: RECEIVE STS-1/STS-3 TRANSPORT INTERRUPT STATUS REGISTER - BYTE 0 (ADDRESS LOCATION= 0X020B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of SF Defect ConditionIn-terrupt Sta-tus	Change of SD Defect Condition Interrupt Sta-tus	Detection of REI-L Event Error Inter-rupt Status	Detection of B2 Byte Error Inter-rupt Status	Detection of B1 Byte Error Inter-rupt Status	Change of LOF Defect Condition Interrupt Sta-tus	Change of SEF Defect Interrupt Sta-tus	Change of LOS Defect Condition Interrupt Sta-tus
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Change of Signal Failure (SF) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of SF Defect Condition Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the SF Defect Condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the SF Defect Condition.

- 0 - Indicates that the Change of SF Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of SF Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the SF defect condition is currently being declared by reading out the state of BIT 4(SF Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 6 - Change of Signal Degrade (SD) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of SD Defect Condition Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenver the Receive STS-1/STS-3 TOH Processor block declares the SD Defect Condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the SD Defect Condition.

- 0 - Indicates that the Change of SD Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of SD Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the SD Defect condition is currently being declareds by reading out the state of BIT 3 (SD Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 5 - Detection of REI-L (Line - Remote Error Indicator) Event Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of REI-L Event Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt anytime it detects an REI-L event within the incoming STS-1/STS-3 data-stream.

- 0 - Indicates that the Detection of REI-L Event Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of REI-L Event Interrupt has occurred since the last read of this register.

BIT 4 - Detection of B2 Byte Error Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of B2 Byte Error Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STS-1/STS-3 data-stream.

- 0 - Indicates that the Detection of B2 Byte Error Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of B2 Byte Error Interrupt has occurred since the last read of this register.

BIT 3 = Detection of B1 Byte Error Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of B1 Byte Error Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt anytime it

detects a B1 byte error within the incoming STS-1/STS-3 data-stream.

- 0 - Indicates that the Detection of B1 Byte Error Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of B1 Byte Error Interrupt has occurred since the last read of this register

BIT 2 - Change of Loss of Frame (LOF) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of LOF Defect Condition interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the LOF Defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the LOF Defect condition.

- 0 - Indicates that the Change of LOF Defect Condition interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of LOF Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the LOF defect condition by reading out the state of BIT 2 (LOF Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 1 - Change of SEF Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of SEF Defect Condition Interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the SEF defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the SEF defect condition.

- 0 - Indicates that the Change of SEF Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of SEF Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the SEF defect condition by reading out the state of BIT 1 (SEF Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 0 (Address Location= 0x0207).*

BIT 0 - Change of Loss of Signal (LOS) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of LOS Defect Condition interrupt has occurred since the last read of this register. The Receive STS-1/STS-3 TOH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the LOS defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the LOS defect condition.

- 0 - Indicates that the Change of LOS Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of LOS Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the LOS defect condition by reading out the contents of BIT 0 (LOS Defect Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 0 (Address Location= 0x0207).*

TABLE 79: RECEIVE STS-1/STS-3 TRANSPORT INTERRUPT ENABLE REGISTER - BYTE 2 (ADDRESS LOCATION= 0X020D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-LDefect Condition Interrupt Enable	Change of RDI-LDefect Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT 1- Change of AIS-L (Line AIS) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of AIS-L Defect Condition interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.

- When the Receive STS-1/STS-3 TOH Processor block declares the AIS-L defect condition.·
- When the Receive STS-1/STS-3 TOH Processor block clears the AIS-L defect condition.

▶ 0 - Disables the Change of AIS-L Defect Condition Interrupt.

▶ 1 - Enables the Change of AIS-L Defect Condition Interrupt.

BIT 0 - Change of RDI-L (Line Remote Defect Indicator) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of RDI-L Defect Condition interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.· When the Receive STS-1/STS-3 TOH Processor block declares the RDI-L defect condition.· When the Receive STS-1/STS-3 TOH Processor block clears the RDI-L defect condition.

▶ 0 - Disables the Change of RDI-L Defect Condition Interrupt.

▶ 1 - Enables the Change of RDI-L Defect Condition Interrupt.

TABLE 80: RECEIVE STS-1/STS-3 TRANSPORT INTERRUPT ENABLE REGISTER - BYTE 1 (ADDRESS LOCATION= 0X020E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable Defect ConditionInterrupt Enable	Change in Section Trace Message Unstable Defect Condition Interrupt Enable	New Section Trace Message Interrupt Enable	Change in Section Trace Message Mismatch Defect Condition Interrupt Enable	Unused	Change in K1, K2 Byte Unstable Defect ConditionInterrupt Enable	New K1K2 Byte Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - New S1 Byte Value Interrupt Enable

This READ/WRITE bit-field is used to enable or disable the New S1 Byte Value Interrupt.

If this interrupt is enabled, then the Receive STS-1/STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STS-1/STS-3 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STS-1/STS-3 frames.

▶ 0 - Disables the New S1 Byte Value Interrupt.

▶ 1 - Enables the New S1 Byte Value Interrupt.

BIT 6 - Change in S1 Byte Unstable Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in S1 Byte Unstable Defect Condition Interrupt..

If the user enables this bit-field, then the Receive STS-1/STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions

- When the Receive STS-1/STS-3 TOH Processor block declares the S1 Byte Unstable defect condition
- When the Receive STS-1/STS-3 TOH Processor block clears the S1 Byte Unstable defect condition.

▶ 0 - Disables the Change in S1 Byte Unstable Defect Condition Interrupt.

▶ 1 - Enables the Change in S1 Byte Unstable Defect Condition Interrupt.

BIT 5 - Change in Section Trace Message Unstable defect condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in Section Trace Message Unstable Defect Condition Interrupt.

If this interrupt is enabled, then the Receive STS-1/STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the Section Trace Message Unstable defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the Section Trace Message Unstable defect condition.

- 0 - Disable the Change of Section Trace Message Unstable defect condition Interrupt.
- 1 - Enables the Change of Section Trace Message Unstable defect condition Interrupt.

BIT 4 - New Section Trace Message Interrupt Enable

This READ/WRITE bit-field is used to enable or disable the New Section Trace Message interrupt.

If this interrupt is enabled, then the Receive STS-1/STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new Section Trace Message within the incoming STS-1/STS-3 data-stream. The Receive STS-1/STS-3 TOH Processor block will accept a new Section Trace Message after it has received it 3 (or 5) consecutive times.

- 0 - Disables the New Section Trace Message Interrupt.
- 1 - Enables the New Section Trace Message Interrupt.

BIT 2 - Unused

BIT 3 - Change in Section Trace Mismatch Defect Condition interrupt enable:

This READ/WRITE bit-field is used to either enable or disable the Change in Section Trace Mismatch defect condition interrupt.

If this interrupt is enabled, then the Receive STS-1/STS-3 TOH Processor block will generate an interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the Section Trace Message Mismatch Defect condition.
- whenever the Receive STS-1/STS-3 TOH Processor block clears the Section Trace Message Mismatch defect condition.

NOTE: *The user can determine whether or not the Receive STS-1/STS-3 TOH Processor block is currently declaring the Section Trace Message Mismatch defect condition by reading the state of BIT 2 (Section Trace Message Mismatch Defect Condition Declared) within the Receive STS-1/STS-3 Transport Status Register - Byte 1 (Address Location= 0x0206).*

BIT 1 - Change of K1, K2 Byte Unstable Defect Condition - Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of K1, K2 Byte Unstable defect condition interrupt. If this interrupt is enabled, then the Receive STS-1/STS-3 TOH Processor block will generate an Interrupt in response to either of the following events.a.Whenever the Receive STS-1/STS-3 TOH Processor block declares the K1, K2 Byte Unstable defect condition. b.Whenever the Receive STS-1/STS-3 TOH Processor block clears the K1, K2 Byte Unstable defect condition.

- 0 - Disables the Change of K1, K2 Byte Unstable Defect Condition Interrupt.
- 1 - Enables the Change of K1, K2 Byte Unstable Defect Condition Interrupt.

BIT 0 - New K1, K2 Byte Value Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the New K1, K2 Byte Value Interrupt. If this interrupt is enabled, then the Receive STS-1/STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STS-1/STS-3 TOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STS-1/STS-3 frames.

- 0 - Disables the New K1, K2 Byte Value Interrupt.
- 1 - Enables the New K1, K2 Byte Value Interrupt.

TABLE 81: RECEIVE STS-1/STS-3 TRANSPORT INTERRUPT STATUS REGISTER - BYTE 0 (ADDRESS LOCATION= 0X020F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of SF Defect-Condition Interrupt Enable	Change of SD Defect Condition Interrupt Enable	Detection of REI-L Event Interrupt Enable	Detection of B2 Byte Error Inter-rupt Enable	Detection of B1 Byte Error Inter-rupt Enable	Change of LOF Defect Condition Interrupt Enable	Change of SEF Defect Condition Interrupt Enable	Change of LOS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Change of Signal Failure (SF) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of Signal Failure (SF) Defect Condition Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to any of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor block declares the SF defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the SF defect condition.

▶ 0 - Disables the Change of SF Defect Condition Interrupt.

▶ 1 - Enables the Change of SF Defect Condition Interrupt.

BIT 6 - Change of Signal Degrade (SD) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of Signal Degrade (SD) Defect Condition Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following events.

- Whenever the Receive STS-1/STS-3 TOH Processor blolck declares the SD defect condition.
- Whenever the Receive STS-1/STS-3 TOH Processor block clears the SD defect condition.

▶ 0 - Disables the Change of SD Defect Condition Interrupt.

▶ 1 - Enables the Change of SD Defect Condition Interrupt.

BIT 5 - Detection of REI-L (Line - Remote Error Indicator) Event Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of REI-L Event interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt anytime the Receive STS-1/STS-3 TOH Processor block detects an REI-L condition within the incoming STS-1/STS-3 data-stream.

▶ 0 - Disables the Detection of REI-L Event Interrupt.

▶ 1 - Enables the Detection of REI-L Event Interrupt.

BIT 4 - Detection of B2 Byte Error Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of B2 Byte Error Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt anytime the Receive STS-1/STS-3 TOH Processor block detects a B2 byte error within the incoming STS-1/STS-3 data-stream.

▶ 0 - Disables the Detection of B2 Byte Error Interrupt.

▶ 1 - Enables the Detection of B2 Byte Error Interrupt.

BIT 3 - Detection of B1 Byte Error Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Detection of B1 Byte Error Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt anytime the Receive STS-1/STS-3 TOH Processor block detects a B1 byte error within the incoming STS-1/STS-3 data-stream.

▶ 0 - Disables the Detection of B1 Byte Error Interrupt.

▶ 1 - Enables the Detection of B1 Byte Error Interrupt.

BIT 2 - Change of Loss of Frame (LOF) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of LOF Defect Condition interrupt. If this

interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions

- When the Receive STS-1/STS-3 TOH Processor block declares the LOF defect condition
- When the Receive STS-1/STS-3 TOH Processor block clears the LOF defect condition.

- 0 - Disables the Change of LOF Defect Condition Interrupt.
- 1 - Enables the Change of LOF Defect Condition Interrupt.

BIT 1 - Change of SEF Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of SEF Defect Condition Interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.

- When the Receive STS-1/STS-3 TOH Processor block declares the SEF defect condition.
- When the Receive STS-1/STS-3 TOH Processor block clears the SEF defect condition.

- 0 - Disables the Change of SEF Defect Condition Interrupt.
- 1 - Enables the Change of SEF Defect Condition Interrupt.

BIT 0 - Change of Loss of Signal (LOS) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of LOF Defect Condition interrupt. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.

- When the Receive STS-1/STS-3 TOH Processor block declares the LOF defect condition.
- When the Receive STS-1/STS-3 TOH Processor block clears the LOF defect condition.

- 0 - Disables the Change of LOF Defect Condition Interrupt.
- 1 - Enables the Change of LOF Defect Condition Interrupt.

TABLE 82: RECEIVE STS-1/STS-3 TRANSPORT - B1 BYTE ERROR COUNT REGISTER - BYTE 3 (ADDRESS LOCATION= 0X0210)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Count - MSB

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - B1 Byte Error Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a B1 byte errorwithin the incoming STS-1/STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor Block is configured to count B1 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-1/STS-3 frame) that are in error

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count B1 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 frame that contains an erred B1 byte.

TABLE 83: RECEIVE STS-1/STS-3 TRANSPORT - B1 BYTE ERROR COUNT REGISTER - BYTE 2 (ADDRESS LOCATION= 0X0211)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - B1 Byte Error Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a B1 byte error.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count B1 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-1/STS-3 frame) that are in error.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count B1 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 frame that contains an erred B1 byte.

TABLE 84: RECEIVE STS-1/STS-3 TRANSPORT - B1 BYTE ERROR COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X0212)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - B1 Byte Error Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a B1 byte error.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count B1 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-1/STS-3 frame) that are in error

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count B1 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 frame that contains an erred B1 byte.

TABLE 85: RECEIVE STS-1/STS-3 TRANSPORT - B1 BYTE ERROR COUNT REGISTER - BYTE 0 (ADDRESS LOCATION= 0X0213)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B1 Byte Error Count - LSB

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - B1 Byte Error Count Register - Bytes 3 through 1, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a B1 byte error.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor Block is configured to count B1 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-1/STS-3 frame) that are in error.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count B1 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 frame that contains an erred B1 byte.

TABLE 86: RECEIVE STS-1/STS-3 TRANSPORT - B2 BYTE ERROR COUNT REGISTER - BYTE 3 (ADDRESS LOCATION= 0X0214)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B2 Byte Error Count - MSB

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - B2 Byte Error Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a B2 byte (or BIP-24) error within the incoming STS-1/STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STS-1/STS-3 frame) that are in error.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count B2 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 frame that contains an erred B2 byte or errored BIP-24.

TABLE 87: RECEIVE STS-1/STS-3 TRANSPORT - B2 BYTE ERROR COUNT REGISTER - BYTE 2 (ADDRESS LOCATION= 0X0215)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B2 Byte Error Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive Transport - B2 Byte Error Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a B2 byte or BIP-24 error within the incoming STS-1/STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STS-1/STS-3 frame) that are in error.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 frame that contains an erred B2 byte or erred BIP-24.

TABLE 88: RECEIVE STS-1/STS-3 TRANSPORT - B2 BYTE ERROR COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X0216)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B2 Byte Error Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive Transport - B2 Byte Error Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a B2 byte or BIP-24 error within the incoming STS-1/STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processror block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STS-1/STS-3 frame) that are in error.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count B2 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 frame that contains an erred B2 byte or erred BIP-24.

TABLE 89: RECEIVE STS-1/STS-3 TRANSPORT - B2 BYTE ERROR COUNT REGISTER - BYTE 0 (ADDRESS LOCATION= 0X0217)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B2 Byte Error Count - LSB

This RESET-upon-READ register, along with Receive Transport - B2 Byte Error Count Register - Bytes 3 through 1, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a B2 byte or BIP-24 error within the incoming STS-1/STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count B2 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STS-1/STS-3 frame) that are in error.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count B2 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 frame that contains an erred B2 byte or erred BIP-24.

TABLE 90: RECEIVE STS-1/STS-3 TRANSPORT - REI-L EVENT COUNT REGISTER - BYTE 3 (ADDRESS LOCATION = 0X0218)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-L Event Count - MSB

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - REI-L Event Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STS-1 or STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count REI-L events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte within each incoming STS-1/STS-3 frame.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count REI-L events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1 or STS-3 frame that contains a non-zero REI-L value.

TABLE 91: RECEIVE STS-1/STS-3 TRANSPORT - REI-L EVENT COUNT REGISTER - BYTE 2 (ADDRESS LOCATION= 0X0219)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-L Event Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - REI-L Event Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STS-1 or STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count REI-L events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte (or the contents within the M1 byte) within each incoming STS-1 (or STS-3) frame.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count REI-L events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1 or STS-3 frame that contains a non-zero REI-L value.

TABLE 92: RECEIVE STS-1/STS-3 TRANSPORT - REI-L EVENT COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X021A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-L Event Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - REI-L Event Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a Line -Remote Error Indicator event within the incoming STS-1 or STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count REI-L events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte (or the contents within the M1 byte) within each incoming STS-1 (or STS-3) frame.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count REI-L events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1 or STS-3 frame that contains a non-zero REI-L value.

TABLE 93: RECEIVE STS-1/STS-3 TRANSPORT - REI-L EVENT COUNT REGISTER - BYTE 0 (ADDRESS LOCATION= 0X021B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-L Event Count - LSB

This RESET-upon-READ register, along with Receive STS-1/STS-3 Transport - REI-L Event Count Register - Bytes 3

through 1, function as a 32 bit counter, which is incremented anytime the Receive STS-1/STS-3 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STS-1 or STS-3 data-stream.

NOTES:

1. If the Receive STS-1/STS-3 TOH Processor block is configured to count REI-L events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte (or the contents within the M1 byte) within each incoming STS-1 (or STS-3) frame.

2. If the Receive STS-1/STS-3 TOH Processor block is configured to count REI-L events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1 or STS-3 frame that contains a non-zero REI-L value.

TABLE 94: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVED K1 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X021F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0]Filtered/Accepted K1 Byte Value

These READ-ONLY bit-fields contain the value of the most recently filtered K1 byte value that the Receive STS-1/STS-3 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-1 or STS-3 frames.

This register should be polled by Software in order to determine various APS codes.

TABLE 95: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVED K2 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X0223)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0]Filtered/Accepted K2 Byte Value

These READ-ONLY bit-fields contain the value of the most recently filtered K2 Byte value that the Receive STS-1/STS-3 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-1 or STS-3 frames.

This register should be polled by Software in order to determine various APS codes.

TABLE 96: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVED S1 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X0227)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_S1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Filtered/Accepted S1 Byte Value

These READ-ONLY bit-fields contain the value of the most recently filtered S1 byte value that the Receive STS-1/STS-3 TOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STS-1 or STS-3 frames.

TABLE 97: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE IN-SYNC THRESHOLD REGISTER (ADDRESS = 0X022B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			FRPATOUT[1:0]		FRPATIN[1:0]		Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT [4:3] - FRPATOUT[1:0]

BIT [2:1] - FRPATIN[1:0]

BIT 0 - Unused

TABLE 98: RECEIVE STS-1/STS-3 TRANSPORT - LOS THRESHOLD VALUE - MSB (ADDRESS LOCATION= 0X022E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - LOS Threshold Value - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - LOS Threshold Value - LSB register is used specify the number of consecutive (All Zero) bytes that the Receive STS-1/STS-3 TOH Processor block must detect (within the incoming STS-1/STS-3 data-stream) before it can declare the LOS defect condition.

NOTE: *This register contains the MSB (Most Significant Byte) of this 16-bit expression.*

TABLE 99: RECEIVE STS-1/STS-3 TRANSPORT - LOS THRESHOLD VALUE - LSB (ADDRESS LOCATION= 0X022F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - LOS Threshold Value - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - LOS Threshold Value - MSB register is used to specify the number of consecutive (All Zero) bytes that the Receive STS-1/STS-3 TOH Processor block must detect (within the incoming STS-1/STS-3 data-stream) before it can declare the LOS defect condition.

NOTE: *This register contains the LSB (Least Significant Byte) of this 16-bit expression.*

TABLE 100: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF SET MONITOR INTERVAL - BYTE 2 (ADDRESS LOCATION= 0X0231)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_MONITOR_INTERVAL - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF SET Monitor Interval - Byte

1 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) Defect Declaration.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1/STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SF Defect Declaration monitoring period. If, during this SF Defect Declaration Monitoring Period, the Receive STS-1/STS-3 TOH Processor block accumulates more B2 byte (or BIP-24) errors than that specified within the Receive Transport SF SET Threshold register, then the Receive STS-1/STS-3 TOH Processor block will declare the SF defect condition.

NOTES:

1. The value that the user writes into these three (3) SF Set Monitor Window registers, specifies the duration of the SF Defect Declaration Monitoring Period, in terms of ms.

2. This particular register byte contains the MSB (most significant byte) value of the three registers that specify the SF Defect Declaration Monitoring Period.

TABLE 101: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF SET MONITOR INTERVAL - BYTE 1 (ADDRESS LOCATION= 0X0232)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_MONITOR_INTERVAL (Bits 15 through 8)

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF SET Monitor Interval - Byte 2 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) Defect Declaration.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1/STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SF Defect Declaration Monitoring Period. If, during this SF Defect Declaration Monitoring Period the Receive STS-1/STS-3 TOH Processor block accumulate more B2 byte (or BIP-24) errors than that specified within the Receive STS-1/STS-3 Transport SF SET Threshold register, then the Receive STS-1/STS-3 TOH Processor block will declare the SF defect condition.

NOTE: *The value that the user writes into these three (3) SF Set Monitor Window registers, specifies the duration of the SF Defect Declaration Monitoring Period, in terms of ms.*

TABLE 102: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF SET MONITOR INTERVAL - BYTE 0 (ADDRESS LOCATION= 0X0233)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_MONITOR_INTERVAL - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF SET Monitor Interval - Byte 2 and Byte 1 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) Defect Declaration.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1/STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SF Defect Declaration Monitoring Period. If, during this SF Defect Declaration Monitoring Period, the Receive STS-1/STS-3 TOH Processor block accumulates more B2 byte (or BIP-24) errors than that specified within the Receive STS-1/STS-3 Transport SF SET Threshold register, then the Receive STS-1/STS-3 TOH Processor block will declare the SF defect condition.

NOTES:

1. The value that the user writes into these three (3) SF Set Monitor Window registers, specifies the duration of the SF Defect Declaration Monitoring Period, in terms of ms.

2. This particular register byte contains the LSB (least significant byte) value of the three registers that specify the SF Defect Declaration Monitoring period.

TABLE 103: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF SET THRESHOLD - BYTE 1 (ADDRESS LOCATION= 0X0236)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_THRESHOLD - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF SET Threshold - Byte 0 registers are used to specify the number of B2 byte (or BIP-24) errors that will cause the Receive STS-1/STS-3 TOH Processor block to declare the SF (Signal Failure) Defect condition.

When the Receive STS-1/STS-3 TOH Processor block is checking for declaring the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the SF Defect Declaration Monitoring Period. If the number of accumulated B2 byte (or BIP-24) errors exceeds that value, which is programmed into this and the Receive STS-1/STS-3 Transport SF SET Threshold - Byte 0 register, then the Receive STS-1/STS-3 TOH Processor block will declare the SF defect condition.

NOTE: *This particular register byte contains the MSB (most significant byte) value of this 16-bit expression.*

TABLE 104: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF SET THRESHOLD - BYTE 0 (ADDRESS LOCATION= 0X0237)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_SET_THRESHOLD - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF SET Threshold - Byte 1 registers are used to specify the number of B2 byte (or BIP-24) errors that will cause the Receive STS-1/STS-3 TOH Processor block to declare the SF (Signal Failure) Defect condition.

When the Receive STS-1/STS-3 TOH Processor block is checking for declaring the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the SF Defect Monitoring Period. If the number of accumulated B2 byt (or BIP-24)e errors exceeds that which has been programmed into this and the Receive STS-1/STS-3 Transport SF SET Threshold - Byte 1 register, then the Receive STS-1/STS-3 TOH Processor block will declare the SF defect condition.

TABLE 105: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF CLEAR THRESHOLD - BYTE 1 (ADDRESS LOCATION= 0X023A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_THRESHOLD - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF CLEAR Threshold - Byte 0 registers are used to specify the upper limit for the number of B2 byte (or BIP-24) errors that will cause the Receive STS-1/STS-3 TOH Processor block to clear the SF (Signal Failure) defect condition.

When the Receive STS-1/STS-3 TOH Processor block is checking for clearing the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the SF Defect Clearance Monitoring Period. If the number of accumulated B2 byte (or BIP-24) errors is less than that programmed into this and the Receive STS-1/STS-3 Transport SF CLEAR Threshold - Byte 0 register, then the Receive STS-1/STS-3 TOH Processor block clear the SF defect condition.

TABLE 106: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF CLEAR THRESHOLD - BYTE 0 (ADDRESS LOCATION= 0X023B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_THRESHOLD - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF CLEAR Threshold - Byte 1 registers are used to specify the upper limit for the number of B2 byte (or BIP-24) errors that will cause the Receive STS-1/STS-3 TOH Processor block to clear the SF (Signal Failure) defect condition.

When the Receive STS-1/STS-3 TOH Processor block is checking for clearing the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the SF Defect Clearance Monitoring Period. If the number of accumulated B2 byte (or BIP-24) errors is less than that programmed into this and the Receive STS-1/STS-3 Transport SF CLEAR Threshold - Byte 1 register, then the Receive STS-1/STS-3 TOH Processor block will clear the SF defect condition.

TABLE 107: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD SET MONITOR INTERVAL - BYTE 2 (ADDRESS LOCATION= 0X023D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - SD_SET_MONITOR_INTERVAL - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD SET Monitor Interval - Byte 1 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect declaration.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SD Defect Declaration monitoring period. If, during this SD Defect Declaration Monitoring period, the Receive STS-1/STS-3 TOH Processor block accumulates more B2 byte (or BIP-24) errors than that specified within the Receive STS-1/STS-3 Transport SD SET Threshold register, then the Receive STS-1/STS-3 TOH Processor block will declare the SD defect condition.

NOTES:

1. The value that the user writes into these three (3) SD Set Monitor Window registers, specifies the duration of the SD Defect Declaration Monitoring Period, in terms of ms.

2. This particular register byte contains the MSB (Most significant byte) value of the three registers that specify the SD Defect Declaration Monitoring Period.

TABLE 108: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD SET MONITOR INTERVAL - BYTE 1 (ADDRESS LOCATION= 0X023E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - SD_SET_MONITOR_INTERVAL - Bits 15 through 8

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD SET Monitor Interval - Byte 2 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect declaration.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine it it should declare the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SD Defect Declaration Monitoring Period. If, during this SD Defect Declaration Monitoring Period the Receive STS-1/STS-3 TOH Processor block accumulates more B2 byte (or BIP-24) errors than that specified within the Receive STS-1/STS-3 Transport SD SET Threshold register, then the Receive STS-1/STS-3 TOH Processor block will declare the SD defect condition.

NOTE: *The value that the user writes into these three (3) SD Set Monitor Window registers, specifies the duration of the SD Defect Declaration Monitoring Period, in terms of ms.*

TABLE 109: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD SET MONITOR INTERVAL - BYTE 0 (ADDRESS LOCATION= 0X023F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - SD_SET_MONITOR_INTERVAL - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD SET Monitor Interval - Byte 2 and Byte 1 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect declaration.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-speciifed SD Defect Declaration Monitoring Period. If, during this SD Defect Declaration Monitoring Period, the Receive STS-1/STS-3 TOH Processor block accmulattes more B2 byte (or BIP-24) errors than that specified within the Receive STS-1/STS-3 Transport SD SET Threshold register, then the Receive STS-1/STS-3 TOH Processor block will declare the SD defect condition.

NOTES:

1. *The value that the user writes into these three (3) SD Set Monitor Window registers, specifies the duration of the SD Defect Declaration Monitoring Period, in terms of ms.*
2. *This particular register byte contains the LSB (least significant byte) value of the three registers that specify the SD Defect Declaration Monitoring period.*

TABLE 110: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD SET THRESHOLD - BYTE 1 (ADDRESS LOCATION= 0X0242)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_SET_THRESHOLD - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD SET Threshold - Byte 0 registers are used to specify the number of B2 byte (or BIP-24) errors that will cause the Receive STS-1/STS-3 TOH Processor block to declare the SD (Signal Degrade) defect condition.

When the Receive STS-1/STS-3 TOH Processor block is checking for declaring the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the SD Defect Declaration Monitoring Period. If the number of accumulated B2 byte (or BIP-24) errors exceeds that value, which is programmed into this and the Receive STS-1/STS-3 Transport SD SET Threshold - Byte 0 register, then the Receive STS-1/STS-3 TOH Processor block will declare the SD defect condition.

TABLE 111: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD SET THRESHOLD - BYTE 0 (ADDRESS LOCATION= 0X0243)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_SET_THRESHOLD - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD SET Threshold - Byte 1 registers are used to specify the number of B2 byte (or BIP-24) errors that will cause the Receive STS-1/STS-3 TOH Processor block to declare an SD (Signal Degrade) defect condition.

When the Receive STS-1/STS-3 TOH Processor block is checking for declaring the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the SD Defect Monitoring Period. If the number of accumulated B2 byte (or BIP-24) errors exceeds that which has been programmed into this and the Receive STS-1/STS-3 Transport SD SET Threshold - Byte 1 register, then the Receive STS-1/STS-3 TOH Processor block will declare the SD defect condition.

TABLE 112: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD CLEAR THRESHOLD - BYTE 1 (ADDRESS LOCATION= 0X0246)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_THRESHOLD - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD CLEAR Threshold - Byte 0 registers are used to specify the upper limit for the number of B2 byte (or BIP-24) errors that will cause the Receive STS-1/STS-3 TOH Processor block to clear the SD (Signal Degrade) defect condition.

When the Receive STS-1/STS-3 TOH Processor block is checking for clearing the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the SD Defect Clearance Monitoring Period. If the number of accumulated B2 byte (or BIP-24) errors is less than that programmed into this and the Receive STS-1/STS-3 Transport

SD CLEAR Threshold - Byte 0 register, then the Receive STS-1/STS-3 TOH Processor block will clear the SD defect condition.

TABLE 113: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD CLEAR THRESHOLD - BYTE 1 (ADDRESS LOCATION= 0X0247)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_THRESHOLD - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD CLEAR Threshold - Byte 1 registers are used to specify the upper limit for the number of B2 byte (or BIP-24) errors that will cause the Receive STS-1/STS-3 TOH Processor block to clear the SD (Signal Degrade) defect condition.

When the Receive STS-1/STS-3 TOH Processor block is checking for clearing the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the SD Defect Clearance Monitoring Period. If the number of accumulated B2 byte (or BIP-24) errors is less than that programmed into this and the Receive STS-1/STS-3 Transport SD CLEAR Threshold - Byte 1 register, then the Receive STS-1/STS-3 TOH Processor block will clear the SD defect condition.

TABLE 114: RECEIVE STS-1/STS-3 TRANSPORT - FORCE SEF DEFECT CONDITION REGISTER (ADDRESS LOCATION= 0X024B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							SEF FORCE
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Unused

BIT 0 - SEF Defect Condition FORCE

This READ/WRITE bit-field is used to force the Receive STS-1/STS-3 TOH Processor block (within the corresponding Channel) to declare the SEF defect condition. The Receive STS-1/STS-3 TOH Processor block will then attempt to reacquire framing.

Writing a 1 into this bit-field configures the Receive STS-1/STS-3 TOH Processor block to declare the SEF defect. The Receive STS-1/STS-3 TOH Processor block will automatically set this bit-field to 0 once it has reacquired framing (e.g., has detected two consecutive STS-1 or STS-3 frames with the correct A1 and A2 bytes).

TABLE 115: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SECTION TRACE MESSAGE BUFFER CONTROL REGISTER (ADDRESS LOCATION= 0X024F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive Section Trace Message Buffer Read Select	Receive Section Trace Message Accept Threshold	Section Trace Message Alignment Type	Receive Section Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT 4Receive Section Trace Message Buffer Read Selection

This READ/WRITE bit-field is used to specify which of the following Receive Section Trace Message buffer segments to read.

- The Actual Receive Section Trace Message Buffer which contains the contents of the most recently received (and accepted) Section Trace Message via the incoming STS-1 or STS-3 data-stream.
- The Expected Receive Section Trace Message Buffer which contains the contents of the Section Trace Message that the user expects to receive. The contents of this particular buffer are usually specified by the user.

▶ 0 - Executing a READ to the Receive Section Trace Message Buffer address space, will return contents within the Actual Receive Section Trace Message buffer.

▶ 1 - Executing a READ to the Receive Section Trace Message Buffer address space will return contents within the Expected Receive Section Trace Message Buffer.

NOTE: *In the case of the Receive STS-3 TOH Processor block, the Receive Section Trace Message Buffer is located at Address Location 0x0400 through 0x043F.*

BIT 3 - Receive Section Trace Message Accept Threshold

This READ/WRITE bit-field is used to select the number of consecutive times that the Receive STS-1/STS-3 TOH Processor block must receive a given Section Trace Message, before it is accepted, as described below. Once a given Section Trace Message has been accepted then it can be read out of the Actual Receive Section Trace Message Buffer.

▶ 0 - The Receive STS-1/STS-3 TOH Processor block accepts the Section Trace Message after it has received it the third time in succession.

▶ 1 - The Receive STS-1/STS-3 TOH Processor block accepts the Section Trace Message after it has received in the fifth time in succession.

BIT 2 - Section Trace Message Alignment Type

This READ/WRITE bit-field is used to specify how the Receive STS-1/STS-3 TOH Processor block will locate the boundary of the Section Trace Message within the incoming STS-1 or STS-3 data-stream, as indicated below.

▶ 0 - Message boundary is indicated by Line Feed.

▶ 1 - Message boundary is indicated by the presence of a 1 in the MSB of the first byte (within the Section Trace Message).

BIT [1:0] - Receive Section Trace Message Length[1:0]

These READ/WRITE bit-fields are used to specify the length of the Section Trace Message that the Receive STS-1/STS-3 TOH Processor block will receive. The relationship between the content of these bit-fields and the corresponding Receive Section Trace Message Length is presented below

Trace Message Length

RECEIVE SECTION TRACE MESSAGE LENGTH[1:0]	RESULTING RECEIVE SECTION TRACE MESSAGE LENGTH (IN TERMS OF BYTES)
00	1 Byte
01	16 Bytes
10/11	64 Bytes

TABLE 116: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD BURST ERROR TOLERANCE - BYTE 1 (ADDRESS LOCATION= 0X0252)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_BURST_TOLERANCE - MSB

These READ/WRITE bits, along with the contents of the Receive STS-1/STS-3 Transport - SD BURST Tolerance - Byte 0 registers are used to specify the maximum number of B2 byte (or BIP-24) errors that the corresponding Receive STS-1/STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 or STS-3 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.

NOTE: *The purpose of this feature is to are used to provide some level of B2 error burst filtering, when the Receive STS-1/STS-3 TOH Processor block is accumulating B2 byte (or BIP-24) errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-1/STS-3 TOH Processor block to detect B2 bit errors in multiple Sub-Interval periods before it will declare the SD defect condition.*

TABLE 117: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD BURST ERROR TOLERANCE - BYTE 0 (ADDRESS LOCATION= 0X0253)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_BURST_TOLERANCE - LSB

These READ/WRITE bits, along with the contents of the Receive STS-1/STS-3 Transport - SD BURST Tolerance - Byte 1 registers are used to specify the maximum number of B2 byte (or BIP-24) errors that the corresponding Receive STS-1/STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 or STS-3 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.

NOTE: *The purpose of this feature is to are used to provide some level of B2 error burst filtering, when the Receive STS-1/STS-3 TOH Processor block is accumulating B2 byte (or BIP-24) errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-1/STS-3 TOH Processor block to detect B2 bit errors in multiple Sub-Interval periods before it will declare the SD defect condition.*

TABLE 118: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF BURST ERROR TOLERANCE - BYTE 1 (ADDRESS LOCATION= 0X0256)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_BURST_TOLERANCE - MSB

These READ/WRITE bits, along with the contents of the Receive STS-1/STS-3 Transport - SF BURST Tolerance - Byte 0 registers are used to specify the maximum number of B2 byte (or BIP-24) errors that the corresponding Receive STS-1/STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 or STS-3 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition.

NOTE: *The purpose of this feature is to are used to provide some level of B2 error burst filtering, when the Receive STS-1/STS-3 TOH Processor block is accumulating B2 byte (or BIP-24) errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-1/STS-3 TOH Processor block to detect B2 bit errors in multiple Sub-Interval periods before it will declare the SF defect condition.*

TABLE 119: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF BURST ERROR TOLERANCE - BYTE 0 (ADDRESS LOCATION= 0X0257)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_BURST_TOLERANCE - LSB

These READ/WRITE bits, along with the contents of the Receive STS-1/STS-3 Transport - SF BURST Tolerance - Byte 1 registers are used to specify the maximum number of B2 byte (or BIP-24)errors that the corresponding Receive STS-1/STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 or STS-3 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition.

NOTE: *The purpose of this feature is to are used to provide some level of B2 error burst filtering, when the Receive STS-1/STS-3 TOH Processor block is accumulating B2 byte (or BIP-24) errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-1/STS-3 TOH Processor block to detect B2 bit errors in multiple Sub-Interval periods before it will declare the SF defect condition.*

TABLE 120: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD CLEAR MONITOR INTERVAL - BYTE 2 (ADDRESS LOCATION= 0X0259)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_MONITOR_INTERVAL - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD Clear Monitor Interval - Byte 1 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect clearance.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SD Defect Clearance Monitoring period. If, during this SD Defect Clearance Monitoring period, the Receive STS-1/STS-3 TOH Processor block accumulates less B2 byte (or BIP-24) errors than that programmed into the Receive STS-1/STS-3 Transport SD Clear Threshold register, then the Receive STS-1/STS-3 TOH Processor block will clear the SD defect condition.

NOTES:

1. *The value that the user writes into these three (3) SD Clear Monitor Window Registers, specifies the duration of the SD Defect Clearance Monitoring Period, in terms of ms.*
2. *This particular register byte contains the MSB (Most significant byte) value of the three registers that specifiy the SD Defect Clearance Monitoring period.*

TABLE 121: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD CLEAR MONITOR INTERVAL - BYTE 1 (ADDRESS LOCATION= 0X025A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_MONITOR_INTERVAL - Bits 15 through 8

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD Clear Monitor Interval - Byte 2 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect clearance.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SD Defect Clearance Monitoring period. If, during this SD Defecf Clearance Monitoring Period, the Receive STS-1/STS-3 TOH Processor block accumulates less B2 byte (or BIP-24) errors than that programmed into the Receive STS-1/STS-3 Transport SD Clear Threshold register, then the Receive STS-1/STS-3 TOH Processor block will clear the SD defect condition.

NOTE: *The value that the user writes into these three (3) SD Clear Monitor Window Registers, specifies the duration of the SD Defect Clearance Monitoring Period, in terms of ms.*

TABLE 122: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SD CLEAR MONITOR INTERVAL - BYTE 0 (ADDRESS LOCATION= 0X025B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WIN-DOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SD_CLEAR_MONITOR_INTERVAL - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SD Clear Monitor Interval - Byte 2 and Byte 1 registers are used to specify the length of the monitoring period (in terms of ms) for SD (Signal Degrade) defect clearance

.When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SD Defect Clearance Monitoring period. If, during this SD Defect Clearance Monitoring period, the Receive STS-1/STS-3 TOH Processor block accumulates less B2 byte (or BIP-24) errors than that programmed into the Receive STS-1/STS-3 Transport SD Clear Threshold register, then the Receive STS-1/STS-3 TOH Processor block will clear the SD defect condition

NOTES:

1. *The value that the user writes into these three (3) SD Clear Monitor Window Registers, specifies the duration of the SD Defect Clearance Monitoring Period, in terms of ms.*
2. *This particular register byte contains the LSB (least significant byte) value of the three registers that specify the SD Defect Clearance Monitoring period.*

TABLE 123: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF CLEAR MONITOR INTERVAL - BYTE 2 (ADDRESS LOCATION= 0X025D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_MONITOR_INTERVAL - MSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF Clear Monitor Interval - Byte 1 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) defect clearance.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-

specified SF Defect Clearance Monitoring period. If, during this SF Defect Clearance Monitoring period, the Receive STS-1/STS-3 TOH Processor block accumulates less B2 byte (or BIP-24) errors than that programmed into the Receive STS-1/STS-3 Transport SF Clear Threshold register, then the Receive STS-1/STS-3 TOH Processor blolck will clear the SF defect condition.

NOTES:

1. The value that the user writes into these three (3) SF Clear Monitor Window Registers, specifies the duration of the SF Defect Clearance Monitoring Period, in terms of ms.

2. This particular register byte contains the MSB (Most significant byte) value of the three registers that specify the SF Defect Clearance Monitoring period.

TABLE 124: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF CLEAR MONITOR INTERVAL - BYTE 1 (ADDRESS LOCATION= 0X025E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_MONITOR_INTERVAL - Bits 15 through 8

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF Clear Monitor Interval - Byte 2 and Byte 0 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) defect clearance.

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SF Defect Clearance Monitoring period. If, during this SF Defect Clearance Monitoring period, the Receive STS-1/STS-3 TOH Processor block accumulates less B2 byte (or BIP-24) errors than that programmed into the Receive STS-1/STS-3 Transport SF Clear Threshold register, then the Receive STS-1/STS-3 TOH Processor block will clear the SF defect condition.

NOTE: *The value that the user writes into these three (3) SF Clear Monitor Window Registers, specifies the duration of the SF Defect Clearance Monitoring Period, in terms of ms.*

TABLE 125: RECEIVE STS-1/STS-3 TRANSPORT - RECEIVE SF CLEAR MONITOR INTERVAL - BYTE 0 (ADDRESS LOCATION= 0X025F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - SF_CLEAR_MONITOR_INTERVAL - LSB

These READ/WRITE bits, along the contents of the Receive STS-1/STS-3 Transport - SF Clear Monitor Interval - Byte 2 and Byte 1 registers are used to specify the length of the monitoring period (in terms of ms) for SF (Signal Failure) defect clearance

When the Receive STS-1/STS-3 TOH Processor block is checking the incoming STS-1 or STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte (or BIP-24) errors throughout the user-specified SF Defect Clearance Monitoring period. If, during this SF Defect Clearance Monitoring period, the Receive STS-1/STS-3 TOH Processor block accumulates less B2 byte (or BIP-24) errors than that programmed into the Receive STS-1/STS-3 Transport SF Clear Threshold register, then the Receive STS-1/STS-3 TOH Processor block will clear the SF defect condition.

NOTES:

1. The value that the user writes into these three (3) SF Clear Monitor Window Registers, specifies the duration of the SF Defect Clearance Monitoring Period, in terms of ms.

2. This particular register byte contains the LSB (Least Significant byte) value of the three registers that specify the SF Defect Clearance Monitoring period.

TABLE 126: RECEIVE STS-1/STS-3 TRANSPORT - AUTO AIS CONTROL REGISTER (ADDRESS LOCATION= 0X0263)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit AIS-P (Down-stream) upon Section Trace Mes-sage Unsta-ble	Transmit AIS-P (Down-stream) Upon Sec-tion Trace Message Mismatch	Transmit AIS-P (Down-stream) upon SF	Transmit AIS-P (Down-stream) upon SD	Unused	Transmit AIS-P (Down-stream) upon LOF	Transmit AIS-P (Down-stream) upon LOS	Transmit AIS-P (Down-stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Transmit Path AIS upon Declaration of the Section Trace Message Unstable Defect Condition

This READ/WRITE bit-field is used to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STS-1/STS-3 POH Processor block), anytime it declares the Section Trace Message Unstable defect condition within the incoming STS-1 or STS-3 data-stream.

- 0 - Does not configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever (and for the duration that) it declares the Section Trace Message Unstable defect condition.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever (and for the duration that) it declares the Section Trace Message Unstable defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 6 - Transmit Path AIS (AIS-P) upon Declaration of the Section Trace Message Mismatch Defect Condition

This READ/WRITE bit-field is used to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STS-1/STS-3 POH Processor blocks), anytime (and for the duration that) it declares the Section Trace Message Mismatch defect condition within the incoming STS-1/STS-3 data stream.

- 0 - Does not configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Section Trace Mismatch defect condition.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever (and for the duration that) it declares the Section Trace Message Mismatch defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 5 - Transmit Path AIS upon declaration of the Signal Failure (SF) defect condition

This READ/WRITE bit-field is used to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STS-1/STS-3 POH Processor block), anytime (and for the duration that) it declares the SF defect condition.

- 0 - Does not configure the Receive STS-1/STS-3 TOH Processor block to transmit the AIS-P indicator (via the downstream traffic) upon declaration of the SF defect.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) anytime (and for the duration that) it declares the SF defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 4 - Transmit Path AIS upon declaration of the Signal Degrade (SD) defect

This READ/WRITE bit-field is used to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STS-1/STS-3 POH Processor block) anytime (and for the duration that) it declares the SD defect condition.

- 0 - Does not configure the Receive STS-1/STS-3 TOH Processor block to transmit the AIS-P indicator (via the downstream traffic) upon declaration of the SD defect.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) anytime (and for the duration that) it declares the SD defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 3 - Unused

BIT 2 - Transmit Path AIS upon declaration of the Loss of Frame (LOF) defect

This READ/WRITE bit-field is used to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STS-1/STS-3 POH Processor block), anytime (and for the duration that) it declares the LOF defect condition.

- 0 - Does not configure the Receive STS-1/STS-3 TOH Processor block to transmit the AIS-P indicator (via the downstream traffic) upon declaration of the LOF defect.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) anytime (and for the duration that) it declares the LOF defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 1 - Transmit Path AIS upon declaration of the Loss of Signal (LOS) defect

This READ/WRITE bit-field is used to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STS-1/STS-3 POH Processor block), anytime (and for the duration that) it declares the LOS defect condition.

- 0 - Does not configure the Receive STS-1/STS-3 TOH Processor block to transmit the AIS-P indicator (via the downstream traffic) anytime it declares the LOS defect condition.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) anytime (and for the duration that) it declares the LOS defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 0 - Automatic Transmission of AIS-P Enable

This READ/WRITE bit-field serves two purposes.

It is used to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the Receive STS-1/STS-3 POH Processor block), upon detection of an SF, SD, Section Trace Mismatch, Section Trace Unstable, LOF or LOS defect conditions.

It also is used to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards the Receive STS-1/STS-3 POH Processor block) anytime it declares the AIS-L defect condition within the incoming STS-1/STS-3 datastream.

- 0 - Configures the Receive STS-1/STS-3 TOH Processor block to NOT automatically transmit the AIS-P indicator (via the downstream traffic) upon declaration of the AIS-L defect condition or any of the above-mentioned defect conditions.
- 1 - Configures the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) upon declaration of the AIS-L defect or any of the above-mentioned defect conditions.

NOTE: *The user must also set the corresponding bit-fields (within this register) to 1 in order to configure the Receive STS-1/STS-3 TOH Processor block to automatically transmit the AIS-P indicator upon declaration of a given alarm/defect condition.*

TABLE 127: RECEIVE STS-1/STS-3 TRANSPORT - AUTO AIS (IN DOWNSTREAM T1/E1S) CONTROL REGISTER (ADDRESS LOCATION= 0X026B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Transmit AIS (via Down-stream T1/E1s) upon LOS	Transmit AIS (via Down-stream T1/E1s) upon LOF	Transmit AIS (via Down-stream T1/E1s) upon SD	Transmit AIS (via Down-stream T1/E1s) upon SF	Unused	Transmit AIS (via Down-stream T1/E1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Unused

BIT 5 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon declaration of the LOS (Loss of Signal) defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares the LOS defect condition.3

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, anytime the Receive STS-1/STS-3 TOH Processor block declares the LOS defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares the LOS defect condition.

BIT 4 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon declaration of the LOF (Loss of Frame) defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares the LOF defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime the Receive STS-1/STS-3 TOH Processor block declares the LOF defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares the LOF defect condition.

BIT 3 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon declaration of the SD (Signal Degrade) defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares the SD defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime the Receive STS-1/STS-3 TOH Processor block declares the SD defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares the SD defect condition.

BIT 2 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon declaration of the Signal Failure (SF) defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, anytime (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares the SF defect condition.

- 0 - Does not configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, anytime the Receive STS-1/STS-3 TOH Processor block declares the SF defect condition.

- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares the SF defect condition.

BIT 1 - Unused

BIT 0 - Automatic Transmission of DS1/E1 AIS (via the downstream DS1/E1s) Enable

This READ/WRITE bit-field serves two purposes.It is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, upon declaration of either the SF, SD, LOS or LOF defect conditions via the Receive STS-1/STS-3 TOH Processor block.

It also is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicator, via its outbound DS1/E1 signals, upon declaration of the AIS-L defect condition, via the Receive STS-1/STS-3 TOH Processor block.

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicator, whenever the Receive STS-1/STS-3 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions.

- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicator, whenever (and for the duration that) the Receive STS-1/STS-3 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions.

TABLE 128: RECEIVE STS-1/STS-3 TRANSPORT - A1, A2 BYTE ERROR COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X026E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive A1, A2 Byte Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive A1, A2 Byte Error Count Register - MSB Register

This RESET-upon-READ register, along with the Receive STS-1/STS-3 Transport - A1, A2 Byte Error Count Register - Byte

0 presents a 16-bit representation of the total number of A1 and A2 byte errors that the Receive STS-1/STS-3 TOH Processor block has detected (within the incoming STS-1/STS-3 data-stream) since the last read of this register.

NOTE: *This register contains the MSB (Most Significant Byte) of this 16-bit expression.*

TABLE 129: RECEIVE STS-1/STS-3 TRANSPORT - A1, A2 BYTE ERROR COUNT REGISTER - BYTE 0 (ADDRESS LOCATION= 0X026F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive A1, A2 Byte Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive A1, A2 Byte Error Count Register - LSB Register

This RESET-upon-READ register, along with the Receive STS-1/STS-3 Transport - A1, A2 Byte Error Count Register - Byte 1 presents a 16-bit representation of the total number of A1 and A2 byte errors that the Receive STS-1/STS-3 TOH Processor block has detected (within the incoming STS-1/STS-3 data-stream) since the last read of this register.

NOTE: *This register contains the LSB (Least Significant Byte) of this 16-bit expression.*

2.4 RECEIVE STS-1 POH PROCESSOR BLOCK REGISTERS

The register map for the Receive STS-1 POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the Receive STS-1/STS-3 POH Processor block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328, with the Receive STS-1 POH Processor block highlighted is presented below in Figure 4.

FIGURE 4. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WITH THE RECEIVE STS-1 POH PROCESSOR BLOCK HIGHLIGHTED

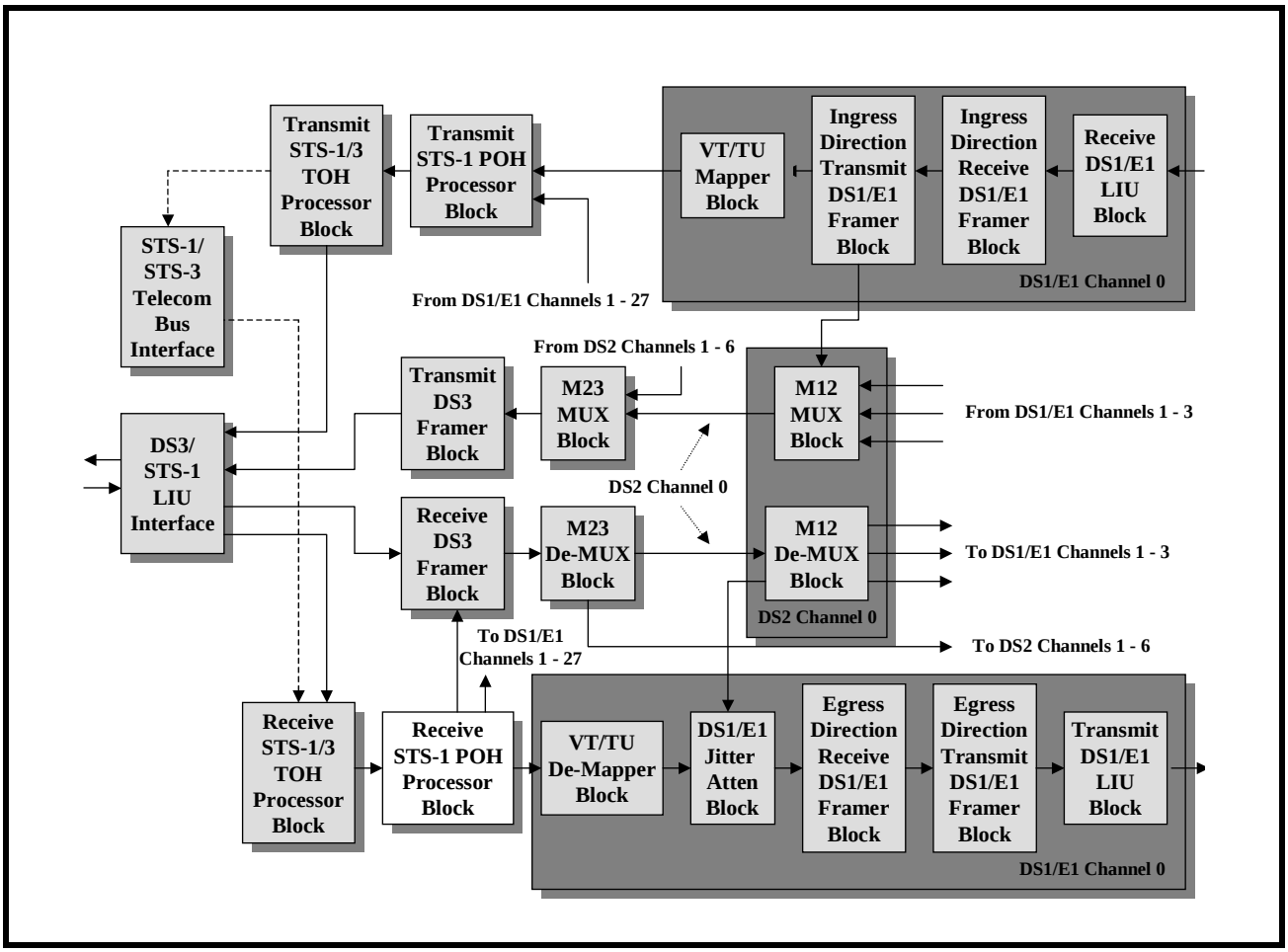


TABLE 130: RECEIVE STS-1 PATH - RECEIVE CONTROL REGISTER - BYTE 2 (ADDRESS = 0X0281)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Payload_Type[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT [1:0] - Payload_Type[1:0]

TABLE 131: RECEIVE STS-1 PATH - RECEIVE CONTROL REGISTER - BYTE 0 (ADDRESS LOCATION= 0X0283)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				CheckStuff	RDI-PType	REI-PError Type	B3 Error Type
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT 3 - Check (Pointer Adjustment) Stuff Select

This READ/WRITE bit-field is used to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored.

- 0 - Disables this SONET standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted.
- 1 - Enables this SONET standard implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation will be ignored.

BIT 2 - Path - Remote Defect Indicator Type Select

This READ/WRITE bit-field is used to configure the Receive STS-1 POH Processor block to support either the Single-Bit or the Enhanced RDI-P form of signaling, as described below.

- 0 - Configures the Receive STS-1 POH Processor block to support Single-Bit RDI-P.

In this mode, the Receive STS-1 POH Processor block will only monitor BIT 5, within the G1 byte (of the incoming SPE data), in order to declare and clear the RDI-P defect condition.

- 1 - Configures the Receive STS-1 POH Processor block to support Enhanced RDI-P (ERDI-P).

In this mode, the Receive STS-1 POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P defect condition.

BIT 1 - REI-P Error Type

This READ/WRITE bit-field is used to specify how the Receive STS-1 POH Processor block will count (or tally) REI-P events, for Performance Monitoring purposes. The user can configure the Receive STS-1 POH Processor block to increment REI-P events on either a per-bit or per-frame basis.

If the user configures the Receive STS-1 POH Processor block to increment REI-P events on a per-bit basis, then it will increment the Receive Path REI-P Error Count register by the value of the lower nibble within the G1 byte of the incoming STS-1/STS-3 data-stream.

If the user configures the Receive STS-1 POH Processor block to increment REI-P events on a per-frame basis, then it will increment the Receive Path REI-P Error Count register each time it receives an STS-1/STS-3 frame, in which the lower nibble of the G1 byte (bits 1 through 4) are set to a non-zero value.

- 0 - Configures the Receive STS-1 POH Processor block to count or tally REI-P events on a per-bit basis.
- 1 - Configures the Receive STS-1 POH Processor block to count or tally REI-P events on a per-frame basis.

BIT 0 - B3 Error Type

This READ/WRITE bit-field is used to specify how the Receive STS-1 POH Processor block will count (or tally) B3 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-1 POH Processor block to increment B3 byte errors on either a per-bit or per-frame basis.

If the user configures the Receive STS-1 POH Processor block to increment B3 byte errors on a per-bit basis, then it will increment the Receive Path B3 Byte Error Count register by the number of bits (within the B3 byte value) that is in error.

If the user configures the Receive STS-1 POH Processor block to increment B3 byte errors on a per-frame basis, then it will increment the Receive Path B3 Byte Error Count register each time it receives an STS-1/STS-3 frame that contains an erred B3 byte.

- 0 - Configures the Receive STS-1 POH Processor block to count B3 byte errors on a per-bit basis
- 1 - Configures the Receive STS-1 POH Processor block to count B3 byte errors on a per-frame basis.

TABLE 132: RECEIVE STS-1 PATH - CONTROL REGISTER - BYTE 1 (ADDRESS LOCATION= 0X0286)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Path Trace Message Unstable Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:1] - Unused

BIT 0 - Path Trace Message Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the Path Trace Message Unstable defect condition. The Receive STS-1 POH Processor block will declare the Path Trace Message Unstable defect condition, whenever the Path Trace Message Unstable counter reaches the value 8. The Path Trace Message Unstable counter will be incremented for each time that it receives a Path Trace message that differs from the previously received message. The Path Trace Unstable counter is cleared to 0 whenever the Receive STS-1 POH Processor block has received a given Path Trace Message 3 (or 5) consecutive times.

NOTE: *Receiving a given Path Trace Message 3 (or 5) consecutive times also sets this bit-field to 0*

- 0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the Path Trace Message Unstable defect.
- 1 - Indicates that the Receive STS-1 POH Processor blolck is currently declaring the Path Trace Message Unstable defect condition.

TABLE 133: RECEIVE STS-1 PATH - SONET RECEIVE POH STATUS - BYTE 0 (ADDRESS LOCATION= 0X0287)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P Defect Declared	C2 Byte UnstableDe-fect Declared	UNEQ-PDe-fectDeclared	PLM-PDe-fectDeclared	RDI-PDe-fectDeclared	RDI-P Unstable-Condition	LOP-PDe-fectDeclared	AIS-PDefect-Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Trace Identification Mismatch (TIM-P) Defect Indicator

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the Path Trace Identification Mismatch (TIM-P) defect condition. The Receive STS-1 POH Processor block will declare the TIM-P defect condition, when none of the received 64-byte string (received via the J1 byte, within the incoming STS-1/STS-3 data-stream) matches the expected 64 byte message.The Receive STS-1 POH Processor block will clear the TIM-P defect condition, when 80% of the received 64 byte string (received via the J1 byte) matches the expected 64 byte message.

- 0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the TIM-P defect condition.
- 1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the TIM-P defect condition.

BIT 6 - C2 Byte (Path Signal Label Byte) Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the Path Signal Label Byte Unstable defect condition. The Receive STS-1 POH Processor block will declare the C2 (Path Signal Label Byte) Unstable defect condition, whenever the C2 Byte Unstable counter reaches the value 5. The C2 Byte Unstable counter will be incremented for each time that it receives an SPE with a C2 byte value that differs from the previously received C2 byte value. The C2 Byte Unstable counter is cleared to 0 whenever the Receive STS-1 POH Processor block has received 3 (or 5) consecutive SPEs that each contains the same C2 byte

value.Note:Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to 0.

- 0 - Indicates that the Receive STS-1 POH Processor block is currently NOT declaring the C2 (Path Signal Label Byte) Unstable defect condition.
- 1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the C2 (Path Signal Label Byte) Unstable defect condition.

BIT 5 - Path - Unequipped (UNEQ-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the UNEQ-P defect condition. The Receive STS-1 POH Processor block will declare the UNEQ-P defect condition, anytime that it receives at least five (5) consecutive STS-1/STS-3 frames, in which the C2 byte was set to the value 0x00 (which indicates that the SPE is Unequipped).

The Receive STS-1 POH Processor block will clear the UNEQ-P defect condition, if it receives at least five (5) consecutive STS-1/STS-3 frames, in which the C2 byte was set to a value other than 0x00.

- 0 - Indicates that the Receive STS-1 POH Processor block is currently NOT declaring the UNEQ-P defect condition.
- 1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the UNEQ-P defect condition.

NOTE: *:The Receive STS-1 POH Processor block will not declare the UNEQ-P defect condition if it configured to expect to receive STS-1/STS-3 frames with C2 bytes being set to 0x00 (e.g., if the Receive STS-1 Path - Expected Path Label Value Register -Address Location= 0x0297) is set to 0x00.*

BIT 4 - Path Payload Mismatch (PLM-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the PLM-P defect condition.The Receive STS-1 POH Processor block will declare the PLM-P defect condition, if it receives at least five (5) consecutive STS-1/STS-3 frames, in which the C2 byte was set to a value other than that which it is expecting to receive. Whenever the Receive STS-1 POH Processor block is determining whether or not it should declare the PLM-P defect, it will check the contents of the following two registers.

- The Receive STS-1 Path - Received Path Label Value Register (Address Location= 0xN196).
- The Receive STS-1 Path - Expected Path Label Value Register (Address Location= 0xN197).

The Receive STS-1 Path - Expected Path Label Value Register contains the value of the C2 bytes, that the Receive STS-1 POH Processor blocks expects to receive.The Receive STS-1 Path - Received Path Label Value Register contains the value of the C2 byte, that the Receive STS-1 POH Processor block has most received validated (by receiving this same C2 byte in five consecutive STS-1/STS-3 frames). The Receive STS-1 POH Processor block will declare the PLM-P defect condition if the contents of these two register do not match. The Receive STS-1 POH Processor block will clear the PLM-P defect condition if whenever the contents of these two registers do match.

- 0 - Indicates that the Receive STS-1 POH Processor block is currently NOT declaring the PLM-P defect condition.
- 1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the PLM-P defect condition

NOTE: *The Receive STS-1 POH Processor block will clear the PLM-P defect, upon declaring the UNEQ-P defect condition.*

BIT 3 - Path Remote Defect Indicator (RDI-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the RDI-P defect condition.

If the Receive STS-1 POH Processor block is configured to support the Single-bit RDI-P function, then it will declare the RDI-P defect condition if BIT 5 (within the G1 byte of the incoming STS-1/STS-3 frame) is set to 1 for RDI-P_THRD number of incoming consecutive STS-1/STS-3 frames.

If the Receive STS-1 POH Processor block is configured to support the Enhanced RDI-P (ERDI-P) function, then it will declare the RDI-P defect condition if Bits 5, 6 and 7 (within the G1 byte of the incoming STS-1/STS-3 frame) are set to [0, 1, 0], [1, 0, 1] or [1, 1, 0] for RDI-P_THRD number of consecutive STS-1/STS-3 frames.

- 0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the RDI-P defect condition.
- 1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the RDI-P defect condition.

NOTE: *The user can specify the value for RDI-P_THRD by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the Receive STS-1 Path - SONET Receive RDI-P Register (Address Location= 0x0293).*

BIT 2 - RDI-P (Path - Remote Defect Indicator) Unstable Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the RDI-P Unstable defect condition. The Receive STS-1 POH Processor block will declare a RDI-P I Unstable defect

condition whenever the RDI-P Unstable Counter reaches the value RDI-P THRD. The RDI-P Unstable counter is incremented for each time that the Receive STS-1 POH Processor block receives an RDI-P value that differs from that of the previous STS-1/STS-3 frame. The RDI-P Unstable counter is cleared to 0 whenever the same RDI-P value is received in RDI-P_THRD consecutive STS-1/STS-3 frames.

NOTE: *Receiving a given RDI-P value, in RDI-P_THRD consecutive STS-1/STS-3 frames also clears this bit-field to 0.*

- 0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the RDI-P Unstable defect condition.
- 1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the RDI-P Unstable defect condition.

NOTE: *The user can specify the value for RDI-P_THRD by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the Receive STS-1 Path - SONET Receive RDI-P Register (Address Location= 0x0293).*

BIT 1 - Loss of Pointer Indicator (LOP-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition.

The Receive STS-1 POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-1 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-1 POH Processor block will clear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive incoming STS-1/STS-3 frames.

- 0 - Indicates that the Receive STS-1 POH Processor block is NOT declaring the LOP-P defect condition.
- 1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the LOP-P defect condition.

BIT 0 - Path AIS (AIS-P) Defect Declared

This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the AIS-P defect condition. The Receive STS-1 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STS-1/STS-3 frames.·

- The H1, H2 and H3 bytes are set to an All Ones pattern.·
- The entire SPE is set to an All Ones pattern.

The Receive STS-1 POH Processor block will clear the AIS-P defect condition when it detects a valid STS-1/STS-3 pointer (H1 and H2 bytes) and a set or normal NDF for three consecutive STS-1/STS-3 frames.

- 0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the AIS-P defect condition.
- 1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the AIS-P defect condition

NOTE: *The Receive STS-1 POH Processor block will NOT declare the LOP-P defect condition if it detects an All Ones pattern in the H1, H2 and H3 bytes. It will, instead, declare the AIS-P defect condition.*

TABLE 134: RECEIVE STS-1 PATH - SONET RECEIVE PATH INTERRUPT STATUS - BYTE 2 (ADDRESS LOCATION= 0X0289)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	Unused	Change in TIM-P Defect Condition Interrupt Status	Change in Path Trace Message Unstable Defect Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT 4 - Detection of AIS Pointer Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of AIS Pointer interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it detects an AIS Pointer in the incoming STS-1/STS-3 data stream.

NOTE: An AIS Pointer is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an All Ones pattern.

- 0 - Indicates that the Detection of AIS Pointer interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of AIS Pointer interrupt has occurred since the last read of this register.

BIT 3 - Detection of Pointer Change Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of Pointer Change Interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the TOH bytes).

- 0 - Indicates that the Detection of Pointer Change Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of Pointer Change Interrupt has occurred since the last read of this register.

BIT 2 - Unused

BIT 1 - Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt

This RESET-upon-READ bit-field indicates whether or not the Change in TIM-P Defect Condition interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- Whenever the Receive STS-1 POH Processor block declares the TIM-P defect condition.
- Whenever the Receive STS-1 POH Processor block clears the TIM-P defect condition.

- 0 - Indicates that the Change in TIM-P Defect Condition Interrupt has not occurred since the last read of this register.
- 1 - Indicates that the Change in TIM-P Defect Condition Interrupt has occurred since the last read of this register.

BIT 0 - Change in Path Trace Identification Message Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in Path Trace Message Unstable Defect Condition Interrupt has occurred since the last read of this register.If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt in response to either of the following events.

- Whenever the Receive STS-1 POH Processor block declare the Path Trace Message Unstable Defect Condition.
- Whenever the Receive STS-1 POH Processor block clears the Path Trace Message Unstable defect condition.

- 0 - Indicates that the Change in Path Trace Message Unstable Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in Path Trace Message Unstable Defect Condition Interrupt has occurred since the last read of this register.

TABLE 135: RECEIVE STS-1 PATH - SONET RECEIVE PATH INTERRUPT STATUS - BYTE 1 (ADDRESS LOCATION= 0X028A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Defect Condition Interrupt Status	Change in PLM-P Defect Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Defect Condition Interrupt Status	Change in RDI-P Unstable Defect Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - New Path Trace Message Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New Path Trace Message Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted (or validated) a new Path Trace Message.

- 0 - Indicates that the New Path Trace Message Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New Path Trace Message Interrupt has occurred since the last read of this register.

BIT 6 - Detection of REI-P Event Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of REI-P Event Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an REI-P event within the incoming STS-1/STS-3 data-stream.

- 0 - Indicates that the Detection of REI-P Event Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of REI-P Event Interrupt has occurred since the last read of this register.

BIT 5 - Change in UNEQ-P (Path - Unequipped) Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in UNEQ-P Defect Condition interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.

- When the Receive STS-1 POH Processor block declares the UNEQ-P Defect Condition.
- When the Receive STS-1 POH Processor block clears the UNEQ-P Defect Condition.

- 0 - Indicates that the Change in UNEQ-P Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in UNEQ-P Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine if the Receive STS-1 POH Processor block is currently declaring the UNEQ-P defect condition by reading out the state of BIT 5 (UNEQ-P Defect Declared) within the Receive STS-1 Path - SONET Receive POH Status - Byte 0 Register (Address Location= 0xN187).*

BIT 4 - Change in PLM-P (Path - Payload Mismatch) Defect Condition Interrupt Status

This RESET-upon-READ bit indicates whether or not the Change in PLM-P Defect Condition interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.

- When the Receive STS-1 POH Processor block declares the PLM-P Defect Condition.
- When the Receive STS-1 POH Processor block clears the PLM-P Defect Condition.

- 0 - Indicates that the Change in PLM-P Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in PLM-P Defect Condition Interrupt has occurred since the last read of this register.

BIT 3 - New C2 Byte Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New C2 Byte Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.

- 0 - Indicates that the New C2 Byte Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New C2 Byte Interrupt has occurred since the last read of this register.

BIT 2 - Change in C2 Byte Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in C2 Byte Unstable Defect Condition Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STS-1 POH Processor block declares the C2 Byte Unstable defect condition.
- When the Receive STS-1 POH Processor block clears the C2 Byte Unstable defect condition.

- 0 - Indicates that the Change in C2 Byte Unstable Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in C2 Byte Unstable Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine whether or not the Receive STS-1 POH Processor block is currently declaring the C2 Byte Unstable Defect Condition by reading out the state of BIT6 (C2 Byte Unstable Defect Declared) within the Receive STS-1 Path - SONET Receive POH Status - Byte 0 Register (Address Location= 0x0287).*

BIT 1 - Change in RDI-P Unstable Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in RDI-P Unstable Defect Condition interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.

- When the Receive STS-1 POH Processor block declares an RDI-P Unstable defect condition.
- When the Receive STS-1 POH Processor block clears the RDI-P Unstable defect condition.

- 0 - Indicates that the Change in RDI-P Unstable Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in RDI-P Unstable Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine the current state of RDI-P Unstable Defect condition by reading out the state of BIT 2 (RDI-P Unstable Defect Condition) within the Receive STS-1 Path - SONET Receive POH Status - Byte 0 Register (Address Location= 0x0287).*

BIT 0 - New RDI-P Value Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the New RDI-P Value interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it receives and validates a new RDI-P value.

- 0 - Indicates that the New RDI-P Value Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the New RDI-P Value Interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the New RDI-P Value by reading out the contents of the RDI-P ACCEPT[2:0] bit-fields. These bit-fields are located in Bits 6 through 4, within the Receive STS-1 Path - SONET Receive RDI-P Register (Address Location= 0x0293).*

TABLE 136: RECEIVE STS-1 PATH - SONET RECEIVE PATH INTERRUPT STATUS - BYTE 0 (ADDRESS LOCATION= 0X028B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Dec-rement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Defect Condition Interrupt Status	Change of AIS-P Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Detection of B3 Byte Error Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of B3 Byte Error Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STS-1/STS-3 data stream.

- 0 - Indicates that the Detection of B3 Byte Error Interrupt has NOT occurred since the last read of this interrupt.

- 1 - Indicates that the Detection of B3 Byte Error Interrupt has occurred since the last read of this interrupt.

BIT 6 - Detection of New Pointer Interrupt Status

This RESET-upon-READ indicates whether the Detection of New Pointer interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1/STS-3 frame.

NOTE: *Pointer Adjustments with NDF will not generate this interrupt.*

- 0 - Indicates that the Detection of New Pointer Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of New Pointer Interrupt has occurred since the last read of this register.

BIT 5 - Detection of Unknown Pointer Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of Unknown Pointer interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime that it detects a pointer that does not fit into any of the following categories.

- An Increment Pointer
- A Decrement Pointer
- An NDF Pointer
- An AIS (e.g., All Ones) Pointer
- New Pointer

- 0 - Indicates that the Detection of Unknown Pointer interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of Unknown Pointer interrupt has occurred since the last read of this register.

BIT 4 - Detection of Pointer Decrement Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of Pointer Decrement Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a Pointer Decrement event.

- 0 - Indicates that the Detection of Pointer Decrement interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of Pointer Decrement interrupt has occurred since the last read of this register.

BIT 3 - Detection of Pointer Increment Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of Pointer Increment Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a Pointer Increment event.

- 0 - Indicates that the Detection of Pointer Increment interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of Pointer Increment interrupt has occurred since the last read of this register.

BIT 2 - Detection of NDF Pointer Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Detection of NDF Pointer interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.

- 0 - Indicates that the Detection of NDF Pointer interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of NDF Pointer interrupt has occurred since the last read of this register.

BIT 1 - Change of LOP-P Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change in LOP-P Defect Condition interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STS-1 POH Processor block declares the LOP-P defect condition.

- ·When the Receive STS-1 POH Processor block clears the LOP-P defect condition.

▶ 0 - Indicates that the Change in LOP-P Defect Condition interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the Change in LOP-P Defect Condition interrupt has occurred since the last read of this register.

NOTE: *The user can determine if the Receive STS-1 POH Processor block is currently declaring the LOP-P defect condition by reading out the state of BIT 1 (LOP-P Defect Declared) within the Receive STS-1 Path - SONET Receive POH Status - Byte 0 Register (Address Location=0x0287).*

BIT 0 - Change of AIS-P Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Change of AIS-P Defect Condition Interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- Whenever the Receive STS-1 POH Processor block declares the AIS-P defect condition.
- Whenever the Receive STS-1 POH Processor block clears the AIS-P defect condition.

▶ 0 - Indicates that the Change of AIS-P Defect Condition Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the Change of AIS-P Defect Condition Interrupt has occurred since the last read of this register.

NOTE: *The user can determine if the Receive STS-1 POH Processor block is currently declaring the AIS-P defect condition by reading out the state of BIT 0 (AIS-P Defect Declared) within the Receive STS-1 Path - SONET Receive POH Status - Byte 0 Register (Address Location= 0x0287).*

TABLE 137: RECEIVE STS-1 PATH - SONET RECEIVE PATH INTERRUPT ENABLE - BYTE 2 (ADDRESS LOCATION = 0X028D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	Unused	Change in TIM-P Defect Condition Interrupt Enable	Change in Path Trace Message Unstable Defect Condition Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - Unused

BIT 4 - Detection of AIS Pointer Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of AIS Pointer interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an AIS Pointer, in the incoming STS-1/STS-3 data stream.

NOTE: *An AIS Pointer is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an All Ones Pattern.*

▶ 0 - Disables the Detection of AIS Pointer Interrupt.

▶ 1 - Enables the Detection of AIS Pointer Interrupt.

BIT 3 - Detection of Pointer Change Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of Pointer Change Interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new pointer value.

▶ 0 - Disables the Detection of Pointer Change Interrupt.

▶ 1 - Enables the Detection of Pointer Change Interrupt.

BIT 2 - Unused

BIT 1 - Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt

This READ/WRITE bit-field is used to either enable or disable the Change in TIM-P Condition interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- If the TIM-P defect condition is declared.
- If the TIM-P defect condition is cleared.

- 0 - Disables the Change in TIM-P Defect Condition Interrupt.
- 1 - Enables the Change in TIM-P Defect Condition Interrupt.

BIT 0 - Change in Path Trace Message Unstable Defect Condition Interrupt Status

This READ/WRITE bit-field is used to either enable or disable the Change in Path Trace Message Unstable Defect Condition Interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- Whenever the Receive STS-1 POH Processor block declares the Path Trace Message Unstable Defect Condition.· Whenever the Receive STS-1 POH Processor block clears the Path Trace Message Unstable Defect Condition.

- 0 - Disables the Change in Path Trace Message Unstable Defect Condition interrupt.
- 1 - Enables the Change in Path Trace Message Unstable Defect Condition interrupt.

TABLE 138: RECEIVE STS-1 PATH - SONET RECEIVE PATH INTERRUPT ENABLE - BYTE 1 (ADDRESS LOCATION= 0X028E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Defect Condition Interrupt Enable	Change in PLM-P Defect Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Defect Condition Interrupt Enable	Change in RDI-P Unstable Defect Condition Interrupt Enable	New RDI-PValue Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - New Path Trace Message Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the New Path Trace Message Interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message.

- 0 - Disables the New Path Trace Message Interrupt.
- 1 - Enables the New Path Trace Message Interrupt.

BIT 6 - Detection of REI-P Event Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of REI-P Event Interrupt.

If this interrupt is enabled, then he Receive STS-1 POH Processor block will generate an interrupt anytime it detects an REI-P condition in the coming STS-1/STS-3 data-stream.

- 0 - Disables the Detection of REI-P Event Interrupt.
- 1 - Enables the Detection of REI-P Event Interrupt.

BIT 5 - Change in UNEQ-P (Path - Unequipped) Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in UNEQ-P Defect Condition interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions

- When the Receive STS-1 POH Processor block declares the UNEQ-P Defect Condition.
- When the Receive STS-1 POH Processor block clears the UNEQ-P Defect Condition.

▶ 0 - Disables the Change in UNEQ-P Defect Condition Interrupt.

▶ 1 - Enables the Change in UNEQ-P Defect Condition Interrupt.

BIT 4 - Change in PLM-P (Path - Payload Label Mismatch) Defect Condition Interrupt Enable

This READ/WRITE bit is used to either enable or disable the Change in PLM-P Defect Condition interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.

- Whenever the Receive STS-1 POH Processor block declares the PLM-P defect Condition.
- Whenever the Receive STS-1 POH Processor block clears the PLM-P defect Condition.

▶ 0 - Disables the Change in PLM-P Defect Condition Interrupt.

▶ 1 - Enables the Change in PLM-P Defect Condition Interrupt.

BIT 3 - New C2 Byte Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the New C2 Byte Interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.

▶ 0 - Disables the New C2 Byte Interrupt.

▶ 1 - Enables the New C2 Byte Interrupt.

NOTE: *The user can obtain the value of this New C2 byte by reading the contents of the Receive STS-1 Path - Received Path Label Value Register (Address Location= 0x0296).*

BIT 2 - Change in C2 Byte Unstable Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in C2 Byte Unstable Condition Interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STS-1 POH Processor block declares the C2 Byte Unstable defect condition.
- When the Receive STS-1 POH Processor block clears the C2 Byte Unstable defect condition.

▶ 0 - Disables the Change in C2 Byte Unstable Defect Condition Interrupt.

▶ 1 - Enables the Change in C2 Byte Unstable Defect Condition Interrupt.

BIT 1 - Change in RDI-P Unstable Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in RDI-P Unstable Defect Condition interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.

- Whenever the Receive STS-1 POH Processor block declares the RDI-P Unstable defect condition.
- Whenever the Receive STS-1 POH Processor block clears the RDI-P Unstable defect condition.

▶ 0 - Disables the Change in RDI-P Unstable Defect Condition Interrupt.

▶ 1 - Enables the Change in RDI-P Unstable Defect Condition Interrupt.

BIT 0 - New RDI-P Value Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the New RDI-P Value interrupt.If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it receives and validates a new RDI-P value.

▶ 0 - Disables the New RDI-P Value Interrupt.

▶ 1 - Enable the New RDI-P Value Interrupt.

TABLE 139: RECEIVE STS-1 PATH - SONET RECEIVE PATH INTERRUPT ENABLE - BYTE 0 (ADDRESS LOCATION= 0X028F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte ErrorInter-ruptEnable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Inter-rupt Enable	Detection of Pointer Dec-rement Inter-rupt Enable	Detection of Pointer IncrementIn-terrupt Enable	Detection of NDF Pointer-Interrupt Enable	Change of LOP-P DefectCondi-tion Interrupt Enable	Change of AIS-P DefectCondi-tionInterrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Detection of B3 Byte Error Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of B3 Byte Error Interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STS-1/STS-3 data-stream.

- 0 - Disables the Detection of B3 Byte Error interrupt.
- 1 - Enables the Detection of B3 Byte Error interrupt.

BIT 6 - Detection of New Pointer Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of New Pointer interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1/STS-3 frame.

NOTE: *:Pointer Adjustments with NDF will not generate this interrupt.*

- 0 - Disables the Detection of New Pointer Interrupt.
- 1 - Enables the Detection of New Pointer Interrupt.

BIT 5 - Detection of Unknown Pointer Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of Unknown Pointer interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a Pointer Adjustment that does not fit into any of the following categories.· An Increment Pointer.· A Decrement Pointer· An NDF Pointer· AIS Pointer· New Pointer.

- 0 - Disables the Detection of Unknown Pointer Interrupt.
- 1 - Enables the Detection of Unknown Pointer Interrupt.

BIT 4 - Detection of Pointer Decrement Interrupt Enable

This READ/WRITE bit-field is used to enable or disable the Detection of Pointer Decrement Interrupt.

If this interrupt is enabled, then the Receive STS-1/STS-3 TOH Processor block will generate an interrupt anytime it detects a Pointer-Decrement event.

- 0 - Disables the Detection of Pointer Decrement Interrupt.
- 1 - Enables the Detection of Pointer Decrement Interrupt.

BIT 3 - Detection of Pointer Increment Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of Pointer Increment Interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a Pointer Increment event.

- 0 - Disables the Detection of Pointer Increment Interrupt.
- 1 - Enables the Detection of Pointer Increment Interrupt.

BIT 2 - Detection of NDF Pointer Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Detection of NDF Pointer Interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects

an NDF Pointer event.

- 0 - Disables the Detection of NDF Pointer interrupt.
- 1 - Enables the Detection of NDF Pointer interrupt.

BIT 1 - Change of LOP-P Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change in LOP (Loss of Pointer) Condition interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STS-1 POH Processor block declares the LOP-P defect condition condition.
- When the Receive STS-1 POH Processor block clears the LOP-P defect condition.

- 0 - Disable the Change of LOP-P Defect Condition Interrupt.
- 1 - Enables the Change of LOP-P Defect Condition Interrupt.

NOTE: *The user can determine the current state of the LOP-P Defect condition by reading out the contents of BIT 1 (LOP-P Defect Declared) within the Receive STS-1 Path - SONET Receive POH Status - Byte 0 (Address Location= 0x0287).*

BIT 0 - Change of AIS-P Defect Condition Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of AIS-P (Path AIS) Defect Condition interrupt.

If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

- When the Receive STS-1 POH Processor block declares the AIS-P Defect condition.
- When the Receive STS-1 POH Processor block clears the AIS-P Defect condition.

- 0 - Disables the Change of AIS-P Defect Condition Interrupt.
- 1 - Enables the Change of AIS-P Defect Condition Interrupt.

NOTE: *The user can determine the current state of the AIS-P Defect Condition by reading out the contents of BIT 0 (AIS-P Defect Declared) within the Receive STS-1 Path - SONET Receive POH Status - Byte 0 (Address Location= 0x0287).*

TABLE 140: RECEIVE STS-1 PATH - SONET RECEIVE RDI-P REGISTER (ADDRESS LOCATION= 0X0293)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RDI-P_ACCEPT[2:0]			RDI-P THRESHOLD[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT [6:4] - Accepted RDI-P Value

These READ-ONLY bit-fields contain the value of the most recently accepted RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value that has been accepted by the Receive STS-1 POH Processor block.

NOTE: *A given RDI-P value will be accepted by the Receive STS-1 POH Processor block, if this RDI-P value has been consistently received in RDI-P THRESHOLD[3:0] number of STS-1/STS-3 frames.*

BIT [3:0] - RDI-P Threshold[3:0]

These READ/WRITE bit-fields are used to defined the RDI-P Acceptance Threshold for the Receive STS-1 POH Processor Block.

The RDI-P Acceptance Threshold is the number of consecutive STS-1/STS-3 frames, in which the Receive STS-1 POH Processor block must receive a given RDI-P value, before it accepts or validates it.

The most recently accepted RDI-P value is written into the RDI-P ACCEPT[2:0] bit-fields, within this register.

TABLE 141: RECEIVE STS-1 PATH - RECEIVED PATH LABEL VALUE (ADDRESS LOCATION= 0X0296)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received_C2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
1	1	1	1	1	1	1	1

BIT [7:0] - Received Filtered C2 Byte Value

These READ-ONLY bit-fields contain the value of the most recently accepted C2 byte, via the Receive STS-1 POH Processor block.

The Receive STS-1 POH Processor block will accept a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive STS-1/STS-3 frames.

NOTE: *The Receive STS-1 POH Processor block uses this register, along the Receive STS-1 Path - Expected Path Label Value Register (Address Location = 0x0297), when declaring or clearing the UNEQ-P and PLM-P defect conditions.*

TABLE 142: RECEIVE STS-1 PATH - EXPECTED PATH LABEL VALUE (ADDRESS LOCATION= 0X0297)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Expected_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT [7:0] - Expected C2 Byte Value

These READ/WRITE bit-fields are used to specify the C2 (Path Label Byte) value, that the Receive STS-1 POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P defect conditions.

If the contents of the Received C2 Byte Value[7:0] (see Receive STS-1 Path - Received Path Label Value register) matches the contents in these register, then the Receive STS-1 POH will not declare any defect conditions.

NOTE: *The Receive STS-1 POH Processor block uses this register, along with the Receive STS-1 Path - Receive Path Label Value Register (Address Location = 0x0296), when declaring or clearing the UNEQ-P and PLM-P defect conditions.*

TABLE 143: RECEIVE STS-1 PATH - B3 BYTE ERROR COUNT REGISTER - BYTE 3 (ADDRESS LOCATION= 0X0298)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Error Count - MSB

This RESET-upon-READ register, along with Receive STS-1 Path - B3 Byte Error Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error.

NOTES:

1. *If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1/STS-3 SPE) that are in error.*
2. *If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 SPE that contains an erred B3 byte.*

TABLE 144: RECEIVE STS-1 PATH - B3 BYTE ERROR COUNT REGISTER - BYTE 2 (ADDRESS LOCATION= 0X0299)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Error Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive STS-1 Path - B3 Byte Error Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error.

NOTES:

1. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1/STS-3 SPE) that are in error.

2. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 SPE that contains an erred B3 byte.

TABLE 145: RECEIVE STS-1 PATH - B3 BYTE ERROR COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X029A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Error Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive STS-1 Path - B3 Byte Error Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error.

NOTES:

1. *If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1/STS-3 SPE) that are in error.*
2. *If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 SPE that contains an erred B3 byte.*

TABLE 146: RECEIVE STS-1 PATH - B3 BYTE ERROR COUNT REGISTER - BYTE 0 (ADDRESS LOCATION= 0X029B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Error Count - LSB

This RESET-upon-READ register, along with Receive STS-1 Path - B3 Byte Error Count Register - Bytes 3 through 1 function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error.

NOTES:

1. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a per-bit basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1/STS-3 SPE) that are in error.

2. f the Receive STS-1 POH Processor block is configured to count B3 byte errors on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 SPE that contains an erred B3 byte.

TABLE 147: RECEIVE STS-1 PATH - REI-P EVENT COUNT REGISTER - BYTE 3 (ADDRESS LOCATION= 0X029C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-P Event Count - MSB

This RESET-upon-READ register, along with Receive STS-1 Path - REI-P Error Count Register - Bytes 2 through 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path - Remote Error Indicator event within the incoming STS-1/STS-3 SPE data-stream.

NOTES:

1. *If the Receive STS-1 POH Processor block is configured to count REI-P events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1/STS-3 SPE.*
2. *If the Receive STS-1 POH Processor block is configured to count REI-P events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 SPE that contains a non-zero REI-P value.*

TABLE 148: RECEIVE STS-1 PATH - REI-P EVENT COUNT REGISTER - BYTE 2 (ADDRESS LOCATION= 0X029D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-P Event Count (Bits 23 through 16)

This RESET-upon-READ register, along with Receive STS-1 Path - REI-P Error Count Register - Bytes 3, 1 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path - Remote Error Indicator event within the inconing STS-1/STS-3 SPE data-stream.

NOTES:

1. If the Receive STS-1 POH Processor block is configured to count REI-P events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1/STS-3 frame.

2. If the Receive STS-1 POH Processor block is configured to count REI-P events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 SPE that contains a non-zero REI-P value.

TABLE 149: RECEIVE STS-1 PATH - REI-P EVENT COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X029E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-P Event Count - (Bits 15 through 8)

This RESET-upon-READ register, along with Receive STS-1 Path - REI-P Error Count Register - Bytes 3, 2 and 0, function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path - Remote Error Indicator event within the incoming STS-1/STS-3 SPE data-stream.

NOTES:

1. If the Receive STS-1 POH Processor block is configured to count REI-P events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1/STS-3 SPE.

2. If the Receive STS-1 POH Processor block is configured to count REI-P events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 SPE that contains a non-zero REI-P value

TABLE 150: RECEIVE STS-1 PATH - REI-P EVENT COUNT REGISTER - BYTE 0 (ADDRESS LOCATION= 0X029F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - REI-P Event Count - LSB

This RESET-upon-READ register, along with Receive STS-1 Path - REI-P Error Count Register - Bytes 3 through 1, function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path - Remote Error Indicator event within the incoming STS-1/STS-3 SPE data-stream.

NOTES:

1. If the Receive STS-1 POH Processor block is configured to count REI-P events on a per-bit basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte.

2. If the Receive STS-1 POH Processor block is configured to count REI-P events on a per-frame basis, then it will increment this 32 bit counter each time that it receives an STS-1/STS-3 SPE that contains a non-zero REI-P value.

TABLE 151: RECEIVE STS-1 PATH - RECEIVE PATH TRACE MESSAGE BUFFER CONTROL REGISTER (ADDRESS LOCATION= 0X02A3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		New Message Ready	Receive Path Trace Message Buffer Read Select	Receive Path Trace Message Accept Threshold	Path Trace Message Alignment Type	Receive Path Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Unused

BIT 5 - New Message Ready

This READ/WRITE bit-field indicates whether or not the Receive Path Trace Message buffer has received a new expected value.

- 0 - Indicates NO new expected value has been downloaded into the receive J1 trace buffer.
- 1 - Indicates a new expected value has been downloaded into the receive J1 trace buffer and can be used to make comparisons with the accepted J1 message.

BIT 4 - Receive Section Trace Message Buffer Read Selection

This READ/WRITE bit-field is used to specify which of the following Receive Path Trace Message buffer segments to

read.

a. The Actual Receive Path Trace Message Buffer. The Actual Receive Path Trace Message Buffer contains the contents of the most recently received (and accepted) Path Trace Message via the incoming STS-1/STS-3 data-stream.

b. The Expected Receive Path Trace Message Buffer. The Expected Receive Path Trace Message Buffer contains the contents of the Path Trace Message that the user expects to receive. The contents of this particular buffer are usually specified by the user.

- 0 - Executing a READ to the Receive J1 Trace Buffer, will return contents within the Valid Message buffer.
- 1 - Executing a READ to the Receive J1 Trace Buffer, will return contents within the Expected Message Buffer.

NOTE: *In the case of the Receive STS-1 POH Processor block, the Receive J1 Trace Buffer is located at Address Location 0x0500 through 0x053F.*

BIT 3 - Path Trace Message Accept Threshold

This READ/WRITE bit-field is used to select the number of consecutive times that the Receive STS-1 POH Processor block must receive a given Receive Trace Message, before it is accepted and loaded into the Receive Path Trace Message.

- 0 - The Receive STS-1 POH Processor block accepts the Path Trace Message after it has received it the third time in succession.
- 1 - The Receive SONET POH Processor block accepts the incoming Path Trace Message after it has received in the fifth time in succession.

BIT 2 - Path Trace Message Alignment Type

This READ/WRITE bit-field is used to specify have the Receive STS-1 POH Processor block will locate the boundary of the J1 Trace Message.

- 0 - Message boundary is indicated by Line Feed.
- 1 - Message boundary is indicated by the presence of a 1 in the MSB of a the first byte (within the J1 Trace Message).

BIT [1:0] - Path Trace Message Length[1:0]

These READ/WRITE bit-fields are used to specify the length of the Receive Path Trace Message that the Receive STS-1 POH Processor block will receive. The relationship between the content of these bit-fields and the corresponding Receive Path Trace Message Length is presented below.

Receive Trace Path Message Length

MSG LENGTH[1:0]	RESULTING PATH TRACE MESSAGE LENGTH
00	1 Byte
01	16 Bytes
10/11	64 Bytes

TABLE 152: RECEIVE STS-1 PATH - POINTER VALUE - BYTE 1 (ADDRESS LOCATION= 0X02A6)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Current_Pointer Val-ueMSB[9:8]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT [1:0]Current Pointer Value - MSB

These READ-ONLY bit-fields, along with that from the Receive STS-1 Path - Pointer Value - Byte 0 Register combine to reflect the current value of the pointer that the Receive STS-1 POH Processor block is using to locate the SPE within the incoming STS-1/STS-3 data stream.Note

These register bits comprise the Upper Byte value of the Pointer Value.

TABLE 153: RECEIVE STS-1 PATH - POINTER VALUE - BYTE 0 (ADDRESS LOCATION= 0X02A7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Current_Pointer_Value_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Current Pointer Value - LSB

These READ-ONLY bit-fields, along with that from the Receive STS-1 Path - Pointer Value - Byte 1 Register combine to reflect the current value of the pointer that the Receive STS-1 POH Processor block is using to locate the SPE within the incoming STS-1/STS-3 data stream.Note

These register bits comprise the Lower Byte value of the Pointer Value.

TABLE 154: RECEIVE STS-1 PATH - RECEIVE AUTO AIS - C2 BYTE VALUE REGISTER (ADDRESS = 0X02B9)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Defect_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Defect_C2_Byte_Value[7:0]

These READ/WRITE bit-fields are used to configure the Receive STS-1 POH Processor block to automatically force the transmission of the DS1/E1 AIS pattern (in the Egress Direction of all 28 channels) anytime it accepts a C2 byte value matching that written into this register.

NOTE: *The chip will only automatically transmit the DS1/E1 AIS Pattern if BIT 1 (Defect C2 Byte Downstream AIS Enable), within the Receive STS-1 Path - Receive Auto AIS - C2 Byte Control Register is set to 1.*

TABLE 155: RECEIVE STS-1 PATH - RECEIVE AUTO AIS - C2 BYTE CONTROL REGISTER (ADDRESS = 0X02BA)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Defect C2 Byte Down-stream AIS Enable	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/O
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT 1] - Defect C2 Byte Downstream AIS Enable

BIT 0 - Unused

TABLE 156: RECEIVE STS-1 PATH - AUTO AIS CONTROL REGISTER (ADDRESS LOCATION= 0X02BB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Transmit AIS-P (Down-stream) Upon C2 Byte Unstable	Transmit AIS-P (Down-stream) Upon UNEQ-P	Transmit AIS-P (Down-stream) Upon PLM-P	Transmit AIS-P (Down-stream) Upon Path Trace Message Unstable	Transmit AIS-P (Down-stream) upon TIM-P	Transmit AIS-P (Down-stream) upon LOP-P	Transmit AIS-P (Down-stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT 6 - Transmit Path AIS (Downstream) upon Declaration of the Unstable C2 Byte Defect Condition

This READ/WRITE bit-field is used to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks), anytime (and for the duration that) it declares the Unstable C2 Byte Defect condition within the incoming STS-1/STS-3 data-stream.

- 0 - Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Unstable C2 Byte defect condition.
- 1 - Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Unstable C2 Byte defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 5 - Transmit Path AIS (Downstream) upon Declaration of the UNEQ-P (Path - Unequipped) Defect Condition

This READ/WRITE bit-field is used to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks), anytime (and for the duration that) it declares the UNEQ-P defect condition.

- 0 - Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the UNEQ-P defect condition.
- 1 - Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the UNEQ-P defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 4 - Transmit Path AIS (Downstream) upon Declaration of the PLM-P (Path - Payload Label Mismatch) Defect Condition

This READ/WRITE bit-field is used to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks), anytime (and for the duration that) it declares the PLM-P defect condition.

- 0 - Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the PLM-P defect condition.
- 1 - Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the PLM-P defect condition.Note

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 3 - Transmit Path AIS (Downstream) upon declaration of the Path Trace Message Unstable Defect Condition

This READ/WRITE bit-field is used to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks), anytime (and for the duration that) it declares the Path Trace Message Unstable defect condition within

the incoming STS-1/STS-3 data-stream.

- 0 - Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Path Trace Message Unstable defect condition.
- 1 - Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic) whenever it declares the Path Trace Message Unstable defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 2 - Transmit Path AIS (Downstream) upon declaration of the TIM-P (Path Trace Message Identification Mismatch) defect condition

This READ/WRITE bit-field is used to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks), anytime (and for the duration that) it declares the TIM-P defect condition within the incoming STS-1/STS-3 data-stream.

- 0 - Does not configure the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the downstream traffic) whenever it declares the TIM-P defect condition.
- 1 - Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the downstream traffic) whenever it declares the TIM-P defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 1 - Transmit Path AIS (Downstream) upon Detection of Loss of Pointer (LOP-P) Defect Condition

This READ/WRITE bit-field is used to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks), anytime (and for the duration that) it declares the LOP-P defect condition within the incoming STS-1/STS-3 data-stream.

- 0 - Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the LOP-P defect condition.
- 1 - Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the LOP-P defect condition.

NOTE: *The user must also set BIT 0 (Transmit AIS-P Enable) to 1 to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*

BIT 0 - Automatic Transmission of AIS-P Enable

This READ/WRITE bit-field serves two purposes.

- It is used to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS indicator, via the down-stream traffic (e.g., towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks), upon detection of an UNEQ-P, PLM-P, LOP-P or LOS conditions.
- It also is used to configure the Receive STS-1 POH Processor block to automatically transmit a Path (AIS-P) Indicator via the downstream traffic (e.g., towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks) anytime it detects an AIS-P condition in the incoming STS-1/STS-3 data-stream.

- 0 - Configures the Receive STS-1 POH Processor block to NOT automatically transmit the AIS-P indicator (via the downstream traffic, towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks) whenever it declares any of the above-mentioned defect conditions.
- 1 - Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the downstream traffic, towards each of the 28 Egress Direction Transmit DS1/E1 Framer blocks) whenever it declares any of the above-mentioned defect condition.

NOTE: *The user must also set the corresponding bit-fields (within this register) to 1 in order to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator upon detection of a given alarm/defect condition.*

TABLE 157: RECEIVE STS-1 PATH - SONET RECEIVE AUTO ALARM REGISTER - BYTE 0 (ADDRESS LOCATION= 0X02C3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Transmit AIS (via Downstream T1/E1s) upon LOP-P	Transmit AIS (via Down-stream T1/E1s) uponPLM-P	Unused	Transmit AIS (via Down-stream T1/E1s) upon UNEQ-P	Transmit AIS (via Down-stream T1/E1s) upon TIM-P	Transmit AIS (via Down-stream T1/E1s) upon AIS-P	Unused
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT 7 - Unused

BIT 6 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon declaration of the LOP-P defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the LOP-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, anytime the Receive STS-1 POH Processor block declares the LOP-P defect.
- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the LOP-P defect.

BIT 5 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon declaration of the PLM-P defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the PLM-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime the Receive STS-1 POH Processor block declares the PLM-P defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the PLM-P defect condition.

BIT 4 - Unused

BIT 3 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon declaration of the UNEQ-P defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the UNEQ-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime the Receive STS-1 POH Processor block declares the UNEQ-P defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the UNEQ-P defect condition.

BIT 2 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon declaration of the TIM-P defect condition

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the TIM-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime the Receive STS-1 POH Processor block declares

the TIM-P defect condition.

- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the TIM-P defect condition.

BIT 1 - Transmit DS1/E1 AIS (via Downstream T1/E1s) upon AIS-P

This READ/WRITE bit-field is used to configure each of the 28 Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the AIS-P defect condition.

- 0 - Does not configure all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS Indicator via the downstream DS1/E1 signal, anytime the Receive STS-1 POH Processor block declares the AIS-P defect condition.
- 1 - Configures all 28 of the Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the AIS-P Indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the AIS-P defect condition.

BIT 0 - Unused

TABLE 158: RECEIVE STS-1 PATH - RECEIVE NEGATIVE POINTER ADJUSTMENT COUNT REGISTER - BYTE 1 (ADDRESS = 0X02C4)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Negative Pointer Adjustment Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Negative Pointer Adjustment Count - MSB

These RESET-upon-READ bits, along with that in Receive STS-1 Path - Receive Negative Pointer Adjustment Count Register - Byte 0 present a 16-bit representation of the number of Negative (or Decrementing) Pointer Adjustments that the Receive STS-1 POH Processor block has detected since the last read of these registers.

NOTE: *This register contains the MSB (Most Significant Bits) of this 16-bit expression.*

TABLE 159: RECEIVE STS-1 PATH - RECEIVE NEGATIVE POINTER ADJUSTMENT COUNT REGISTER - BYTE 0 (ADDRESS = 0X02C5)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Negative Pointer Adjustment Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Negative Pointer Adjustment Count - LSB

These RESET-upon-READ bits, along with that in Receive STS-1 Path - Receive Negative Pointer Adjustment Count Register - Byte 1 present a 16-bit representation of the number of Negative (or Decrementing) Pointer Adjustments that the Receive STS-1 POH Processor block has detected since the last read of these registers.

NOTE: *This register contains the LSB (Least Significant Bits) of this 16-bit expression.*

TABLE 160: RECEIVE STS-1 PATH - RECEIVE POSITIVE POINTER ADJUSTMENT COUNT REGISTER - BYTE 1 (ADDRESS = 0X02C6)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Positive Pointer Adjustment Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Positive Pointer Adjustment Count - MSB

These RESET-upon-READ bits, along with that in Receive STS-1 Path - Receive Positive Pointer Adjustment Count Register - Byte 0 present a 16-bit representation of the number of Positive (or Incrementing) Pointer Adjustments that the Receive STS-1 POH Processor block has detected since the last read of these registers.

NOTE: *This register contains the MSB (Most Significant Bits) of this 16-bit expression.*

TABLE 161: RECEIVE STS-1 PATH - RECEIVE POSITIVE POINTER ADJUSTMENT COUNT REGISTER - BYTE 0 (ADDRESS = 0X02C7)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Positive Pointer Adjustment Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Positive Pointer Adjustment Count - LSB

These RESET-upon-READ bits, along with that in Receive STS-1 Path - Receive Positive Pointer Adjustment Count Register - Byte 1 present a 16-bit representation of the number of Positive (or Incrementing) Pointer Adjustments that the Receive STS-1 POH Processor block has detected since the last read of these registers.

NOTE: *This register contains the LSB (Least Significant Bits) of this 16-bit expression.*

TABLE 162: RECEIVE STS-1 PATH - RECEIVE J1 BYTE CAPTURE REGISTER (ADDRESS LOCATION= 0X02D3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
J1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - J1 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received STS-1/STS-3 frame. This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new J1 byte value.

TABLE 163: RECEIVE STS-1 PATH - RECEIVE B3 BYTE CAPTURE REGISTER (ADDRESS LOCATION= 0X02D7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - B3 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received STS-1/STS-3 frame.

This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new B3 byte value.

TABLE 164: RECEIVE STS-1 PATH - RECEIVE C2 BYTE CAPTURE REGISTER (ADDRESS LOCATION= 0X02DB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
C2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - C2 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received STS-1/STS-3 frame. This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new C2 byte value.

TABLE 165: RECEIVE STS-1 PATH - RECEIVE G1 BYTE CAPTURE REGISTER (ADDRESS LOCATION= 0X02DF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
G1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - G1 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the G1 byte, within the most recently received STS-1/STS-3 frame. This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new G1 byte value.

TABLE 166: RECEIVE STS-1 PATH - RECEIVE F2 BYTE CAPTURE REGISTER (ADDRESS LOCATION=0X02E3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - F2 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received STS-1/STS-3 frame. This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new F2 byte value.

TABLE 167: RECEIVE STS-1 PATH - RECEIVE H4 BYTE CAPTURE REGISTER (ADDRESS LOCATION= 0X02E7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - H4 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received STS-1/STS-3 frame. This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new H4 byte value.

TABLE 168: RECEIVE STS-1 PATH - RECEIVE Z3 BYTE CAPTURE REGISTER (ADDRESS LOCATION= 0X02EB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Z3 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received STS-1/STS-3 frame. This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new Z3 byte value.

TABLE 169: RECEIVE STS-1 PATH - RECEIVE Z4 (K3) BYTE CAPTURE REGISTER (ADDRESS LOCATION= 0X02EF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Z4 (K3) Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the Z4 (K3) byte, within the most recently received STS-1/STS-3 frame. This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new Z4 (K3) byte value.

TABLE 170: RECEIVE STS-1 PATH - RECEIVE Z5 BYTE CAPTURE REGISTER (ADDRESS LOCATION= 0X02F3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Z5 Byte Captured Value[7:0]

These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received STS-1/STS-3 frame.

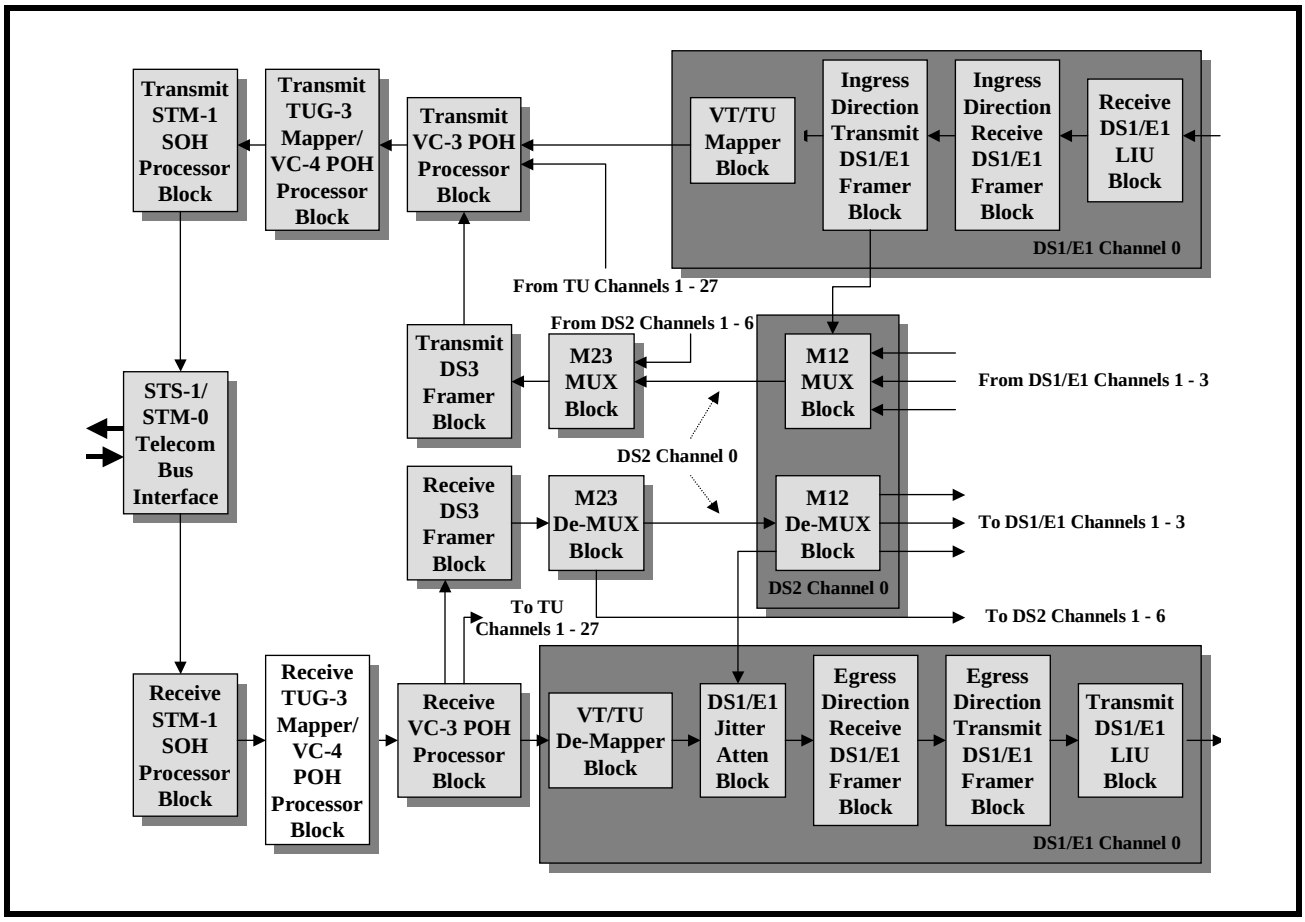
This particular value is stored in this register for one STS-1/STS-3 frame period. During the next STS-1/STS-3 frame period, this value will be overridden with a new Z5 byte value.

2.5 RECEIVE TUG-3 MAPPER/VC-4 POH PROCESSOR BLOCK REGISTERS (SDH/TUG-3 APPLICATIONS ONLY)

The register map for the Receive TU-3 Mapper/VC-4 POH Processor block is presented and discussed in detail within the "SDH Version of the Register Map".

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328 device, with the Receive TUG-3 Maper/VC-4 POH Processor block "highlighted" is presented below in Figure 5.

FIGURE 5. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328 DEVICE, WITH THE RECEIVE TUG-3 MAPPER/VC-4 POH PROCESSOR BLOCK "HIGHLIGHTED"



For detailed on the "Receive TUG-3 Mapper/VC-4 POH Processor Block" Registers, please see the "XRT86SH328 28-Channel DS1/E1 Framer/LIU with DS3 MUX and TU-Mapper IC - Register Map & Description - SDH Applications"

2.6 TRANSMIT STS-1/STS-3 TOH PROCESSOR BLOCK REGISTERS

The register map for the Transmit STS-1/STS-3 TOH Processor block is presented in the Table below. Additionally, a detailed description of each of the Transmit STS-1/STS-3 TOH Processor Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328, with the Transmit STS-1/STS-3 TOH Processor Block highlighted is presented below in Figure 6.

FIGURE 6. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WITH THE TRANSMIT STS-1/STS-3 TOH PROCESSOR BLOCK HIGHLIGHTED

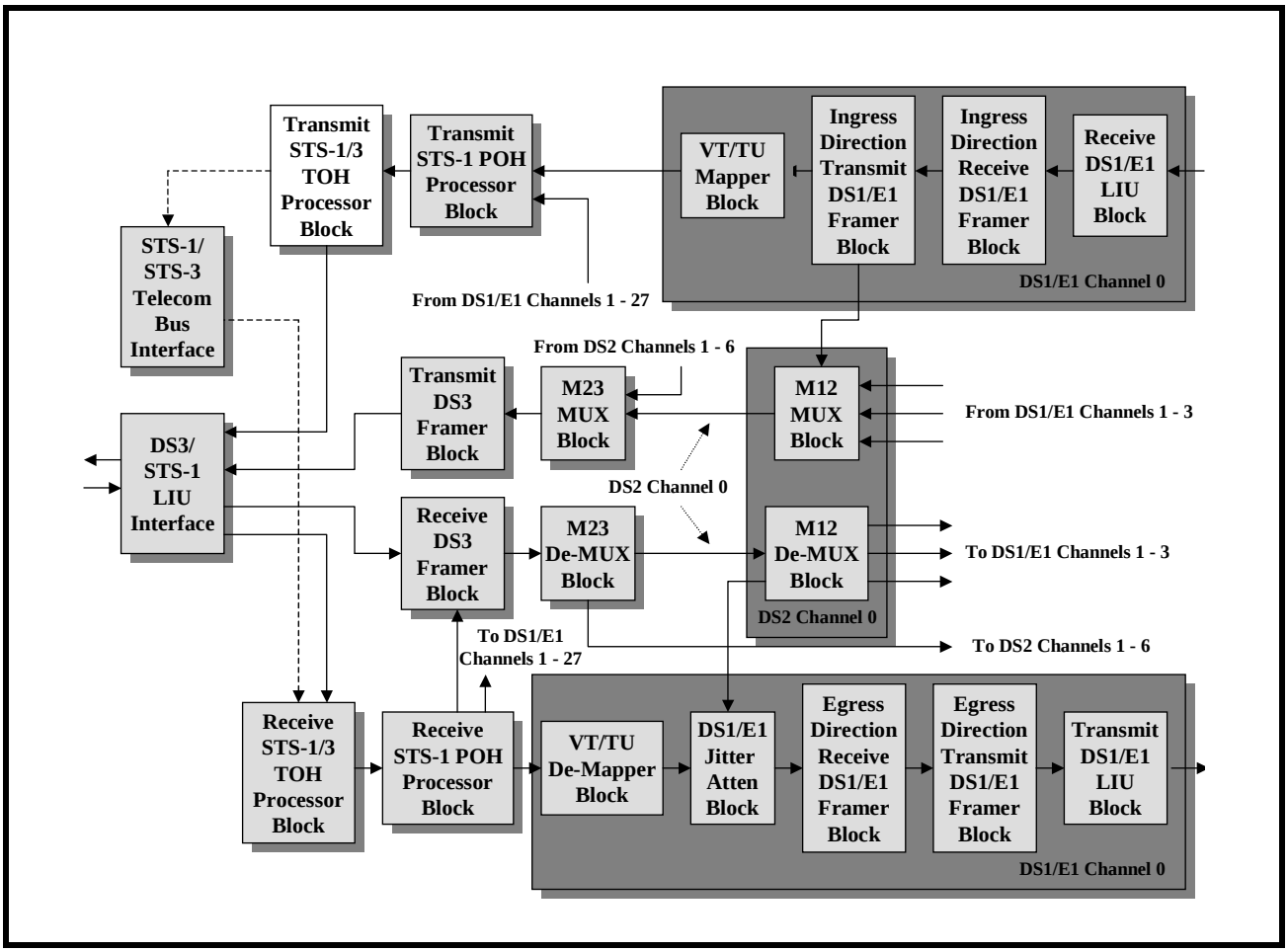


TABLE 171: TRANSMIT STS-1/STS-3 TRANSPORT- TRANSMIT CONTROL REGISTER - BYTE 3 (ADDRESS LOCATION = 0X0700)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Control_Pointer[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT [3:0] - Control_Pointer[3:0]

TABLE 172: TRANSMIT STS-1/STS-3 TRANSPORT - TRANSMIT CONTROL REGISTER - BYTE 2 (ADDRESS LOCATION = 0X0701)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Auto Transmit AIS-L Enable	Section DCC Relocate	Line DCC Relocate				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:3] - Unused

BIT 2 - Auto Transmit AIS-L Enable

BIT 1 - Section DCC Relocate

BIT 0 - Line DCC Relocate

TABLE 173: TRANSMIT STS-1/STS-3 TRANSPORT - TRANSMIT CONTROL REGISTER - BYTE 1 (ADDRESS LOCATION= 0X0702)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		E2 Insert-Method	E1 Insert Method	F1 Insert Method	S1 Insert Method	K1K2 Insert Method	M0M1 Insert Method[1]
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Unused

BIT 5 - E2 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the E2 byte, within the transmit output STS-1/STS-3 or STS-3 data stream.

0 - E2 Byte is obtained from TxTOH Serial Input Port.]

1 - E2 Byte is obtained from the contents within the Transmit Transport - E2 Byte Value register (Address Location = 0x0747). This selection provides the user with software control over the value of the outbound E2 byte.

BIT 4 - E1 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the E1 byte, within the transmit output STS-1 or STS-3 data stream.

0 - E1 Byte is obtained from TxTOH Serial Input Port.

1 - E1 Byte is obtained from the contents within the Transmit Transport - E1 Byte Value register (Address Location= 0x0743). This selection provides the user with software control over the value of the outbound E1 byte.

BIT 3 - F1 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the F1 byte, within the transmit output STS-1 or STS-3 data stream.

0 - F1 Byte is obtained from TxTOH Serial Input Port.

1 - F1 Byte is obtained from the contents within the Transmit Transport - F1 Byte Value register (Address Location= 0x073F). This selection provides the user with software control over the value of the outbound F1 byte.

BIT 2 - S1 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the S1 byte, within the transmit output STS-1 or STS-3 data stream.

0 - S1 Byte is obtained from TxTOH Serial Input Port.

1 - S1 Byte is obtained from the contents within the Transmit Transport - S1 Byte Value register (Address Location= 0x073B). This selection provides the user with software control over the value of the outbound S1 byte.

BIT 1 - K1K2 Byte Insert Method

This READ/WRITE bit-field is used to specify the source of the contents of the K1 and K2 bytes, within the transmit output STS-1 or STS-3 data stream.

0 - K1 and K2 Bytes are obtained from TxTOH Serial Input Port.

1 - K1 and K2 Bytes are obtained from the contents within the Transmit Transport - K1K2 Byte Value register - Byte 1 (Address Location= 0x072E) and the Transmit Transport - K1K2 Byte Value register - Byte 2 (Address Location= 0x072F). This selection provides the user with software control over the value of the outbound K1 and K2 bytes.

BIT 0 - M0M1 Insert Method

This READ/WRITE bit-field, along with M0M1 Insert Method[0] (located in the Transmit Transport - SONET Control Register - Byte 0) are used to specify the source of the contents of the M0/M1 byte, within the transmit output STS-1 or STS-3 data stream. The relationship between these two bit-fields and the corresponding source of the M0/M1 byte is presented below.

Source of M)/M1 Byte

M0M1 Insert Method[1:0]		Source of M0/M1 Byte
0	0	From the Receive STS-1/STS-3 TOH Processor block (B2 byte (or BIP-24) Error Count)
0	1	Obtained from the contents of the Transmit STS-1/STS-3 Transport - M0/M1 Byte Value register (Address Location= 0x0737).
1	0	M0/M1 byte is obtained from the TxTOH Serial Input Port.
1	1	From the Receiver STS-1/STS-3 TOH Processor block (B2 byte (or BIP-24) Error Count).

Table 174: Transmit STS-1/STS-3 Transport - Transmit Control Register - Byte 0 (Address Location= 0x0703)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M0M1 Insert Method[0]	Unused	RDI-L Force	AIS-L Force	LOSForce	Scramble Enable	B2 Error Insert	A1A2 Error Insert
R/W	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - M0M1 Insert Method

This READ/WRITE bit-field, along with M0M1 Byte Insert Method[1] (located in the Transmit STS-1/STS-3 Transport - SONET Control Register - Byte 1) are used to specify the source of the contents of the M0/M1 byte, within the transmit output STS-1 or STS-3 data stream. The relationship between these two bit-fields and the corresponding source of the M0/M1 byte is presented below.

Source of M0/M1 Byte

M0M1 Byte Insert Method[1:0]		Source of M0/M1 Byte
0	0	From the Receive STS-1/STS-3 TOH Processor block (B2 Byte Error Count)
0	1	Obtained from the contents of the Transmit STS-1/STS-3 Transport - M0/M1 Byte Value register (Address Location= 0x0737).
1	0	M0/M1 byte is obtained from the TxTOH Serial Input Port.
1	1	From the Receive STS-1/STS-3 TOH Processor block (B2 Byte Error Count).

BIT6 - Unused

BIT 5 - Transmit Line - Remote Defect Indicator

This READ/WRITE bit-field is used to (by software control) force the Transmit STS-1/STS-3 TOH Processor block to generate and transmit the RDI-L indicator to the remote terminal equipment.

- 0 - Does not configure the Transmit STS-1/STS-3 TOH Processor block to generate and transmit the RDI-L indicator.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to generate and transmit the RDI-L indicator.

In this case, the Transmit STS-1/STS-3 TOH Processor block will force bits 6, 7 and 8 (of the K2 byte) to the value 1, 1, 0.

NOTE: *This bit-field is ignored if the Transmit STS-1/STS-3 TOH Processor block is currently transmitting the Line AIS (AIS-L) indicator or LOS pattern.*

BIT 4 - Transmit Line - AIS Indicator

This READ/WRITE bit-field is used to (by software control) force the Transmit STS-1/STS-3 TOH Processor block to generate and transmit the AIS-L indicator to the remote terminal equipment.

- 0 - Does not configure the Transmit STS-1/STS-3 TOH Processor block to generate and transmit the AIS-L indicator.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to generate and transmit the AIS-L indicator.

In this case, the Transmit STS-1/STS-3 TOH Processor block will force all bits (within the outbound STS-1 or STS-3 frame) with the exception of the Section Overhead Bytes to an All Ones pattern.

NOTE: *This bit-field is ignored if the Transmit STS-1/STS-3 TOH Processor block is transmitting the LOS pattern.*

BIT 3 - Transmit LOS Pattern

This READ/WRITE bit-field is used to (by software control) force the Transmit STS-1/STS-3 TOH Processor block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment.

- 0 - Does not configure the Transmit STS-1/STS-3 TOH Processor block to generate and transmit the LOS pattern.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to transmit the LOS pattern. In this case, the Transmit STS-1/STS-3 TOH Processor block will force all bytes (within the outbound SONET frame) to an All Zeros pattern.

BIT 2 - Scramble Enable

This READ/WRITE bit-field is used to either enable or disable the Scrambler, within the Transmit STS-1/STS-3 TOH Processor block circuitry.

- 0 - Disables the Scrambler.
- 1 - Enables the Scrambler.

BIT 1 - Transmit B2 Byte Error Insert Enable

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 TOH Processor block to insert errors into the outbound B2 bytes, per the contents within the Transmit STS-1/STS-3 Transport - Transmit B2 Byte Error Mask Register.

- 0 - Configures the Transmit STS-1/STS-3 TOH Processor block to NOT insert errors into the B2 bytes, within the outbound STS-1 or STS-3 signal.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to insert into the B2 bytes (per the contents within the Transmit B2 Byte Error Mask Register).

BIT 0 - Transmit A1A2 Byte Error Insert Enable

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 TOH Processor block to insert errors into the outbound A1 and A2 bytes, within the outbound STS-1 or STS-3 data-stream.

- 0 - Configures the Transmit STS-1/STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-1 or STS-3 Data-stream.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to insert errors into the A1 and A2 bytes, within the outbound STS-1 or STS-3 Data-stream.

TABLE 175: TRANSMIT STS-1/STS-3 TRANSPORT - TRANSMIT A1 BYTE ERROR REGISTER (ADDRESS LOCATION = 0X0717)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Transmit Erred A1Byte Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Unused

BIT 0 - Transmit Erred A1 Byte Enable

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 TOH Processor block to transmit a continuous stream of STS-1 or STS-3 frames, in which the A1 byte is erred.

- 0 - Configures the Transmit STS-1/STS-3 TOH Processor block to NOT transmit STS-1 or STS-3 frames with erred A1 bytes.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to transmit STS-1 or STS-3 frames with erred A1 bytes.

TABLE 176: TRANSMIT STS-1/STS-3 TRANSPORT - TRANSMIT A2 BYTE ERROR REGISTER (ADDRESS LOCATION = 0X071F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Transmit Erred A2 Byte Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Unused

BIT 0 - Transmit Erred A2 Byte Enable

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 TOH Processor block to transmit a continuous stream of STS-1 or STS-3 frames, in which the A2 byte is erred.

- 0 - Configures the Transmit STS-1/STS-3 TOH Processor block to NOT transmit STS-1 or STS-3 frames with erred A2 bytes.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to transmit STS-1 or STS-3 frames with erred A2 bytes.

TABLE 177: TRANSMIT STS-1/STS-3 TRANSPORT - TRANSMIT B1 BYTE ERROR MASK REGISTER (ADDRESS LOCATION = 0X0723)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0]B1 Byte Error Mask[7:0]

These READ/WRITE bit-fields are used to insert bit errors into the B1 bytes, within the outbound STS-1 or STS-3 Data stream. The Transmit STS-1/STS-3 TOH Processor block will perform an XOR operation with the contents of the B1 byte, and this register. The results of this calculation will be inserted into the B1 byte position within the outbound STS-1 or STS-3 Data stream. For each bit-field (within this register) that is set to 1, the corresponding bit, within the B1 byte will be in error.

NOTE: For normal operation, the user should set this register to 0x00.

TABLE 178: TRANSMIT STS-1/STS-3 TRANSPORT - TRANSMIT B2 BYTE ERROR MASK REGISTER (ADDRESS LOCATION = 0X0727)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Transmit B2 Error Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:1] - Unused]

BIT 0 - Transmit B2 Byte Error Enable

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 TOH Processor block to perform the XOR operation with the contents of the Transmit STS-1/STS-3 Transport -Transmit B2 Bit Error Mask Register (Address Location = 0x072B)

- 0 - Disables the XOR operation. In this case, the Transmit STS-1/STS-3 TOH Processor block will NOT perform the XOR operation with the Transmit STS-1/STS-3 Transport - Transmit B2 Bit Error Mask Register. As a consequence, the Transmit STS-1/STS-3 TOH Processor block will transmit a continuous stream of STS-1s with no B2 byte errors.
- 1 - Enables the XOR operation. In this setting, the Transmit STS-1/STS-3 TOH Processor will perform the XOR operation of the value of the B2 byte (within the outbound STS-1 or STS-3 frame) with the contents within the Transmit STS-1/STS-3 Transport - Transmit B2 Bit Error Mask register.

TABLE 179: TRANSMIT STS-1/STS-3 TRANSPORT - TRANSMIT B2 BIT ERROR MASK REGISTER (ADDRESS LOCATION= 0X072B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_B2_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit B2 Error Mask-Byte

These READ/WRITE bit-fields are used to insert B2 byte errors into the outbound STS-1 or STS-3 Data-stream, for diagnostic purposes.

If BIT 0 (Transmit B2 Error Enable) within the Transmit STS-1/STS-3 Transport - Transmit B2 Byte Error Register (Address Location = 0xN927) is set to 1, then Transmit STS-1/STS-3 TOH Processor block will be configured to perform an XOR operation between the contents of this register, with the contents of the outbound B2 byte. The results of this calculation is written back into the B2 byte position, within the outbound STS-1 or STS-3 Data. Hence, for every bit (within this register) that is set to 1, the corresponding bit (within the outbound B2 byte) will be erred.

NOTES:

1. *1. For normal (e.g., un-erred) operation, the user should ensure that this register is set to the value 0x00.*
2. *These register bits are ignored unless BIT 0 (Transmit B2 Error Enable), within the Transmit STS-1/STS-3 Transport - Transmit B2 Byte Error Register has been set to 1.*

TABLE 180: TRANSMIT STS-1/STS-3 TRANSPORT - K2 BYTE VALUE REGISTER - BYTE 1 (ADDRESS LOCATION= 0X072E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_K2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit K2 Byte Value

If the appropriate K1K2 Insert Method is selected, then these READ/WRITE bit-fields will are used to specify the contents of the K2 byte, within the outbound STS-1/STS-3 signal.

NOTE: *If BIT 1 (K1K2 Insert Method) within the Transmit STS-1/STS-3 Transport - SONET Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STS-1/STS-3 TOH Processor block will load the contents of this register into the K2 byte-field, within each outbound STS-1 or STS-3 frame. These register bits are ignored if BIT 1 (K1K2 Insert Method) is set to 0.*

TABLE 181: TRANSMIT STS-1/STS-3 TRANSPORT - K1 BYTE VALUE REGISTER - BYTE 1 (ADDRESS LOCATION= 0X072F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_K1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit K1 Byte Value

If the appropriate K1K2 Insert Method is selected, then these READ/WRITE bit-fields will are used to specify the contents of the K1 byte, within the outbound STS-1/STS-3 signal.

NOTE: *If BIT 1 (K1K2 Insert Method) within the Transmit STS-1/STS-3 Transport - SONET Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STS-1/STS-3 TOH Processor block will load the contents of this register into the K1 byte-field, within each outbound STS-1 or STS-3 frame. These register bits are ignored if BIT 1 (K1K2 Insert Method) is set to 0.*

TABLE 182: TRANSMIT STS-1/STS-3 TRANSPORT - RDI-L CONTROL REGISTER (ADDRESS LOCATION= 0X0733)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				External RDI-L Enable	Transmit RDI-L upon AIS	Transmit RDI-L upon LOF	Transmit RDI-L upon LOS
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT 3 - External Transmit Line Remote Defect Indicator (RDI-L) Enable

This READ/WRITE bit-field is used to externally insert the value for bits 6, 7 and 8 (of the K2 byte) into the outbound STS-1 or STS-3 Data stream. If the user enables this feature, then the user can enable or disable the insertion of the RDI-L indicator, via the TxPOH_n input pin.

0 - Disables this feature.

1 - Enables this feature.

BIT 2 - Transmit Line Remote Defect Indicator (RDI-L) upon Detection of AIS-L

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 TOH Processor block to automatically transmit a RDI-L indicator to the remote terminal anytime (and for the duration) that the Receive STS-1/STS-3 TOH Processor block is detecting a Line AIS (AIS-L) indicator.

- 0 - Configures the Transmit STS-1/STS-3 TOH Processor block to NOT automatically transmit the RDI-L indicator, upon the Receive STS-1/STS-3 TOH Processor block detecting the AIS-L indicator.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to automatically transmit the RDI-L indicator, upon the Receive STS-1/STS-3 TOH Processor block detecting the AIS-L indicator.

BIT 1 - Transmit Line Remote Defect Indicator (RDI-L) upon Detection of LOF

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 TOH Processor block to automatically transmit a RDI-L indicator to the remote terminal anytime (and for the duration) that the Receive STS-1/STS-3 TOH Processor block is declaring the LOF defect

- .0 - Configures the Transmit STS-1/STS-3 TOH Processor block to NOT automatically transmit the RDI-L indicator, whenever the Receive STS-1/STS-3 TOH Processor block declares the LOF defect.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to automatically transmit the RDI-L indicator, whenever the Receive STS-1/STS-3 TOH Processor block declares the LOF defect.

BIT 0 - Transmit Line Remote Defect Indicator (RDI-L) upon Detection of LOS

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 TOH Processor block to automatically transmit a RDI-L indicator to the remote terminal anytime (and for the duration) that the Receive STS-1/STS-3 TOH Processor block is declaring the LOS defect.

- 0 - Configures the Transmit STS-1/STS-3 TOH Processor block to NOT automatically transmit the RDI-L indicator, whenever the Receive STS-1/STS-3 TOH Processor block declares the LOS defect.
- 1 - Configures the Transmit STS-1/STS-3 TOH Processor block to automatically transmit the RDI-L indicator, whenever the Receive STS-1/STS-3 TOH Processor block declares the LOS defect.

TABLE 183: TRANSMIT STS-1/STS-3 TRANSPORT - M0M1 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X0737)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_M0M1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit M0M1 Byte Value

If the appropriate M0M1 Insert Method is selected, then these READ/WRITE bit-fields will are used to specify the contents of the M0M1 byte, within the outbound STS-1/STS-3 signal.

NOTE: *If BIT 0 (M0M1 Insert Method - BIT 1) within the Transmit STS-1/STS-3 Transport - SONET Transmit Control Register - Byte 1 (Address Location= 0x0702) and BIT7 (M0M1 Byte Insert Method - BIT 0) within the Transmit STS-1/STS-3 Transport - SONET Transmit Control Register - Byte 0 (Address Location= 0x0703) are set to 0, 1, then the STS-1/STS-3 Transmit block will load the contents of this register into the M0M1 byte-field, within each outbound STS-1 or STS-3 frame. These register bits are ignored if the M0M1 Insert Method[1:0] bits are set to any value other than 0, 1.*

TABLE 184: TRANSMIT STS-1/STS-3 TRANSPORT - S1 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X073B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_S1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit S1 Byte Value

If the appropriate S1 Insert Method is selected, then these READ/WRITE bit-fields will are used to specify the contents of the S1 byte, within the outbound STS-1/STS-3 signal. If BIT 2 (S1 Insert Method) within the Transmit STS-1/STS-3

Transport - SONET Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the STS-1/STS-3 Transmit block will load the contents of this register into the S1 byte-field, within each outbound STS-1 or STS-3 frame.

NOTE: *These register bits are ignored if BIT 2 (S1 Insert Method) is set to 0.*

TABLE 185: TRANSMIT STS-1/STS-3 TRANSPORT - F1 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X073F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_F1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit F1 Byte Value

If the appropriate F1 Byte Insert Method is selected, then these READ/WRITE bit-fields will are used to specify the contents of the F1 byte, within the outbound STS-1/STS-3 signal.

NOTE: *If BIT 3 (F1 Byte Insert Method) within the Transmit STS-1/STS-3 Transport - SONET Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STS-1/STS-3 TOH Processor block will load the contents of this register into the F1 byte-field, within each outbound STS-1 or STS-3 frame. These register bits are ignored if BIT 3 (F1 Insert Method) is set to 0.*

TABLE 186: TRANSMIT STS-1/STS-3 TRANSPORT - E1 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X0743)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_E1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit E1 Byte Value

If the appropriate E1 Byte Insert Method is selected, then these READ/WRITE bit-fields will are used to specify the contents of the E1 byte, within the outbound STS-1/STS-3 signal. Note

NOTE: *If BIT 4 (E1 Insert Method) within the Transmit STS-1/STS-3 Transport - SONET Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STS-1/STS-3 TOH Processor block will load the contents of this register into the E1 byte-field, within each outbound STS-1 or STS-3 frame. These register bits are ignored if BIT 4 (E1 Insert Method) is set to 0.*

TABLE 187: TRANSMIT STS-1/STS-3 TRANSPORT - E2 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X0747)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_E2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit E2 Byte Value

If the appropriate E2 Byte Insert Method is selected, then these READ/WRITE bit-fields will are used to specify the contents of the E2 byte, within the outbound STS-1/STS-3 signal.

NOTE: *If BIT 5 (E2 Insert Method) within the Transmit STS-1/STS-3 Transport - SONET Transmit Control Register - Byte 1 (Address Location= 0x0702) is set to 1, then the Transmit STS-1/STS-3 TOH Processor block will load the contents of this register into the E2 byte-field, within each outbound STS-1 or STS-3 frame. These register bits are ignored if BIT 5 (E2 Insert Method) is set to 0.*

TABLE 188: TRANSMIT STS-1/STS-3 TRANSPORT - J0 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X074B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_J0_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit J0 Byte Value

These READ/WRITE bits are used to specify the value of the J0 byte, that will be transmitted via the Transport Overhead, within the very next STS-1 or STS-3 frame. This register is only valid if the Transmit STS-1/STS-3 TOH Processor block is configured to read out the contents from this register and insert it into the J0 byte-field within each outbound STS-1 or STS-3 frame. The user accomplishes this by setting Bits 1 and 0 (J0_TYPE), within the Transmit STS-1/STS-3 Transport - J0 Byte Control Register (Address Location= 0x074F) to 1, 0.

TABLE 189: TRANSMIT STS-1/STS-3 TRANSPORT - TRANSMITTER J0 BYTE CONTROL REGISTER (ADDRESS LOCATION= 0X074F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Message Length[1:0]		J0_TYPE[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT [3:2] - Message Length[1:0]

These two READ/WRITE bit-fields are used to specify the length of the message that is to be repetitively transmitted via the J0 byte as shown in the table below.

Message Length

MSG_LENGTH[1:0]	CORRESPONDING MESSAGE LENGTH(BYTES)
00	1 Byte
01	16 Bytes
10 or 11	64 Bytes

BIT [1:0] - Transmit J0 Source[1:0]

These two READ/WRITE bit-fields are used to specify the source of the message that will be transported via the J0 byte/message, within the outbound STS-1 or STS-3 Data-stream, as shown in the table below

Source of J0 Byte Message

0_TYPE[1:0]	CORRESPONDING SOURCE OF J0 BYTE/MESSAGE.
00	Automatically set the J0 Byte, in each outbound STS-1 or STS-3 frame to 0x01.
01	The Transmit Section TraceMessage BufferThe Transmit STS-1/STS-3 Section Trace Buffer Memory is located at Address locations 0x0900 through 0x093F.

Source of J0 Byte Message

0_TYPE[1:0]	CORRESPONDING SOURCE OF J0 BYTE/MESSAGE.
10	From the Transmit J0 Byte Value[7:0] Register. In this setting, the Transmit STS-1/STS-3 TOH Processor block will read out the contents of the Transmit J0 Value[7:0] Register (Address Location= 0x074B), and will insert this value into the J0 byte of each outbound STS-1 or STS-3 frame.
11	From the TxPOH_n Input pin.

2.7 TRANSMIT STS-1/STS-3 POH PROCESSOR BLOCK REGISTERS

The register map for the Transmit STS-1/STS-3 POH Processor block is presented in the Table below. Additionally, a detailed description of each of the Transmit STS-1/STS-3 POH Processor block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328, with the Transmit STS-1/STS-3 POH Processor block highlighted is presented below in Figure 7.

FIGURE 7. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WITH THE TRANSMIT STS-1/STS-3 POH PROCESSOR BLOCK HIGHLIGHTED

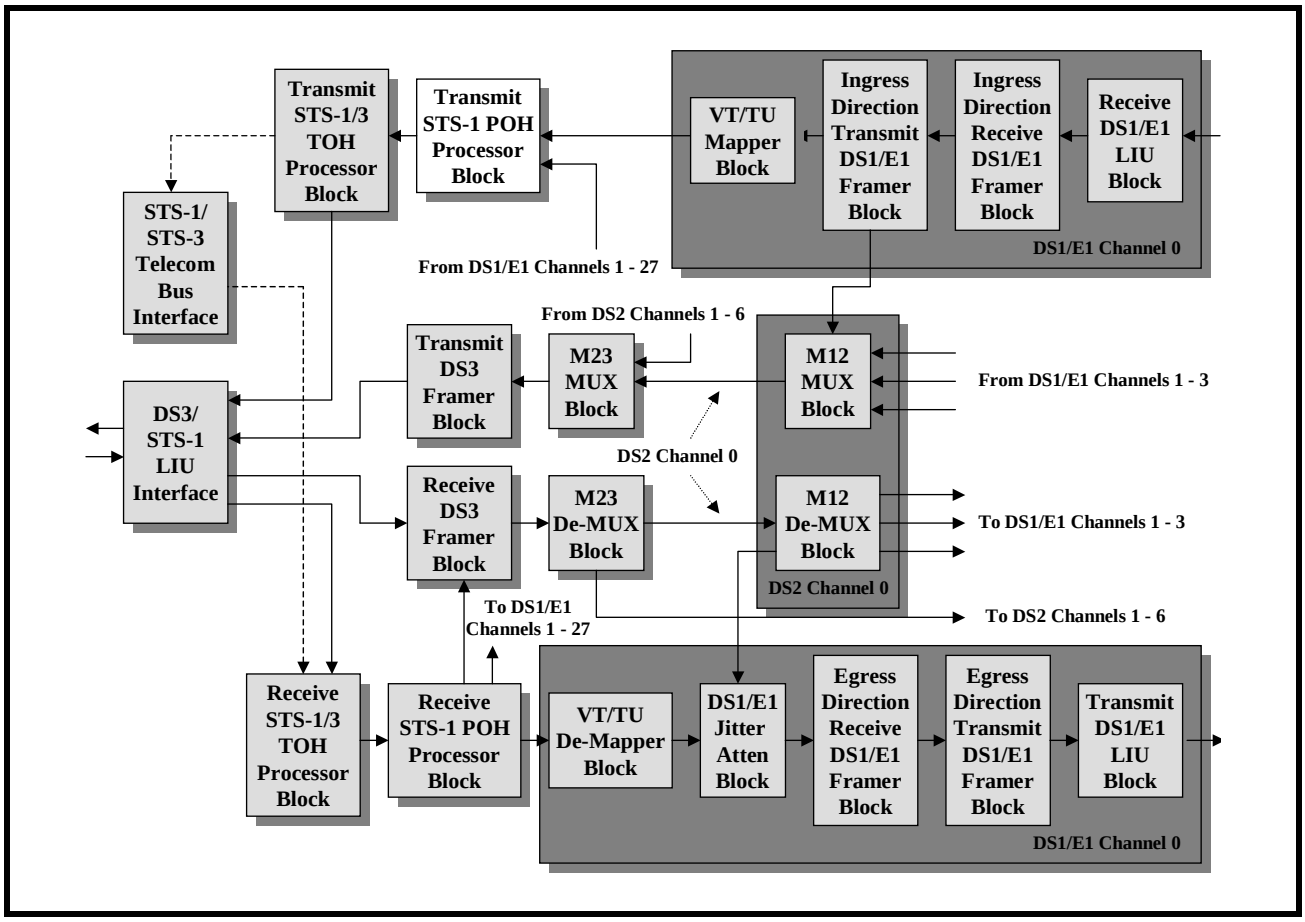


TABLE 190: TRANSMIT STS-1/STS-3 PATH - TRANSMIT CONTROL REGISTER - BYTE 2 (ADDRESS LOCATION = 0X0781)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Payload_Type[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT [1:0] - Payload_Type[1:0]

TABLE 191: TRANSMIT STS-1/STS-3 PATH - TRANSMIT CONTROL REGISTER - BYTE 1 (ADDRESS LOCATION = 0X0782)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Z5 Insertion-Type	Z4 Insertion-Type	Z3 Insertion-Type	H4 Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT 3 - Z5 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to use either the Transmit STS-1/STS-3 Path - Transmit Z5 Value Register or the TPOH input pin as the source for the Z5 byte, in the outbound STS-1/STS-3 SPE.

- 0 - Configures the Transmit STS-1/STS-3 POH Processor block to use the Transmit STS-1/STS-3 Path - Transmit Z5 Value Register (Address Location= 0x07B3).
- 1 - Configures the Transmit STS-1/STS-3 POH Processor block to use the TPOH input as the source for the Z5 byte, in the outbound STS-1/STS-3 SPE.

BIT 2 - Z4 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to use either the Transmit STS-1/STS-3 Path - Transmit Z4 Value Register or the TPOH input pin as the source for the Z4 byte, in the outbound STS-1/STS-3 SPE.

- 0 - Configures the Transmit STS-1/STS-3 POH Processor block to use the Transmit STS-1/STS-3 Path - Transmit Z4 Value Register (Address Location= 0x07AF).
- 1 - Configures the Transmit STS-1/STS-3 POH Processor block to use the TPOH input as the source for the Z4 byte, in the outbound STS-1/STS-3 SPE.

BIT 1 - Z3 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to use either the Transmit STS-1/STS-3 Path - Transmit Z3 Value Register or the TPOH input pin as the source for the Z3 byte, in the outbound STS-1/STS-3 SPE.

- 0 - Configures the Transmit STS-1/STS-3 POH Processor block to use the Transmit STS-1/STS-3 Path - Transmit Z3 Value Register (Address Location = 0x07AB).
- 1 - Configures the Transmit STS-1/STS-3 POH Processor block to use the TPOH input as the source for the Z3 byte, in the outbound STS-1/STS-3 SPE.

BIT 0 - H4 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to use either the Transmit STS-1/STS-3 Path - Transmit H4 Value Register or the TPOH input pin as the source for the H4 byte, in the outbound STS-1/STS-3 SPE.

- 0 - Configures the Transmit STS-1/STS-3 POH Processor block to use the Transmit STS-1/STS-3 Path - Transmit H4 Value Register (Address Location= 0x07A7).
- 1 - Configures the Transmit STS-1/STS-3 POH Processor block to use the TPOH input as the source for the H4 byte, in the outbound STS-1/STS-3 SPE.

TABLE 192: TRANSMIT STS-1/STS-3 PATH - TRANSMIT CONTROL REGISTER - BYTE 0 (ADDRESS LOCATION= 0X0783)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2 Insertion Type	REI-P Insertion Type[1:0]		RDI-P Insertion Type[1:0]		C2 Byte Insertion Type	C2 Byte Auto Insert Mode Enable	Transmit AIS-P Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - F2 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to use either the Transmit STS-1/STS-3 Path - Transmit F2 Value Register or the TPOH input pin as the source for the F2 byte, in the outbound STS-1/STS-3 SPE.

▶ 0 - Configures the Transmit STS-1/STS-3 POH Processor block to use the Transmit STS-1/STS-3 Path - Transmit F2 Value Register (Address Location= 0x07A3).

▶ 1 - Configures the Transmit STS-1/STS-3 POH Processor block to use the TPOH input as the source for the F2 byte, in the outbound STS-1/STS-3 SPE.

BIT [6:5] - REI-P Insertion Type[1:0]

These two READ/WRITE bit-fields are used to configure the Transmit STS-1/STS-3 POH Processor block to use one of the three following sources for the REI-P bit-fields (e.g., bits 1 through 4, within the G1 byte of the outbound STS-1/STS-3 SPE).

- From the corresponding Receive STS-1/STS-3 POH Processor block (e g., when it detects B3 bytes in its incoming SPE data).
- From the Transmit G1 Byte Value Register (Address Location= 0x079F).
- From the TPOH input pin.

▶ 00/11 - Configures the Transmit STS-1/STS-3 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon receive conditions as detected by the corresponding Receive STS-1/STS-3 POH Processor block.

▶ 01 - Configures the Transmit STS-1/STS-3 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the contents within the Transmit G1 Byte Value register (Address Location= 0x079F).

▶ 10 - Configures the Transmit STS-1/STS-3 POH Processor block to use the TPOH input pin as the source of Bits 1 through 4 (in the G1 byte of the outbound SPE).

BIT [4:3] - RDI-P Insertion Type[1:0]

These two READ/WRITE bit-fields are used to configure the Transmit STS-1/STS-3 POH Processor block to use one of the three following sources for the RDI-P bit-fields (e.g., bits 5 through 7, within the G1 byte of the outbound STS-1/STS-3 SPE).

- From the Receive STS-1/STS-3 POH Processor block (e g., when it detects various alarm conditions within its incoming SPE data).
- From the Transmit G1 Byte Value Register (Address Location = 0x079F).
- From the TPOH input pin.

▶ 00/11 - Configures the Transmit STS-1/STS-3 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon receive conditions as detected by the Receive STS-1/STS-3 POH Processor block.

▶ 01 - Configures the Transmit STS-1/STS-3 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the contents within the Transmit G1 Byte Value register.

▶ 10 - Configures the Transmit STS-1/STS-3 POH Processor block to use the TPOH input pin as the source of Bits 5 through 7 (in the G1 byte of the outbound SPE).

BIT 2 - C2 Insertion Type

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to use either the Transmit STS-1/STS-3 Path - Transmit C2 Byte Value Register or the TPOH input pin as the source for the C2 byte, in

the outbound STS-1/STS-3 SPE.

- 0 - Configures the Transmit STS-1/STS-3 POH Processor block to use the Transmit STS-1/STS-3 Path - Transmit C2 Value Register (Address Location= 0x079B).
- 1 - Configures the Transmit STS-1/STS-3 POH Processor block to use the TPOH input as the source for the C2 byte, in the outbound STS-1/STS-3 SPE.

BIT 1 - Auto-Insert PDI-P Indicator Enable

This READ/WRITE bit-field are used to configure the Transmit STS-1/STS-3 POH Processor block to automatically insert the PDI-P (Path - Payload Defect Indicator) whenever the AIS-P indicator is received from the Receive SONET POH Processor block.

If this feature is enabled, then the Transmit STS-1/STS-3 POH Processor block will automatically set the C2 byte (within the outbound SPE) to 0xFC (to indicate a PDI-P condition) whenever it receives the AIS-P indicator, from the Receive SONET POH Processor block.

BIT 0 - Transmit AIS-P Enable

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to (via software control) transmit an AIS-P indicator to the remote PTE.If this feature is enabled, then the Transmit STS-1/STS-3 POH Processor block will automatically set the H1, H2, H3 and all the SPE bytes to an All Ones pattern, prior to routing this data to the Transmit STS-1/STS-3 TOH Processor block.

- 0 - Configures the Transmit STS-1/STS-3 POH Processor block to NOT transmit the AIS-P indicator to the remote PTE.
- 1 - Configures the Transmit STS-1/STS-3 POH Processor block to transmit the AIS-P indicator to the remote PTE.

TABLE 193: TRANSMIT STS-1/STS-3 PATH - TRANSMITTER J1 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X0793)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_J1_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit J1 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the J1 byte, within each outbound STS-1/STS-3 SPE.

If the user configures the Transmit STS-1/STS-3 POH Processor block to this register as the source of the J1 byte, then it will automatically write the contents of this register into the J1 byte location, within each outbound STS-1/STS-3 SPE.

This feature is enabled whenever the user writes a 0 into BIT 2 (C2 Insertion Type) within the Transmit STS-1/STS-3 Path - J1 Control Register register (Address Location= 0x0783).

TABLE 194: TRANSMIT STS-1/STS-3 PATH - TRANSMIT B3 BYTE ERROR MASK REGISTER (ADDRESS LOCATION= 0X0797)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_B3_Byte_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit B3 Byte Mask[7:0]

This READ/WRITE bit-field is used to insert errors into the B3 byte, within the outbound STS-1/STS-3 SPE, prior to transmission to the Transmit STS-1/STS-3 TOH Processor block.

The Transmit STS-1/STS-3 POH Processor block will perform an XOR operation with the contents of this register, and the B3 byte value. The results of this operation will be written back into the B3 byte of the outbound STS-1/STS-3 SPE.

NOTE: If the user sets a particular bit-field, within this register, to 1, then that corresponding bit, within the outbound B3 byte will be in error. For normal operation, the user should set this register to 0x00.

TABLE 195: TRANSMIT STS-1/STS-3 PATH - TRANSMIT C2 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X079B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit C2 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the C2 byte, within each outbound STS-1/STS-3 SPE.

If the user configures the Transmit STS-1/STS-3 POH Processor block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each outbound STS-1/STS-3 SPE.

This feature is enabled whenever the user writes a 0 into BIT 2 (C2 Byte Insertion Type) within the Transmit STS-1/STS-3 Path - SONET Control Register - Byte 0 register (Address Location= 0x0783).

TABLE 196: TRANSMIT STS-1/STS-3 PATH - TRANSMIT G1 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X079F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_G1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit G1 Byte Value:

These READ/WRITE bit-fields are used to have software control over the contents of the RDI-P and REI-P bit-fields, within each G1 byte in the outbound STS-1/STS-3 SPE.

NOTE: If the users sets REI-P_Insertion_Type[1:0] and RDI-P_Insertion_Type[1:0] bits to the value [0, 1], then contents of the REI-P and the RDI-P bit-fields (within each G1 byte of the outbound STS-1/STS-3 SPE) will be dictated by the contents of this register. The REI-P_Insertion_Type[1:0] and RDI-P_Insertion_Type[1:0] bit-fields are located in the Transmit STS-1/STS-3 Path - SONET Control Register - Byte 0 Register (Address Location= 0x0783)

TABLE 197: TRANSMIT STS-1/STS-3 PATH - TRANSMIT F2 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X07A3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_F2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit F2 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the F2 byte, within each outbound STS-1/STS-3 SPE.

If the user configures the Transmit STS-1/STS-3 POH Processor block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each outbound STS-1/STS-3 SPE.

This feature is enabled whenever the user writes a 0 into BIT7 (F2 Byte Insertion Type) within the Transmit STS-1/STS-3 Path - SONET Control Register - Byte 0 register (Address Location= 0x0783).

TABLE 198: TRANSMIT STS-1/STS-3 PATH - TRANSMIT H4 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X07A7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit H4 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the H4 byte, within each outbound STS-1/STS-3 SPE.

If the user configures the Transmit STS-1/STS-3 POH Processor block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each outbound STS-1/STS-3 SPE.

This feature is enabled whenever the user writes a 0 into BIT 0 (H4 Insertion Type) within the Transmit STS-1/STS-3 Path - SONET Control Register - Byte 1 register (Address Location= 0x07A7).

TABLE 199: TRANSMIT STS-1/STS-3 PATH - TRANSMIT Z3 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X07AB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Z3 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the Z3 byte, within each outbound STS-1/STS-3 SPE.If the user configures the Transmit STS-1/STS-3 POH Processor block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each outbound STS-1/STS-3 SPE.

This feature is enabled whenever the user writes a 0 into BIT 1 (Z3 Insertion Type) within the Transmit STS-1/STS-3 Path - SONET Control Register - Byte 0 register (Address Location= 0x0782).

TABLE 200: TRANSMIT STS-1/STS-3 PATH - TRANSMIT Z4 BYTE VALUE REGISTER (ADDRESS LOCATION= 0XN9AF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Z4 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the Z4 byte, within each outbound STS-1/STS-3 SPE.

If the user configures the Transmit STS-1/STS-3 POH Processor block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each outbound STS-1/STS-3 SPE.

This feature is enabled whenever the user writes a 0 into BIT 2 (Z4 Insertion Type) within the Transmit STS-1/STS-3 Path - SONET Control Register - Byte 0 register (Address Location= 0x0782).

TABLE 201: TRANSMIT STS-1/STS-3 PATH - TRANSMIT Z5 BYTE VALUE REGISTER (ADDRESS LOCATION= 0X07B3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Z5 Byte Value

These READ/WRITE bit-fields are used to have software control over the value of the Z5 byte, within each outbound STS-1/STS-3 SPE.

If the user configures the Transmit STS-1/STS-3 POH Processor block to this register as the source of the Z5 byte, then it will automatically write the contents of this register into the Z5 byte location, within each outbound STS-1/STS-3 SPE.

This feature is enabled whenever the user writes a 0 into BIT 3 (Z5 Insertion Type) within the Transmit STS-1/STS-3 Path - SONET Control Register - Byte 0 register (Address Location= 0x0782).

TABLE 202: TRANSMIT STS-1/STS-3 PATH - TRANSMIT PATH CONTROL REGISTER (ADDRESS LOCATION= 0X07B7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Pointer Force	Check Stuff	Insert Nega-tive Stuff	InsertPosi-tive Stuff	InsertContin-uous NDF Events	InsertSingle NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Unused

BITt 5 - Pointer Force

This READ/WRITE bit-field is used to load the values contained within the Transmit STS-1/STS-3 POH Arbitrary H1 Pointer and Transmit STS-1/STS-3 POH Arbitrary H2 Pointer registers (Address Location= 0x07BF and 0x07C3) into the H1 and H2 bytes (within the outbound STS-1 or STS-3 Data stream).

The actual location of the SPE will NOT be adjusted, per the value of H1 and H2 bytes. Hence, this feature should cause the remote terminal to declare an Invalid Pointer condition.

- 0 - Configures the Transmit STS-1/STS-3 POH and TOH Processors to transmit STS-1 or STS-3 Data with normal and correct H1 and H2 bytes.
- 1 - Configures the Transmit STS-1/STS-3 POH and TOH Processor blocks to overwrite the values of the H1 and H2 bytes (in the outbound STS-1 or STS-3 Data-stream) with the values in the Transmit STS-1/STS-3 POH Arbitrary H1 and H2 Pointer registers.

BITt 4 - Check Stuff Monitoring

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH and TOH Processor blocks to only execute a Positive, Negative or NDF event (via the Insert Positive Stuff, Insert Negative Stuff, Insert Continuous or Single NDF options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 STS-1/STS-3 frame periods.

- 0 - Disables this feature.In this mode, the Transmit STS-1/STS-3 POH and TOH Processor block will execute a software-commanded pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 STS-1/STS-3 frame periods.
- 1 - Enables this feature.In this mode, the Transmit STS-1/STS-3 POH and TOH Processor block will ONLY execute a software-commanded pointer adjustment event, if no pointer adjustment event has occurred during the last 3 STS-1/STS-3 frame periods.

BITt 3 - Insert Negative Stuf

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH and TOH Processor blocks to insert a negative-stuff into the outbound STS-1 or STS-3 Data stream. This command, in-turn will cause a Pointer

Decrementing event at the remote terminal.

- Writing a 0 to 1 transition into this bit-field causes the following to happen.
  - A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STS-1 or STS-3 Data stream).
  - The D bits, within the H1 and H2 bytes will be inverted (to denote a Decrementing Pointer Adjustment event).
  - The contents of the H1 and H2 bytes will be decremented by 1, and will be used as the new pointer from this point on.

NOTE: *Once the user writes a 1 into this bit-field, the XRT86SH328 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to 0.*

BITt 2 - Insert Positive Stuff

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH and TOH Processor blocks to insert a positive-stuff into the outbound STS-1 or STS-3 Data stream. This command, in-turn will cause a Pointer Incrementing event at the remote terminal.

- Writing a 0 to 1 transition into this bit-field causes the following to happen.
  - A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STS-1 or STS-3 Data-stream, immediately after the H3 byte position within the outbound STS-1 or STS-3 Data stream).
  - The I bits, within the H1 and H2 bytes will be inverted (to denote a Incrementing Pointer Adjustment event).
  - The contents of the H1 and H2 bytes will be incremented by 1, and will be used as the new pointer from this point on.Note

NOTE: *Once the user writes a 1 into this bit-field, the XRT86SH328 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to 0.*

BITt 1 - Insert Continuous NDF Events

This READ/WRITE bit-field is used configure the Transmit STS-1/STS-3 POH and TOH Processor blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STS-1 or STS-3 Data stream.

As the Transmit STS-1/STS-3 POH and TOH Processor blocks insert the NDF event into the STS-1 or STS-3 Data stream, it will proceed to load in the contents of the Transmit STS-1/STS-3 POH Arbitrary H1 Pointer and Transmit STS-1/STS-3 POH Arbitrary H2 Pointer registers into the H1 and H2 bytes (within the outbound STS-1 or STS-3 Data stream).

- 0 - Configures the Transmit STS-1/STS-3 TOH and POH Processor blocks to not continuously insert NDF events into the outbound STS-1 or STS-3 Data stream.

- 1- Configures the Transmit STS-1/STS-3 TOH and POH Processor blocks to continuously insert NDF events into the outbound STS-1 or STS-3 Data stream.

BITt 0 - Insert Single NDF Event

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH and TOH Processor blocks to insert a New Data Flag (NDF) pointer adjustment into the outbound STS-1 or STS-3 Data stream.

- Writing a 0 to 1 transition into this bit-field causes the following to happen
  - The N bits, within the H1 byte will set to the value 1001
  - The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the Transmit STS-1/STS-3 POH - Arbitrary H1 Pointer and Transmit STS-1/STS-3 POH Arbitrary H2 Pointer registers (Address Location= 0x07BF and 0xN9C3).

NOTE: *Afterwards, the N bits will resume their normal value of 0110 and this new pointer value will be used as the new pointer from this point on. Once the user writes a 1 into this bit-field, the XRT86SH328 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to 0.*

TABLE 203: TRANSMIT STS-1/STS-3 PATH - SONET PATH J1 CONTROL REGISTER (ADDRESS LOCATION= 0X07BB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Insertion_Method[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Unused

BIT [1:0] - J1 Byte Insertion_Method[1:0]

These READ/WRITE bit-fields are used to specify the method that the user will use to insert the J1 byte into the outbound STS-1/STS-3 SPE. The relationship between the contents of these bit-fields and the corresponding J1 Byte Insertion Method is presented below.

Insertion Method

J1 BYTE INSERTION METHOD[1:0]	RESULTING INSERTION METHOD
00	Insert the value 0x00
01	Not Valid
10	Insert from the Transmit SONET Path - Transmit J1 Byte Value Register (Address Location= 0x0793)
11	Insert via the TxPOH_n input port

TABLE 204: TRANSMIT STS-1/STS-3 PATH - TRANSMIT ARBITRARY H1 POINTER REGISTER (ADDRESS LOCATION= 0X07BF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NDF Bits				SS Bits		H1 Pointer Value	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - NDF (New Data Flag) Bits

These READ/WRITE bit-fields are used provide the value that will be loaded into the NDF bit-field (of the H1 byte), whenever a 0 to 1 transition occurs in BIT 5 (Pointer Force) within the Transmit STS-1/STS-3 Path - Transmit Path Control Register (Address Location= 0x07B7).

BIT [3:2] - SS Bits

These READ/WRITE bit-fields is used to provide the value that will be loaded into the SS bit-fields (of the H1 byte) whenever a 0 to 1 transition occurs in BIT 5 (Pointer Force) within the Transmit STS-1/STS-3 Path - Transmit Path Control Register (Address Location= 0x07B7).

The SS bits have no functional value, within the H1 byte.

BIT [1:0] - H1 Pointer Value[1:0]

These two READ/WRITE bit-fields, along with the constants of the Transmit STS-1/STS-3 Path - Transmit Arbitrary H2 Pointer Register (Address Location= 0x07C3) are used to provide the contents of the Pointer Word.

These two READ/WRITE bit-fields are used to define the value of the two most significant bits within the Pointer word. Whenever a 0 to 1 transition occurs in BIT 5 (Pointer Force) within the Transmit STS-1/STS-3 Path - Transmit Path Control Register (Address Location= 0x07B7), the values of these two bits will be loaded into the two most significant

bits within the Pointer Word.

TABLE 205: TRANSMIT STS-1/STS-3 PATH - TRANSMIT ARBITRARY H2 POINTER REGISTER (ADDRESS LOCATION= 0X07C3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H2 Pointer Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - H2 Pointer Value[1:0]

These eight READ/WRITE bit-fields, along with the constants of bits 1 and 0 within the Transmit STS-1/STS-3 Path - Transmit Arbitrary H1 Pointer Register (Address Location= 0x07C3) are used to provide the contents of the Pointer Word. These two READ/WRITE bit-fields are used to define the value of the eight least significant bits within the Pointer word.

- Whenever a 0 to 1 transition occurs in BIT 5 (Pointer Force) within the Transmit STS-1/STS-3 Path - Transmit Path Control Register (Address Location= 0x07B7), the values of these eight bits will be loaded into the H2 byte, within the outbound STS-1 or STS-3 Data stream.

TABLE 206: TRANSMIT STS-1/STS-3 PATH - TRANSMIT CURRENT POINTER BYTE REGISTER - BYTE 1 (ADDRESS LOCATION= 0X07C6)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Tx_Pointer_High[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	1	0

BIT [7:2] - Unused

BIT [1:0] - Transmit Pointer Word - High[1:0]

These two READ-ONLY bits, along with the contents of the Transmit STS-1/STS-3 Path - Transmit Current Pointer Byte Register - Byte 0 (Address Location= 0x07C7) reflect the current value of the pointer (or offset of SPE within the STS-1/STS-3 frame). These two bits contain the two most significant bits within the 10-bit pointer word.

TABLE 207: TRANSMIT STS-1/STS-3 PATH - TRANSMIT CURRENT POINTER BYTE REGISTER - BYTE 0 (ADDRESS LOCATION= 0X07C7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx_Pointer_Low[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	1	0	1	0

BIT [7:0] - Transmit Pointer Word - Low[7:0]

These two READ-ONLY bits, along with the contents of the Transmit STS-1/STS-3 Path - Transmit Current Pointer Byte Register - Byte 1 (Address Location= 0x07C6) reflect the current value of the pointer (or offset of SPE within the STS-1/STS-3 frame). These two bits contain the eight least significant bits within the 10-bit pointer word.

TABLE 208: TRANSMIT STS-1/STS-3 PATH - RDI-P CONTROL REGISTER - BYTE 2 (ADDRESS LOCATION= 0X07C9)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				PLM-P RDI-P Code[2:0]			Transmit RDI-P upon PLM-P
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT [3:1] - PLM-P (Path - Payload Mismatch) - RDI-P Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STS-1/STS-3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the outbound STS-1/STS-3 SPE), whenever the corresponding Receive STS-1/STS-3 POH Processor block detects and declares a PLM-P condition. In order to enable this feature, the user must set BIT 0 (RDI-P upon PLM-P) within this register to 1.

BIT 0 - Transmit RDI-P upon PLM-P

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 3 through 1 - within this register) whenever the corresponding Receive STS-1/STS-3 POH Processor block declares a PLM-P condition.

- 0 - Disables the automatic transmission of RDI-P upon detection of PLM-P.
- 1 - Enables the automatic transmission of RDI-P upon detection of PLM-P.

TABLE 209: TRANSMIT STS-1/STS-3 PATH - RDI-P CONTROL REGISTER - BYTE 1 (ADDRESS LOCATION= 0X07CA)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P RDI-P Code[2:0]			Transmit RDI-P upon TIM -P	UNEQ-P RDI-P Code[2:0]			Transmit RDI-P upon UNEQ-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - TIM-P (Path - Trace Identification Message Mismatch) - RDI-P Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STS-1/STS-3 POH Processor block will transmit within the RDI-P bit-fields of the G1 byte (within the outbound STS-1/STS-3 SPE), whenever the Receive STS-1/STS-3 POH Processor block detects and declares the TIM-P defect condition.

To enable this feature, the user must set BIT 4 (Transmit RDI-P upon TIM-P) within this register to 1.

BIT 4 - Transmit RDI-P upon TIM-P

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 - within this register) whenever the corresponding Receive STS-1/STS-3 POH Processor block declares the TIM-P defect condition.

- 0 - Disables the automatic transmission of RDI-P upon detection of TIM-P.
- 1 - Enables the automatic transmission of RDI-P upon detection of TIM-P.

BIT [3:1] - UNEQ-P (Path - Unequipped) - RDI-P Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STS-1/STS-3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the outbound STS-1/STS-3 SPE), whenever the Receive STS-1/STS-3 POH Processor block detects and declares the UNEQ-P defect condition.

To enable this feature, the user must set BIT 0 (Transmit RDI-P upon UNEQ-P) within this register to 1.

BIT 0 - Transmit RDI-P upon UNEQ-P

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 3 through 1 - within this register) whenever the corresponding Receive STS-1/STS-3 POH Processor block declares the UNEQ-P defect condition.

- 0 - Disables the automatic transmission of RDI-P upon detection of UNEQ-P.
- 1 - Enables the automatic transmission of RDI-P upon detection of UNEQ-P.

TABLE 210: TRANSMIT STS-1/STS-3 PATH - RDI-P CONTROL REGISTER - BYTE 0 (ADDRESS LOCATION= 0X07CB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOP-P RDI-P Code[2:0]			Transmit RDI-P upon LOP-P	AIS-P RDI-P Code[2:0]			Transmit RDI-P upon AIS-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:5] - LOP-P (Path - Loss of Pointer) - RDI-P Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STS-1/STS-3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the outbound STS-1/STS-3 SPE), whenever the corresponding Receive STS-1/STS-3 POH Processor block detects and declares a LOP-P condition.

To enable this feature, the user must set BIT 4 (RDI-P upon LOP-P) within this register to 1.

BIT 4 - Transmit RDI-P upon LOP-P

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 - within this register) whenever the corresponding Receive STS-1/STS-3 POH Processor block declares a LOP-P condition

- 0 - Disables the automatic transmission of RDI-P upon detection of LOP-P.
- 1 - Enables the automatic transmission of RDI-P upon detection of LOP-P.

BIT[3:1]AIS-P (Path - AIS) - RDI-P Code

These three READ/WRITE bit-fields are used to specify the value that the Transmit STS-1/STS-3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the outbound STS-1/STS-3 SPE), whenever the corresponding Receive STS-1/STS-3 POH Processor block detects and declares an AIS-P condition.

To enable this feature, the user must set BIT 4 (RDI-P upon AIS-P) within this register to 1.

BIT 0 - Transmit RDI-P upon AIS-P

This READ/WRITE bit-field is used to configure the Transmit STS-1/STS-3 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 - within this register) whenever the corresponding Receive STS-1/STS-3 POH Processor block declares a AIS-P condition.

- 0 - Disables the automatic transmission of RDI-P upon detection of AIS-P.
- 1 - Enables the automatic transmission of RDI-P upon detection of AIS-P.

TABLE 211: TRANSMIT STS-1/STS-3 PATH - SERIAL PORT CONTROL REGISTER (ADDRESS LOCATION= 0X07CF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				TxPOH Clock Speed[4:0]			
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT 3:0] - TxPOHClk Output Clock Signal Speed

These READ/WRITE bit-fields are used to specify the frequency of the TxPOHClk output clock signal. The formula that relates the contents of these register bits to the TxPOHClk frequency is presented below.

FREQ = 51.84 /[2 * (TxPOH_CLOCK_SPEED + 1)

For STS-3/STS-1/STS-3 applications, the frequency of the RxPOHClk output signal must be in the range of 2.36MHz to 25.92MHz

TABLE 212: TRANSMIT STS-1/STS-3 PATH - TRANSMIT NEGATIVE POINTER ADJUSTMENT COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X07D0)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Negative_Pointer_Adjustment_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Negative Pointer Adjustment Count - MSB

This RESET-upon-READ register, along with the Transmit Negative Pointer Adjustment Count Register - Byte 0 presents a 16-bit representation of the number of Negative (or Decrementing) Pointer Adjustments that have occurred

(in the outbound STS-1 or STS-3 Data-stream) since the last read of this register.

NOTE: *This register contains the MSB (Most Significant Bits) of this 16-bit expression.*

TABLE 213: TRANSMIT STS-1/STS-3 PATH - TRANSMIT NEGATIVE POINTER ADJUSTMENT COUNT REGISTER - BYTE 0 (ADDRESS LOCATION= 0X07D1)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Negative_Pointer_Adjustment_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Negative Pointer Adjustment Count - LSB

This RESET-upon-READ register, along with the Transmit Negative Pointer Adjustment Count Register - Byte 1 presents a 16-bit representation of the number of Negative (or Decrementing) Pointer Adjustments that have occurred (in the outbound STS-1 or STS-3 Data-stream) since the last read of this register.

NOTE: *This register contains the LSB (Least Significant Bits) of this 16-bit expression.*

TABLE 214: TRANSMIT STS-1/STS-3 PATH - TRANSMIT POSITIVE POINTER ADJUSTMENT COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X07D2)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Positive_Pointer_Adjustment_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Positive Pointer Adjustment Count - MSB

This RESET-upon-READ register, along with the Transmit Positive Pointer Adjustment Count Register - Byte 0 presents a 16-bit representation of the number of Positive (or Incrementing) Pointer Adjustments that have occurred (in the outbound STS-1 or STS-3 Data-stream) since the last read of this register.

NOTE: *This register contains the MSB (Most Significant Bits) of this 16-bit expression.*

TABLE 215: TRANSMIT STS-1/STS-3 PATH - TRANSMIT POSITIVE POINTER ADJUSTMENT COUNT REGISTER - BYTE 1 (ADDRESS LOCATION= 0X07D3)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Positive_Pointer_Adjustment_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit Positive Pointer Adjustment Count - LSB

This RESET-upon-READ register, along with the Transmit Positive Pointer Adjustment Count Register - Byte 1 presents a 16-bit representation of the number of Positive (or Incrementing) Pointer Adjustments that have occurred (in the outbound STS-1 or STS-3 Data-stream) since the last read of this register.

NOTE: *This register contains the LSB (Least Significant Bits) of this 16-bit expression.*

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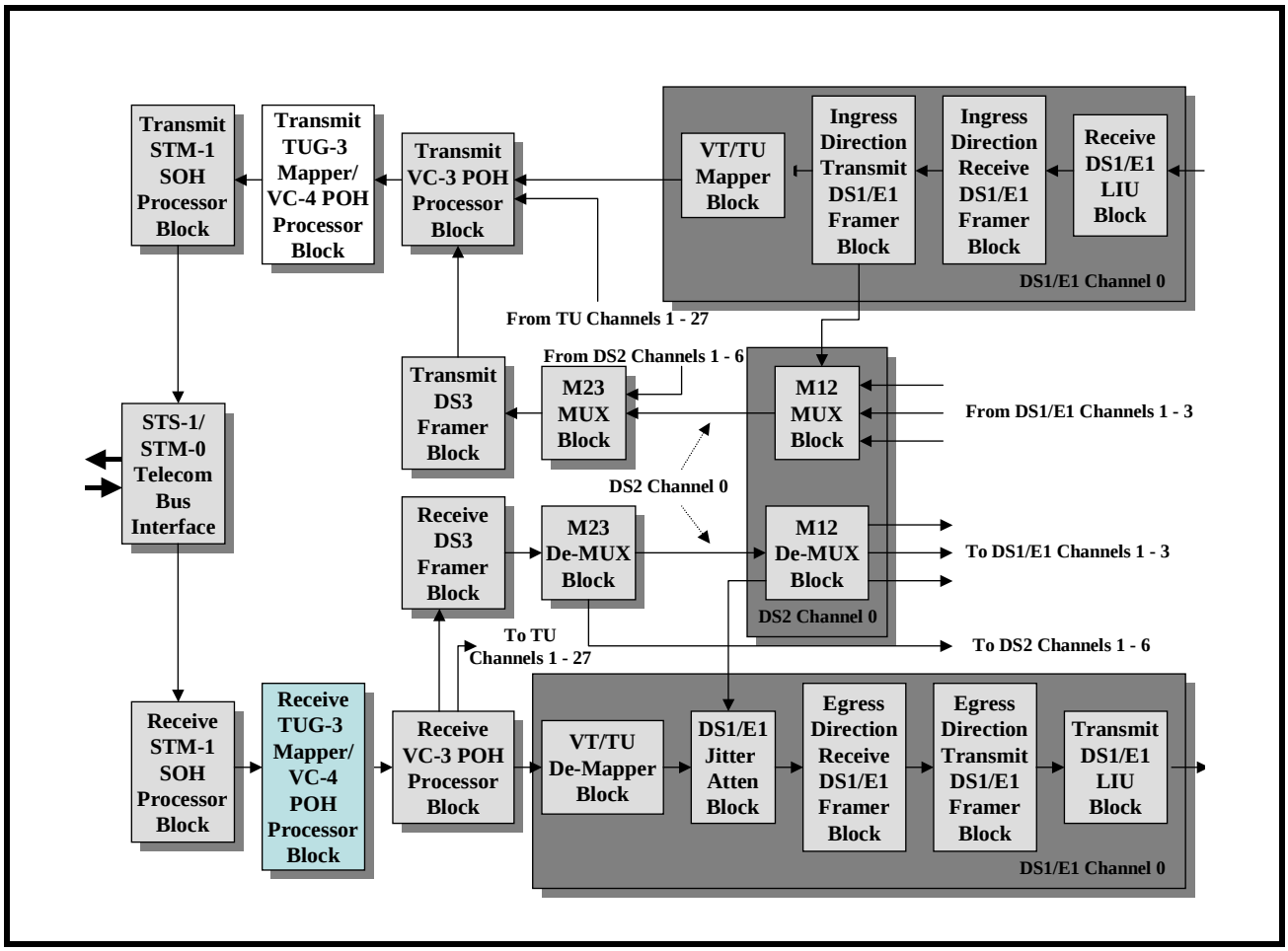
2.8 Transmit TUG-3 MAPPER/VC-4 POH Processor Block Registers (SDH/TUG-3 Applications Only)

The register map for the Transmit TU-3 Mapper/VC-4 POH Processor block is presented an discussed in detail within the "SDH Version of the Register Map".

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328 device, with the Transmit TUG-3 Maper/VC-4 POH Processor block "highlighted" is presented below in Figure _.

FIGURE 8. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328 DEVICE, WITH THE TRANSMIT TUG-3 MAPPER/VC-4 POH PROCESSOR BLOCK "HIGHLIGHTED"



For detailed on the "Transmit TUG-3 Mapper/VC-4 POH Processor Block" Registers, please see the "XRT86SH328 28-Channel DS1/E1 Framer/LIU with DS3 MUX and TU-Mapper IC - Register Map & Description - SDH Applications".

2.9 Global VT MAPPER BLOCK CONTROL REGISTERS

The register map for the Global VT Mapper block is presented in the Table below. Additionally, a detailed description of each of the Global VT Mapper Control registers is presented below.

TABLE 216: GLOBAL CONTROL - VT-MAPPER BLOCK - VT MAPPER BLOCK CONTROL REGISTER (ADDRESS = 0X0C03)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Latch Count	REI-V Enable	Unused	SONET/SDH Loop-Back
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Unused

BIT 3 - Latch Count

- A "0 to 1" transition within this bit-field commands each of the VT-De-Mapper blocks to update the contents within the following Bit-Fields/PMON registers.

BIT FIELDS	REGISTER NAME	ADDRESS LOCATION
VT-Payload Pointer Increment Count[3:0]	Channel Control VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 1	0xND4A
BIP-2 Error Count[11:8]	Channel Control VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 1	0xND4A
BIP-2 Error Count[7:0]	Channel Control VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 0	0xND4B
VT-Payload Pointer Decrement Count[3:0]	Channel Control - VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 1	0xND4E
REI-V Event Count[11:8]	Channel Control - VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 1	0xND4E
REI-V Event Count[7:0]	Channel Control - VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 0	0xND4F

BIT 2 - REI-V Enable

This READ/WRITE bit-field is used to configure a given Transmit VT-Mapper block to automatically insert the appropriate REI-V value (based upon the number of B2 bit errors that are detected by the corresponding Receive VT-Mapper block) into the V5 byte, within its outbound VT1.5 or VT2 data-stream.

- 0 - Configures the Transmit VT-Mapper block to NOT automatically insert the REI-V value into each V5 byte, within the outbound VT data-stream.
- 1 - Configures the Transmit VT-Mapper block to automatically insert the REI-V value into each V5 byte, within the outbound VT data-stream.

BIT 1 - Unused

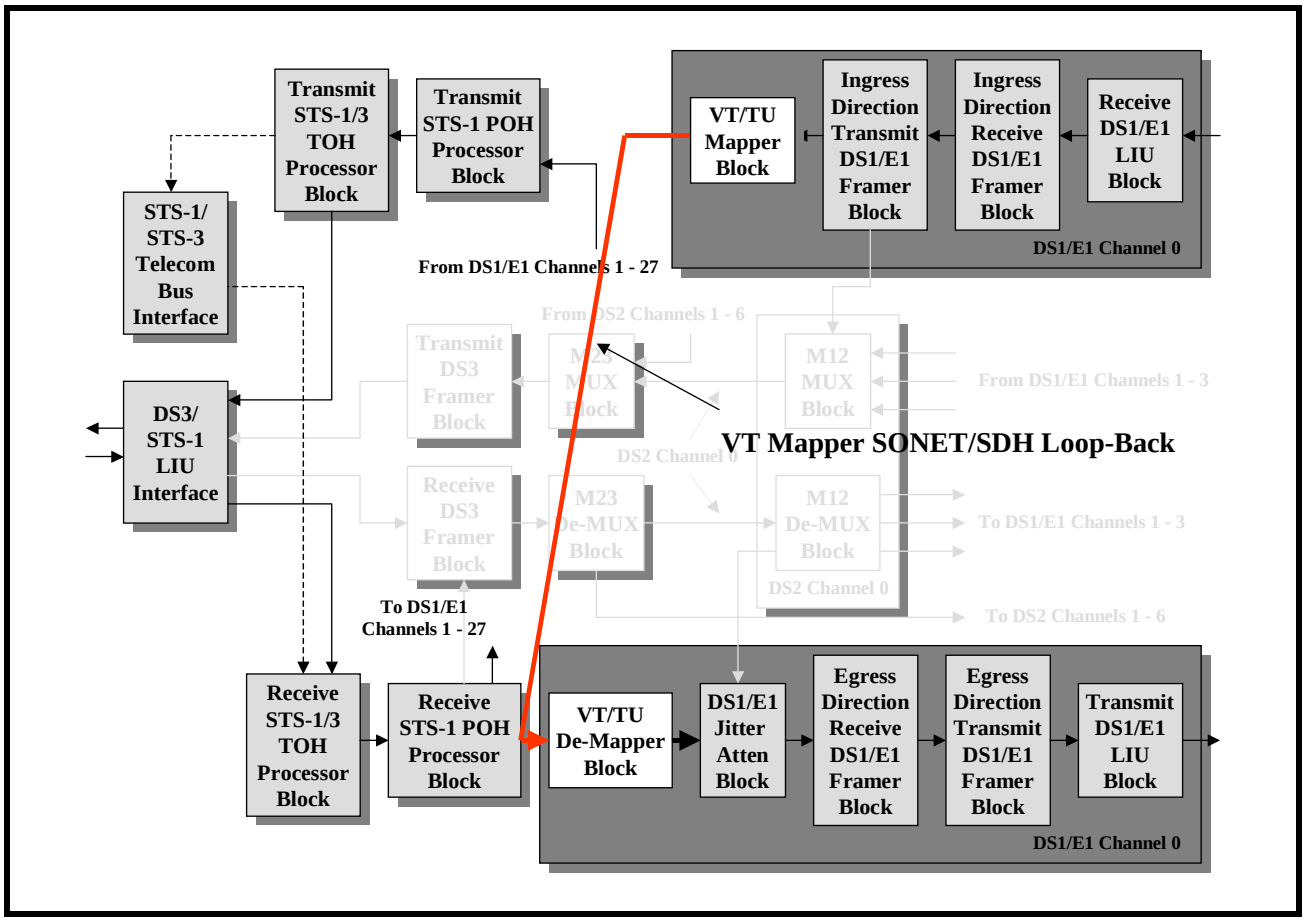
BIT 0 - VT Mpper SONET/SDH Loop-Back

This READ/WRITE bit-field permits the user to configure the XRT86SH328 device to operate in the "VT Mapper SONET/SDH Loop-back" Mode. If the user configures the XRT86SH328 device to operate in this mode, then the outputs (from each of the 28 VT-Mapper blocks) will be internally looped back into the inputs of their corresponding VT-De-Mapper block.

Figure _ presents an illustration of the XRT86SH328 device whenever it has been configured to operate in the "VT Mapper SONET/SDH Loop-back" Mode.

Figure _, Illustration of the Functional Block Diagram of the XRT86SH328 device with the "VT-Mapper SONET/SDH Loop-back" path depicted.

FIGURE 9. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328 WITH THE VT-MAPPER SONET/SDH LOOP-BACK PATH DEPICTED



- 0 - Does not configure the XRT86SH328 device to operate in the "VT-Mapper SONET/SDH Loop-back" Mode.
- 1 - Configures the XRT86SH328 device to operate in the "VT-Mapper SONET/SDH Loop-back" Mode.

TABLE 217: GLOBAL CONTROL - VT-MAPPER BLOCK - TEST PATTERN CONTROL REGISTER - BYTE 1 (ADDRESS = 0X0C0E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Latch Error Count	Insert Pat-tern Error	Reserved					
R/W	R/W	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT7 - Latch Error Count

A 0 to 1 transition within this bit-field commands the Test Pattern Receiver to latch its current Bit Error Count into Bits 6 - 0 (Test Pattern Error Count[14:8]) and BIT [7:0] (Test Pattern Error Count[7:0]) within the VT Mapper - Test Pattern Detector Error Count Register (Address Locations = 0x0C16 and 0x0C17).

BIT6 - Insert Pattern Error

This bit-field is used to configure the VT-Mapper Test Pattern Generator block to insert a single bit-error into the outbound VT data-stream. A 0 to 1 transition within this bit-field will command the VT-Mapper Test Pattern Generator block to insert a single bit-error into the outbound VT data-stream.

Bits [5 - 0] - Reserved

TABLE 218: GLOBAL VT-MAPPER BLOCK - TEST PATTERN CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0C0F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT1.5 Transmit Test Pattern[1:0]		VT2 Transmit Test Pattern[1:0]		VT3 Transmit Test Pattern[1:0]		VT6 Transmit Test Pattern[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 6 - VT1.5 Transmit Test Pattern[1:0]

This READ/WRITE bit-field is used to specify the test pattern that the VT1.5 Test Pattern Generator will generate and transmit.

Transmitted Test Pattern

VT1.5 TRANSMIT TEST PATTERN[1:0]	TEST PATTERN TRANSMITTED
00	All Zeros Pattern
01	All Ones Pattern
10	Repeating 1010… Pattern
11	2^15-1 PRBS Pattern

BIT[5:4] - VT2 Transmit Test Pattern[1:0]

This READ/WRITE bit-field is used to specify the test pattern that the VT2 Test Pattern Generator will generate and transmit.

Transmitted Test Pattern

VT2 TRANSMIT TEST PATTERN[1:0]	TEST PATTERN TRANSMITTED
00	All Zeros Pattern
01	All Ones Pattern
10	Repeating 1010… Pattern
11	2^15-1 PRBS Pattern

BIT[3:2] - VT3 Transmit Test Pattern[1:0]

This READ/WRITE bit-field is used to specify the test pattern that the VT3 Test Pattern Generator will generate and transmit.

Transmitted Test Pattern

VT3 TRANSMIT TEST PATTERN[1:0]	TEST PATTERN TRANSMITTED
00	All Zeros Pattern
01	All Ones Pattern
10	Repeating 1010… Pattern
11	2^15-1 PRBS Pattern

BIT[1:0] - VT6 Transmit Test Pattern[1:0]

This READ/WRITE bit-field is used to specify the test pattern that the VT6 Test Pattern Generator will generate and transmit.

Transmitted Test Pattern

VT6 TRANSMIT TEST PATTERN[1:0]	TEST PATTERN TRANSMITTED
00	All Zeros Pattern
01	All Ones Pattern
10	Repeating 1010… Pattern
11	2^15-1 PRBS Pattern

TABLE 219: GLOBAL CONTROL - VT-MAPPER BLOCK - TEST PATTERN DROP REGISTER - BYTE 1 (ADDRESS = 0X0C12)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Channel Size[1:0]		Test Channel Drop Side SONET/SDH	Test Channel Drop Side[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7-6 - Test Channel Size[1:0]:

These two READ/WRITE bit-fields are used to specify the Size of the Test Channel (e.g., the Channel that will be used to transport the user-specified Test Pattern.

Test Channel Size

TEST CHANNEL SIZE[1:0]	TEST CHANNEL SIZE
00	VT-6
01	VT-3
10	VT2/TU-12
11	VT1.5/TU-11

BIT 5 - Test Channel Drop Side SONET/SDH

This READ/WRITE bit-field is used to select the source of the Test Channel. In this case, the user can either select either a DS1/E1 Channel originating from the Receive SONET/SDH Block or a DS1/E1 Channel originating from the Ingress Direction DS1/E1 Blocks.

- 0 - Configures the Test Channel Source to be one of the DS1/E1 Channels, originating from the Ingress Direction DS1/E1 Blocks.
- 1 - Configures the Test Channel Source to be the DS1/E1 Channels, originating from the Receive SONET/SDH Blocks

BIT[4:0] - Test Channel Drop Side[4:0]

These READ/WRITE bit-fields are used to select which data-stream will be output via the Test Channel.

Output Data Stream via Test Channel

TEST CHANNEL DROP SIDE[4:0]	TEST CHANNEL USED
00000	Do Not Use
00001	DS1/E1 Channel 1
00010	DS1/E1 Channel 2
00011	DS1/E1 Channel 3
00100	DS1/E1 Channel 4
00101	DS1/E1 Channel 5
00110	DS1/E1 Channel 6
00111	DS1/E1 Channel 7
01000	DS1/E1 Channel 8
01001	DS1/E1 Channel 9
01010	DS1/E1 Channel 10
01011	DS1/E1 Channel 11
01100	DS1/E1 Channel 12
01101	DS1/E1 Channel 13
01110	DS1/E1 Channel 14
01111	DS1/E1 Channel 15
10000	DS1/E1 Channel 16
10001	DS1/E1 Channel 17
10010	DS1/E1 Channel 18
10011	DS1/E1 Channel 19
10100	DS1/E1 Channel 20
10101	DS1/E1 Channel 21
10110	DS1/E1 Channel 22
10111	DS1/E1 Channel 23
11000	DS1/E1 Channel 24
11001	DS1/E1 Channel 25
11010	DS1/E1 Channel 26
11011	DS1/E1 Channel 27
11100	DS1/E1 Channel 28
11101	AIS will be Generated
11110	Test Channel Input
11111	User Selected Test Pattern

TABLE 220: GLOBAL CONTROL - VT-MAPPER BLOCK - TEST PATTERN DROP REGISTER - BYTE 0 (ADDRESS = 0X0C13)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive (Expected) Pattern[1:0]		Test Channel Drop Side - SONET/SDH	Test Channel Drop Side[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 6 - Receive (Expected) Pattern:

This READ/WRITE bit-field is used to specify the Test Pattern, that the VT-Mapper Pattern Receiver should be expecting, as shown in the table below.

Expected Test Pattern

RECEIVE (EXPECTED) PATTERN[1:0]	EXPECTED TEST PATTERN
00	All Zeros Pattern
01	All Ones Pattern
10	Repeating 1010… Pattern
11	2^15-1 PRBS Pattern

BIT 5 - Test Channel Drop-Side SONET/SDH

This READ/WRITE bit-field is used to select which set of DS1/E1 traffic should be used, as a basis of comparison against the Test Signal. In this case, the user can either select the either the DS1/E1 traffic originating from the Ingress Direction DS1/E1 Blocks or the DS1/E1 traffic originating from the Receive SONET/SDH Blocks.

- 0 - Configures the Pattern Receiver to compare the Test Signal with one of the DS1/E1 Channels, originating from the Ingress Direction DS1/E1 Blocks.
- 1 - Configures the Pattern Receiver to compare the Test Signal with one of the DS1/E1 Channels, originating from the Receive SONET/SDH Blocks.

BIT[4:0] - Test Channel Drop Side[4:0]:

These READ/WRITE bit-fields are used to select which data-stream will be compared with the Test Signal.

Test Channel Selection

TEST CHANNEL DROP SIDE[4:0]	TEST CHANNEL USED
00000	Do Not Use
00001	DS1/E1 Channel 1
00010	DS1/E1 Channel 2
00011	DS1/E1 Channel 3
00100	DS1/E1 Channel 4
00101	DS1/E1 Channel 5
00110	DS1/E1 Channel 6
00111	DS1/E1 Channel 7

Test Channel Selection

TEST CHANNEL DROP SIDE[4:0]	TEST CHANNEL USED
01000	DS1/E1 Channel 8
01001	DS1/E1 Channel 9
01010	DS1/E1 Channel 10
01011	DS1/E1 Channel 11
01100	DS1/E1 Channel 12
01101	DS1/E1 Channel 13
01110	DS1/E1 Channel 14
01111	DS1/E1 Channel 15
10000	DS1/E1 Channel 16
10001	DS1/E1 Channel 17
10010	DS1/E1 Channel 18
10011	DS1/E1 Channel 19
10100	DS1/E1 Channel 20
10101	DS1/E1 Channel 21
10110	DS1/E1 Channel 22
10111	DS1/E1 Channel 23
11000	DS1/E1 Channel 24
11001	DS1/E1 Channel 25
11010	DS1/E1 Channel 26
11011	DS1/E1 Channel 27
11100	DS1/E1 Channel 28
11101	AIS will be Generated
11110	Test Channel Input
11111	Disable Pattern Receiver

TABLE 221: GLOBAL CONTROL - VT-MAPPER - TEST PATTERN DETECTOR ERROR COUNT REGISTER - UPPER BYTE (ADDRESS = 0X0C16)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT-Mapper Test Pattern Sync	Test Pattern Error Count[14:8]						
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT7 - VT-Mapper Test Pattern Sync:

This READ-ONLY bit-field indicates whether or not the VT-Mapper Pattern Receiver is currently declaring Pattern Sync with the incoming Test Signal.

- 0 - VT-Mapper Pattern Receiver is NOT currently declaring Pattern Sync with the incoming Test Signal.
- 1 - VT-Mapper Pattern Receiver is currently declaring Pattern Sync with the incoming Test Signal.

BIT[6:0] - Test Pattern Error Count[14:8]:

These seven (7) RESET-upon-READ bit-fields, along with the Test Pattern Error Count[7:0] bit-fields function as a 15-bit Pattern Bit Error Count Register. If the VT-Mapper Pattern Receiver is currently declaring Pattern Sync with the designated Test Signal, then it will increment this register (by the value of 1) each time that it detects Pattern Bit Error.

These seven (7) bit-fields function as the seven most-significant bits of this 15-bit counter.

TABLE 222: GLOBAL CONTROL - VT-MAPPER - TEST PATTERN DETECTOR ERROR COUNT REGISTER - LOWER BYTE (ADDRESS = 0X0C17)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Test Pattern Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT[7:0] - Test Pattern Error Count[7:0]:

These eight (8) RESET-upon-READ bit-fields, along with the Test Pattern Error Count[14:8] bit-fields function as a 15-bit Pattern Bit Error Count Register. If the VT-Mapper Pattern Receiver is currently declaring Pattern Sync with the designated Test Signal, then it will increment this register (by the value of 1) each time that it detects Pattern Bit Error.

These eight (8) bit-fields function as the eight least-significant bits of this 15-bit counter.

TABLE 223: GLOBAL CONTROL - VT-MAPPER - TRANSMIT TRIBUTARY SIZE SELECT REGISTER (ADDRESS = 0X0C1A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		TxTributary Size Select - VT#6[1:0]		TxTributary Size Select - VT#5[1:0]		TxTributary Size Select - VT#4[1:0]	
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	1	1	1	1	1

Bits 7 - 6 - Unused:

BIT[5:4] - Transmit Tributary Size Select for VT# 6[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 6) will support.

Size of VT #6

TXTRIBUTARY SIZE SELECT - VT#6[1:0]	RESULTING SIZE OF VT # 6
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

NOTE: *This configuration setting only applies to the Transmit VT-Mapper block. This configuration setting does not configure the Receive VT-De-Mapper block to expect any particular VT-type within VT Group # 6. The user*

must separately configure the Receive VT-De-Mapper block's handling of VT-Group # 6 by setting Bits 4 and 5 (RxTributary Size Select - VT# 6[1:0]) within the VT-Mapper - Receive Tributary Size Select Register (Address = 0x0C1E).

BIT[3:2] - Transmit Tributary Size Select for VT# 5[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 5) will support.

Size of VT #5

TxTributary Size Select - VT#5[1:0]	Resulting Size of VT # 5
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[1:0] - Transmit Tributary Size Select for VT# 4[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 4), will support.

Size of VT #4

TxTributary Size Select - VT#4[1:0]	Resulting Size of VT # 4
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

Table 224: Global Control - VT-Mapper - Transmit Tributary Size Select Register (Address = 0x0C1B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTributary Size Select - VT#3[1:0]		TxTributary Size Select - VT#2[1:0]		TxTributary Size Select - VT#1[1:0]		TxTributary Size Select - VT#0[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

Bits 7 - 6 - Transmit Tributary Size Select for VT# 3[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 3), will support.

TxTributary Size Select of VT#3

TxTributary Size Select - VT#3[1:0]	Resulting Size of VT # 3
00	VT-6
01	VT-3

TxTributary Size Select of VT#3

TxTributary Size Select - VT#3[1:0]	Resulting Size of VT # 3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[5:4] - Transmit Tributary Size Select for VT# 2[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 2) will support.

TxTributary Size Select of VT#2

TxTributary Size Select - VT#2[1:0]	Resulting Size of VT # 2
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[3:2] - Transmit Tributary Size Select for VT# 1[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper block (associated with Virtual Tributary Group # 1) will support.

TxTributary Size Select of VT#1

TxTributary Size Select - VT#1[1:0]	Resulting Size of VT # 1
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[1:0] - Transmit Tributary Size Select for VT# 0[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Transmit VT-Mapper Block (associated with Virtual Tributary Group # 0) will support.

TxTributary Size Select of VT#0

TxTributary Size Select - VT#0[1:0]	Resulting Size of VT # 0
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

TABLE 225: GLOBAL CONTROL - VT-MAPPER - RECEIVE TRIBUTARY SIZE SELECT REGISTER (ADDRESS = 0X0C1E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		RxTributary Size Select - VT#6[1:0]		RxTributary Size Select - VT#5[1:0]		RxTributary Size Select - VT#4[1:0]	
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	1	1	1	1	1

Bits 7 - 6 - Unused:

BIT[5:4] - Receive Tributary Size Select for VT# 6[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper Block (associated with Virtual Tributary Group # 6) will support.

Resulting Size of VT#6

RXTRIBUTARY SIZE SELECT - VT#6[1:0]	RESULTING SIZE OF VT # 6
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[3:2] - Receive Tributary Size Select for VT# 5[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 5) will support.

Resulting Size of VT#5

RXTRIBUTARY SIZE SELECT - VT#5[1:0]	RESULTING SIZE OF VT # 5
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[1:0] - Receive Tributary Size Select for VT# 4[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 4) will support.

Resulting Size of VT#4

RXTRIBUTARY SIZE SELECT - VT#4[1:0]	RESULTING SIZE OF VT # 4
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

TABLE 226: GLOBAL CONTROL - VT-MAPPER - RECEIVE TRIBUTARY SIZE SELECT REGISTER (ADDRESS = 0X0C1F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTributary Size Select - VT#3[1:0]		RxTributary Size Select - VT#2[1:0]		RxTributary Size Select - VT#1[1:0]		RxTributary Size Select - VT#0[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT[7:6] - Receive Tributary Size Select for VT# 3[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 3) will support.

Resulting Size of VT#3

RXTRIBUTARY SIZE SELECT - VT#3[1:0]	RESULTING SIZE OF VT # 3
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[5:4] - Receive Tributary Size Select for VT# 2[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 2) will support.

Resulting Size of VT#2

RXTRIBUTARY SIZE SELECT - VT#2[1:0]	RESULTING SIZE OF VT # 2
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[3:2] - Receive Tributary Size Select for VT# 1[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 1) will support.

Resulting Size of VT#1

RXTRIBUTARY SIZE SELECT - VT#1[1:0]	RESULTING SIZE OF VT # 1
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

BIT[1:0] - Receive Tributary Size Select for VT# 0[1:0]:

These two READ/WRITE bit-fields are used to specify the VT-size (or the bit-rate to be supported by) that the Receive VT-Mapper block (associated with Virtual Tributary Group # 0) will support.

Resulting Size of VT#0

RXTRIBUTARY SIZE SELECT - VT#0[1:0]	RESULTING SIZE OF VT # 0
00	VT-6
01	VT-3
10	VT-2/TU-12
11	VT-1.5/TU-11

2.10 DS3 MAPPER CONTROL REGISTERS

TABLE 227: DS3 MAPPER BLOCK - CONTROL REGISTER - BYTE 1 (ADDRESS LOCATION = 0X0D02)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						Default_R	Default_O
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	1	1

BIT[7:0] - Reserved

BIT 1 - Default_R Value:

When a DS3 signal is mapped into an STS-1/STS-3 SPE or a VC-3, there are numerous bits that are also stuffed into the STS-1/STS-3 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STS-1/STS-3 SPE or an SDH VC-3.

One such bit is referred to as an R bit. Currently, the standards do not define a use for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment.

This READ/WRITE bit-field is used to set the value for the R bits in the outbound STS-1/STS-3 SPE or SDH VC-3.

NOTES:

1. The XRT86SH328 includes a corresponding READ-ONLY register bit, in which one can obtain the value for the R bits in the incoming STS-1/STS-3 SPE or SDH VC-3. This register bit is located in BIT 1 (Received R) within the DS3 Mapper Block - Receive Status Register - Byte 1 (Address = 0x0D06).

2. This register bit is only active if the XRT86SH328 has been configured to operate in the M13 MUX which is Asynchronously mapped into STS-1/STS-3 Mode.

BIT 0 - Default_O Value:

When a DS3 signal is mapped into a STS-1/STS-3 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that are also stuffed into the STS-1/STS-3 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STS-1/STS-3 SPE or an SDH VC-3.

One such bit is referred to as an 0 bit. Currently, the standards do not define a use for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment.

This READ/WRITE bit-field is used to set the value for the O bits in the outbound STS-1/STS-3 SPE or SDH VC-3.

NOTES:

1. The XRT86SH328 includes a corresponding READ-ONLY register bit in which one can obtain the value for the O bits in the incoming STS-1/STS-3 SPE or SDH VC-3. This register bit is located in BIT 0 (Received O) within the DS3 Mapper Block - Receive Status Register - Byte 1 (Address = 0x0D06).

2. This register bit is only active if the XRT86SH328 has been configured to operate in the M13 MUX Asynchronously Mapped into STS-1/STS-3 Mode.

TABLE 228: DS3 MAPPER BLOCK - CONTROL REGISTER - BYTE 0 (ADDRESS LOCATION = 0X0D03)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							Gap Clock in Egress T1/E1
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT[7:1] - Reserved

BIT 0 - Gap Clock in Egress T1/E1

This READ/WRITE bit-field permits the user to apply some "clock-smoothing" to the Egress Direction T1/E1 signals prior to being routed to the Transmit DS1/E1 LIU Block, as depicted below.

- 0 - Configures the chip to perform "clock-smoothing" on all Egress Direction T1/E1 signals prior to being routed to the Transmit DS1/E1 LIU Blocks.
- 1- Disables this "clock-smoothing" feature.

TABLE 229: DS3 MAPPER BLOCK - RECEIVE STATUS REGISTER - BYTE 1 (ADDRESS LOCATION = 0X0D06)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						Received_R	Received_O
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	1	1

BIT[7:2] - Reserved:

BIT 1 - Received_R:

When a DS3 signal is de-mapped from an STS-1/STS-3 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that were also stuffed into the STS-1/STS-3 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STS-1/STS-3 SPE or an SDH VC-3.

One such bit is referred to as an R bit. Currently, the standards do not define a use for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment.

This READ-ONLY bit-field contains the value of the R bits within the most recently received STS-1/STS-3 SPE or SDH VC-3.

NOTE: *The XRT86SH328 includes a corresponding READ/WRITE register bit, in which one can set the value for the R bits, in the outbound STS-1/STS-3 SPE or SDH VC-3. This register bit is located in BIT 1 (Default_R) within the DS3 Mapper Block - Control Register - Byte 1 (Address = 0x0D02).*

BIT 0 - Received_O:

When a DS3 signal is de-mapped from an STS-1/STS-3 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that were also stuffed into the STS-1/STS-3 SPE or the VC-3 in order to accommodate the frequency difference between DS3 and an STS-1/STS-3 SPE or an SDH VC-3.

One such bit is referred to as an O bit. Currently, the standards do not define a use for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment.

This READ-ONLY bit-field contains the value of the O bits within the most recently received STS-1/STS-3 SPE or SDH VC-3.

NOTE: *The XRT86SH328 includes a corresponding READ/WRITE register bit, in which one can set the value for the R bits, in the outbound STS-1/STS-3 SPE or SDH VC-3. This register bit is located in BIT 1 (Default R) within the DS3 Mapper Block - Control Register - Byte 1 (Address = 0x0D02).*

TABLE 230: DS3 MAPPER BLOCK - RECEIVE STATUS REGISTER - BYTE 0 (ADDRESS LOCATION = 0X0D07)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				Receive FIFO Over-run	Receive FIFO Under-run	Transmit FIFO Over-run	Transmit FIFO Under-run
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT[7:4] - Reserved:

BIT 3 - Receive FIFO Overrun

This READ-ONLY bit-field indicates whether or not the DS3 Mapper block is currently declaring a Receive FIFO Overrun condition.

A Receive FIFO Overrun condition will only occur if DS3 data is output from the DS3 Mapper block to the Receive DS3 Framer block at a much faster rate than that which the Receive DS3 Framer block handles and processes the incoming DS3 data-stream.

- 0 - Indicates that the DS3 Mapper Block is NOT currently declaring the Receive FIFO Overrun condition.
- 1 - Indicates that the DS3 Mapper Block is currently declaring the Receive FIFO Overrun condition.

BIT 2 - Receive FIFO Underrun

This READ-ONLY bit-field indicates whether or not the DS3 Mapper block is currently declaring the Receive FIFO Underrun condition.

A Receive FIFO Underrun condition will only occur if DS3 data is output from the DS3 Mapper block to the Receive DS3 Framer block at a much slower rate than that which the Receive DS3 Framer block handles and processes the incoming DS3 data-stream.

- 0 - Indicates that the DS3 Mapper Block is NOT currently declaring the Receive FIFO Underrun condition.
- 1 - Indicates that the DS3 Mapper Block is currently declaring the Receive FIFO Underrun condition.

BIT 1 - Transmit FIFO Overrun

This READ-ONLY bit-field indicates whether or not the DS3 Mapper block is currently declaring a Transmit FIFO Overrun condition.

A Transmit FIFO Overrun condition will occur if DS3 data is output from the Transmit DS3 Framer block (towards the DS3 Mapper Block) at a much faster rate than which the DS3 Mapper block handles and processes the outbound DS3 data-stream.

- 0 - Indicates that the DS3 Mapper Block is NOT currently declaring the Transmit FIFO Overrun condition.
- 1 - Indicates that the DS3 Mapper Block is currently declaring the Transmit FIFO Overrun condition.

BIT 0 - Transmit FIFO Underrun

This READ-ONLY bit-field indicates whether or not the DS3 Mapper block is currently declaring a Transmit FIFO Underrun condition.

A Transmit FIFO Underrun condition will occur if DS3 data is output from the Transmit DS3 Framer block (towards the DS3 Mapper Block) at a much slower rate than that which the DS3 Mapper Block handles and processes the outbound DS3 data-stream.

- 0 - Indicates that the DS3 Mapper Block is NOT currently declaring the Transmit FIFO Underrun condition.
- 1 - Indicates that the DS3 Mapper Block is currently declaring the Transmit FIFO Underrun condition.

TABLE 231: DS3 MAPPER BLOCK - RECEIVE MAPPER INTERRUPT STATUS REGISTER - BYTE 0 (ADDRESS = 0X0D0B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				Receive FIFO Over-run Interrupt Status	Receive FIFO Under-run Interrupt Status	Transmit FIFO Over-run Interrupt Status	Transmit FIFO Under-run Interrupt Status
R/O	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT[7:4] - Reserved

BIT 3 - Receive FIFO Overrun Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Receive FIFO Overrun interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the DS3 Mapper block will generate this interrupt anytime it declares a Receive FIFO Overrun condition.

- 0 - Indicates that the Receive FIFO Overrun interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Receive FIFO Overrun interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the current status of the Receive FIFO Overrun condition by reading the state of BIT 3 (Receive FIFO Overrun Condition) within the DS3 Mapper - Status Register - Byte 0 (Address = 0x0D07).*

BIT 2 - Receive FIFO Underrun Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Receive FIFO Underrun interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the DS3 Mapper Block will generate this interrupt anytime it declares a Receive FIFO Underrun condition.

- 0 - Indicates that the Receive FIFO Underrun interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Receive FIFO Underrun interrupt has occurred since the last read of this register.

NOTE: *The user can obtain the current status of the Receive FIFO Underrun condition by reading the state of BIT 2 (Receive FIFO Underrun Condition) within the DS3 Mapper - Status Register - Byte 0 (Address = 0x0D07).*

BIT 1 - Transmit FIFO Overrun Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Transmit FIFO Overrun interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the DS3 Mapper block will generate this interrupt anytime it declares a Transmit FIFO Overrun condition.

- 0 - Indicates that the Transmit FIFO Overrun Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Transmit FIFO Overrun Interrupt has occurred since the last read of this register.

NOTE: *The user can determine the current status of the Transmit FIFO Overrun condition by reading the state of BIT 1 (Transmit FIFO Overrun Condition) within the DS3 Mapper Block - Status Register - Byte 0 (Address = 0x0D07).*

BIT 0 - Transmit FIFO Underrun Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the Transmit FIFO Underrun interrupt has occurred since the last read of this register.

If this interrupt is enabled, then the DS3 Mapper block will generate this interrupt anytime it declares a Transmit FIFO Underrun condition.

- 0 - Indicates that the Transmit FIFO Underrun interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Transmit FIFO Underrun interrupt has occurred since the last read of this register.

NOTE: The user can determine the current state of the Transmit FIFO Underrun condition by reading the state of BIT 0 (Transmit FIFO Underrun Condition) within the DS3 Mapper Block - Status Register - Byte 0 (Address = 0x0D07).

TABLE 232: DS3 MAPPER BLOCK - RECEIVE MAPPER INTERRUPT ENABLE REGISTER - BYTE 0 (ADDRESS = 0X0D0E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				Receive FIFO Over-run Interrupt Enable	Receive FIFO Under-run Interrupt Enable	Transmit FIFO Over-run Interrupt Enable	Transmit FIFO Under-run Interrupt Enable
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT[7:4] - Reserved:

BIT 3 - Receive FIFO Overrun Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Receive FIFO Overrun Interrupt.

If this interrupt is enabled, then the DS3 Mapper block will generate an interrupt anytime it declares the Receive FIFO Overrun condition.

- 0 - Disables this interrupt.
- 1 - Enables this interrupt.

BIT 2 - Receive FIFO Underrun Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the 'Receive FIFO Underrun interrupt.

If this interrupt is enabled, then the DS3 Mapper Block will generate an interrupt anytime it declares the Receive FIFO Underrun condition.

- 0 - Disables this interrupt.
- 1 - Enables this interrupt.

BIT 1 - Transmit FIFO Overrun Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Transmit FIFO Overrun interrupt.

If this interrupt is enabled, then the DS3 Mapper block will generate an interrupt anytime it declares the Transmit FIFO Overrun condition.

- 0 - Disables this interrupt.
- 1 - Enables this interrupt.

BIT 0 - Transmit FIFO Underrun Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Transmit FIFO Underrun interrupt.

If this interrupt is enabled, then the DS3 Mapper block will generate an interrupt anytime that the DS3 Mapper block declares the Transmit FIFO Underrun condition.

- 0 - Disables this interrupt.
- 1 - Enables this interrupt.

TABLE 233: DS3 MAPPER BLOCK - POINTER JUSTIFICATION STATUS REGISTER - BYTE 2 (ADDRESS = 0X0D21)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PStuff	Unused						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT7 - Pstuff:

BIT[6:0] - Unused:

TABLE 234: DS3 MAPPER BLOCK - POINTER JUSTIFICATION STATUS REGISTER - BYTE 1 (ADDRESS = 0X0D22)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

TABLE 235: DS3 MAPPER BLOCK - POINTER JUSTIFICATION STATUS REGISTER - BYTE 0 (ADDRESS = 0X0D23)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

TABLE 236: DS3 MAPPER BLOCK - POINTER JUSTIFICATION JITTER CONTROL REGISTER - BYTE 1 (ADDRESS = 0X0D26)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

TABLE 237: DS3 MAPPER BLOCK - POINTER JUSTIFICATION JITTER CONTROL REGISTER - BYTE 0 (ADDRESS = 0X0D27)

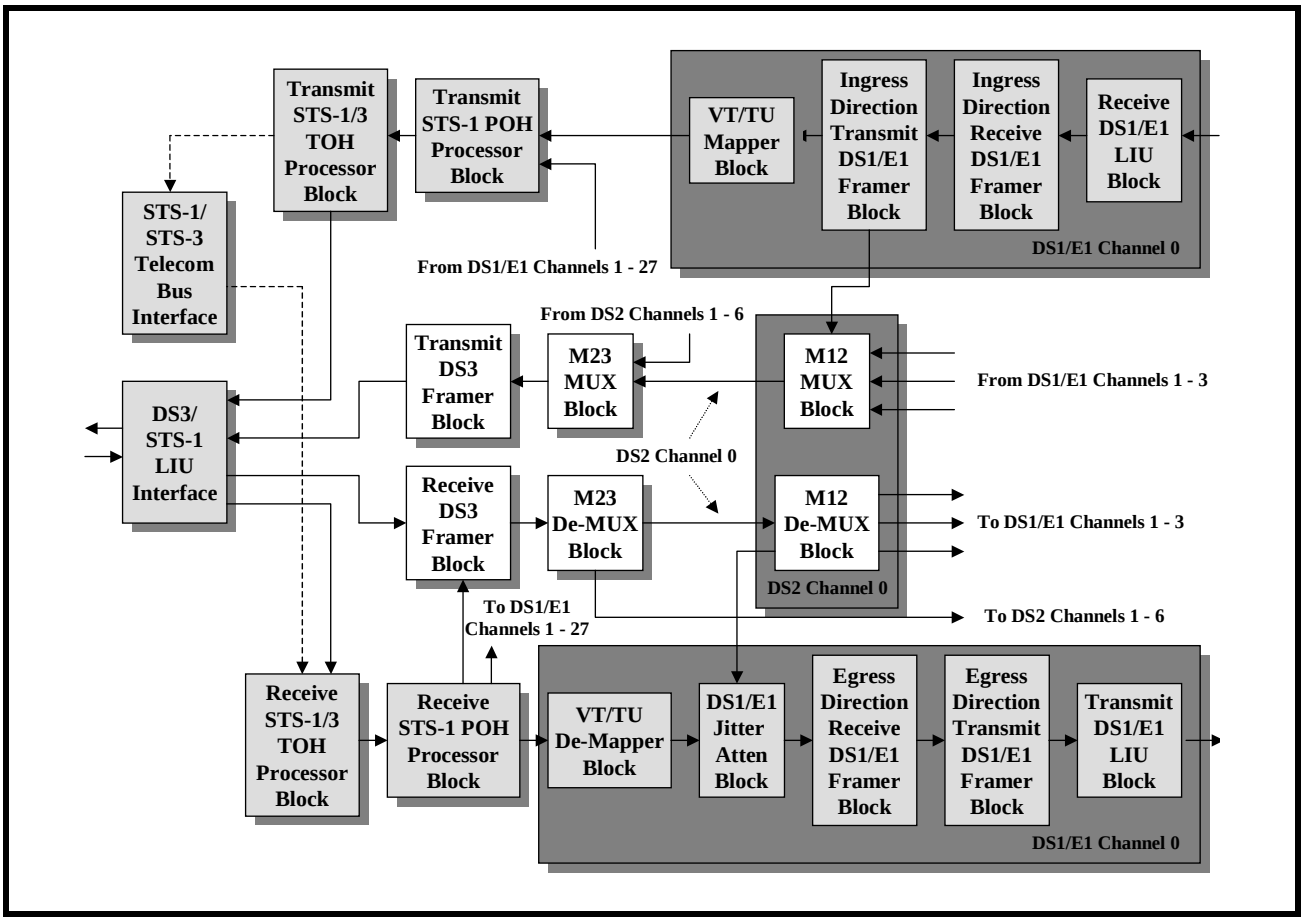
BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

2.11 DS3 Framer and M13 MUX Block Registers

The register map for the DS3 Framer and M13 MUX block is presented in the Tables below. Additionally, a detailed description of each of the DS3 Framer and M13 MUX Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328, with the various functions that are controlled/monitored via the DS3 Framer and M13 MUX Block Register highlighted is presented below in **Figure 10**.

FIGURE 10. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WITH THE FUNCTIONAL BLOCKS (WHICH ARE CONTROLLED/MONITORED VIA THE DS3 FRAMER AND M13 MUX BLOCK REGISTERS) HIGHLIGHTED.



NOTE: *These functional blocks are only active if the XRT86SH328 has been configured to operate in either the M13 MUX or in the M13 MUX, which is Asynchronously Mapped into STS-1/STS-3 Mode.*

TABLE 238: DS3 FRAMER BLOCK OPERATING MODE REGISTER (ADDRESS = 0X0E00)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS3 Framer Local Loop-Back	Set DS3 Mode	Internal LOS Enable	DS3 Framer Block Soft-ware RESET	Reserved	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	1	1	0	0	0	1	1

BIT7 - DS3 Framer Local Loop-back Mode:

This READ/WRITE bit-field is used to configure the DS3/E3 Framer block to operate in the DS3 Framer block to operate in the DS3 Framer Local Loop-back Mode. If the DS3 Framer block has been configured to operate in the Framer Local Loop-back Mode, then the output of the Transmit DS3 Framer block will be internally looped-back into the Receive DS3 Framer block.

- 0 - Configures the DS3/E3 Framer block to operate in the Normal Operation (e.g., Non-DS3 Framer Local Loop-back) mode
- 1 - Configures the DS3/E3 Framer block to operate in the DS3 Framer Local Loop-back Mode.

BIT6 - Set DS3 Mode

To use the Transmit and Receive DS3 Framer blocks, within the XRT86SH328, then the user MUST set this bit-field to 1.

BIT 5 - Internal LOS Enable

This READ/WRITE bit-field is used to enable or disable the Internal LOS Detector within the Receive DS3 Framer block. If the user enables the Internal LOS Detector, then the Receive DS3 Framer block will be configured to check the incoming DS3 signal for a sufficient number of consecutive all zero bits and it will declare and clear the LOS defect condition based upon the 1s density and the number of consecutive 0bits within the incoming DS3 data-stream.

If the user disables the Internal LOS Detector, then the Receive DS3 Framer block will NOT be configured to check the incoming DS3 data-stream for a sufficient number of consecutive 0 bits, and it will NOT declare nor clear the LOS defect condition based upon the 1s density and the number of consecutive 0 bits within the incoming DS3 data-stream.

- 0 - Disables the Internal LOS Detector
- 1 - Enables the Internal LOS Detector.

BIT 4 - DS3 Framer Block Software RESET

This READ/WRITE bit-field is used to execute a Software RESET to the Transmit and Receive DS3 Framer block. If the user executes this Software RESET, then the contents of the Transmit/Receive DS3 Framer block configuration registers will not be reset to their default values. Instead, internal state machines (within the Transmit and Receive DS3 Framer blocks) will be reset.

- A 0 to 1 transition in this bit-field commands a Software RESET to Transmit and Receive DS3 Framer block.

BIT 3 - Reserved

BIT 2 - Frame Format

This READ/WRITE bit-field is used to configure the Transmit and Receive DS3 Framer blocks to operate in either the C-Bit Parity or the M13/M23 Framing formats.

- 0 - Configures the Transmit and Receive DS3 Framer blocks to operate in the C-bit Parity Framing format.
- 1 - Configures the Transmit and Receive DS3 Framer blocks to operate in the M13/M23 Framing format.

BIT[1:0] - Transmit DS3 Framer Block Timing Reference Select[1:0]

The user should set these bit-fields to either [1, 0] or [1, 1] for proper operation.

TABLE 239: DS3 FRAMER BLOCK - I/O CONTROL REGISTER (ADDRESS = 0X0E01)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	Unused		Transmit Line Clock Invert	Receive Line Clock Invert	Reframe
R/W	R/O	R/W	R/O	R/O	R/W	R/W	R/W
1	0	1	0	0	0	0	0

BIT7 - Disable Transmit Loss of Clock Feature

This READ/WRITE bit-field is used to either enable or disable the Transmit Loss of Clock feature.

If this feature is enabled, then the DS3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a Loss of Transmit Clock Event were to occur.

The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3 Framer blocks) from hanging in the event of a Loss of Clock event.

- 0 - Enables the Transmit Loss of Clock feature.
- 1 - Disables the Transmit Loss of Clock feature

BIT6 - LOC

BIT 5 - Disable Receive Loss of Clock Feature

This READ/WRITE bit-field is used to either enable or disable the Receive Loss of Clock feature.

If this feature is enabled, then the DS3 Framer block will enable some circuitry that will terminate the current READ or

WRITE access (to the Microprocessor Interface), if a Loss of Receive Clock Event were to occur.

The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3 Framer blocks) from hanging in the event of a Loss of Clock event.

- 0 - Enables the Receive Loss of Clock feature.
- 1 - Disables the Receive Loss of Clock feature

Bits 4 -3 - Unused

BIT 2 - Transmit Line Clock Invert

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to update the TxDS3POS and TxDS3NEG output pins upon either the rising or falling edge of TxDS3LineClk.

- 0 - Configures the Transmit DS3 Framer block to update the TxDS3POS/TxDS3NEG upon the rising edge of the TxDS3LineClk. The user should insure that the LIU IC will sample TxDS3POS/TxDS3NEG upon the falling edge of TxDS3LineClk.
- 1 - Configures the Transmit DS3 Framer block to update the TxDS3POS/TxDS3NEG upon the falling edge of the TxDS3LineClk. The user should insure that the LIU IC will sample TxDS3POS/TxDS3NEG upon the rising edge of TxDS3LineClk.

BIT 1 - Receive Line Clock Invert

This READ/WRITE bit-field is used to configure Receive DS3 Framer block to sample and latch the RxDS3POS/RxDS3NEG input pins upon either the rising or falling edge of RxDS3LineClk.

- 0 - Configures the Receive DS3 Framer block to sample the RxDS3POS/RxDS3NEG input pins upon the falling edge of the RxDS3LineClk input signal.
- 1 - Configures the Receive DS3 Framer block to sample the RxDS3POS/RxDS3NEG input pins upon the rising edge of the RxDS3LineClk input signal.

BIT 0 - Receive DS3 Framer Block - Reframe Command

A 0 to 1 transition, within this bit-field commands the Receive DS3 Framer block to exit the Frame Maintenance Mode, and go back and enter the Frame Acquisition Mode.

NOTE: *The user should go back and set this bit-field to 0 following execute of the Reframe Command.*

TABLE 240: DS3 FRAMER BLOCK - BLOCK INTERRUPT ENABLE REGISTER (ADDRESS = 0X0E04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive DS3 Framer Block Interrupt Enable	Unused		M13 MUX Block Interrupt Enable	Unused		Transmit DS3 Framer Block Interrupt Enable	One Second Interrupt Enable
R/W	R/O	R/O	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Receive DS3 Framer Bock Interrupt Enable:

This READ/WRITE bit-field is used to enable or disable the Receive DS3 Framer Block for Interrupt Generation. If the user enables the Receive DS3 Framer block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the Source Level, as well, in order for these interrupt to be enabled.

However, if the user disables the Receive DS3 Framer block (for Interrupt Generation) at the Block Level, then ALL Receive DS3 Framer-related blocks are disabled.

- 0 - Disables all Receive DS3 Framer blocks interrupts.
- 1 - Enables the Receive DS3 Framer block for Interrupt Generation (at the Block Level)

Bits 6 - 5 - Unused:

Bit 4 - M13 MUX Block Interrupt Enable:

This READ/WRITE bit-field is used to enable or disable the M13 MUX block for Interrupt Generation. If the user enables

the M13 MUX block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the Source level as well, in order for these interrupts to be enabled.

However, if the user disables the M13 MX block (for Interrupt Generation) at the Block Level, then ALL M13 MUX block-related interrupts are disabled.

- 0 - Disables all M13 MUX block-related interrupts.
- 1 - Enables all M13 MUX block-related interrupts.

Bits 3 - 2 - Unused

Bit 1 - Transmit DS3 Framer Block Interrupt Enable:

This READ/WRITE bit-field is used to enable or disable the Transmit DS3 Framer block for Interrupt Generation. If the user enables the Transmit DS3 Framer block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the Source level as well, in order for these interrupts to be enabled.

However, if the user disables the Transmit DS3 Framer block (for Interrupt Generation) at the Block Level, then ALL Transmit DS3 Framer block-related interrupts are disabled.

- 0 - Disables all Transmit DS3 Framer block-related Interrupts.
- 1 - Enables the Transmit DS3 Framer block for Interrupt Generation (at the Block Level).

Bit 0 - One Second Interrupt Enable:

This READ/WRITE bit-field is used to enable or disable the One-Second Interrupt within the DS3/E3 Framer block. If the user enables this interrupt, then the DS3/E3 Framer block will generate an interrupt at one second intervals.

0 - Disables the One Second Interrupt

1 - Enables the One Second Interrupt.

TABLE 241: DS3 FRAMER BLOCK - BLOCK INTERRUPT STATUS REGISTER (ADDRESS = 0X0E05)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive DS3 Framer Block Interrupt Status	Unused		M13 MUX Block Interrupt Status	Unused		Transmit DS3 Framer Block Interrupt Status	One Second Interrupt Status
RUR	R/O	R/O	RUR	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

Bit 7 - Receive DS3 Framer Bock Interrupt Status:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block is requesting interrupt service.

- 0 - Indicates that the Receive DS3 Framer block is NOT currently requesting interrupt service.
- 1 - Indicates that the Receive DS3 Framer block is currently requesting interrupt service.

Bits 6 - 5 - Unused:

Bit 4 - M13 MUX Block Interrupt Status:

This READ-ONLY bit-field indicates whether or not the M13 MUX block is requesting interrupt service.

- 0 - Indicates that the M13 MUX block is NOT currently requesting interrupt service.
- 1 - Indicates that the M13 MUX block is currently requesting interrupt service.

Bits 3 - 2 - Unused

Bit 1 - Transmit DS3 Framer Block Interrupt Status:

This READ-ONLY bit-field indicates whether or not the Transmit DS3 Framer block is requesting interrupt service.

- 0 - Indicates that the Transmit DS3 Framer block is NOT currently requesting interrupt service.
- 1 - Indicates that the Transmit DS3 Framer block is currently requesting interrupt service.

Bit 0 - One Second Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not a One Second interrupt has occurred since the last read of this register.

- 0 - Indicates that the One Second Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the One Second Interrupt has occurred since the last read of this register.

TABLE 242: DS3 FRAMER BLOCK - M23 CONFIGURATION REGISTER (ADDRESS = 0X0E07)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Must Set to 0				M13 Local Loop-back Mode	Reserved	M23 Loop-Back Codes[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT[7:4] - Must Set to 0:

Each of these READ/WRITE bit-fields MUST be set to 0 for proper operation.

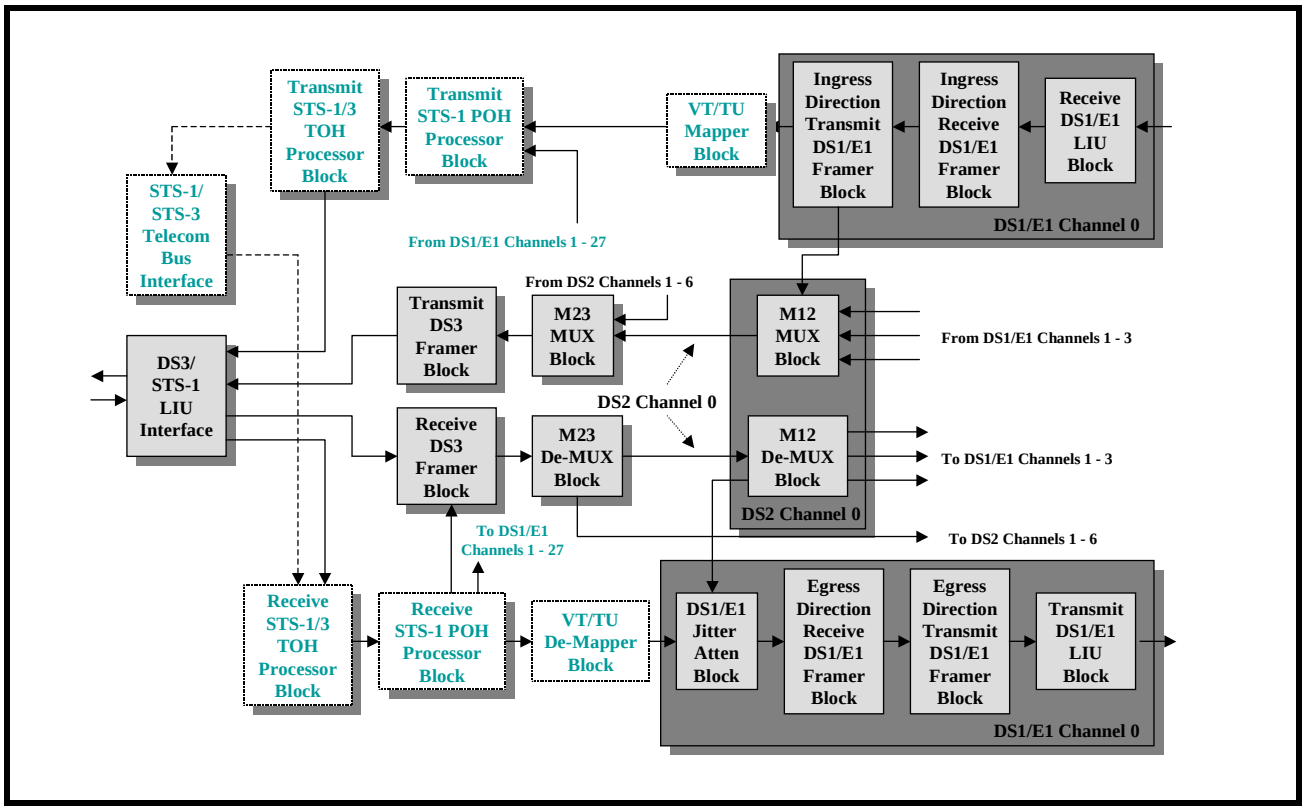
BIT 3 - M13 Local Loop-back Mode

This READ/WRITE bit-field is used to configure the XRT86SH328 to operate in the M13 Local Loop-Back Mode. If the user configures the XRT86SH328 to operate in the M23 Local Loop-back Mode, then the output of the M23 MUX Block will be internally routed to the input of the M13 DEMUX Block.

- 0 - Configures the XRT86SH328 to operate in the Normal Mode
- 1 - Configures the XRT86SH328 to operate in the M13 Local Loop-back Mode

Figure 11 presents an illustration of the XRT86SH328, whenever it has been configured to operate in the M13 Local Loop-back Mode.

FIGURE 11. AN ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WHENEVER IT HAS BEEN CONFIGURED TO OPERATE IN THE M13 LOCAL LOOP- BACK MODE



BIT 2 - Reserved

BIT[1:0] - M23 Loop-back Codes[1:0]

These READ/WRITE bit-fields are used to specify the coding (or the values that the Transmit DS3 Framer block will set the C-bits to) in order to request the remote terminal equipment to operate in the remote DS3 Loop-back Mode.

Codes to Request Remote DS3 Loop-Back Mode

M23 LOOP-BACK CODES[1:0]	C-BIT SETTINGS TO REQUEST DS2 LOOP-BACK CODES	COMMENTS
00/11	Cj1 = Cj2 = Cj3*	The Transmit DS3 Framer block will invert the state of the Cj3 bit (from that of the corresponding Cj1 and Cj2 bits) in order to request that the remote terminal execute a DS2 remote Loop-back within the jth DS2 Channel.
01	Cj1 = Cj2* = Cj3	The Transmit DS3 Framer block will insert the state of the of the Cj2 bit (from that of the corresponding Cj1 and Cj3 bits) in order to request that the remote terminal execute a remote Loop-back within the jth DS2 Channel.
10	Cj1* = Cj2 = Cj3	The Transmit DS3 Framer block will invert the state of the Cj1 bit (from that of the corresponding Cj2 and Cj3 bits) in order to request that the remote terminal execute a remote Loop-back within the jth DS2 Channel.

NOTE: *Anytime the Transmit DS3 Framer block has been configured to transmit a DS2 Loop-back request code to the remote terminal equipment, then it will set the C-bits to the appropriate value (based upon the user-selection) as specified in the above table. Further, the Transmit DS3 Framer block will transmit these DS2 Loop-back request codes (to the remote terminal equipment) for the appropriate DS2 channel, whenever the user*

commands it to do so by setting any one of the bits within the DS3 Framer Block - M23 - DS2 Loop-back Request Register (Address = 0x0E09) to 1.

TABLE 243: DS3 FRAMER BLOCK - M23 TRANSMIT DS2 AIS COMMAND REGISTER (ADDRESS = 0X0E08)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Transmit DS2 AIS - DS2 Channel 6	Transmit DS2 AIS - DS2 Channel 5	Transmit DS2 AIS - DS2 Channel 4	Transmit DS2 AIS - DS2 Channel 3	Transmit DS2 AIS - DS2 Channel 2	Transmit DS2 AIS - DS2 Channel 1	Transmit DS2 AIS - DS2 Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved

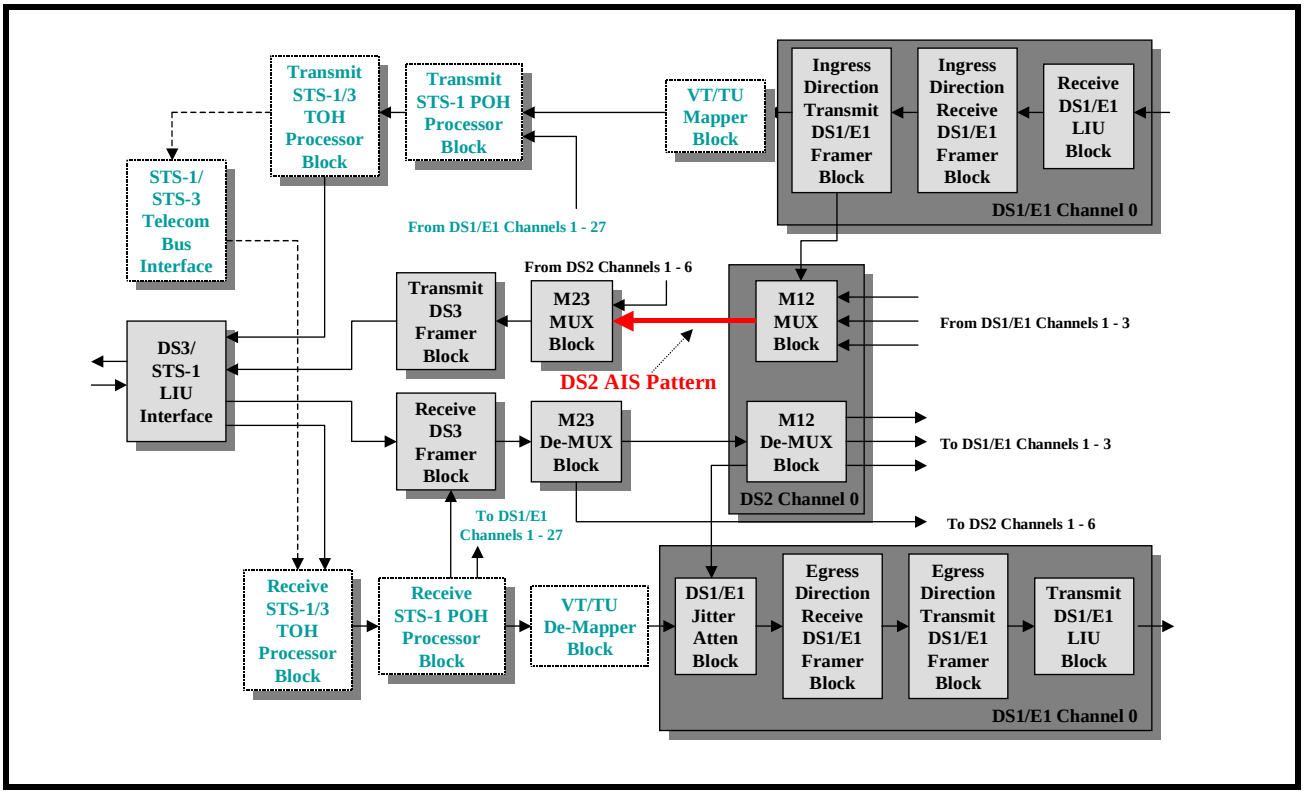
BIT6 - Transmit DS2 AIS - DS2 Channel 6:

This READ/WRITE bit-field is used to configure the M12 MUX block (associated with DS2 Channel 6) to transmit the DS2 AIS indicator, towards the Transmit DS3 Framer block (and within the outbound DS3 data-stream).

- 0 - Configures the M12 MUX block (associated with DS2 Channel 6) to transmit normal data.
- 1 - Configures the M12 MUX block (associated with DS2 Channel 6) to transmit the DS2 AIS indicator.

Figure 12 presents an illustration of the XRT86SH328, whenever the M12 MUX has been configured to transmit the DS2 AIS indicator towards both the M23 MUX and the Transmit DS3 Framer blocks.

FIGURE 12. AN ILLUSTRATION OF THE XRT86SH328, WHENEVER THE M12 MUX HAS BEEN CONFIGURED TO TRANSMIT THE DS2 AIS INDICATOR TOWARDS BOTH THE M23 MUX AND THE TRANSMIT DS3 FRAMER BLOCK



BIT 5 - Transmit DS2 AIS - DS2 Channel 5:

See BIT6 description.

BIT 4 - Transmit DS2 AIS - DS2 Channel 4:

See BIT6 description.

TBIT 3 - Transmit DS2 AIS - DS2 Channel 3:

See BIT6 description.

BIT 2 - Transmit DS2 AIS - DS2 Channel 2:

See BIT6 description.

BIT 1 - Transmit DS2 AIS - DS2 Channel 1:

See BIT6 description.

BIT 0 - Transmit DS2 AIS - DS2 Channel 0

See BIT6 description.

TABLE 244: DS3 FRAMER BLOCK - M23 - DS2 LOOP-BACK REQUEST REGISTER (ADDRESS = 0X0E09)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Transmit DS2 Loop-back Request - DS2 Channel 6	Transmit DS2 Loop-back Request - DS2 Channel 5	Transmit DS2 Loop-back Request - DS2 Channel 4	Transmit DS2 Loop-back Request - DS2 Channel 3	Transmit DS2 Loop-back Request - DS2 Channel 2	Transmit DS2 Loop-back Request - DS2 Channel 1	Transmit DS2 Loop-back Request - DS2 Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT6 - Transmit DS2 Loop-back Request - DS2 Channel 6:

This READ/WRITE bit-field is used to command the Transmit DS3 Framer block to transmit the Loop-back Request indicator, for DS2 Channel 6.

- 0 - The Transmit DS3 Framer block will NOT transmit the Loop-back Request for DS2 Channel #6 (Normal Operation)
- 1 - The Transmit DS3 Framer block will transmit the Loop-back Request for DS2 Channel # 6.

NOTE: *Whenever the user executes this command, then the Transmit DS3 Framer block will invert the appropriate C-bit of the three (e.g., C71, C72 or C73) based upon the user's setting of Bits 1 and 0 (M23 Loop-back Codes[1:0]) within the DS3 Framer Block - M23 Configuration Register (Address = 0x0E07).*

BIT 5 - Transmit DS2 Loop-back Request - DS2 Channel 5:

See BIT6 description.

BIT 4 - Transmit DS2 Loop-back Request - DS2 Channel 4:

See BIT6 description.

BIT 3 - Transmit DS2 Loop-back Request - DS2 Channel 3:

See BIT6 description.

BIT 2 - Transmit DS2 Loop-back Request - DS2 Channel 2:

See BIT6 description.

BIT 1 - Transmit DS2 Loop-back Request - DS2 Channel 1:

See BIT6 description.

BIT 0 - Transmit DS2 Loop-back Request - DS2 Channel 0:

See BIT6 description.

TABLE 245: DS3 FRAMER BLOCK - M23 LOOP-BACK ACTIVATION REGISTER (ADDRESS = 0X0E0A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Remote DS2 Loop-back - DS2 Channel 6	Remote DS2 Loop-back - DS2 Channel 5	Remote DS2 Loop-back - DS2 Channel 4	Remote DS2 Loop-back - DS2 Channel 3	Remote DS2 Loop-back - DS2 Channel 2	Remote DS2 Loop-back - DS2 Channel 1	Remote DS2 Loop-back - DS2 Channel 0
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved

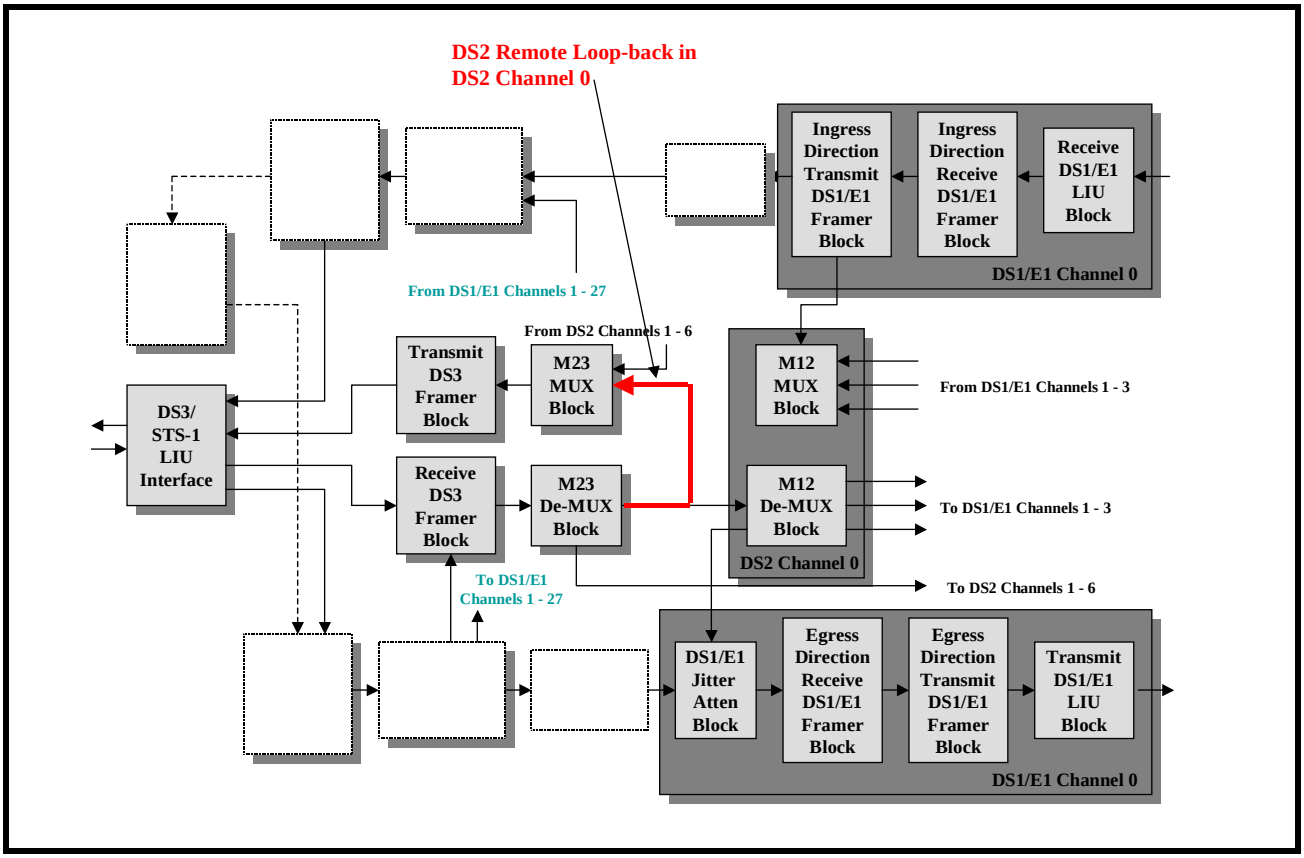
BIT6 - Remote DS2 Loop-back - DS2 Channel 6

This READ/WRITE bit-field is used to configure the XRT86SH328 to perform a Remote Loop-back of DS2 Channel 6. If the user configures the XRT86SH328 to perform this loop-back, then the Receive Direction DS2 signal (associated with Channel 6) will internally be looped back into the Transmit Direction.

- 0 - Configures DS2 Channel 6 to operate in the Normal (No Loop-back) Mode
- 1 - Configures DS2 Channel 6 to operate in the Remote Loop-back Mode.

Figure 13 presents an illustration of the Functional Block diagram of the XRT86SH328, whenever a given DS2 Channel has been configured to operate in the Remote DS2 Loop-back Mode.

FIGURE 13. AN ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WHENEVER A GIVEN DS2 CHANNEL HAS BEEN CONFIGURED TO OPERATE IN THE REMOTE DS2 LOOP-BACK MODE



BIT 5 - Remote DS2 Loop-back - DS2 Channel 5

See BIT6 description.

BIT 4 - Remote DS2 Loop-back - DS2 Channel 4

See BIT6 description.

BIT 3 - Remote DS2 Loop-back - DS2 Channel 3

See BIT6 description.

BIT 2 - Remote DS2 Loop-back - DS2 Channel 2

See BIT6 description.

BIT 1 - Remote DS2 Loop-back - DS2 Channel 1

See BIT6 description.

BIT 0 - Remote DS2 Loop-back - DS2 Channel 0

See BIT6 description.

TABLE 246: DS3 FRAMER BLOCK - M23 MUX FORCE RECEIVE DS2 AIS COMMAND REGISTERS (ADDRESS = 0X0E0B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Generate DS2 AIS Receive Path - DS2 Channel 7	Generate DS2 AIS Receive Path - DS2 Channel 6	Generate DS2 AIS Receive Path - DS2 Channel 5	Generate DS2 AIS Receive Path - DS2 Channel 4	Generate DS2 AIS Receive Path - DS2 Channel 3	Generate DS2 AIS Receive Path - DS2 Channel 2	Generate DS2 AIS Receive Path -DS2 Channel 1
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

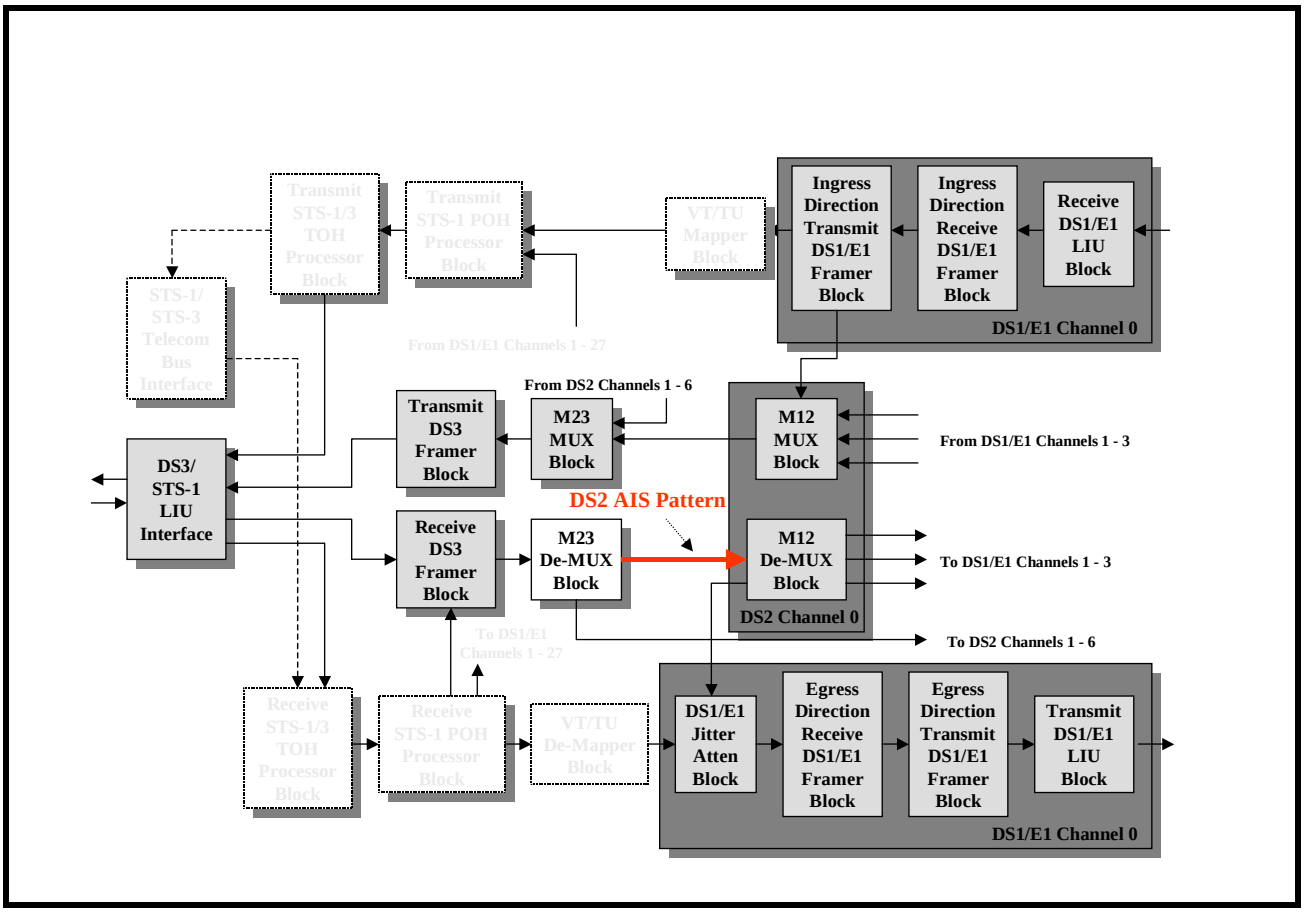
BIT6 - Generate DS2 AIS Receive Path - DS2 Channel 7

This READ/WRITE bit-field is used to configure the M23 De-MUX block to overwrite the contents of the de-muxed DS2 data-stream (associated with DS2 Channel 7) with the DS2 AIS indicator in the Egress Direction, towards its corresponding (down-stream) M12 De-MUX block.

- 0 - The M23 De-MUX block will transmit normal DS2 data to the down-stream circuitry.
- 1 - The M23 De-MUX block will transmit the DS2 AIS indicator within DS2 Channel 7, within the Egress Direction.

Figure 14 presents an illustration of the Functional Block diagram of the XRT86SH328, whenever a given DS2 Channel has been configured to transmit the DS2 AIS indicator in the Egress Direction.

FIGURE 14. AN ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WHENEVER THE M23 DE-MUX HAS BEEN CONFIGURED TO TRANSMIT THE DS2 AIS INDICATOR IN THE EGRESS DIRECTION OF DS2 CHANNEL 0



BIT 5 - Generate DS2 AIS Receive Path - DS2 Channel 6

See BIT 6 description.

BIT 4 - Generate DS2 AIS Receive Path - DS2 Channel 5

See BIT 6 description.

BIT 3 - Generate DS2 AIS Receive Path - DS2 Channel 4

See BIT 6 description.

BIT 2 - Generate DS2 AIS Receive Path - DS2 Channel 3

See BIT 6 description.

BIT 1 - Generate DS2 AIS Receive Path - DS2 Channel 2

See BIT 6 description.

BIT 0 - Generate DS2 AIS Receive Path - DS2 Channel 1

See BIT 6 description.

TABLE 247: DS3 FRAMER AND M13 MUX BLOCK - DS3 TEST REGISTER (ADDRESS = 0X0E0C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			PRBS Lock Detect	PRBS Receiver Enable	PRBS Generator Enable	Reserved	
R/O	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:5] - Reserved

BIT 4 - PRBS Lock Detect

This READ-ONLY bit-field indicates whether or not the PRBS Receiver (within the Receive DS3 Framer block) has acquired PRBS Lock with the payload data of the incoming DS3 data-stream, as described below.

- 0 - Indicates that the PRBS Receiver does not have PRBS Lock with the incoming data-stream.
- 1 - Indicates that the PRBS Receiver does have PRBS Lock with the incoming data-stream.

NOTE: *This bit-field is only valid if the PRBS Receiver has been enabled.*

BIT 3 - PRBS Receiver Enable

This READ/WRITE bit-field is used to either enable or disable the PRBS Receiver within the Receive DS3 Framer block. Once the user enables the PRBS Receiver, then it will proceed to attempt to acquire and maintain pattern sync (or PRBS Lock) within the payloadbits, within the incoming DS3 data-stream.

- 0 - Disables the PRBS Receiver
- 1 - Enables the PRBS Receiver.

BIT 2 - PRBS Generator Enable

This READ/WRITE bit-field is used to either enable or disable the PRBS Generator within the Transmit DS3 Framer block. Once the user enables the PRBS Generator block, then it will proceed to insert a PRBS Pattern into the payload bits, within the outbound DS3 data-stream.

- 0 - Disables the PRBS Generator
- 1 - Enables the PRBS Generator.

BIT 1 - Receive DS3 Framer By-Pass

BIT 0 - Transmit DS3 Framer By-Pass

TABLE 248: DS3 FRAMER AND M13 MUX BLOCK - DS3 TEST REGISTER # 2 (ADDRESS = 0X0E0E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	PRBS Type	BER Control[1:0]		Unused			Unframed PRBS
R/O	R/W	R/W	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT7 - Unused

BIT6 - PRBS Type

This READ/WRITE bit-field is used to select between two possible PRBS Patterns, that the PRBS Generator and Receiver will be handling.

- 0 - The PRBS Generator and Receiver will be handling a 2^15-1 PRBS Pattern.
- 1 - The PRBS Generator and Receiver will be handling a 2^23-1 PRBS Pattern.

NOTE: *This READ/WRITE bit-field is only active if the PRBS Receiver and Generator have been enabled.*

BIT[5:4] - BER Control[1:0]

These two READ/WRITE bit-fields are used to select the rate at which the PRBS Generator (within the Transmit DS3 Framer block) will generate and transmit Bit-Errors, within the outbound DS3/PRBS Data-Stream.

The Relationship between the BER Control[1:0] bit-fields and the Resulting Bit Error-Rate that the PRBS Generator will. Insert within the outbound DS3/PRBS data-stream

BER CONTROL[1:0]	RESULTING BIT ERROR RATE INSERTED WITHIN THE OUTBOUND DS3/PRBS DATA-STREAM
00, 11	No Bit Errors Selected (Normal Operation)
01	1 Bit per 1000 Bits are Erred
10	1 Bit per 1,000,000 Bits are Erred

NOTE: *These bit-fields are only active if the PRBS Generator has been enabled.*

BIT[3:1] - Unused

BIT 0 - Unframed PRBS

This READ/WRITE bit-field is used to configure the PRBS Generator and the Transmit DS3 Framer block to transmit either a Frame or an Unframed PRBS Pattern, within the outbound DS3 data-stream.

- 0 - Configures the PRBS Generator/Transmit DS3 Framer to transmit a Framed PRBS Pattern, whenever the PRBS Generator has been enabled.
- 1 - Configures the PRBS Generator/Transmit DS3 Framer to transmit an Unframed PRBS Pattern, whenever the PRBS Generator has been enabled.

NOTE: *This bit-field is only active if the PRBS Generator has been enabled.*

TABLE 249: DS3 FRAMER BLOCK - RECEIVE DS3 CONFIGURATION & STATUS REGISTER (ADDRESS = 0X0E10)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS3 AIS Defect Declared	DS3 LOS Defect Declared	DS3 Idle Pattern Declared	DS3 OOF Defect Declared	Reserved	Framing with Valid P-Bits	F Sync Algo	M Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	1	0	1	0	0

BIT7 - DS3 AIS Defect Declared:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block is currently declaring the AIS defect condition, within the incoming DS3 data-stream.

- 0 - Indicates that the Receive DS3 Framer block is NOT currently declaring the AIS defect condition within the incoming DS3 data-stream.
- 1 - Indicates that the Receive DS3 Framer block is currently declaring the AIS defect condition within the incoming DS3 data-stream.

BIT6 - DS3 LOS Defect Declared:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block is currently declaring the LOS defect condition, within the incoming DS3 data-stream.

- 0 - Indicates that the Receive DS3 Framer block is NOT currently declaring the LOS defect condition within the incoming DS3 data-stream.
- 1 - Indicates that the Receive DS3 Framer block is currently declaring the LOS defect condition within the incoming DS3 data-stream.

BIT 5 - DS3 Idle Pattern Declared:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block is currently declaring the DS3 Idle

Pattern, within the incoming DS3 data-stream.

- 0 - Indicates that the Receive DS3 Framer block is NOT currently declaring the Idle Pattern condition within the incoming DS3 data-stream.
- 1 - Indicates that the Receive DS3 Framer block is currently declaring the Idle Pattern condition within the incoming DS3 data-stream.

BIT 4 - DS3 OOF Defect Declared:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block is currently declaring the OOF (Out-of-Frame) defect condition.

- 0 - Indicates that the Receive DS3 Framer block is NOT currently declaring the OOF defect condition.
- 1 - Indicates that the Receive DS3 Framer block is currently declaring the OOF defect condition.

BIT 3 - Reserved:

BIT 2 - Framing with Valid P-Bits:

This READ/WRITE bit-field is used to configure the Receive DS3 Framer block to use either of the following two different sets of DS3 Frame Acquisition/Maintenance criteria.

- Normal Framing Acquisition/Maintenance Criteria (without P-bit Checking)

In this mode, the Receive DS3 Framer block will declare the In-Frame state, once it has successfully completed both the F-Bit Search and the M-Bit Search states.

- Framing Acquisition/Maintenance with P-bit Checking:

In this mode, the Receive DS3 Framer block will (in addition to passing through the F-Bit Search and M-Bit Search states) also verify valid P-bits prior to declaring the In-Frame state.

- 0 - Configures the Receive DS3 Framer block to use the Normal Framing Acquisition/Maintenance Criteria (without P-bit Checking)
- 1 - Configures the Receive DS3 Framer block to use the Framing Acquisition/Maintenance with P-Bit Checking criteria.

BIT 1 - F-Bit Search State Criteria Select:

This READ/WRITE bit-field is used to configure the Receive DS3 Framer block to use either one of the following DS3 Out-of-Frame (OOF) Defect Declaration criteria.

- 0 - Configures the Receive DS3 Framer block to declare the OOF defect condition, whenever it determines that 6 out of the most recent 15 F-bits (within the incoming DS3 data-stream) are erred.
- 1 - Configures the Receive DS3 Framer block to declare the OOF defect condition whenever it determines that 3 out of the most recent 15 F-bits (within the incoming DS3 data-stream) are erred.

BIT 0 - M-Bit Search State Criteria:

This READ/WRITE bit-field is used to configure the Receive DS3 Framer block to use either one of the following DS3 Out-of-Frame (OOF) Defect Declaration criteria.

- 0 - Configures the Receive DS3 Framer block to NOT declare the OOF defect condition whenever it detects M-bit errors.
- 1 - Configures the Receive DS3 Framer block to declare the OOF defect condition whenever it detects M-bit errors within 3 out of 4 of the most recently received DS3 frames.

TABLE 250: DS3 FRAMER BLOCK - RECEIVE DS3 STATUS REGISTER (ADDRESS = 0X0E11)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			DS3 FERF/RDI Defect Declared	Received AIC State	Received FEBE[2:0] Values		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT7 - 5 - Reserved:

BIT 4 - DS3 FERF/RDI Defect Declared:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block is currently declaring the FERF/RDI defect condition.

- 0 - Indicates that the Receive DS3 Framer block is NOT currently declaring the FERF/RDI defect condition.
- 1 - Indicates that the Receive DS3 Framer block is currently declaring the FERF/RDI defect condition.

BIT 3 - Received AIC State:

This READ-ONLY bit-field reflects the current state of the AIC bit-field within the incoming DS3 data-stream.

- 0 - Indicates that the Receive DS3 Framer block has received at least 2 consecutive M-frames that have the AIC bit-field set to 0.
- 1 - Indicates that the Receive DS3 Framer block has received at least 63 consecutive M-frames that have the AIC bit-field set to 1.

BIT[2:0] - Received FEBE[2:0] Value:

These READ-ONLY bit-fields reflects the FEBE value within the most recently received DS3 frame.

- Received FEBE[2:0] = [1, 1, 1] reflects a normal condition. All other values for Received FEBE[2:0] indicates an erred condition at the remote terminal equipment.

NOTE: *This bit-field is only active if the Transmit/Receive DS3 Framer blocks have been configured to operate in the C-bit Parity Framing format.*

TABLE 251: DS3 FRAMER BLOCK - RECEIVE DS3 INTERRUPT ENABLE REGISTER (ADDRESS = 0X0E12)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP-Bit Error Interrupt Enable	Change of DS3 LOS Defect Condition Interrupt Enable	Change of DS3 AIS Defect Condition Interrupt Enable	Change of DS3 Idle Condition Interrupt Enable	Change of DS3 FERF/RDID efect Condition Interrupt Enable	Change of AIC State Interrupt Enable	Change of DS3 OOF Defect Condition Interrupt Enable	Detection of P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Detection of CP-Bit Error Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Detection of CP-bit Error interrupt, within the XRT86SH328. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt anytime it detects at least one CP-bit error within the incoming DS3 data-stream.

- 0 - Disables the Detection of CP-Bit Error Interrupt.
- 1 - Enables the Detection of CP-Bit Error Interrupt.

NOTE: *This bit-field is only active if the Transmit and Receive DS3 Framer blocks have been configured to operate in the C-bit Parity framing format.*

BIT6 - Change of DS3 LOS Defect Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change in DS3 LOS (Loss of Signal) defect condition, within the XRT86SH328. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt in response to either of the following conditions.

- The instant that the Receive DS3 Framer block declares the LOS defect condition.
- The instant that the Receive DS3 Framer block clears the LOS defect condition.

- 0 - Disables the Change in DS3 LOS Defect Condition Interrupt.
- 1 - Enables the Change in DS3 LOS Defect Condition Interrupt.

BIT 5 - Change of DS3 AIS Defect Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change in DS3 AIS (Alarm Indication Signal) defect condition interrupt within the XRT86SH328. If this interrupt is enabled, then the Receive DS3 Framer block will generate

an interrupt in response to either of the following events.

- The instant that the Receive DS3 Framer block declares the AIS defect condition.
- The instant that the Receive DS3 Framer block clears the AIS defect condition.

▶ 0 - Disables the Change in AIS Defect Condition interrupt.

▶ 1 - Enables the Change in DS3 AIS Defect Condition Interrupt.

BIT 4 - Change of DS3 Idle Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change in DS3 Idle Condition interrupt, within the Receive DS3 Framer block. If the user enables this interrupt then the Receive DS3 Framer block will generate an interrupt in response to either of the following conditions.

- The instant that the Receive DS3 Framer block detects and declares the DS3 Idle condition.
- The instant that the Receive DS3 Framer block clears the DS3 Idle condition.

▶ 0 - Disables the Change in DS3 Idle Condition Interrupt.

▶ 1 - Enables the Change in DS3 Idle Condition Interrupt.

BIT 3 - Change of DS3 FERF/RDI Defect Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change in DS3 FERF/RDI Defect Condition Interrupt. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt in response to either of the following condition.

- The instant that the Receive DS3 Framer block declares the FERF/RDI defect condition.
- The instant that the Receive DS3 Framer block clears the FERF/RDI defect condition.

▶ 0 - Disables the Change in DS3 FERF/RDI Defect Condition Interrupt.

▶ 1 - Enables the Change in DS3 FERF/RDI Defect Condition Interrupt.

BIT 2 - Change of AIC State Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change in AIC State interrupt. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt in response to it detecting a change in the AIC bit-field, within the incoming DS3 data-stream.

▶ 0 - Disables the Change of AIC State Interrupt.

▶ 1 - Enables the Change of AIC State Interrupt.

BIT 1 - Change of DS3 OOF Defect Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change of DS3 OOF Defect Condition Interrupt. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt in response to either of the following conditions.

- The instant that the Receive DS3 Framer block declares the DS3 OOF Defect Condition.
- The instant that the Receive DS3 Framer block cleares the DS3 OOF Defect Condition.

▶ 0 - Disables the Change in DS3 OOF Defect Condition Interrupt.

▶ 1 - Enables the Change in DS3 OOF Defect Condition Interrupt.

BIT 0 - Detection of P-Bit Error Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Detection of P-Bit Error Interrupt. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt anytime it detects P-bit errors within the incoming DS3 data-stream.

▶ 0 - Disables the Detection of P-Bit Error Interrupt

▶ 1 - Enables the Detection of P-Bit Error Interrupt

TABLE 252: DS3 FRAMER BLOCK - RECEIVE DS3 INTERRUPT STATUS REGISTER (ADDRESS = 0X0E13)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP-Bit Error Interrupt Status	Change of DS3 LOS Defect Condition Interrupt Status	Change of DS3 AIS Defect Condition Interrupt Status	Change of DS3 Idle Condition Interrupt Status	Change of DS3 FERF/RDID efect Condition Interrupt Status	Change of AIC State Interrupt Status	Change of DS3 OOF Defect Condition Interrupt Status	Detection of P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT7 - Detection of CP-Bit Error Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Detection of CP-Bit Error Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Detection of CP-Bit Error Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of CP-Bit Error Interrupt has occurred since the last read of this register.

NOTE: *This bit-field is only active if the Transmit and Receive DS3 Framer block are configured to operate in the C-Bit Parity Framing Format.*

BIT6 - Change of DS3 LOS Defect Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Change in DS3 LOS Defect Condition Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Change in DS3 LOS Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in DS3 LOS Defect Condition Interrupt has occurred since the last read of this register.

BIT 5 - Change of DS3 AIS Defect Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Change of DS3 AIS Defect Condition Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Change of DS3 AIS Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of DS3 AIS Defect Condition Interrupt has occurred since the last read of this register.

BIT 4 - Change of DS3 Idle Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Change in DS3 Idle Condition interrupt has occurred since the last read of this register.

- 0 - Indicates that the Change of DS3 Idle Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of DS3 Idle Condition Interrupt has occurred since the last read of this register.

BIT 3 - Change of DS3 FERF/RDI Defect Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Change of DS3 FERF/RDI Defect Condition Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Change of DS3 FERF/RDI Defect Condition interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change in DS3 FERF/RDI Defect Condition interrupt has occurred since the last read of this register.

BIT 2 - Change of AIC State Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Change in AIC State Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Change in AIC State interrupt has NOT occurred since the last read of this register.

- 1 - Indicates that the Change in AIC State Interrupt has occurred since the last read of this register.

BIT 1 - Change of DS3 OOF Defect Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Change in DS3 OOF Defect Condition interrupt has occurred since the last read of this register.

- 0 - Indicates that the Change of DS3 OOF Defect Condition Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of DS3 OOF Defect Condition Interrupt has occurred since the last read of this register.

BIT 0 - Detection of P-Bit Error Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Detection of P-Bit Error Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Detection of P-Bit Error Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Detection of P-Bit Error Interrupt has occurred since the last read of this register.

TABLE 253: DS3 FRAMER BLOCK - RECEIVE DS3 SYNC DETECT REGISTER (ADDRESS = 0X0E14)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						F - Sync Algorithm	One and Only
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT[7:2] - Reserved:

BIT 1 - F-Sync Algorithm

This READ/WRITE bit-field is used to select the F-bit acquisition criteria when the Receive DS3 Framer block is operating in the F-Bit Search state.

- 0 - Configures the Receive DS3 Framer block to move onto the M-Bit Search state, when it has properly located 10 consecutive F-bits.
- 1 - Configures the Receive DS3 Framer block to move onto the M-Bit Search state, when it has properly located 16 consecutive F-bits.

BIT 0 - One and Only:

This READ/WRITE bit-field is used to select the F-bit acquisition criteria that the Receive DS3 Framer block will use, whenever it is operating in the F-Bit Search state, as described below.

- 0 - Configures the Receive DS3 Framer block to move onto the M-Bit Search state, whenever it has properly located 10 (or 16) consecutive F-bits (as configured in BIT 1 of this register).
- 1 - Configures the Receive DS3 Framer block to move onto the M-Bit Search state, whenever (1) it has properly located 10 (or 16) consecutive F-bits and (2) when it has located and identified only one viable F-Bit Alignment candidate.

NOTE: *If this bit is set to 1, then the Receive DS3 Framer block will NOT transition into the M-Bit Search state as long as at least two viable candidate sets of bits appears to function as the F-bits.*

TABLE 254: DS3 FRAMER BLOCK - RECEIVE DS3 FEAC REGISTER (ADDRESS = 0X0E16)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxFEAC_Code[5:0]						Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	1	1	0

BIT7 - Unused:

BIT[6:1] - Receive FEAC Code[5:0]:

These READ-ONLY bit-fields contain the value of the most recently validated FEAC Code word.

NOTE: *These register bits are only active if the Transmit and Receive DS3 Framer blocks have been configured to operate in the C-bit Parity Framing format.*

BIT 0 - Unused:

TABLE 255: DS3 FRAMER BLOCK - RECEIVE DS3 FEAC INTERRUPT ENABLE/STATUS REGISTER (ADDRESS = 0X0E17)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Set to [0, 0, 0]			FEAC Valid	Receive FEAC Removal Interrupt Enable	Receive FEAC Removal Interrupt Status	Receive FEAC Valid Interrupt Enable	Receive FEAC Valid Interrupt Status
R/W	R/W	R/W	R/O	R/W	RUR	R/W	RUR
0	0	0	0	0	0	0	0

Bits 7 - 5 - Set to [0, 0, 0]:

- Please set these three bit-fields to 0 (the default value) for normal operation.

BIT 4 - FEAC Message Valid:

This READ-ONLY bit-field indicates that the FEAC Code word (which resides within the Receive DS3 FEAC Register) has been validated by the Receive FEAC Controller block. The Receive FEAC Controller block will validate a FEAC Codeword if it has received this same codeword in 8 out of the last 10 FEAC Messages.

Polled systems can monitor this bit-field when checking for a newly validated FEAC Codeword.

- 0 - Indicates that the FEAC Message (residing in the Receive DS3 FEAC register) is no longer validated.
- 1 - Indicates that the FEAC Message (residing in the Receive DS3 FEAC register) has been validated.

BIT 3 - Receive FEAC Removal Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Receive FEAC Message Removal interrupt. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt anytime the most recently validated FEAC Message has been removed. The Receive FEAC Controller will remove a validated FEAC codeword, if it has received a different codeword in 3 out of the last 10 FEAC Messages.

- 0 - Disables the Receive FEAC Message Removal Interrupt.
- 1 - Enables the Receive FEAC Message Removal Interrupt.

BIT 2 - Receive FEAC Removal Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Receive FEAC Message Removal Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Receive FEAC Message Removal Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Receive FEAC Message Removal Interrupt has occurred since the last read of this register.

BIT 1 - Receive FEAC Valid Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Receive FEAC Message Validation Interrupt. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt anytime the Receive FEAC Controller block has validated a new FEAC Code word.

- 0 - Disables the Receive FEAC Message Validation Interrupt.
- 1 - Enables the Receive FEAC Message Validation Interrupt.

BIT 0 - Receive FEAC Valid Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Receive FEAC Message Validation Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Receive FEAC Message Validation Interrupt has NOT occurred since the last read of this

register.

- 1 - Indicates that the Receive FEAC Message Validation Interrupt has occurred since the last read of this register.

TABLE 256: DS3 FRAMER BLOCK - RECEIVE LAPD CONTROL REGISTER (ADDRESS = 0X0E18)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Any Kind of LAPD Message	Unused				Receive LAPD Controller Block Enable	Receive LAPD Message Interrupt Enable	Receive LAPD Message Interrupt Status
R/W	R/O	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT7 - Receive Any Kind of LAPD Message:

This READ/WRITE bit-field is used to configure the Receive LAPD Controller block to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller block will be capable of receiving any kind of HDLC Message (with any value the header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes.

- 0 - Does not invoke the Any Kind of HDLC Message feature.

In this case, the Receive LAPD Controller block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.

- 1 - Invokes this Any Kind of HDLC Message feature.

In this case, the Receive LAPD Controller block will be able to receive HDLC Messages that contains any header byte values.

NOTE: *The user can determine the size (or byte count) of the most recently received LAPD/PMDL Message by reading the contents of the Receive LAPD Byte Count Register (Address = 0x0E84).*

BIT[6:3] - Unused:

BIT 2 - Receive LAPD Controller Block Enable:

This READ/WRITE bit-field is used to either enable or disable the Receive LAPD Controller block within the Receive DS3 Framer block. If the user enables the Receive LAPD Controller block, then it will immediately begin extracting out and monitoring the data (being carried via the DL bits) within the incoming DS3 data-stream.

- 0 - Disables the Receive LAPD Controller block.
- 1 - Enables the Receive LAPD Controller block.

BIT 1 - Receive LAPD Message Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Receive LAPD Message Interrupt. If this interrupt is enabled, then the Receive DS3 Framer block will generate an interrupt anytime the Receive LAPD Controller block receives a new PMDL Message.

- 0 - Disables the Receive LAPD Message Interrupt.
- 1 - Enables the Receive LAPD Message Interrupt.

BIT 0 - Receive LAPD Message Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Receive LAPD Message Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Receive LAPD Message Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Receive LAPD Message' Interrupt has occurred since the last read of this register.

TABLE 257: DS3 FRAMER BLOCK - RECEIVE DS3 LAPD STATUS REGISTER (ADDRESS = 0X0E19)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Receive ABORT	RxLAPD_Msg_Type[1:0]		Receive C/R Type	Receive LAPD FCS Error Detected	End of Message	Flag Sequence Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT7 - Unused:

BIT6 - Receive ABORT:

This READ-ONLY bit-field indicates that the Receive LAPD Controller block has received an ABORT sequence (e.g., a string of seven consecutive 0s) within the incoming data-stream.

- 0 - Indicates that the Receive LAPD Controller block has NOT received an ABORT sequence.
- 1 - Indicates that the Receive LAPD Controller block has received an ABORT sequence.

NOTE: *Once the Receive LAPD Controller block receives an ABORT Sequence, it will set this bit-field high until it receives another LAPD Message.*

BIT[5:4] - Receive LAPD Message Type[1:0]:

These two READ-ONLY bit-fields indicate the type of LAPD Message that is residing within the Receive LAPD Message Buffer. The relationship between the contents of these two bit-fields and the corresponding message type is presented below.

Message Type

RECEIVE LAPD MESSAGE TYPE[1:0]		MESSAGE TYPE
0	0	CL Path Identification
0	1	Idle Signal Identification
1	0	Test Signal Identification
1	1	ITU-T Path Identification

BIT 3 - Receive C/R Type:

This READ-ONLY bit-field indicates the value of the C/R bit-field (within one of the header bytes) of the most recently received LAPD Message.

BIT 2 - Receive LAPD FCS Error Detected:

This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error or not.

- 0 - Indicates that the most recently received LAPD Message frame does not contain an FCS error.
- 1 - Indicates that the most recently received LAPD Message frame does contain an FCS error.

BIT 1 - End of Message:

This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block has received a complete LAPD Message.

- 0 - Indicates that the Receive LAPD Controller block is currently receiving a LAPD Message, but has not received the complete message.
- 1 - Indicates that the Receive LAPD Controller block has received a complete LAPD Message.

NOTE: *Once the Receive LAPD Controller block sets this bit-field high, this bit-field will remain high until the Receive LAPD Controller block begins to receive a new LAPD Message.*

BIT 0 - Flag Sequence Present:

This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel).

- 0 - Indicates that the Receive LAPD Controller block is NOT currently receiving the Flag Sequence octet within the incoming Data Link channel.
- 1 - Indicates that the Receive LAPD Controller block is currently receiving a continuous stream of Flag Sequence octets within the incoming Data Link channel.

TABLE 258: DS3 FRAMER BLOCK - M12 CONFIGURATION REGISTER - DS2 CHANNEL # 1 (ADDRESS = 0X0E1A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			Set G.747 Mode	Set G.747 Reserved Bit	M12 FERF Bit Setting	M12 Loop-back Code[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7, 5 - Reserved

BIT 4 - Set G.747 Mode

This READ/WRITE bit-field is used to configure the M12 MUX and De-MUX (associated with DS2 Channel # 1) to operate in either the DS2 or the G.747 Mode. If the user configures the M12 MUX and De-MUX to operate in the DS2 Mode, then all of the following will be true.

- The M12 MUX will multiplex four (4) DS1 signals into a DS2 signal, prior to routing it to the M23 MUX.
- The M12 De-MUX will accept a DS2 data-stream (from the M23 De-MUX) and it will de-multiplex this data-stream into four (4) DS1 signals (prior to being output to the Egress Direction Receive DS1/E1 Framer block).

Likewise, if the user configures the M12 MUX and De-MUX to operate in the G.747 Mode, then all of the following will be true.

- The M12 MUX will multiplex three (3) E1 signals into a G.747 data-stream, prior to routing it to the M23 MUX
- The M12 De-MUX will accept a G.747 data-stream (from the M23 De-MUX) and it will de-multiplex this data-stream into three (3) E1 signals (prior to being output to the Egress Direction Receive DS1/E1 Framer block).

- 0 - Configures the M12 MUX (associated with DS2 Channel # 1) to operate in the DS2 Mode.
- 1 - Configures the M12 MUX (associated with DS2 Channel # 1) to operate in the G.747 Mode.

BIT 3 - Set G.747 Reserved Bit

This READ/WRITE bit-field is used to configure M12 MUX to set the Reserved bit (within a G.747 data-stream) to either a 0 or 1.

- 0 - Configures the M12 MUX to set the G.747 Reserved bit (within the outbound G.747 data-stream) to 0.
- 1 - Configures the M12 MUX to set the G.747 Reserved bit (within the outbound G.747 data-stream) to 1.

NOTE: *This bit-field is only active if the M12 MUX/De-MUX has been configured to operate in the G.747 Mode.*

BIT 2 - Set M12 FERF Bit Value

Bits 1, 0 - M12 Loop-back Code[1:0]:

These READ/WRITE bit-fields are used to specify the coding (or the values that the M12 MUX block will set the C-bits, within its outbound DS2 data-stream to) in order to request that the remote terminal equipment operate in the remote DS1 Loop-back Mode.

Loop-Back Codes

M12 Loop-Back Codes[1:0]	C-Bit Settings to Request DS2 Loop-back Codes	Comments
00/11	Cj1 = Cj2 = Cj3*	The M12 MUX block will invert the state of the Cj3 bit (from that of the corresponding Cj1 and Cj2 bits) within the outbound DS2 signal in order to request that the remote terminal execute a remote Loop-back within the jth DS1 signal.
01	Cj1 = Cj2* = Cj3	The M12 MUX block will insert the state of the of the Cj2 bit (from that of the corresponding Cj1 and Cj3 bits) within the outbound DS2 signal in order to request that the remote terminal execute a remote Loop-back within the jth DS1 signal.
10	Cj1* = Cj2 = Cj3	The M12 MUX block will invert the state of the Cj1 bit (from that of the corresponding Cj2 and Cj3 bits) in order to request that the remote terminal execute a remote Loop-back within the jth DS1 signal.

Note: Anytime the M12 MUX block has been configured to transmit a DS2 Loop-back request code, then it will set the C-bits to the appropriate value (based upon the user-selection) as specified in the above table.

Table 259: DS3 Framer Block - M12 Configuration Register - DS2 Channel # 2 (Address = 0x0E1B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			Set G.747 Mode	Set G.747 Reserved Bit	M12 FERF Bit Setting	M12 Loop-back Code[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 258 above, for Bit descriptions, substituting Channel 2 for Channel 1.

Table 260: DS3 Framer Block - M12 Configuration Register - DS2 Channel # 3 (Address = 0x0E1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			Set G.747 Mode	Set G.747 Reserved Bit	M12 FERF Bit Setting	M12 Loop-back Code[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 258 above, for Bit descriptions, substituting Channel 3 for Channel 1.

Table 261: DS3 Framer Block - M12 Configuration Register - DS2 Channel # 4 (Address = 0x0E1D)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			Set G.747 Mode	Set G.747 Reserved Bit	M12 FERF Bit Setting	M12 Loop-back Code[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 258 above, for Bit descriptions, substituting Channel 4 for Channel 1.

TABLE 262: DS3 FRAMER BLOCK - M12 CONFIGURATION REGISTER - DS2 CHANNEL # 5 (ADDRESS = 0X0E1E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			Set G.747 Mode	Set G.747 Reserved Bit	M12 FERF Bit Setting	M12 Loop-back Code[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 258 above, for Bit descriptions, substituting Channel 5 for Channel 1.

TABLE 263: DS3 FRAMER BLOCK - M12 CONFIGURATION REGISTER - DS2 CHANNEL # 6 (ADDRESS = 0X0E1F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			Set G.747 Mode	Set G.747 Reserved Bit	M12 FERF Bit Setting	M12 Loop-back Code[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 258 above, for Bit descriptions, substituting Channel 6 for Channel 1.

TABLE 264: DS3 FRAMER BLOCK - M12 CONFIGURATION REGISTER - DS2 CHANNEL # 7 (ADDRESS = 0X0E20)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved			Set G.747 Mode	Set G.747 Reserved Bit	M12 FERF Bit Setting	M12 Loop-back Code[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 258 above, for Bit descriptions, substituting Channel 7 for Channel 1.

TABLE 265: DS3 FRAMER BLOCK - M12 DE-MUX FORCE DS1/E1 AIS REGISTER - DS2 CHANNEL # 1 (ADDRESS = 0X0E21)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force Receive DS1/E1 AIS - DS1/E1 Channel 4	Force Receive DS1/E1 AIS - DS1/E1 Channel 3	Force Receive DS1/E1 AIS - DS1/E1 Channel 2	Force Receive DS1/E1 AIS - DS1/E1 Channel 1	Force Transmit DS1/E1 AIS - DS1/E1 Channel 4	Force Transmit DS1/E1 AIS - DS1/E1 Channel 3	Force Transmit DS1/E1 AIS - DS1/E1 Channel 2	Force Transmit DS1/E1 AIS - DS1/E1 Channel 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Force Receive DS1/E1 AIS - DS1/E1 Channel 4

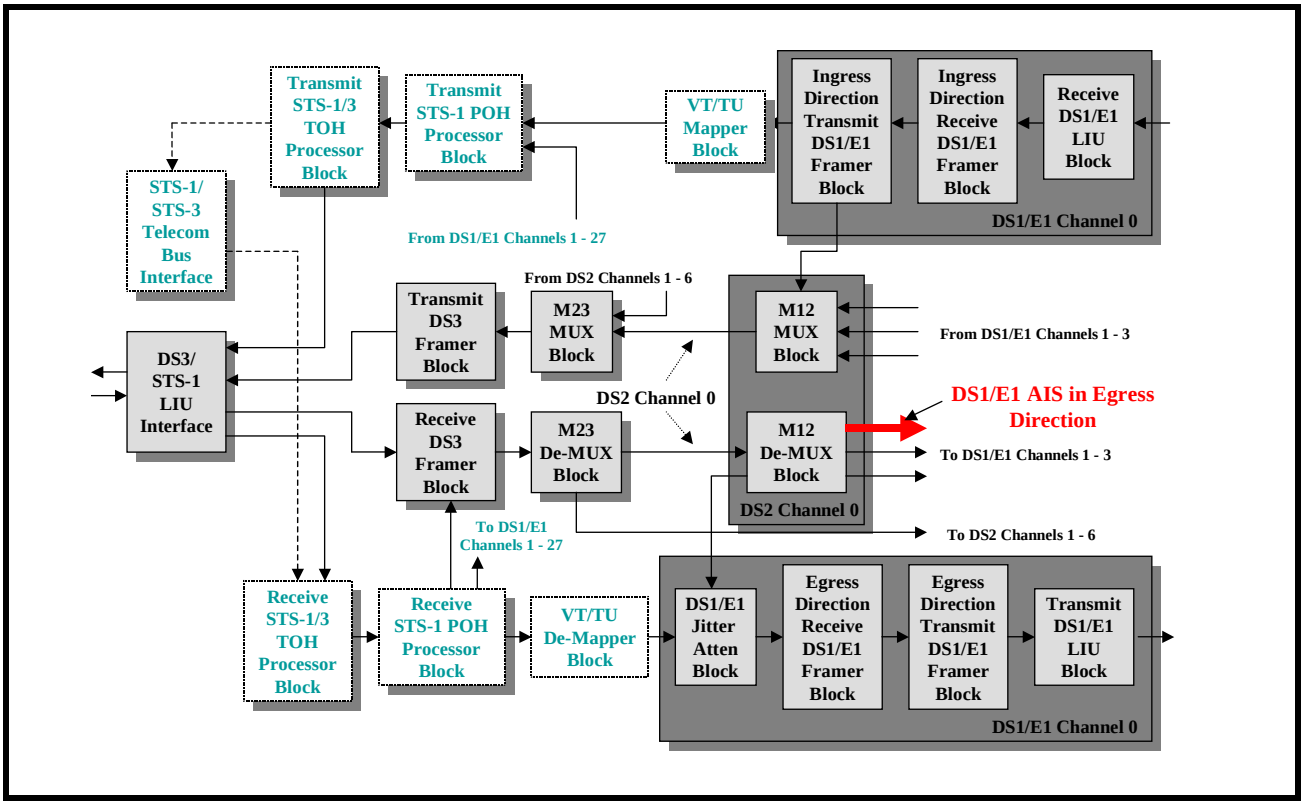
This READ/WRITE bit-field is used to force the M12 De-MUX Block (associated with DS2 Channel # 0) to overwrite the Egress Direction or De-Multiplexed DS1/E1 Signal associated with DS1/E1 Channel 4, with a DS1/E1 AIS Pattern as it is de-muxing this DS1/E1 signal from the incoming DS2 data-stream, as described below.

- 0 - Configures the M12 De-MUX block to NOT transmit the DS1/E1 AIS Pattern, via Egress Direction DS1/E1 Channel 4.
- 1 - Configures the M12 De-MUX block to transmit the DS1/E1 AIS Pattern, via Egress Direction DS1/E1 Channel 4.

Figure 15 presents an illustration of the Functional Block diagram of the XRT86SH328, whenever a given M12 De-MUX block has been configured to transmit the DS1/E1 AIS indicator (within a given DS1/E1 signal) in the Egress Direction.

NOTE: For normal operation, the user MUST set this bit-field to 0.

FIGURE 15. AN ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WHENEVER A GIVEN M12 DE-MUX BLOCK HAS BEEN CONFIGURED TO TRANSMIT THE DS1/E1 AIS INDICATOR (WITHIN A GIVEN DS1/E1 SIGNAL) IN THE EGRESS DIRECTION



BIT6 - Force Receive DS1/E1 AIS - DS1/E1 Channel 3

See Description of BIT7.

BIT 5 - Force Receive DS1/E1 AIS - DS1/E1 Channel 2

See Description of BIT7.

BIT 4 - Force Receive DS1/E1 AIS - DS1/E1 Channel 1

See Description of BIT7.

BIT 3 - Force Transmit DS1/E1 AIS - DS1/E1 Channel 4

This READ/WRITE bit-field is used to force the M12 MUX Block (associated with DS2 Channel # 0) to overwrite the Ingress Direction DS1/E1 Signal (associated with DS1/E1 Channel 4, with a DS1/E1 AIS Pattern. If the user invoke this feature, then the M12 MUX Block will transmit a DS1/E1 AIS pattern (within DS1/E1 Channel 4) towards the M23 MUX Block.

- 0 - Configures the M12 MUX Block to NOT transmit the DS1/E1 AIS Pattern, via the Ingress Direction DS1/E1 Channel 3.
- 1 - Configures the M12 MUX Block to transmit the DS1/E1 AIS Pattern, via the Ingress Direction DS1/E1 Channel 3.

NOTE: For normal operation, the user MUST set this bit-field to 0.

BIT 2 - Force Transmit DS1/E1 AIS - DS1/E1 Channel 3

See description of BIT 3.

BIT 1 - Force Transmit DS1/E1 AIS - DS1/E1 Channel 2

See description of BIT 3.

BIT 0 - Force Transmit DS1/E1 AIS - DS1/E1 Channel 1

See description of BIT 3.

TABLE 266: DS3 FRAMER BLOCK - M12 AIS REGISTER - DS2 CHANNEL # 1 (ADDRESS = 0X0E22)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force Receive DS1/E1 AIS - DS1/E1 Channel 7	Force Receive DS1/E1 AIS - DS1/E1 Channel 6	Force Receive DS1/E1 AIS - DS1/E1 Channel 5	Force Receive DS1/E1 AIS - DS1/E1 Channel 4	Force Transmit DS1/E1 AIS - DS1/E1 Channel 7	Force Transmit DS1/E1 AIS - DS1/E1 Channel 6	Force Transmit DS1/E1 AIS - DS1/E1 Channel 5	Force Transmit DS1/E1 AIS - DS1/E1 Channel 4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Figure 265 above, for Bit descriptions, substituting DS2 Channel 1 for DS2 Channel 0 and Receive

TABLE 267: DS3 FRAMER BLOCK - M12 AIS REGISTER - DS2 CHANNEL # 2 (ADDRESS = 0X0E23)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force Receive DS1/E1 AIS - DS1/E1 Channel 11	Force Receive DS1/E1 AIS - DS1/E1 Channel 10	Force Receive DS1/E1 AIS - DS1/E1 Channel 9	Force Receive DS1/E1 AIS - DS1/E1 Channel 8	Force Transmit DS1/E1 AIS - DS1/E1 Channel 11	Force Transmit DS1/E1 AIS - DS1/E1 Channel 10	Force Transmit DS1/E1 AIS - DS1/E1 Channel 9	Force Transmit DS1/E1 AIS - DS1/E1 Channel 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Figure 265 above, for Bit descriptions, substituting DS2 Channel 2 for DS2 Channel 0 and Receive

TABLE 268: DS3 FRAMER BLOCK - M12 AIS REGISTER - DS2 CHANNEL # 3 (ADDRESS = 0X0E24)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force Receive DS1/E1 AIS - DS1/E1 Channel 15	Force Receive DS1/E1 AIS - DS1/E1 Channel 14	Force Receive DS1/E1 AIS - DS1/E1 Channel 13	Force Receive DS1/E1 AIS - DS1/E1 Channel 12	Force Transmit DS1/E1 AIS - DS1/E1 Channel 15	Force Transmit DS1/E1 AIS - DS1/E1 Channel 14	Force Transmit DS1/E1 AIS - DS1/E1 Channel 13	Force Transmit DS1/E1 AIS - DS1/E1 Channel 12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Figure 265 above, for Bit descriptions, substituting DS2 Channel 3 for DS2 Channel 0 and Receive DS1/E1 AIS - DS1/E1 Channel [15:12] Receive DS1/E1 AIS - DS1/E1 Channel [3:0].

TABLE 269: DS3 FRAMER BLOCK - M12 AIS REGISTER - DS2 CHANNEL # 4 (ADDRESS = 0X0E25)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force Receive DS1/E1 AIS - DS1/E1 Channel 19	Force Receive DS1/E1 AIS - DS1/E1 Channel 18	Force Receive DS1/E1 AIS - DS1/E1 Channel 17	Force Receive DS1/E1 AIS - DS1/E1 Channel 16	Force Transmit DS1/E1 AIS - DS1/E1 Channel 19	Force Transmit DS1/E1 AIS - DS1/E1 Channel 18	Force Transmit DS1/E1 AIS - DS1/E1 Channel 17	Force Transmit DS1/E1 AIS - DS1/E1 Channel 16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Figure 265 above, for Bit descriptions, substituting DS2 Channel 4 for DS2 Channel 0 and Receive DS1/E1 AIS - DS1/E1 Channel [19:16] Receive DS1/E1 AIS - DS1/E1 Channel [3:0].

TABLE 270: DS3 FRAMER BLOCK - M12 AIS REGISTER - DS2 CHANNEL # 5 (ADDRESS = 0X0E26)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force Receive DS1/E1 AIS - DS1/E1 Channel 23	Force Receive DS1/E1 AIS - DS1/E1 Channel 22	Force Receive DS1/E1 AIS - DS1/E1 Channel 21	Force Receive DS1/E1 AIS - DS1/E1 Channel 20	Force Transmit DS1/E1 AIS - DS1/E1 Channel 23	Force Transmit DS1/E1 AIS - DS1/E1 Channel 22	Force Transmit DS1/E1 AIS - DS1/E1 Channel 21	Force Transmit DS1/E1 AIS - DS1/E1 Channel 20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Figure 265 above, for Bit descriptions, substituting DS2 Channel 5 for DS2 Channel 0 and Receive DS1/E1 AIS - DS1/E1 Channel [23:20] Receive DS1/E1 AIS - DS1/E1 Channel [3:0].

TABLE 271: DS3 FRAMER BLOCK - M12 AIS REGISTER - DS2 CHANNEL # 6 (ADDRESS = 0X0E27)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force Receive DS1/E1 AIS - DS1/E1 Channel 27	Force Receive DS1/E1 AIS - DS1/E1 Channel 26	Force Receive DS1/E1 AIS - DS1/E1 Channel 25	Force Receive DS1/E1 AIS - DS1/E1 Channel 21	Force Transmit DS1/E1 AIS - DS1/E1 Channel 27	Force Transmit DS1/E1 AIS - DS1/E1 Channel 26	Force Transmit DS1/E1 AIS - DS1/E1 Channel 25	Force Transmit DS1/E1 AIS - DS1/E1 Channel 24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Figure 265 above, for Bit descriptions, substituting DS2 Channel 5 for DS2 Channel 0 and Receive DS1/E1 AIS - DS1/E1 Channel [27:21] Receive DS1/E1 AIS - DS1/E1 Channel [3:0].

TABLE 272: DS3 FRAMER BLOCK - M12 LOOP-BACK REGISTER - 1 (ADDRESS = 0X0E28)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M12 Remote Loop Back Mode - DS1 Channel 3	M12 Remote Loop-Back Mode - DS1 Channel 2	M12 Remote Loop-Back Mode - DS1 Channel 1	M12 Remote Loop-Back Mode - DS1 Channel 0	M12 Loop-Back Request - DS1 Channel 3	M12 Loop-Back Request - DS1 Channel 2	M12 Loop-Back Request - DS1 Channel 1	M12 Loop-Back Request - DS1 Channel 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

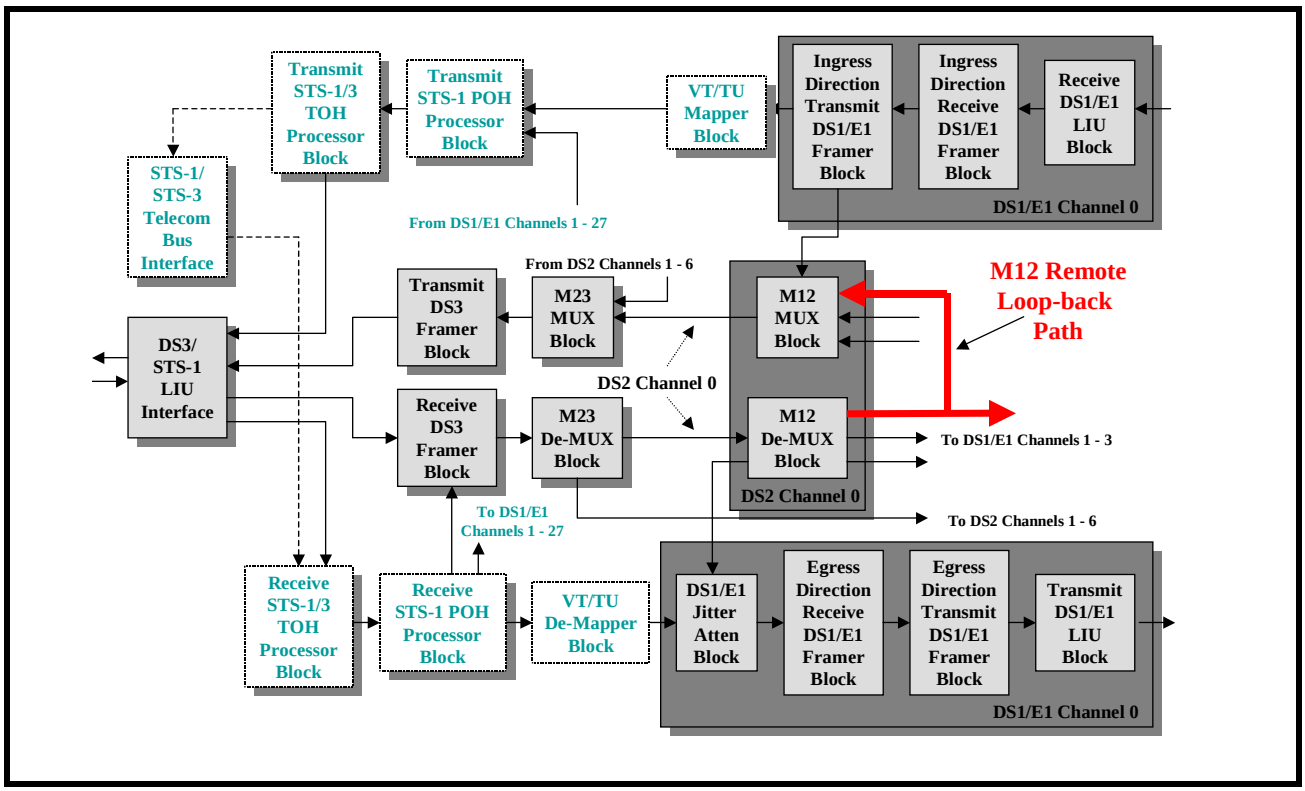
BIT7 - M12 Remote Loop-Back Mode - DS1 Channel 3

This READ/WRITE bit-field is used to configure DS1 Channel 3 to operate in the M12 Remote Loop-back Mode. If the user configures DS1 Channel 3 to operate in the M12 Remote Loop-back Mode, then the Egress Direction DS1 Channel 3 signal (as it is de-multiplexed from the DS2 signal by the M12 De-MUX block) will be internally looped back into the Ingress Direction (back towards the M12 MUX block).

- 0 - Configures DS1 Channel 3 to NOT operate in the M12 Remote Loop-back Mode (Normal Operation)
- 1 - Configures DS1 Channel 3 to operate in the M12 Remote Loop-back Mode.

Figure 16 presents an illustration of the Functional Block Diagram of the XRT86SH328, whenever it has been configured to operate in the M12 Remote Loop-back Mode.

FIGURE 16. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WHENEVER IT HAS BEEN CONFIGURED TO OPERATE IN THE M12 REMOTE LOOP-BACK MODE



BIT6 - M12 Remote Loop-Back Mode - DS1 Channel 2

See description of BIT7.

BIT 5 - M12 Remote Loop-Back Mode - DS1 Channel 1

See description of BIT7.

BIT 4 - M12 Remote Loop-Back Mode - DS1 Channel 0

See description of BIT7.

BIT 3 - M12 Loop-back Request - DS1 Channel 3

This READ/WRITE bit-field is used to command the M12 MUX block to transmit the Loop-back Request indicator for DS1 Channel 3.

- 0 - The M12 MUX block will NOT transmit the Loop-back Request for DS1 Channel 3 (Normal Operation).
- 1 - The M12 MUX block will transmit the Loop-back Request for DS1 Channel 3.

NOTE: *Whenever the user executes this command, then the M12 MUX Block (associated with DS2 Channel # 0) will invert the appropriate C-bits of the three (e.g., C41, C42 or C43) within the outbound DS2 data-stream based upon the user's settings of Bits 1 and 0 (M12 Loop-back Codes[1:0]) within the DS3 Framer Block - M12 Configuration Register - DS2 Channel # 0 (Address = 0x0E1A).*

BIT 2 - M12 Loop-back Request - DS1 Channel 2

See description of BIT 3.

BIT 1 - M12 Loop-back Request - DS1 Channel 1

See description of BIT 3.

BIT 0 - M12 Loop-back Request - DS1 Channel 0

See description of BIT 3.

TABLE 273: DS3 FRAMER BLOCK - M12 LOOP-BACK REGISTER - 2 (ADDRESS = 0X0E29)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M12 Remote Loop Back Mode - DS1 Channel 7	M12 Remote Loop-Back Mode - DS1 Channel 6	M12 Remote Loop-Back Mode - DS1 Channel 5	M12 Remote Loop-Back Mode - DS1 Channel 4	M12 Loop-Back Request - DS1 Channel 7	M12 Loop-Back Request - DS1 Channel 6	M12 Loop-Back Request - DS1 Channel 5	M12 Loop-Back Request - DS1 Channel 4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] See Table 272 above for bit descriptions, substituting Channel [7:4] for Channel [3:0}.

TABLE 274: DS3 FRAMER BLOCK - M12 LOOP-BACK REGISTER - 3 (ADDRESS = 0X0E2A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M12 Remote Loop Back Mode - DS1 Channel 11	M12 Remote Loop-Back Mode - DS1 Channel 10	M12 Remote Loop-Back Mode - DS1 Channel 9	M12 Remote Loop-Back Mode - DS1 Channel 8	M12 Loop-Back Request - DS1 Channel 11	M12 Loop-Back Request - DS1 Channel 10	M12 Loop-Back Request - DS1 Channel 9	M12 Loop-Back Request - DS1 Channel 8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] See Table 272 above for bit descriptions, substituting Channel [11:8] for Channel [3:0}.

TABLE 275: DS3 FRAMER BLOCK - M12 LOOP-BACK REGISTER - 4 (ADDRESS = 0X0E2B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M12 Remote Loop Back Mode - DS1 Channel 15	M12 Remote Loop-Back Mode - DS1 Channel 14	M12 Remote Loop-Back Mode - DS1 Channel 13	M12 Remote Loop-Back Mode - DS1 Channel 12	M12 Loop-Back Request DS1 Channel 15	M12 Loop-Back Request DS1 Channel 14	M12 Loop-Back Request DS1 Channel 13	M12 Loop-Back Request DS1 Channel 12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] See Table 272 above for bit descriptions, substituting Channel [15:12] for Channel [3:0}.

TABLE 276: DS3 FRAMER BLOCK - M12 LOOP-BACK REGISTER - 5 (ADDRESS = 0X0E2C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M12 Remote Loop Back Mode - DS1 Channel 19	M12 Remote Loop-Back Mode - DS1 Channel 18	M12 Remote Loop-Back Mode - DS1 Channel 17	M12 Remote Loop-Back Mode - DS1 Channel 16	M12 Loop-Back Request - DS1 Channel 19	M12 Loop-Back Request - DS1 Channel 18	M12 Loop-Back Request - DS1 Channel 17	M12 Loop-Back Request - DS1 Channel 16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] See Table 272 above for bit descriptions, substituting Channel [19:16] for Channel [3:0}.

TABLE 277: DS3 FRAMER BLOCK - M12 LOOP-BACK REGISTER - 6 (ADDRESS = 0X0E2D)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M12 Remote Loop Back Mode - DS1 Channel 23	M12 Remote Loop-Back Mode - DS1 Channel 22	M12 Remote Loop-Back Mode - DS1 Channel 21	M12 Remote Loop-Back Mode - DS1 Channel 20	M12 Loop-Back Request - DS1 Channel 23	M12 Loop-Back Request - DS1 Channel 22	M12 Loop-Back Request - DS1 Channel 21	M12 Loop-Back Request - DS1 Channel 20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] See Table 272 above for bit descriptions, substituting Channel [23:20] for Channel [3:0}.

TABLE 278: DS3 FRAMER BLOCK - M12 LOOP-BACK REGISTER - 7 (ADDRESS = 0X0E2E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M12 Remote Loop Back Mode - DS1 Channel 27	M12 Remote Loop-Back Mode - DS1 Channel 26	M12 Remote Loop-Back Mode - DS1 Channel 25	M12 Remote Loop-Back Mode - DS1 Channel 24	M12 Loop-Back Request - DS1 Channel 27	M12 Loop-Back Request - DS1 Channel 26	M12 Loop-Back Request - DS1 Channel 25	M12 Loop-Back Request - DS1 Channel 24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] See Table 272 above for bit descriptions, substituting Channel [27:24] for Channel [3:0}.

TABLE 279: DS3 FRAMER BLOCK - TRANSMIT DS3 CONFIGURATION REGISTER (ADDRESS = 0X0E30)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force DS3 Tx FERF/RDI	Force X-Bits to 1	Transmit DS3 Idle Signal	Transmit AIS Indicator	Transmit LOS Indicator	Transmit FERF/RDI upon LOS	Transmit FERF/RDI upon LOF	Transmit FERF/RDI upon AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

BIT7 - Force Transmit DS3 FERF/RDI Indicator

This READ/WRITE bit-field is used to force the Transmit DS3 Framer block to transmit the FERF/RDI indicator to the remote terminal equipment by setting both of the X-bits (within each outbound DS3 frame) to 0.

- 0 - Does not force the Transmit DS3 Framer block to transmit the DS3 FERF/RDI indicator. In this case, the Transmit DS3 Framer block will set the X bits (within each outbound DS3 frame) to the appropriate value, depending upon receive conditions (as detected by the Receive DS3 Framer block).
- 1 - Forces the Transmit DS3 Framer block to transmit the DS3 FERF/RDI indicator. In this case, the Transmit DS3 Framer block will force the X bits (within each outbound DS3 frame) to 0.

NOTE: *For normal operation (e.g., where the Transmit DS3 Framer Block will automatically transmit the FERF/RDI indicator whenever the Receive DS3 Framer block declares either the LOS, AIS or LOF/OOF defect conditions) the user MUST set this bit-field to 0.*

BIT6 - Force X-Bits to 1

This READ/WRITE bit-field is used to force the Transmit DS3 Framer block to set the X-bits (within each outbound DS3 frame) to 1.

- 0 - Configures the Transmit DS3 Framer block to automatically set the X bits to the appropriate value, depending upon the receive conditions (as detected by the Receive DS3 Framer block).
- 1 - Configures the Transmit DS3 Framer block to force all of the X bits (within the outbound DS3 data-stream) to 1. In this configuration setting, the Transmit DS3 Framer block will set all X bits to 1 independent of whether the Receive DS3 Framer block is currently declaring any defect conditions.

NOTE: *For normal operation (e.g., where the Transmit DS3 Framer block will automatically transmit the FERF/RDI indicator whenever the Receive DS3 Framer block declares the LOS, AIS or LOF/OOF defect condition) the user MUST set this bit-field to 0.*

BIT 5 - Transmit DS3 Idle Signal

This READ/WRITE bit-field is used to force the Transmit DS3 Framer block to transmit the DS3 Idle Signal pattern to the remote terminal equipment, as described below.

- 0 - Configures the Transmit DS3 Framer block to transmit normal traffic to the remote terminal equipment.
- 1 - Configures the Transmit DS3 Framer block to transmit the DS3 Idle Pattern to the remote terminal equipment.

NOTES:

1. *This bit-field is ignored if Bits 3 (Transmit LOS Indicator) or 4 (Transmit AIS Indicator) are set to 1.*
2. *The exact pattern that the Transmit DS3 Framer block will transmit (whenever this bit-field is set to 1) depends upon the contents within Bits 3 through 0 (Transmit DS3 Idle Pattern[3:0]) within the DS3 Framer Block - Transmit DS3 Pattern Register (Address = 0x0E4C).*

BIT 4 - Transmit AIS Indicator

This READ/WRITE bit-field is used to force the Transmit DS3 Framer block to transmit the DS3 AIS indicator to the remote terminal equipment as described below.

- 0 - Configures the Transmit DS3 Framer block to transmit normal traffic (based upon T1/E1 data that has been multiplexed into a DS3 data-stream) to the remote terminal equipment.
- 1 - Configures the Transmit DS3 Framer block to transmit the DS3 AIS indicator to the remote terminal equipment.

NOTES:

1. *This bit-field is ignored if BIT 3 (Transmit LOS Indicator) is set to 1.*
2. *Whenever this bit-field is set to 1, the Transmit DS3 Framer block will either transmit a Framed repeating 1, 0, 1, 0, …. Pattern, or an Unframed All Ones pattern, depending upon the state of BIT7 (Transmit AIS - Unframed All Ones), within the Transmit DS3 Pattern Register (Address = 0x0E4C).*

BIT 3 - Transmit LOS Indicator

This READ/WRITE bit-field is used to force the Transmit DS3 Framer block to transmit the LOS pattern to the remote terminal equipment, as described below.

- 0 - Configures the Transmit DS3 Framer block to transmit normal traffic to the remote terminal equipment.
- 1 - Configures the Transmit DS3 Framer block to transmit the LOS pattern (e.g., either an All Zeros or All Ones pattern, depending upon user configuration).

NOTE: *Whenever this bit-field is set to 1, it will transmit either an All Zero pattern or an Unframed All Ones pattern, depending upon the state of BIT 4 (Transmit LOS Pattern - All Ones Pattern) within the Transmit DS3 Pattern Register (Address = 0x0E4C).*

BIT 2 - Transmit FERF/RDI upon LOS

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the Receive DS3 Framer block declares the LOS defect condition.

- 0 - Configures the Transmit DS3 Framer block to NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Receive DS3 Framer block declares the LOS defect condition.
- 1 - Configures the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Receive DS3 Framer block declares the LOS defect condition.

BIT 1 - Transmit FERF/RDI upon LOF/OOF:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the Receive DS3 Framer block declares the OOF defect condition, as described below.

- 0 - Configures the Transmit DS3 Framer block to NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Receive DS3 Framer block declares the OOF defect condition.
- 1 - Configures the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator whenever (and for the duration that) the Receive DS3 Framer block declares the OOF defect condition.

BIT 0 - Transmit FERF/RDI upon AIS

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the Receive DS3 Framer block declares the AIS defect condition, as described below.

- 0 - Configures the Transmit DS3 Framer block to NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Receive DS3 Framer block declares the AIS defect condition.
- 1 - Configures the Transmit DS3 Framer block to automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Receive DS3 Framer block declares the AIS defect condition.

TABLE 280: DS3 FRAMER BLOCK - TRANSMIT DS3 FEAC CONFIGURATION & STATUS REGISTER (ADDRESS = 0X0E31)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Transmit FEAC Interrupt Enable	Transmit FEAC Interrupt Status	Transmit FEAC Controller Enable	Transmit FEAC Message	Transmit FEAC Busy
R/O	R/O	R/O	R/W	RUR	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT [7:5] - Unused:

Please set these bits to [0, 0, 0] for normal operation.

BIT 4 - Transmit FEAC Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Transmit FEAC Interrupt. If the user enables this interrupt, then the Transmit FEAC Controller block (within the Transmit DS3 Framer block) will generate an interrupt, once it has completed its 10th transmission of a given FEAC Message to the remote terminal equipment.

- 0 - Disables the Transmit FEAC Interrupt
- 1 - Enables the Transmit FEAC Interrupt.

NOTE: *This bit-field is only active if the Transmit and Receive DS3 Framer blocks have been configured to support the C-bit Parity Framing format.*

BIT 3 - Transmit FEAC Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Transmit FEAC Controller block has generated the Transmit FEAC interrupt since the last read of this register.

- 0 - Indicates that the Transmit FEAC Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Transmit FEAC Interrupt has occurred since the last read of this register.

BIT 2 - Transmit FEAC Controller Enable:

This READ/WRITE bit-field is used to either enable or disable the Transmit FEAC Controller, within the Transmit DS3 Framer block.

- 0 - Disables the Transmit FEAC Controller block.
- 1 - Enables the Transmit FEAC Controller block

BIT 1 - Transmit FEAC Message:

- A 0 to 1 transition, within this bit-field configures the Transmit FEAC Controller block to begin its transmission of the FEAC Message (which consists of the FEAC Code, as specified within the Transmit DS3 FEAC Register.

NOTE: *The user is advised to perform a write operation that resets this bit-field back to 0, following execution of the command to transmit a FEAC Message.*

BIT 0 - Transmit FEAC Busy:

This READ-ONLY bit-field indicates whether or not the Transmit FEAC Controller block is currently busy transmitting a FEAC Message to the remote terminal.

- 0 - Indicates that the Transmit FEAC Controller is NOT currently busy transmitting a given FEAC Message.
- 1 - Indicates that the Transmit FEAC Controller is currently busy transmitting a given FEAC Message to the remote terminal equipment.

TABLE 281: DS3 FRAMER BLOCK - TRANSMIT DS3 FEAC REGISTER (ADDRESS = 0X0E32)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	TxFEAC_Code[5:0]						Unused
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/O
0	1	1	1	1	1	1	0

BIT 7 - Unused:

BIT [6:1] - TxFEAC_Code[5:0]:

These six (6) READ/WRITE bit-fields permit the user to specify the FEAC Code word that the Transmit FEAC Controller block (within the Transmit DS3 Framer block) should transmit to the remote terminal equipment.

Once the user enables the Transmit FEAC Controller and commands it to begin its transmission, the Transmit FEAC Controller will then (1) encapsulate this six-bit code word into a 16-bit structure, and (2) proceed to transmit this 16-bit structure 10 times, repeatedly, and then halt.

NOTE: *These bit-fields are ignored if the user does not enable and use the Transmit FEAC Controller.*

BIT 0 - Unused:

TABLE 282: DS3 FRAMER BLOCK - TRANSMIT DS3 LAPD CONFIGURATION REGISTER (ADDRESS = 0X0E33)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit LAPD Any	Unused			Auto Retransmit	Reserved	Transmit LAPD Message Length	Transmit LAPD Controller Enable
R/W	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT 7 - Transmit LAPD Any:

This READ/WRITE bit-field is used to configure the Transmit LAPD Controller block to transmit any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Transmit LAPD Controller block will be capable of transmitting any kind of HDLC frame (with any value of header bytes). The only restriction is that the size of the HDLC frame must not exceed 82 bytes.

- 0 - Does not invoke this Any Kind of HDLC Message feature. In this case, the Transmit LAPD Controller block will only transmit HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.
- 1 - Invokes this Any Kind of HDLC Message feature. In this case, the Transmit LAPD Controller block will be able to transmit HDLC Messages that contains any header byte values.

NOTE: *If the Any Kind of HDLC Message feature is invoked, then the size of the information payload (in terms of bytes) within the Transmit LAPD byte Count Register Address = 0x0E83) must be indicated.*

BIT [6:4] - Unused:

BIT 3 - Auto Retransmit

This READ/WRITE bit-field is used to configure the Transmit LAPD Controller block to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller block to transmit a given PMDL Message, then the Transmit LAPD Controller block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one second intervals.

- 0 - Disables the Auto-Retransmit Feature:

In this case, the Transmit LAPD Controller block will only transmit a given PMDL Message once. Afterwards the Transmit LAPD Controller block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission.

- 1 - Enables the Auto-Retransmit Features

In this case, the Transmit LAPD Controller block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message buffer) repeatedly at one-second interval.s

NOTE: *This bit-field is ignored if the Transmit LAPD Controller block is disabled.*

BIT 2 - Reserved:

BIT 1 - Transmit LAPD Message Length:

This READ/WRITE bit-field is used to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below.

- 0 - Configures the Transmit LAPD Controller block to transmit a LAPD/PMDL Message that has a payload data size of 76 bytes.
- 1 - Configures the Transmit LAPD Controller block to transmit a LAPD/PMDL Message that has a payload data size of 82 bytes.

BIT 0 - Transmit LAPD Controller Enable:

This READ/WRITE bit-field is used to enable the Transmit LAPD Controller block within the chip. Once the user enables the Transmit LAPD Controller block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the DL within the outbound DS3 data-stream. The Transmit LAPD Controller block will continue to do this until the user commands the Transmit LAPD Controller block to transmit a PMDL Message.

- 0 - Disables the Transmit LAPD Controller block.

- 1 - Enables the Transmit LAPD Controller block.

TABLE 283: DS3 FRAMER BLOCK - TRANSMIT DS3 LAPD STATUS/INTERRUPT REGISTER (ADDRESS = 0X0E34)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit LAPD Message Start	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT [7:4] - Unused:

BIT 3 - Transmit LAPD Message Start:

- A 0 to 1 transition within this bit-field commands the Transmit LAPD Controller block to begin the following activities.
  - Reading out the contents of the Transmit LAPD Message buffer.
  - Zero-stuffing of this data
  - FCS Calculation and Insertion
  - Fragmentation of this composite PMDL Message, and insertion into the DL bit-fields, within each outbound DS3 frame.

BIT 2 - Transmit LAPD Controller Busy:

This READ-ONLY bit-field indicates whether or not the Transmit LAPD Controller block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message.

- 0 - Indicates that the Transmit LAPD Controller block is NOT currently busy transmitting a PMDL message.
- 1 - Indicates that the Transmit LAPD Controller block is currently busy transmitting a PMDL message.

BIT 1 - Transmit LAPD Message Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Transmit LAPD Message Interrupt. If the user enables this interrupt, then the Transmit DS3 Framer block will generate an interrupt anytime the Transmit LAPD Controller block has completed its transmission of a given LAPD/PMDL Message to the remote terminal.

- 0 - Disables the Transmit LAPD Message Interrupt.
- 1 - Enables the Transmit LAPD Message Interrupt.

BIT 0 - Transmit LAPD Message Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Transmit LAPD Message Interrupt has occurred since the last read of this register.

- 0 - Indicates that the Transmit LAPD Message Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the Transmit LAPD Message Interrupt has occurred since the last read of this register.

TABLE 284: DS3 FRAMER BLOCK - TRANSMIT DS3 M-BIT MASK REGISTER (ADDRESS = 0X0E35)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFEBEDat[2:0]			FEBE Register Enable	Transmit P-Bit Error	TxM_Bit_Mask[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 5 - TxFEBEDat[2:0]

These READ/WRITE bit-fields, along with BIT 4 (FEBE Register Enable) are used to configure the Transmit DS3 Framer block to transmit the user-specified FEBE values (to the remote terminal equipment) based upon the contents of these bit-fields.

If the user sets the FEBE Register Enable bit-field to '1, then the Transmit DS3 Framer block will wsrite the contents of these bit-fields into the FEBE bit-fields within each outbound DS3 frame.

If the user sets the FEBE Register Enable bit-field to 0, then these register bits will be ignored.

BIT 4 - FEBE Register Enable

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit user-specified FEBE values (to the remote terminal equipment) per register setting via the TxFEBEDat[2:0] bit-fields. This option is used to exercise software control over the outbound FEBE values, within the outbound DS3 data-stream.

- 0 - Configures the Transmit DS3 Framer block to set the FEBE bit-fields (within each outbound DS3 frame) to the appropriate values based upon receive conditions, as determined by the Receive DS3 Framer block.
- 1 - Configures the Transmit DS3 Framer block to set the write the contents of the TxFEBEDat[2:0] bit-fields into the FEBE bit-positions within each outbound DS3 frame.

BIT 3 - Transmit P-Bit Error

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with erred P-bits as indicated below.

- 0 - Configures the Transmit DS3 Framer block to generate and transmit DS3 frames (with correct P-bit values) to the remote terminal equipment.
- 1 - Configures the Transmit DS3 Framer block to generate and transmit DS3 frames (with erred P-bit values) to the remote terminal equipment.

BIT[2:0] - TxM_Bit_Mask[2:0]

These READ/WRITE bit-fields are used to configure the Transmit DS3 Framer block to transmit DS3 frames with erred M-bits.

These three (3) bit-fields corresponding to each of the three M-bits, within each outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of these bit-fields and the values of the three M-bits. The results of this calculation will be written back into the M-bit position within each outbound DS3 frame.

NOTE: *The user should set these bit-fields to 0, 0, 0 for normal (e.g., un-erred) operation.*

TABLE 285: DS3 FRAMER BLOCK - TRANSMIT DS3 F-BIT MASK REGISTERS # 1 (ADDRESS = 0X0E36)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				F-Bit Mask[27]	F-Bit Mask[26]	F-Bit Mask[25]	F-Bit Mask[24]
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT[7:4] - Unused

BIT 3 - F-Bit Mask[27]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 28th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 28th F-bit. The results of this calculation will be written back into the 28th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 2 - F-Bit Mask[26]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 27th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 27th F-bit. The results of this calculation will be written back into the 27th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 1 - F-Bit Mask[25]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 26th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 26th F-bit. The results of this calculation will be written back into the 26th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 0 - F-Bit Mask[24]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 25th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 25th F-bit. The results of this calculation will be written back into the 25th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

TABLE 286: DS3 FRAMER BLOCK - TRANSMIT DS3 F-BIT MASK REGISTER # 2 (ADDRESS = 0X0E37)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F-Bit Mask[23]	F-Bit Mask[22]	F-Bit Mask[21]	F-Bit Mask[20]	F-Bit Mask[19]	F-Bit Mask[18]	F-Bit Mask[17]	F-Bit Mask[16]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - F-Bit Mask[23]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 24th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 24th F-bit. The results of this calculation will be written back into the 24th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT6 - F-Bit Mask[22]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 23rd F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 23rd F-bit. The results of this calculation will be written back into the 23rd F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 5 - F-Bit Mask[21]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 22nd F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 22nd F-bit. The results of this calculation will be written back into the 22nd F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 4 - F-Bit Mask[20]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 21st F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 21st F-bit. The results of this calculation will be written back into the 21st F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 3 - F-Bit Mask[19]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 20th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 20th F-bit. The results of this calculation will be written back into the 20th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 2 - F-Bit Mask[18]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 19th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 19th F-bit. The results of this calculation will be written back into the 19th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 1 - F-Bit Mask[17]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 18th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 18th F-bit. The results of this calculation will be written back into the 18th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

BIT 0 - F-Bit Mask[16]:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit DS3 frames with a single/particular erred F-bit.

This particular F-bit corresponds with the 17th F-bit within a given outbound DS3 frame. The Transmit DS3 Framer block will perform an XOR operation with the contents of this bit-field and the value of the 17th F-bit. The results of this calculation will be written back into the 17th F-bit position, within each outbound DS3 frame.

NOTE: *The user should set this bit-field to 0 for normal (e.g., un-erred) operation.*

TABLE 287: DS3 FRAMER BLOCK - TRANSMIT DS3 F-BIT MASK REGISTER # 3 (ADDRESS = 0X0E38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F-Bit Mask[15]	F-Bit Mask[14]	F-Bit Mask[13]	F-Bit Mask[12]	F-Bit Mask[11]	F-Bit Mask[10]	F-Bit Mask[9]	F-Bit Mask[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 286 above, for bit descriptions, substituting Mask [15:8] for mask[23:16]

TABLE 288: DS3 FRAMER BLOCK - TRANSMIT DS3 F-BIT MASK REGISTER # 4 (ADDRESS = 0X0E39)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F-Bit Mask[7]	F-Bit Mask[6]	F-Bit Mask[5]	F-Bit Mask[4]	F-Bit Mask[3]	F-Bit Mask[2]	F-Bit Mask[1]	F-Bit Mask[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 286 above, for bit descriptions, substituting Mask [7:0] for mask[23:16]

TABLE 289: DS3 FRAMER BLOCK - M12 DS2 # 1 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X0E3A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	One and Only	DS2 M-Sync	DS2 F-Sync	DS2 LOF - F Bits/ G.747 FAS Bit Error Count	DS2 LOF - M Bits	DS2 LOF - M Bits Disable	DS2 Reframe
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Unused:

BIT 6 - One and Only:

This READ/WRITE bit-field is used to select the F-bit acquisition criteria that the M12 DeMUX block will use, whenever it is operating in the F-Bit Search state, as described below.

- 0 - Configures the M12 De-MUX block to move onto the M-Bit Search state, whenever it has properly located 8 (or 16) consecutive F-bits (as configured in Bit 4 of this register).
- 1 - Configures the M12 De-MUX block to move onto the M-Bit Search state, whenever it has (1) properly located 8 (or 16) consecutive F-bits and (2) when it has located and identified only one viable F-Bit Alignment candidate.

NOTE: *If the user sets this bit-field to 1, then the M12 De-MUX block will NOT transition into the M-Bit Search state as long as at least two viable candidate sets of bits appears to function as the F-bits.*

BIT 5 - DS2 M-Sync:

This READ/WRITE bit-field is used to select the M-Bit Acquisition criteria whenever the M12 De-MUX block is operating in the M-Bit Search state.

- 0 - Configures the M12 De-MUX block to declare the In-Frame state, when it has properly located 4 consecutive M-bits (while detecting no F-bit errors).
- 1 - Configures the M12 De-MUX block to declare the In-Frame state, when it has properly located 8 consecutive M-bits (while detecting no F-bit errors).

BIT 4 - DS2 F-Sync:

This READ/WRITE bit-field is used to select the F-Bit Acquisition criteria whenever the M12 De-MX block is operating in the F-Bit Search state.

- 0 - Configures the M12 De-MUX block to move onto the M-Bit Search state, when it has properly located 8 consecutive F-bits.
- 1 - Configures the M12 De-MUX block to move onto the M-Bit Search state, when it has properly located 16 consecutive F-bits.

BIT 3 - DS2 LOF - F Bits/G.747 FAS Bit Error Count

The exact function of this bit-field depends upon whether the M12 MUX/De-MUX block has been configured to operate in the DS2 or in the G.747 Mode, as described below.

If M12 MUX/M12 De-MUX # 1 is configured to operate in the DS2 Mode:

This READ/WRITE bit-field is used to select the F-Bit LOF (Loss of Frame) Defect criteria for the M12 De-MUX associated with DS2 Channel 1.

- 0 - Configures the M12 De-MUX block to declare the DS2 LOF defect condition whenever the M12 De-MUX block detects two (2) F-bit errors within the four (4) most recently received F-bits within the incoming DS2 data-stream.
- 1 - Configures the M12 De-MUX block to declare the DS2 LOF defect condition whenever the M12 De-MUX defect two (2) F-bit errors within the five (5) most recently received F-bits within the incoming DS2 data-stream.

If M12 MUX/M12 De-MUX # 1 is configured to operate in the G.747 Mode:

This READ/WRITE bit-field is used to specify how the M12 De-MUX increments G.747 Framing Alignment Signal (FAS) errors.

The user can configure the M12 De-MUX to increment the PMON DS2 # 1 Framing Bit Error Count Register on either

a per-bit or per-frame basis, as described below.

Per-Bit Basis:

The M12 De-MUX will increment the DS3 Framer Block - PMON DS2 # 1 Framing Bit Error Count Register once for each bit-error that it detects within the FAS bit-fields of the incoming G.747 data-stream.

Per-Frame Basis:

The M12 De-MUX will increment the DS3 Framer Block - PMON DS2 # 1 Framing Bit Error Count Register once for each time it detects at least one bit-error within the FAS bit-fields of a given incoming G.747 frame.

- 0 - Configures the M12 De-MUX to increment the DS3 Framer Block - PMON DS2 # 1 Framing Bit Error Count Register on a per-bit basis.
- 1 - Configures the M12 De-MUX block to increment the DS3 Framer Block - PMON DS2 # 1 Framing Bit Error Count Register on a per-frame basis.

BIT 2 - DS2 LOF - M Bits

This READ/WRITE bit-field is used to select the M-Bit LOF (Loss of Frame) Defect criteria for the M12 De-MUX block associated with DS2 Channel 1.

- 0 - Configures the M12 De-MUX block to declare the DS2 LOF defect condition whenever the M12 De-MUX block detects M-bit errors within three (3) out of the four (4) most recently received DS2 M-frames.
- 1 - Configures the M12 De-MUX block to declares the DS2 LOF defect condition whenever the M12 De-MUX block detects M-bit errors within two (2) out of the four (4) most recently received DS2 M-frames.

BIT 1 - DS2 LOF - M Bits Disable

This READ/WRITE bit-field is used to configure the M12 De-MUX block to not use M-bit errors as a reason/criteria for declaring the DS2 LOF defect condition.

- 0 - Configures the M12 De-MUX block to declare the DS2 LOF defect condition, based upon the number of M-bit errors (as selected in Bit 2 within this register).
- 1 - Configures the M12 De-MUX block to NOT declare the DS2 LOF defect condition, based upon the occurrences of any M-bit errors.

BIT 0 - DS2 Reframe:

- A 0 to 1 transition, within this bit-field commands the M12 De-MUX block to exit the Frame Maintenance mode, and go back and enter the Frame Acquisition Mode.

NOTE: *The user should go back and set this bit-field to 0 following execution of the Reframe Command.*

TABLE 290: DS3 FRAMER BLOCK - M12 DS2 # 2 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X0E3B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	One and Only	DS2 M-Sync	DS2 F-Sync	DS2 LOF - F Bits/ G.747 FAS Bit Error Count	DS2 LOF - M Bits	DS2 LOF - M Bits Disable	DS2 Reframe
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit [7:0] - See bit description for Table 289, above.

TABLE 291: DS3 FRAMER BLOCK - M12 DS2 # 3 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X0E3C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	One and Only	DS2 M-Sync	DS2 F-Sync	DS2 LOF - F Bits/ G.747 FAS Bit Error Count	DS2 LOF - M Bits	DS2 LOF - M Bits Disable	DS2 Reframe
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit [7:0] - See bit description for Table 289, above.

TABLE 292: DS3 FRAMER BLOCK - M12 DS2 # 4 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X0E3D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	One and Only	DS2 M-Sync	DS2 F-Sync	DS2 LOF - F Bits/ G.747 FAS Bit Error Count	DS2 LOF - M Bits	DS2 LOF - M Bits Disable	DS2 Reframe
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit [7:0] - See bit description for Table 289, above.

TABLE 293: DS3 FRAMER BLOCK - M12 DS2 # 5 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X0E3E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	One and Only	DS2 M-Sync	DS2 F-Sync	DS2 LOF - F Bits/ G.747 FAS Bit Error Count	DS2 LOF - M Bits	DS2 LOF - M Bits Disable	DS2 Reframe
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit [7:0] - See bit description for Table 289, above.

TABLE 294: DS3 FRAMER BLOCK - M12 DS2 # 6 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X0E3F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	One and Only	DS2 M-Sync	DS2 F-Sync	DS2 LOF - F Bits/ G.747 FAS Bit Error Count	DS2 LOF - M Bits	DS2 LOF - M Bits Disable	DS2 Reframe
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit [7:0] - See bit description for Table 289, above.

TABLE 295: DS3 FRAMER BLOCK - M12 DS2 # 7 FRAMER CONFIGURATION REGISTER (ADDRESS = 0X0E40)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	One and Only	DS2 M-Sync	DS2 F-Sync	DS2 LOF - F Bits/ G.747 FAS Bit Error Count	DS2 LOF - M Bits	DS2 LOF - M Bits Disable	DS2 Reframe
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit [7:0] - See bit description for Table 289, above.

TABLE 296: DS3 FRAMER BLOCK - TRANSMIT DS3 PATTERN REGISTER (ADDRESS = 0X0E4C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit AIS - Unframed All Ones	Transmit AIS - C bits not forced to 0	Transmit AIS - Ignore Overhead Data from TxDS3OH Port	Transmit LOS Pattern - All Ones Pattern	DS3 Idle Pattern[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT7 - Transmit AIS - Unframed All Ones:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit either of the following patterns, anytime it is configured to transmit the AIS indicator.

- A Framed, repeating 1, 0, 1, 0… pattern (per Bellcore GR-499-CORE) or
- An Unframed All Ones Pattern.

▶ 0 - Configures the Transmit DS3 Framer block to transmit the Framed, Repeating 1, 0, 1, 0,… Pattern, whenever it is configured to transmit the AIS Indicator.

▶ 1 - Configures the Transmit DS3 Framer block to transmit an Unframed, All Ones Pattern, whenever it is configured to transmit the AIS indicator.

BIT6 - Transmit AIS - C Bits NOT forced to 0

This READ/WRITE bit-field (along with the Transmit AIS - Unframed All Ones bit-field) is used to define the type of AIS data-stream that the Transmit DS3 Framer block will transmit, as described below.

- 0 - Configures the Transmit DS3 Framer block to force all of the C bits to 0 when it is configured to transmit a Framed AIS signal.
- 1 - Configures the Transmit DS3 Framer block to NOT force all of the C bits to 0 when it is configured to transmit a Framed AIS signal. In this case, the C bits can be used to transport FEAC or PMDL Messages.

NOTE: *This bit-field is ignored if the Transmit DS3 Framer block has been configured to transmit an Unframed - All Ones type of AIS signal.*

BIT 5 - Transmit AIS - Ignore Overhead Data from TxDS3OH Port

This READ/WRITE bit-field permits the Transmit DS3 Framer block to either accept or ignore externally supplied DS3 Overhead data, whenever it (the Transmit DS3 Framer block) is transmitting the AIS indicator.

If this feature is used, then (for the duration that the Transmit DS3 Framer block is commanded to transmit the DS3 AIS indicator) the Transmit DS3 Framer block will NOT allow the users to externally insert their DS3 OH bits within the outbound DS3 data-stream, even if the TxOH Source bit-field is set to 1 and if the corresponding F-Bit Mask bit-field is set to 0.

Conversely, if the user does NOT use this feature, then the Transmit DS3 Framer block will allow the users to externally insert theirr own DS3 OH bits (within the outbound DS3 data-stream) even when the Transmit DS3 Framer block is transmitting the DS3 AIS indicator to the remote terminal equipment.

- 0 - Does NOT invoke the Ignore TxDS3OH Port During AIS Feature
- 1 - Invokes the Ignore the TxDS3OH Port During AIS feature.

BIT 4 - Transmit LOS Pattern Select:

This READ/WRITE bit-field is used to configure the Transmit DS3 Framer block to transmit either an All Zeros or an All Ones pattern, anytime it is configured to transmit the LOS Pattern to the remote terminal equipment, as described below.

- 0 - Configures the Transmit DS3 Framer block to transmit an All Zeros pattern whenever it is configured to transmit the LOS pattern.
- 1 - Configures the Transmit DS3 Framer block to transmit an All Ones pattern whenever it is configured to transmit the LOS pattern.

BIT[3:0] - Transmit DS3 Idle Pattern[3:0]

These READ/WRITE bit-fields are used to specify the type of framed, repetitive four-bit pattern that the Transmit DES3 Framer block should generate and transmit, whenever it is configured to transmit the DS3 Idle Pattern.

NOTE: *Setting these bit-fields to [1, 1, 0, 0] configures the Transmit DS3 Framer block to transmit the standard Framed, repeating 1, 1, 0, 0, … pattern (per Bellcore GR-499-CORE) requirements.*

TABLE 297: DS3 FRAMER BLOCK - AUTO T1/E1 AIS UPON DS3 DEFECT CONDITION REGISTER (ADDRESS = 0X0E4D)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Auto DS1/E1AIS upon DS3 LOS Defect	Unused	Auto DS1/E1 AIS upon DS3 OOF Defect	Unused	Auto DS1/E1 AIS upon DS3 AIS Defect
R/O	R/O	R/O	R/W	R/O	R/W	R/O	R/W
0	0	0	0	0	0	0	0

Bits 7 - 5 - Unused

BIT 4 - Auto DS1/E1 AIS upon DS3 LOS Defect

This READ/WRITE bit-field is used to configure all of the Egress Direction Transmit DS1/E1 Framer blocks (within the XRT86SH328) to automatically transmit the DS1/E1 AIS indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive DS3 Framer block declares the LOS defect condition.

- 0 - Does not configure all Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicators via the downstream DS1/E1 signals, anytime the Receive DS3 Framer block declares the LOS defect

condition.

- 1 - Configures all Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicators via the downstream DS1/E1 signals anytime the Receive DS3 Framer block declares the LOS defect condition.

NOTE: This bit-field is only active if the XRT86SH328 has been configured to operate in either the M13 MUX or the M13 MUX which is Asynchronously mapped into STS-1/STS-3 Mode.

BIT 3 - Unused

BIT 2 - Auto DS1/E1 AIS upon DS3 OOF Defect

This READ/WRITE bit-field is used to configure all of the Egress Direction Transmit DS1/E1 Framer blocks (within the XRT86SH328) to automatically transmit the DS1/E1 AIS indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive DS3 Framer block declares the LOF/OOF defect condition.

- 0 - Does not configure all Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicators via the downstream DS1/E1 signals, anytime the Receive DS3 Framer block declares the LOF/OOF defect condition.
- 1 - Configures all Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicators via the downstream DS1/E1 signals anytime the Receive DS3 Framer block declares the LOF/OOF defect condition.

NOTE: This bit-field is only active if the XRT86SH328 has been configured to operate in either the M13 MUX or the M13 MUX which is Asynchronously mapped into STS-1/STS-3 Mode.

BIT 1 - Unused

BIT 0 - Auto DS1/E1 AIS upon DS3 AIS Defect

This READ/WRITE bit-field is used to configure all of the Egress Direction Transmit DS1/E1 Framer blocks (within the XRT86SH328) to automatically transmit the DS1/E1 AIS indicator via the downstream DS1/E1 signals, anytime (and for the duration that) the Receive DS3 Framer block declares the AIS defect condition.

- 0 - Does not configure all Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicators via the downstream DS1/E1 signals, anytime the Receive DS3 Framer block declares the AIS defect condition.
- 1 - Configures all Egress Direction Transmit DS1/E1 Framer blocks to automatically transmit the DS1/E1 AIS indicators via the downstream DS1/E1 signals anytime the Receive DS3 Framer block declares the AIS defect condition.

NOTE: This bit-field is only active if the XRT86SH328 has been configured to operate in either the M13 MUX or the M13 MUX which is Asynchronously mapped into STS-1/STS-3 Mode.

TABLE 298: DS3 FRAMER BLOCK - PMON EXCESSIVE ZERO (EXZ) EVENT COUNT REGISTER - MSB (ADDRESS = 0X0E4E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON EXZ Event Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON EXZ_Event_Count[15:8]:

These RESET-upon-READ bits, along with that within the PMON Excessive Zero Count Register - LSB combine to reflect the cumulative number of instances in which the Receive DS3 Framer block has detected a string of three or more consecutive zeros within the incoming DS3 data-stream, since the last read of this register.

This register contains the Most Significant Byte of this 16-bit expression.

TABLE 299: DS3 FRAMER BLOCK - PMON EXCESSIVE ZERO (EXZ) EVENT COUNT REGISTER - LSB (ADDRESS = 0X0E4F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON EXZ Event Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON EXZ_Event_Count[7:0]:

These RESET-upon-READ bits, along with that within the PMON Excessive Zero Count Register -MSB combine to reflect the cumulative number of instances in which the Receive DS3 Framer block has detected a string of three or more consecutive zeros within the incoming DS3 data-stream, since the last read of this register.

This register contains the Least Significant Byte of this 16-bit expression.

TABLE 300: DS3 FRAMER BLOCK - PMON LINE CODE VIOLATION (LCV) EVENT COUNT REGISTER - MSB (ADDRESS = 0X0E50)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON LCV Event Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON LCV_Event_Count[15:8]:

These RESET-upon-READ bits along with that within the PMON Line Code Violation Count - LSB register combine to reflect the cumulative number of Line Code Violation events that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, since the last read of this register.

This register contains the Most Significant byte of this 16-bit expression.

TABLE 301: DS3 FRAMER BLOCK - PMON LINE CODE VIOLATION (LCV) EVENT COUNT REGISTER - LSB (ADDRESS = 0X0E51)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON LCV Event Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON LCV_Event_Count[7:0]:

These RESET-upon-READ bits along with that within the PMON Line Code Violation Count - MSB register combine to reflect the cumulative number of Line Code Violation events that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, since the last read of this register.

This register contains the Least Significant byte of this 16-bit expression.

TABLE 302: DS3 FRAMER BLOCK - PMON FRAMING BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X0E52)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Framing_Bit_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0]: PMON Framing Bit ErrorCount[15:8]:

These RESET-upon-READ bits, along with that within the DS3 Framer Block - PMON Framing Bit Error Count Register - LSB combine to reflect the cumulative number of Framing bit errors that the Receive DS3 Framer block has detected since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

NOTE: *The Receive DS3 Framer block will increment this register each time that it detects F or M bit errors within the incoming DS3 data-stream.*

TABLE 303: DS3 FRAMER BLOCK - PMON FRAMING BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X0E53)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Framing_Bit_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0]: PMON Framing Bit ErrorCount[7:0]:

These RESET-upon-READ bits, along with that within the DS3 Framer Block - PMON Framing Bit Error Count Register - MSB combine to reflect the cumulative number of Framing bit errors that the Receive DS3 Framer block has detected since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

NOTE: *The Receive DS3 Framer block will increment this register each time that it detects F or M bit errors within the incoming DS3 data-stream.*

TABLE 304: DS3 FRAMER BLOCK - PMON P-BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X0E54)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_P_Bit _Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0]: PMON P-Bit Error Count[15:8]:

These RESET-upon-READ bits, along with that within the DS3 Framer Block - PMON P-bit Error Count Register - LSB combine to reflect the cumulative number of P-bit errors that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

TABLE 305: DS3 FRAMER BLOCK - PMON P-BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X0E55)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_P_Bit_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON P-Bit Error Count[7:0]:

These RESET-upon-READ bits, along with that within the DS3 Framer Block - PMON P-bit Error Count Register - MSB combine to reflect the cumulative number of P-bit errors that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

TABLE 306: DS3 FRAMER BLOCK - PMON FEBE EVENT COUNT REGISTER - MSB (ADDRESS = 0X0E56)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_FEBE_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON FEBE Event Count[15:8]:

These RESET-upon-READ bits, along with that within the PMON FEBE Event Count Register - LSB combine to reflect the cumulative number of FEBE/REI events that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, since the last read of this register. This register contains the Most Significant byte of this 16-expression.

TABLE 307: DS3 FRAMER BLOCK - PMON FEBE EVENT COUNT REGISTER - LSB (ADDRESS = 0X0E57)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_FEBE_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON FEBE Event Count[7:0]:

These RESET-upon-READ bits, along with that within the PMON FEBE Event Count Register - MSB combine to reflect the cumulative number of FEBE/REI events that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, since the last read of this register. This register contains the Least Significant byte of this 16-expression.

TABLE 308: DS3 FRAMER BLOCK - CP-BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X0E58)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_CP_Bit_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON CP-Bit Error Count[15:8]:

These RESET-upon-READ bits, along with that within the DS3 Framer Block - PMON CP-Bit Error Count Register - LSB combine to reflect the cumulative number of CP bit errors that the Receive DS3 Framer block has detected since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

NOTE: *These register bits are not active if the Transmit and Receive DS3 Framer blocks have NOT been configured to support the DS3 C-bit Parity Framing format.*

TABLE 309: DS3 FRAMER BLOCK - CP-BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X0E59)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_CP_Bit_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON CP-Bit Error Count[7:0]:

These RESET-upon-READ bits, along with that within the DS3 Framer Block - PMON CP-Bit Error Count Register - MSB combine to reflect the cumulative number of CP bit errors that the Receive DS3 Framer block has detected since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

NOTE: These register bits are not active if the Transmit and Receive DS3 Framer blocks have NOT been configured to support the DS3 C-bit Parity Framing format.

TABLE 310: DS3 FRAMER BLOCK - PMON DS2 # 1 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X0E5A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_DS2 # 1 Framing Bit Error Count[7:0]/G.747 FAS Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON DS2 # 1 - Framing Bit Error Count[7:0]/G.747 FAS Error Count[7:0]:

The function of this bit-field depends upon whether M12 MUX/De-MUX # 1 has been configured to operate in the DS2 or in the G.747 Mode.

If M12 MUX/De-MUX # 1 has been configured to operate in the DS2 Mode:

These RESET-upon-READ bit-fields reflects the cumulative number of F and M bit errors that the M12 De-MUX Block (associated with DS2 Channel 1) has detected since the last read of this register.

If M21 MUX/De-MUX # 1 has been configured to operate in the G.747 Mode:

This RESET-upon-READ bit-fields reflects the cumulative number of FAS errors that the M12 De-MUX block (associated with DS2 Channel 1) has detected since the last read of this register.

TABLE 311: DS3 FRAMER BLOCK - PMON DS2 # 2 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X0E5B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_DS2 # 2 Framing Bit Error Count[7:0]/G.747 FAS Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] See Figure 310 above, for bit descriptions

TABLE 312: DS3 FRAMER BLOCK - PMON DS2 # 3 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X0E5C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_DS2 # 3 Framing Bit Error Count[7:0]/G.747 FAS Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] See Figure 310 above, for bit descriptions

TABLE 313: DS3 FRAMER BLOCK - PMON DS2 # 4 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X0E5D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_DS2 # 4 Framing Bit Error Count[7:0]/G.747 FAS Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] See Figure 310 above for bit descriptions

TABLE 314: DS3 FRAMER BLOCK - PMON DS2 # 5 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X0E5E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_DS2 # 5 Framing Bit Error Count[7:0]/G.747 FAS Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] See Figure 310 above, for bit descriptions

TABLE 315: DS3 FRAMER BLOCK - PMON DS2 # 6 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X0E5F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_DS2 # 6 Framing Bit Error Count[7:0]/G.747 FAS Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] See Figure 310 above, for bit descriptions

TABLE 316: DS3 FRAMER BLOCK - PMON DS2 # 7 FRAMING BIT ERROR COUNT REGISTER (ADDRESS = 0X0E60)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_DS2 # 7 Framing Bit Error Count[7:0]/G.747 FAS Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] See Figure 310 above for bit descriptions

TABLE 317: DS3 FRAMER BLOCK - PMON G.747 # 1 PARITY BIT ERROR COUNT REGISTER (ADDRESS = 0X0E61)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_G.747 # 1 - Parity Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PMON G.747 # 1 - Parity Error Count[7:0]:

This RESET-upon-READ bit-field reflects the cumulative number of P-bit errors that the M12 De-MUX Block (associated with G.747 Channel # 1) has detected since the last read of this register.

NOTE: *These bit-fields are only active if M12 MUX/De-MUX # 1 has been configured to operate in the G.747 Mode.*

TABLE 318: DS3 FRAMER BLOCK - PMON G.747 # 2 PARITY BIT ERROR COUNT REGISTER (ADDRESS = 0X0E62)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_G.747 # 2 - Parity Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 317 above, for bit descrptions, substituting Channel # 2 for Channel # 1.

TABLE 319: DS3 FRAMER BLOCK - PMON G.747 # 3 PARITY BIT ERROR COUNT REGISTER (ADDRESS = 0X0E63)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_G.747 # 3 - Parity Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 317 above, for bit descrptions, substituting Channel # 3 for Channel # 1.

TABLE 320: DS3 FRAMER BLOCK - PMON G.747 # 4 PARITY BIT ERROR COUNT REGISTER (ADDRESS = 0X0E64)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_G.747 # 4 - Parity Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 317 above, for bit descrptions, substituting Channel # 4 for Channel # 1.

TABLE 321: DS3 FRAMER BLOCK - PMON G.747 # 5 PARITY BIT ERROR COUNT REGISTER (ADDRESS = 0X0E65)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_G.747 # 5 - Parity Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 317 above, for bit descrptions, substituting Channel # 5 for Channel # 1.

TABLE 322: DS3 FRAMER BLOCK - PMON G.747 # 6 PARITY BIT ERROR COUNT REGISTER (ADDRESS = 0X0E66)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_G.747 # 6 - Parity Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 317 above, for bit descrptions, substituting Channel # 6 for Channel # 1.

TABLE 323: DS3 FRAMER BLOCK - PMON G.747 # 7 PARITY BIT ERROR COUNT REGISTER (ADDRESS = 0X0E67)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_G.747 # 7 - Parity Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 317 above, for bit descrptions, substituting Channel # 7 for Channel # 1.

TABLE 324: DS3 FRAMER BLOCK - PRBS BIT ERROR COUNT REGISTER - MSB (ADDRESS = 0X0E68)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PRBS Error Count - Upper Byte:

These RESET-upon-READ bits, along with that within the DS3 Framer Block - PRBS Bit Error Count Register - LSB combine to reflect the cumulative number of PRBS bit errors that the PRBS Receiver (within the Receive DS3 Framer block) has detected since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

NOTE: *This register is only active of the PRBS Receiver (within the Receive DS3 Framer block) has been enabled.*

TABLE 325: DS3 FRAMER BLOCK - PRBS BIT ERROR COUNT REGISTER - LSB (ADDRESS = 0X0E69)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - PRBS Error Count - Lower Byte:

These RESET-upon-READ bits, along with that within the DS3 Framer Block - PRBS Bit Error Count Register - MSB combine to reflect the cumulative number of PRBS bit errors that the PRBS Receiver (within the Receive DS3 Framer block) has detected since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

NOTE: *This register is only active of the PRBS Receiver (within the Receive DS3 Framer block) has been enabled.*

TABLE 326: DS3 FRAMER BLOCK - ONE SECOND ERROR STATUS REGISTER (ADDRESS = 0X0E6D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Erred Second	Severely Erred Second
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:2] - Unused:

BIT 1 - Erred Second:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block has declared the last one-second accumulation period as an Erred Second.

The Receive DS3 Framer block will declare an Erred Second if it detects any of the following events, within a given one-second period.

- P-Bit Errors
- CP-Bit Errors
- Framing Bit (F or M) Errors

▶ 0 - Indicates that the Receive DS3 Framer block has NOT declared the last one-second accumulation period as being an Erred Second.

- 1 - Indicates that the Receive DS3 Framer block has declared the last one-second accumulation period as being an Erred Second.

BIT 0 - Severely Erred Second:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block has declared the last one-second accumulation period as being a Severely Erred Second.

The Receive DS3 Framer block will declares a given one-second period as being a severely erred second if it determines that the BER (Bit Error Rate) during this one-second accumulation period is greater than 10-3 errors/second.

- 0 - Indicates that the Receive DS3 Framer block has NOT declared the last one-second accumulation period as being a severely-erred second.
- 1 - Indicates that the Receive DS3 Framer block has declared the last one-second accumulation period as being a severely-erred second.

TABLE 327: DS3 FRAMER BLOCK - LCV ONE SECOND ACCUMULATOR REGISTER - MSB (ADDRESS = 0X0E6E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_LCV_Accum_Count[15:8]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - One-Second LCV Accumulation Count[15:8]:

These READ-ONLY bits, along with that within the DS3 Framer Block - One Second LCV Accumulation Count Register - MSB combine to reflect the cumulative number of Line Code Violations that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, during the last one-second accumulation period. This register contains the Most Significant byte of this 16-bit expression.

NOTE: *This register is only active if the XRT86SH328 has been configured to operate in the M13 MUX Mode.*

TABLE 328: DS3 FRAMER BLOCK - LCV ONE SECOND ACCUMULATOR REGISTER - LSB (ADDRESS = 0X0E6F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_LCV_Accum_Count[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - One-Second LCV Accumulation Count[7:0]:

These READ-ONLY bits, along with that within the DS3 Framer Block - One Second LCV Accumulation Count Register - LSB combine to reflect the cumulative number of Line Code Violations that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, during the last one-second accumulation period. This register contains the Least Significant byte of this 16-bit expression.

NOTE: *This register is only active if the XRT86SH328 has been configured to operate in the M13 MUX Mode.*

TABLE 329: DS3 FRAMER BLOCK - P-BIT ERROR ONE SECOND ACCUMULATOR REGISTER - MSB (ADDRESS = 0X0E70)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_P_Bit_Error_Accum_Count[15:8]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - One-Second P-Bit Error Accumulation Count[15:8]:

These READ-ONLY bits, along with that within the DS3 Framer Block - One Second P-Bit Error Accumulation Count Register - LSB combine to reflect the cumulative number of P-Bit errors that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, during the last one-second accumulation period. This register contains the Most Significant byte of this 16-bit expression.

TABLE 330: DS3 FRAMER BLOCK - P-BIT ERROR ONE SECOND ACCUMULATOR REGISTER - LSB (ADDRESS = 0X0E71)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_P_Bit_Error_Accum_Count[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - One-Second P-Bit Error Accumulation Count[7:0]:

These READ-ONLY bits, along with that within the DS3 Framer Block - One Second P-Bit Error Accumulation Count Register - MSB combine to reflect the cumulative number of P-Bit errors that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, during the last one-second accumulation period. This register contains the Least Significant byte of this 16-bit expression.

TABLE 331: DS3 FRAMER BLOCK - CP-BIT ERROR ONE SECOND ACCUMULATOR REGISTER - MSB (ADDRESS = 0X0E72)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_CP_Bit_Error_Accum_Count[15:8]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - One-Second CP-Bit Error Accumulation Count[15:8]:

These READ-ONLY bits, along with that within the DS3 Framer Block - One Second CP-Bit Error Accumulation Count Register - LSB combine to reflect the cumulative number of CP-Bit errors that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, during the last one-second accumulation period. This register contains the Most Significant byte of this 16-bit expression.

NOTE: *This register is only active if the Transmit and Receive DS3 Framer blocks have been configured to operate in the DS3, C-bit Parity Framing format.*

TABLE 332: DS3 FRAMER BLOCK - CP-BIT ERROR ONE SECOND ACCUMULATOR REGISTER - LSB (ADDRESS = 0X0E73)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_CP_Bit_Error_Accum_Count[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - One-Second CP-Bit Error Accumulation Count[7:0]:

These READ-ONLY bits, along with that within the DS3 Framer Block - One Second CP-Bit Error Accumulation Count Register - MSB combine to reflect the cumulative number of CP-Bit errors that the Receive DS3 Framer block has detected within the incoming DS3 data-stream, during the last one-second accumulation period. This register contains the Least Significant byte of this 16-bit expression.

NOTE: *This register is only active if the Transmit and Receive DS3 Framer blocks have been configured to operate in the DS3, C-bit Parity Framing format.*

TABLE 333: DS3 FRAMER BLOCK - TRANSMIT LAPD BYTE COUNT REGISTER (ADDRESS = 0X0E83)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx_LAPD_MESSAGE_SIZE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - Transmit LAPD Message Size[7:0]:

These READ/WRITE bit-fields permit the user to specify the size of the information payload (in terms of bytes) within the very next outbound LAPD/PMDL Message whenever Bit 7 (Transmit LAPD Any) within the DS3 Framer Block - Transmit LAPD Configuration Register has been set to 1.

TABLE 334: DS3 FRAMER BLOCK - RECEIVE LAPD BYTE COUNT REGISTER (ADDRESS = 0X0E84)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx_LAPD_MESSAGE_SIZE[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Receive LAPD Message Size[7:0]:

These READ-ONLY bit-fields indicate the size of the most recently received LAPD/PMDL Message, whenever Bit 7 (Receive LAPD Any) within the DS3 Framer Block - Receive LAPD Control Register has been set to 1.

The contents of this register reflect the Receive LAPD Message size, in terns of bytes.

TABLE 335: DS3 FRAMER BLOCK - RECEIVE DS2 LOOP-BACK REQUEST INTERRUPT ENABLE REGISTER (ADDRESS = 0X0E90)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Change of DS2 Loop-back Request - DS2 Channel 6 Interrupt Enable	Change of DS2 Loop-back Request - DS2 Channel 5 Interrupt Enable	Change of DS2 Loop-back Request - DS2 Channel 4 Interrupt Enable	Change of DS2 Loop-back Request - DS2 Channel 3 Interrupt Enable	Change of DS2 Loop-back Request - DS2 Channel 2 Interrupt Enable	Change of DS2 Loop-back Request - DS2 Channel 1 Interrupt Enable	Change of DS2 Loop-back Request - DS2 Channel 0 Interrupt Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT6 - Change of DS2 Loop-back Request - DS2 Channel 6 Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change of DS2 Loop-back Request Interrupt associated with DS2 Channel 6. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following events.

- Whenever the Receive DS3 Framer block detects and flags the DS2 Loop-back request for DS2 Channel 6.
- Whenever the Receive DS3 Framer block clears the DS2 Loop-back request for DS2 Channel 6.

▶ 0 - Disables the Change of DS2 Loop-back Request Interrupt for DS2 Channel 6.

▶ 1 - Enables the Change of DS2 Loop-back Request Interrupt for DS2 Channel 6.

BIT 5 - Change of DS2 Loop-back Request - DS2 Channel 5 Interrupt Enable:

See description of BIT6.

BIT 4 - Change of DS2 Loop-back Request - DS2 Channel 4 Interrupt Enable

See description of BIT6.

BIT 3 - Change of DS2 Loop-back Request - DS2 Channel 3 Interrupt Enable

See description of BIT6.

BIT 2 - Change of DS2 Loop-back Request - DS2 Channel 2 Interrupt Enable

See description of BIT6.

BIT 1 - Change of DS2 Loop-back Request - DS2 Channel 1 Interrupt Enable

See description of BIT6.

BIT 0 - Change of DS2 Loop-back Request - DS2 Channel 0 Interrupt Enable

See description of BIT6.

TABLE 336: DS3 FRAMER BLOCK - RECEIVE DS2 LOOP-BACK REQUEST INTERRUPT STATUS REGISTER (ADDRESS = 0X0E91)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Change of DS2 Loop-back Request - DS2 Channel 6 Interrupt Status	Change of DS2 Loop-back Request - DS2 Channel 5 Interrupt Status	Change of DS2 Loop-back Request - DS2 Channel 4 Interrupt Status	Change of DS2 Loop-back Request - DS2 Channel 3 Interrupt Status	Change of DS2 Loop-back Request - DS2 Channel 2 Interrupt Status	Change of DS2 Loop-back Request - DS2 Channel 1 Interrupt Status	Change of DS2 Loop-back Request - DS2 Channel 0 Interrupt Status
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT6 - Change of DS2 Loop-back Request - DS2 Channel 6 Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Change of DS2 Loop-back Request Status interrupt for DS2 Channel 6 has occurred since the last read of this register. The XRT86SH328 will generate this interrupt in response to either of the following conditions.

- Whenever the Receive DS3 Framer block detects and flags the DS2 Loop-back request, for DS2 Channel 6.
- Whenever the Receive DS3 Framer block clears the DS2 Loop-back request for DS2 Channel 6.

▶ 0 - Indicates that the Change of DS2 Loop-back Request Status Interrupt has NOT occurred since the last read of this register

▶ 1 - Indicates that the Change of DS2 Loop-back Request Status Interrupt has occurred since the last read of this register.

BIT 5 - Change of DS2 Loop-back Request - DS2 Channel 5 Interrupt Status

See description of BIT6.

BIT 4 - Change of DS2 Loop-back Request - DS2 Channel 4 Interrupt Status

See description of BIT6.

BIT 3 - Change of DS2 Loop-back Request - DS2 Channel 3 Interrupt Status

See description of BIT6.

BIT 2 - Change of DS2 Loop-back Request - DS2 Channel 2 Interrupt Status

See description of BIT6.

BIT 1 - Change of DS2 Loop-back Request - DS2 Channel 1 Interrupt Status

See description of BIT6.

BIT 0 - Change of DS2 Loop-back Request - DS2 Channel 0 Interrupt Status

See description of BIT6.

TABLE 337: DS3 FRAMER BLOCK - RECEIVE DS2 LOOP-BACK REQUEST STATUS REGISTER (ADDRESS = 0X0E92)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Receive DS2 Loop-back Request ON - DS2 Channel 6	Receive DS2 Loop-back Request ON - DS2 Channel 5	Receive DS2 Loop-back Request ON - DS2 Channel 4	Receive DS2 Loop-back Request ON - DS2 Channel 3	Receive DS2 Loop-back Request ON - DS2 Channel 2	Receive DS2 Loop-back Request ON - DS2 Channel 1	Receive DS2 Loop-back Request ON - DS2 Channel 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT6 - Receive DS2 Loop-back Request ON - DS2 Channel 6:

This READ-ONLY bit-field indicates whether or not the Receive DS3 Framer block has detected a DS2 Loop-back Request (associated with DS2 Channel # 6) within the incoming DS3 data-stream. The Receive DS3 Framer block will detect and flag a DS2 Loop-back Request if it detects the DS2 Loop-back Codes (pertaining to a given DS2 channel) for 5 consecutive DS3 frames.

- 0 - Indicates that the Receive DS3 Framer block is NOT currently flagging a DS2 Loop-back Request associated with DS2 Channel 6.
- 1 - Indicates that the Receive DS2 Framer block is currently flagging a DS2 Loop-back Request associated with DS2 Channel 6.

BIT 5 - Receive DS2 Loop-back Request ON - DS2 Channel 5

See description of BIT6.

BIT 4 - Receive DS2 Loop-back Request ON - DS2 Channel 4

See description of BIT6.

BIT 3 - Receive DS2 Loop-back Request ON - DS2 Channel 3

See description of BIT6.

BIT 2 - Receive DS2 Loop-back Request ON - DS2 Channel 2

See description of BIT6.

BIT 1 - Receive DS2 Loop-back Request ON - DS2 Channel 1

See description of BIT6.

BIT 0 - Receive DS2 Loop-back Request ON - DS2 Channel 0

See description of BIT6.

TABLE 338: DS3 FRAMER BLOCK - M12 LOOP-BACK INTERRUPT STATUS/ENABLE REGISTER - 1 (ADDRESS = 0X0E93)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of M12 Loop-back Request Condition - DS1 Channel 3 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 2 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 1 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 0 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 3 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 2 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 1 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 0 Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Change of M12 Loop-back Request Condition - DS1 Channel 3 Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the M12 De-MUX block (associated with DS2 Channel 0) has generated the Change of M12 Loop-back Request Condition Interrupt, for DS1 Channel 3, since the last read of this register. The M12 De-MUX block will generate this particular interrupt in response to either of the following events.

- ? Whenever it detects the M12 Loop-back Request indicator for DS1 Channel 3 (within the incoming DS2 signal)
- Whenever it ceases to detect the M12 Loop-back Request indicator for DS1 Channel 3 (within the incoming DS2 signal).

▶ 0 - Indicates that the Change of M12 Loop-back Request Condition Interrupt, for DS1 Channel 3, has NOT occurred since the last read of this register.

▶ 1 - Indicates that the Change of M12 Loop-back Request Condition Interrupt, for DS1 Channel 3, has occurred since the last read of this register.

BIT6 - Change of M12 Loop-back Request Condition - DS1 Channel 2 Interrupt Status

See description of BIT7.

BIT 5 - Change of M12 Loop-back Request Condition - DS1 Channel 1 Interrupt Status

See description of BIT7.

BIT 4 - Change of M12 Loop-back Request Condition - DS1 Channel 0 Interrupt Status

See description of BIT7.

BIT 3 - Change of M12 Loop-back Request Condition - DS1 Channel 3 Interrupt Enable

This READ/WRITE bit-field is used to either enable or disable the Change of M12 Loop-back Request Condition Interrupt for DS1 Channel 3. If this interrupt is enabled, then the XRT86SH328 will generate an interrupt in response to either of the following conditions.

- Whenever the M12 De-MUX Block (associated with DS2 Channel 0) detects the M12 Loop-back Request indicator for DS1 Channel 3 (within the incoming DS2 signal).
- Whenever the M12 De-MUX Block ceases to detect the M12 Loop-back Request indicator for DS1 Channel 3 (within the incoming DS2 signal).

▶ 0 - Disables the Change of M12 Loop-back Request Condition Interrupt for DS1 Channel 3.

▶ 1 - Enables the Change of M12 Loop-back Request Condition Interrupt for DS1 Channel 3.

BIT 2 - Change of M12 Loop-back Request Condition - DS1 Channel 2 Interrupt Enable

See description of BIT 3.

BIT 1 - Change of M12 Loop-back Request Condition - DS1 Channel 1 Interrupt Enable

See description of BIT 3.

BIT 0 - Change of M12 Loop-back Request Condition - DS1 Channel 0 Interrupt Enable

See description of BIT 3.

TABLE 339: DS3 FRAMER BLOCK - M12 LOOP-BACK STATUS REGISTERS - 1 (ADDRESS = 0X0E94)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				M12 Loop-Back Request Status - DS1 Channel 3	M12 Loop-Back Request Status - DS1 Channel 2	M12 Loop-Back Request Status - DS1 Channel 1	M12 Loop-Back Request Status - DS1 Channel 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT7 - 4 - Reserved:

BIT 3 - M12 Loop-Back Request Status - DS1 Channel 3:

This READ/WRITE bit-field indicates whether or not the M12 De-MUX Block (associated with DS2 Channel 0) is currently detecting the M12 Loop-Back Request for DS1 Channel 3, within the incoming DS2 data-stream.

- 0 - Indicates that the M12 De-MUX Block (associated with DS2 Channel 0) is NOT currently detecting the M12 Loop-Back Request for DS1 Channel 3, within the incoming DS2 data-stream.
- 1 - Indicates that the M12 De-MUX Block (associated with DS2 Channel 0) is currently detecting the M12 Loop-Back Request for DS1 Channel 3, within the incoming DS2 data-stream.

BIT 2 - M12 Loop-Back Request Status - DS1 Channel 2:

See description of BIT 3.

BIT 1 - M12 Loop-Back Request Status - DS1 Channel 1:

See description of BIT 3.

BIT 0 - M12 Loop-Back Request Status - DS1 Channel 0:

See description of BIT 3.

TABLE 340: DS3 FRAMER BLOCK - M12 LOOP-BACK INTERRUPT STATUS/ENABLE REGISTER - 2 (ADDRESS = 0X0E95)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of M12 Loop-back Request Condition - DS1 Channel 7 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 6 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 5 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 4 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 7 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 6 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 5 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 4 Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

See Table 338 above for bit descriptions, substituting Channel [7:4] for Channel [3:0].

TABLE 341: DS3 FRAMER BLOCK - M12 LOOP-BACK STATUS REGISTERS - 2 (ADDRESS = 0X0E96)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				M12 Loop-Back Request Status - DS1 Channel 7	M12 Loop-Back Request Status - DS1 Channel 6	M12 Loop-Back Request Status - DS1 Channel 5	M12 Loop-Back Request Status - DS1 Channel 4
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 339 above, for bit descriptions, substituting Channel [7:4] for Channel [3:0].

TABLE 342: DS3 FRAMER BLOCK - M12 LOOP-BACK INTERRUPT STATUS/ENABLE REGISTER - 3 (ADDRESS = 0X0E97)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of M12 Loop-back Request Condition - DS1 Channel 11 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 10 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 9 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 8 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 11 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 10 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 9 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 8 Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

See Table 338 above for bit descriptions, substituting Channel [11:8] for Channel [3:0].

TABLE 343: DS3 FRAMER BLOCK - M12 LOOP-BACK STATUS REGISTERS - 3 (ADDRESS = 0X0E98)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				M12 Loop-Back Request Status - DS1 Channel 11	M12 Loop-Back Request Status - DS1 Channel 10	M12 Loop-Back Request Status - DS1 Channel 9	M12 Loop-Back Request Status - DS1 Channel 8
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 339 above, for bit descriptions, substituting Channel [11:8] for Channel [3:0].

TABLE 344: DS3 FRAMER BLOCK - M12 LOOP-BACK INTERRUPT STATUS/ENABLE REGISTER - 4 (ADDRESS = 0X0E99)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of M12 Loop-back Request Condition - DS1 Channel 15 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 14 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 13 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 12 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 15 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 14 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 13 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 12 Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

See Table 338 above for bit descriptions, substituting Channel [15:12] for Channel [3:0].

TABLE 345: DS3 FRAMER BLOCK - M12 LOOP-BACK STATUS REGISTERS - 4 (ADDRESS = 0X0E9A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				M12 Loop-Back Request Status - DS1 Channel 15	M12 Loop-Back Request Status - DS1 Channel 14	M12 Loop-Back Request Status - DS1 Channel 13	M12 Loop-Back Request Status - DS1 Channel 12
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 339 above, for bit descriptions, substituting Channel [15:12] for Channel [3:0].

TABLE 346: DS3 FRAMER BLOCK - M12 LOOP-BACK INTERRUPT STATUS/ENABLE REGISTER - 5 (ADDRESS = 0X0E9B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of M12 Loop-back Request Condition - DS1 Channel 19 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 18 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 17 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 16 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 19 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 18 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 17 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 16 Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

See Table 338 above for bit descriptions, substituting Channel [19:16] for Channel [3:0].

TABLE 347: DS3 FRAMER BLOCK - M12 LOOP-BACK STATUS REGISTERS - 5 (ADDRESS = 0X0E9C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				M12 Loop-Back Request Status - DS1 Channel 19	M12 Loop-Back Request Status - DS1 Channel 18	M12 Loop-Back Request Status - DS1 Channel 17	M12 Loop-Back Request Status - DS1 Channel 16
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - Bit - See Table 339 above, for bit descriptions, substituting Channel [19:16] for Channel [3:0].

TABLE 348: DS3 FRAMER BLOCK - M12 LOOP-BACK INTERRUPT STATUS/ENABLE REGISTER - 6 (ADDRESS = 0X0E9D)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of M12 Loop-back Request Condition - DS1 Channel 23 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 22 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 21 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 20 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 23 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 22 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 21 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 20 Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

See Table 338 above for bit descriptions, substituting Channel [23:20] for Channel [3:0].

TABLE 349: DS3 FRAMER BLOCK - M12 LOOP-BACK STATUS REGISTERS - 6 (ADDRESS = 0X0E9E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				M12 Loop-Back Request Status - DS1 Channel 23	M12 Loop-Back Request Status - DS1 Channel 22	M12 Loop-Back Request Status - DS1 Channel 21	M12 Loop-Back Request Status - DS1 Channel 20
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 339 above, for bit descriptions, substituting Channel [23:20] for Channel [3:0].

TABLE 350: DS3 FRAMER BLOCK - M12 LOOP-BACK INTERRUPT STATUS/ENABLE REGISTER - 7 (ADDRESS = 0X0E9F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of M12 Loop-back Request Condition - DS1 Channel 27 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 26 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 25 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 24 Interrupt Status	Change of M12 Loop-back Request Condition - DS1 Channel 27 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 26 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 25 Interrupt Enable	Change of M12 Loop-back Request Condition - DS1 Channel 24 Interrupt Enable
RUR	RUR	RUR	RUR	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

See Table 338 above for bit descriptions, substituting Channel [27:24] for Channel [3:0].

TABLE 351: DS3 FRAMER BLOCK - M12 LOOP-BACK STATUS REGISTERS - 7 (ADDRESS = 0X0EA0)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				M12 Loop-Back Request Status - DS1 Channel 27	M12 Loop-Back Request Status - DS1 Channel 26	M12 Loop-Back Request Status - DS1 Channel 25	M12 Loop-Back Request Status - DS1 Channel 24
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - See Table 339 above, for bit descriptions, substituting Channel [27:24] for Channel [3:0].

TABLE 352: DS3 FRAMER BLOCK - DS2 # 1 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0X0EA1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	Change of DS2 LOF Defect Condition Interrupt Enable	Change of DS2 FERF/RDI Defect Condition Interrupt Enable	Change of DS2 RED Alarm Defect Condition Interrupt Enable	Change of DS2 AIS Defect Condition Interrupt Enable	Change of State of Reserved Bit (G.747) Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Unused:

BIT 5 - DS2 COFA (Change of Framing Alignment) Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the DS2 Change of Framing Alignment interrupt for DS2 Channel # 1. If the user enables this interrupt, then the M12 De-MUX block will generate an interrupt anytime it has detected a change in DS2 framing alignment within the incoming DS2 data-stream.

- 0 - Disables the DS2 COFA Interrupt for DS2 Channel 1.
- 1 - Enables the DS2 COFA Interrupt for DS2 Channel 1.

BIT 4 - Change of DS2 LOF Defect Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change of DS2 LOF Defect Condition Interrupt for DS2 Channel 1. If the user enables this interrupt, then the M12 De-MUX block will generate an interrupt in response to either of the following conditions.

- Whenever the M12 De-MUX block declares the DS2 LOF Defect condition, or
- Whenever the M12 De-MUX block clears the DS2 LOF Defect condition.

- 0 - Disables the Change of DS2 LOF Defect Condition Interrupt for DS2 Channel 1.
- 1 - Enables the Change of DS2 LOF Defect Condition Interrupt for DS2 Channel 1.

BIT 3 - Change of DS2 FERF/RDI Defect Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change of DS2 FERF/RDI Defect Condition Interrupt for DS2 Channel 1. If the user enables this interrupt, then the M12 De-MUX block will generate an interrupt in response to either of the following conditions.

- Whenever the M12 De-MUX block declares the DS2 FERF/RDI Defect condition, or
- Whenever the M12 De-MUX block clears the DS2 FERF/RDI Defect condition.

- 0 - Disables the Change of DS2 FERF/RDI Defect Condition Interrupt for DS2 Channel 1.
- 1 - Enables the Change of DS2 FERF/RDI Defect Condition Interrupt for DS2 Channel 1.

BIT 2 - Change of DS2 RED Alarm Defect Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change of DS2 RED Alarm Defect Condition Interrupt for DS2 Channel 1. If the user enables this interrupt, then the M12 De-MUX block will generate an interrupt in response to either of the following conditions.

- Whenever the M12 De-MUX block declares the DS2 RED Alarm Defect condition, or
- Whenever the M12 De-MUX block clears the DS2 RED Alarm Defect condition.

- 0 - Disables the Change of DS2 RED Alarm Defect Condition Interrupt for DS2 Channel 1.
- 1 - Enables the Change of DS2 RED Alarm Defect Condition Interrupt for DS2 Channel 1.

BIT 1 - Change of DS2 AIS Defect Condition Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change of DS2 AIS Defect Condition Interrupt for DS2 Channel 1. If the user enables this interrupt, then the M12 De-MUX block will generate an interrupt in response to either of the following conditions.

- Whenever the M12 De-MUX block declares the DS2 AIS Defect condition, or
- Whenever the M12 De-MUX block clears the DS2 AIS Defect condition.

- 0 - Disables the Change of DS2 AIS Defect Condition Interrupt for DS2 Channel 1.
- 1 - Enables the Change of DS2 AIS Defect Condition Interrupt for DS2 Channel 1.

BIT 0 - Change of State of Reserved Bit (G.747) Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change of State of the G.747 Reserved Bit Interrupt. If the user enables this interrupt, then the M12 De-MUX block will generate an interrupt anytime it detects a change of state in the Reserved Bit within the G.747 Data Stream associated with G.747 Channel # 1.

- 0 - Disables the Change of State of the G.747 Reserved Bit Interrupt for M12 De-MUX Block Channel 1.
- 1 - Enables the Change of State of the G.747 Reserved Bit Interrupt for M12 De-MUX Block Channel 1.

NOTE: *This bit-field is only active if M12 De-MUX Block # 1 has been configured to operate in the G.747 Mode.*

TABLE 353: DS3 FRAMER BLOCK - DS2 # 1 FRAMER INTERRUPT STATUS REGISTER (ADDRESS = 0X0EA2)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Status	Change of DS2 LOF Defect Condition Interrupt Status	Change of DS2 FERF/RDI Defect Condition Interrupt Status	Change of DS2 RED Alarm Defect Condition Interrupt Status	Change of DS2 AIS Defect Condition Interrupt Status	Change of State of Reserved Bit (G.747) Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:6] - Unused:

BIT 5 - DS2 COFA Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the DS2 COFA Interrupt (associated with M12 De-MUX # 1) has occurred since the last read of this register.

- 0 - Indicates that the DS2 COFA Interrupt (associated with M12 De-MUX # 1) has NOT occurred since the last read of this register.
- 1 - Indicates that the DS2 COFA Interrupt (associated with M12 De-MUX # 1) has occurred since the last read of this register.

BIT 4 - Change of DS2 LOF Defect Condition Interrupt Status:

This RESET-upon-READ bit-filed indicates whether or not the Change of DS2 LOF Defect Condition interrupt has occurred (within M12 De-MUX # 1) since the last read of this register.

- 0 - Indicates that the Change of DS2 LOF Defect Condition Interrupt (associated with M12 De-MUX # 1) has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of DS2 LOF Defect Condition Interrupt (associated with M12 De-MUX # 1) has occurred since the last read of this register.

BIT 3 - Change of DS2 FERF/RDI Defect Condition Interrupt Status:

This RESET-upon-READ bit-filed indicates whether or not the Change of DS2 FERF/RDI Defect Condition interrupt has occurred (within M12 De-MUX # 1) since the last read of this register.

- 0 - Indicates that the Change of DS2 FERF/RDI Defect Condition Interrupt (associated with M12 De-MUX # 1) has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of DS2 FERF/RDI Defect Condition Interrupt (associated with M12 De-MUX # 1) has occurred since the last read of this register.

BIT 2 - Change of DS2 RED Alarm Defect Condition Interrupt Status:

This RESET-upon-READ bit-filed indicates whether or not the Change of DS2 RED Alarm Defect Condition interrupt has occurred (within M12 De-MUX # 1) since the last read of this register.

- 0 - Indicates that the Change of DS2 RED Alarm Defect Condition Interrupt (associated with M12 De-MUX # 1) has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of DS2 RED Alarm Defect Condition Interrupt (associated with M12 De-MUX # 1) has occurred since the last read of this register.

BIT 1 - Change of DS2 AIS Defect Condition Interrupt Status:

This RESET-upon-READ bit-filed indicates whether or not the Change of DS2 AIS Defect Condition interrupt has occurred (within M12 De-MUX # 1) since the last read of this register.

- 0 - Indicates that the Change of DS2 AIS Defect Condition Interrupt (associated with M12 De-MUX # 1) has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of DS2 AIS Defect Condition Interrupt (associated with M12 De-MUX # 1) has occurred since the last read of this register.

BIT 0 - Change of State of Reserved Bit (G.747) Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Change of State of the G.747 Reserved Bit Interrupt has occurred (within M12 De-MUX # 1) since the last read of this register.

- 0 - Indicates that the Change of State of the G.747 Reserved Bit Interrupt (associated with M12 De-MUX # 1) has NOT occurred since the last read of this register.
- 1 - Indicates that the Change of State of the G.747 Reserved Bit Interrupt (associated with M12 De-MUX # 1) has occurred since the last read of this register.

NOTE: *This bit-field is only active if M12 De-MUX Block # 1 has been configured to operate in the G.747 Mode.*

TABLE 354: DS3 FRAMER BLOCK - DS2 # 1 FRAMER STATUS REGISTER (ADDRESS = 0X0EA3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			DS2 LOF Defect Declared	DS2 FERF/RDI Defect Declared	DS2 RED Alarm Defect Declared	DS2 AIS Defect Declared	Current State of Reserved Bit (G.747)
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:5] - Unused:

BIT 4 - DS2 LOF Defect Declared:

This READ-ONLY bit-field indicates whether or not M12 De-MUX Block # 1 is currently declaring the DS2 LOF defect condition.

- 0 - Indicates that M12 De-MUX Block # 1 is NOT currently declaring the DS2 LOF defect condition.
- 1 - Indicates that M12 De-MUX Block # 1 is currently declaring the DS2 LOF defect condition.

BIT 3 - DS2 FERF/RDI Defect Declared:

This READ-ONLY bit-field indicates whether or not M12 De-MUX Block # 1 is currently declaring the DS2 FERF/RDI defect condition.

- 0 - Indicates that M12 De-MUX Block # 1 is NOT currently declaring the DS2 FERF/RDI defect condition.
- 1 - Indicates that M12 De-MUX Block # 1 is currently declaring the DS2 FERF/RDI defect condition.

BIT 2 - DS2 RED Alarm Defect Declared:

This READ-ONLY bit-field indicates whether or not M12 De-MUX Block # 1 is currently declaring the DS2 RED Alarm defect condition.

- 0 - Indicates that M12 De-MUX Block # 1 is NOT currently declaring the DS2 RED Alarm defect condition.
- 1 - Indicates that M12 De-MUX Block # 1 is currently declaring the DS2 RED Alarm defect condition.

BIT 1 - DS2 AIS Defect Declared:

This READ-ONLY bit-field indicates whether or not M12 De-MUX Block # 1 is currently declaring the DS2 AIS defect condition.

- 0 - Indicates that M12 De-MUX Block # 1 is NOT currently declaring the DS2 AIS defect condition.
- 1 - Indicates that M12 De-MUX Block # 1 is currently declaring the DS2 AIS defect condition.

BIT 0 - Current State of Reserved Bit (G.747):

This READ-ONLY bit-field reflects the current state of the G.747 Reserve bit, as relieved by M12 De-MUX Block # 1.

TABLE 355: DS3 FRAMER BLOCK - DS2 # 2 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0X0EA4)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	Change of DS2 LOF Defect Condition Interrupt Enable	Change of DS2 FERF/RDI Defect Condition Interrupt Enable	Change of DS2 RED Alarm Defect Condition Interrupt Enable	Change of DS2 AIS Defect Condition Interrupt Enable	Change of State of Reserved Bit (G.747) Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 352 above, substituting Channel 2 for Channel 1 and De-MUx #2 for De-mux #1.

TABLE 356: DS3 FRAMER BLOCK - DS2 # 2 FRAMER INTERRUPT STATUS REGISTER (ADDRESS = 0X0EA5)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Status	Change of DS2 LOF Defect Condition Interrupt Status	Change of DS2 FERF/RDI Defect Condition Interrupt Status	Change of DS2 RED Alarm Defect Condition Interrupt Status	Change of DS2 AIS Defect Condition Interrupt Status	Change of State of Reserved Bit (G.747) Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 353 above, substituting De-Mux #2 for De-Mux #1.

TABLE 357: DS3 FRAMER BLOCK - DS2 # 2 FRAMER STATUS REGISTER (ADDRESS = 0X0EA6)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			DS2 LOF Defect Declared	DS2 FERF/RDI Defect Declared	DS2 RED Alarm Defect Declared	DS2 AIS Defect Declared	Current State of Reserved Bit (G.747)
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 354 above, substituting De-Mux #2 for De-Mux #1.

TABLE 358: DS3 FRAMER BLOCK - DS2 # 3 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0X0EA7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	Change of DS2 LOF Defect Condition Interrupt Enable	Change of DS2 FERF/RDI Defect Condition Interrupt Enable	Change of DS2 RED Alarm Defect Condition Interrupt Enable	Change of DS2 AIS Defect Condition Interrupt Enable	Change of State of Reserved Bit (G.747) Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 352 above, substituting Channel 3 for Channel 1 and De-MUx #3 for De-mux #1.

TABLE 359: DS3 FRAMER BLOCK - DS2 # 3 FRAMER INTERRUPT STATUS REGISTER (ADDRESS = 0X0EA8)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Status	Change of DS2 LOF Defect Condition Interrupt Status	Change of DS2 FERF/RDI Defect Condition Interrupt Status	Change of DS2 RED Alarm Defect Condition Interrupt Status	Change of DS2 AIS Defect Condition Interrupt Status	Change of State of Reserved Bit (G.747) Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 353 above, substituting De-Mux #3 for De-Mux #1.

TABLE 360: DS3 FRAMER BLOCK - DS2 # 3 FRAMER STATUS REGISTER (ADDRESS = 0X0EA9)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			DS2 LOF Defect Declared	DS2 FERF/RDI Defect Declared	DS2 RED Alarm Defect Declared	DS2 AIS Defect Declared	Current State of Reserved Bit (G.747)
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 354 above, substituting De-Mux #3 for De-Mux #1.

TABLE 361: DS3 FRAMER BLOCK - DS2 # 4 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0X0EAA)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	Change of DS2 LOF Defect Condition Interrupt Enable	Change of DS2 FERF/RDI Defect Condition Interrupt Enable	Change of DS2 RED Alarm Defect Condition Interrupt Enable	Change of DS2 AIS Defect Condition Interrupt Enable	Change of State of Reserved Bit (G.747) Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 352 above, substituting Channel 4 for Channel 1 and De-MUx #4 for De-mux #1.

TABLE 362: DS3 FRAMER BLOCK - DS2 # 4 FRAMER INTERRUPT STATUS REGISTER (ADDRESS = 0X0EAB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Status	Change of DS2 LOF Defect Condition Interrupt Status	Change of DS2 FERF/RDI Defect Condition Interrupt Status	Change of DS2 RED Alarm Defect Condition Interrupt Status	Change of DS2 AIS Defect Condition Interrupt Status	Change of State of Reserved Bit (G.747) Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 353 above substituting De-Mux #4 for De-Mux #1.

TABLE 363: DS3 FRAMER BLOCK - DS2 # 4 FRAMER STATUS REGISTER (ADDRESS = 0X0EAC)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			DS2 LOF Defect Declared	DS2 FERF/RDI Defect Declared	DS2 RED Alarm Defect Declared	DS2 AIS Defect Declared	Current State of Reserved Bit (G.747)
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 354 above, substituting De-Mux #4 for De-Mux #1.

TABLE 364: DS3 FRAMER BLOCK - DS2 # 5 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0X0EAD)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	Change of DS2 LOF Defect Condition Interrupt Enable	Change of DS2 FERF/RDI Defect Condition Interrupt Enable	Change of DS2 RED Alarm Defect Condition Interrupt Enable	Change of DS2 AIS Defect Condition Interrupt Enable	Change of State of Reserved Bit (G.747) Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 352 above, substituting Channel 5 for Channel 1 and De-MUx #5 for De-mux #1.

TABLE 365: DS3 FRAMER BLOCK - DS2 # 5 FRAMER INTERRUPT STATUS REGISTER (ADDRESS = 0X0EAE)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Status	Change of DS2 LOF Defect Condition Interrupt Status	Change of DS2 FERF/RDI Defect Condition Interrupt Status	Change of DS2 RED Alarm Defect Condition Interrupt Status	Change of DS2 AIS Defect Condition Interrupt Status	Change of State of Reserved Bit (G.747) Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 353 above substituting De-Mux #5 for De-Mux #1.

TABLE 366: DS3 FRAMER BLOCK - DS2 # 5 FRAMER STATUS REGISTER (ADDRESS = 0X0EAF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			DS2 LOF Defect Declared	DS2 FERF/RDI Defect Declared	DS2 RED Alarm Defect Declared	DS2 AIS Defect Declared	Current State of Reserved Bit (G.747)
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 354 above, substituting De-Mux #5 for De-Mux #1.

TABLE 367: DS3 FRAMER BLOCK - DS2 # 6 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0X0EB0)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	Change of DS2 LOF Defect Condition Interrupt Enable	Change of DS2 FERF/RDI Defect Condition Interrupt Enable	Change of DS2 RED Alarm Defect Condition Interrupt Enable	Change of DS2 AIS Defect Condition Interrupt Enable	Change of State of Reserved Bit (G.747) Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 352 above, substituting Channel 2 for Channel 6 and De-MUx #6 for De-mux #1.

TABLE 368: DS3 FRAMER BLOCK - DS2 # 6 FRAMER INTERRUPT STATUS REGISTER (ADDRESS = 0X0EB1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Status	Change of DS2 LOF Defect Condition Interrupt Status	Change of DS2 FERF/RDI Defect Condition Interrupt Status	Change of DS2 RED Alarm Defect Condition Interrupt Status	Change of DS2 AIS Defect Condition Interrupt Status	Change of State of Reserved Bit (G.747) Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 353 above substituting De-Mux #6 for De-Mux #1.

TABLE 369: DS3 FRAMER BLOCK - DS2 # 6 FRAMER STATUS REGISTER (ADDRESS = 0X0EB2)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			DS2 LOF Defect Declared	DS2 FERF/RDI Defect Declared	DS2 RED Alarm Defect Declared	DS2 AIS Defect Declared	Current State of Reserved Bit (G.747)
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 354 above, substituting De-Mux #6 for De-Mux #1.

TABLE 370: DS3 FRAMER BLOCK - DS2 # 7 FRAMER INTERRUPT ENABLE REGISTER (ADDRESS = 0X0EB3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Enable	Change of DS2 LOF Defect Condition Interrupt Enable	Change of DS2 FERF/RDI Defect Condition Interrupt Enable	Change of DS2 RED Alarm Defect Condition Interrupt Enable	Change of DS2 AIS Defect Condition Interrupt Enable	Change of State of Reserved Bit (G.747) Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 352 above, substituting Channel 7 for Channel 1 and De-MUx #7 for De-mux #1.

TABLE 371: DS3 FRAMER BLOCK - DS2 # 7 FRAMER INTERRUPT STATUS REGISTER (ADDRESS = 0X0EB4)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		DS2 COFA Interrupt Status	Change of DS2 LOF Defect Condition Interrupt Status	Change of DS2 FERF/RDI Defect Condition Interrupt Sta-tus	Change of DS2 RED Alarm Defect Condition Interrupt Status	Change of DS2 AIS Defect Condition Interrupt Status	Change of State of Reserved Bit (G.747) Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 353 above, substituting De-Mux #7 for De-Mux #1.

TABLE 372: DS3 FRAMER BLOCK - DS2 # 7 FRAMER STATUS REGISTER (ADDRESS = 0X0EB5)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			DS2 LOF Defect Declared	DS2 FERF/RDI Defect Declared	DS2 RED Alarm Defect Declared	DS2 AIS Defect Declared	Current State of Reserved Bit (G.747)
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT [7:0] - For bit descriptions see Table 354 above, substituting De-Mux #7 for De-Mux #1.

TABLE 373: DS3 FRAMER BLOCK - M13 DE-MUX REGISTER (ADDRESS = 0X0EB8)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Auto DS1/E1 AIS upon DS2 OOF Defect	Unused	Auto DS1/E1 AIS upon DS2 AIS Defect	Unused
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/O
0	0	0	0	0	0	0	0

BIT [7:4] - Unused:

BIT 3 - Auto DS1/E1 AIS upon DS2 LOF Defect:

This READ/WRITE bit-field is used to configure all of the Egress Direction Transmit DS1/E1 Framer blocks (associated with a given M12 De-MUX block) to automatically transmit the DS1/E1 AIS indicator via each of its three or four downstream DS1/E1 signals, anytime (and for the duration that) the corresponding M12 De-MUX block declares the DS2 LOF defect condition.

- 0 - Does not configure each of the M12 De-MUX blocks to force all of its corresponding Egress Direction Transmit DS1/E1 Framer blocks (within the XRT86SH328) to automatically transmit the DS1/E1 AIS indicator via its downstream DS1/E1 signals, anytime (and for the duration that) the M12 De-MUX block declares the DS2 LOF defect condition.
- 1 - Configures each of the M12 De-MUX blocks to force all of its corresponding Egress Direction Transmit DS1/E1 Framer blocks (within the XRT86SH328) to automatically transmit the DS1/E1 AIS indicator via its downstream DS1/E1 signals, anytime (and for the duration that) the M12 De-MUX block declares the DS2 LOF defect condition.

NOTE: *This bit-setting applies to each of the seven (7) M12 De-MUX blocks within the XRT86SH328.*

BIT 2 - Unused:

BIT 1 - Auto DS1/E1 AIS upon DS2 AIS Defect:

This READ/WRITE bit-field is used to configure all of the Egress Direction Transmit DS1/E1 Framer blocks (associated with a given M12 De-MUX block) to automatically transmit the DS1/E1 AIS indicator via each of its three or four downstream DS1/E1 signals, anytime (and for the duration that) the corresponding M12 De-MUX block declares the DS2 AIS defect condition.

- 0 - Does not configure each of the M12 De-MUX blocks to force all of its corresponding Egress Direction Transmit DS1/E1 Framer blocks (within the XRT86SH328) to automatically transmit the DS1/E1 AIS indicator via its downstream DS1/E1 signals, anytime (and for the duration that) the M12 De-MUX block declares the DS2 AIS defect condition.
- 1 - Configures each of the M12 De-MUX blocks to force all of its corresponding Egress Direction Transmit DS1/E1 Framer blocks (within the XRT86SH328) to automatically transmit the DS1/E1 AIS indicator via its downstream DS1/E1 signals, anytime (and for the duration that) the M12 De-MUX block declares the DS2 AIS defect condition.

NOTE: *This bit-setting applies to each of the seven (7) M12 De-MUX blocks within the XRT86SH328328.*

BIT 0 - Unused:

2.12 T1/E1 LIU CHANNEL CONTROL REGISTERS

- **(N ranges from 0x01 to 0x1C)**

TABLE 374: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN000)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS/QRSS	PRBS_Rx_Tx	RXON	EQC[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - PRBS/QRSS:

These bits are used to select between QRSS and PRBS. To send the a QRSS or PRBS pattern, the TxTEST[2:0] bits in register 0xN002h must be programmed.

- 0 = QRSS
- 1 = PRBS

BIT6 - PRBS/QRSS Direction Select Rx/Tx:

This bit is used to select which direction is used to send the PRBS/QRSS pattern if enabled within the TxTEST[2:0] bits in register 0xN002h.

- 0 = Line Interface (Ttip/Tring)
- 1 = System Side Interface (Clock/Data)

BIT 5 - RXON Receiver Enable:

This bit is used enable the receiver line interface. By default, the receivers are turned off to support redundancy.

- 0 = Disabled.
- 1 = Enabled.

BIT [4:0] - Equalizer Control and Line Build Out:

These bits are used to select the equalizer control and line build out.

Selection Chart for Equalizer Control and Line Build-Out

EQC[4:0]	T1/E1 Mode Receive Sensitivity	Transmit LBO	Cable	Coding
01000	T1 Short Haul	0 - 133 Ft (0.6dB)	100W TP	B8ZS
01001	T1 Short Haul	0 - 133 Ft (0.6dB)	100W TP	B8ZS
01010	T1 Short Haul	0 - 133 Ft (0.6dB)	100W TP	B8ZS
01011	T1 Short Haul	0 - 133 Ft (0.6dB)	100W TP	B8ZS
01100	T1 Short Haul	0 - 133 Ft (0.6dB)	100W TP	B8ZS
01101	T1 Short Haul	Arbitrary Pulse	100W TP	B8ZS
11100	E1 Short Haul	ITU G.703	75W Coax	HDB3
11101	E1 Short Haul	ITU G.703	120W TP	HDB3

Table 375: LIU Channel Control Register 0 (Address = 0xN001)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTSEL	TxTSEL	TERSEL[1:0]		JASEL[1:0]		JABW	FIFOS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - RxTSEL:

This bit is used for the receive line interface to select between Internal (automatic line impedance) and External (high impedance) modes.

- 0 = External Impedance
- 1 = Internal Impedance

BIT6 - TxTSEL:

This bit is used for the transmit line interface to select between Internal (automatic line impedance) and External (high impedance) modes.

- 0 = External Impedance
- 1 = Internal Impedance

BIT [5:4] - TERSEL[1:0]:

These bits are used to select the line impedance for internal termination control.

- 00 = 100W
- 01 = 110W
- 10 = 75W
- 11 = 120W

BIT [3:2] - JASEL[1:0]:

These bits are used to select which path the Jitter Attenuator is placed.

- 00 = Disabled.
- 01 = Transmit Line Interface Path
- 10 = Receive Line Interface Path
- 11 = Receive Line Interface Path
- BIT 1 - Jitter Attenuator Band Width:

The jitter band width is a global setting that is applied in both transmit and receive directions.

- 0 = 10 Hz
- 1 = 1.5 Hz

BIT 0 - First In First Out Bit Depth:

This bit is used for the transmit line interface to select between Internal (automatic line impedance) and External (high impedance) modes.

- 0 = 32-Bit
- 1 = 64-Bit

TABLE 376: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN002)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INVQRSS	TxTEST[2:0]			TXON	LOOP[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Invert QRSS:

INVQRSS is used to invert the transmit QRSS pattern set by the TxTEST[2:0] bits. By default, INVQRSS is disabled and the QRSS will be transmitted with normal polarity.

- 0 = External Impedance
- 1 = Internal Impedance

BIT [6:4] - Tx Test Pattern [2:0]:

These bits are used to select a Test Pattern to be sent to the transmit line interface. If bit 6 in register 0xN000h is set High, then the Test Pattern will be sent out on the receive DS-1/E1 system side.

- 0XX = No Test Pattern
- 100 = Tx QRSS
- 101 = Tx TAOS
- 110 = Reserved
- 111 = Reserved

BIT 3 - TXON Transmitter Enable:

This bit is used enable the transmitter line interface. By default, the transmitters are turned off to support redundancy.

- 0 = Disabled.
- 1 = Enabled.

BIT [2:0] - Loop Back Mode Select [2:0]:

These bits are used to select a loop back mode for diagnostic testing. These bits only represent the loop back modes supported in the LIU section of Voyager. For other loop back mode options, see the register map in other modes of operation.

- 0XX = No Loop Back
- 100 = Dual Loop Back
- 101 = Analog Loop Back
- 110 = Remote Loop Back
- 111 = Digital Loop Back

TABLE 377: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN003)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxRES[1:0]		CODES	Reserved	E1ARBIT	INSBPV	INSBER	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Receiver Fixed External Termination:

RxRES[1:0] are used to select the value for a high precision external resistor to improve return loss.

- 00 = None
- 01 = 240W
- 10 = 210W
- 11 = 150W

BIT 5 - CODES Encoding / Decoding Select:

This bit is used to select the type of encoding/decoding the transmitter and receiver will generate/process.

- 0 = HDB3 (E1), B8ZS (T1)
- 1 = AMI Coding

BIT 4 - Reserved:

BIT 3 - E1Arbitrary Pulse Select:

This bit is used to enable the Arbitrary Pulse Generator for shaping the transmit pulse when E1 mode is selected.

- 0 = Disabled (Normal E1 Pulse Shape ITU G.703)
- 1 = Arbitrary Pulse Enabled

BIT 2 - Insert Bipolar Violation:

When this bit transitions from Low to High, a bipolar violation will be inserted in the transmitted data from TPOS, QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a 0 to this bit before writing a 1.

- 0 to 1 Transition = Insert one bipolar violation

BIT 1 - Insert Bit Error:

When this bit transitions from Low to High, a bit error will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a 0 to this bit before writing a 1.

- 0 to 1 Transition = Insert one bit error

BIT 0 - Reserved:

TABLE 378: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN004)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMOIE	FLSIE	LCVIE	Reserved	AISDIE	RLOSIE	QRPDIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT6 - Digital Monitor Output Interrupt Enable:

- 0 = Masks the DMO function
- 1 = Enables interrupt generation for DMO

BIT 5 - FIFO Limit Status Interrupt Enable:

- 0 = Masks the FLS function
- 1 = Enables interrupt generation for FLS

BIT 4 - Line Code Violation Interrupt Enable:

- 0 = Masks the LCV function
- 1 = Enables interrupt generation for LCV

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal Interrupt Enable:

- 0 = Masks the AIS function
- 1 = Enables interrupt generation for AIS

BIT 1 - Receive Loss of Signal Interrupt Enable:

- 0 = Masks the RLOS function
- 1 = Enables interrupt generation for RLOS

BIT 0 - Quasi Random Pattern Detection Interrupt Enable:

- 0 = Masks the QRPD function
- 1 = Enables interrupt generation for QRPD

TABLE 379: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN005)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMO	FLS	LCV	Reserved	AISD	RLOS	QRPD
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT6 - Digital Monitor Output:

This bit indicates the DMO activity. An interrupt will not occur unless the DMOIE is set High in register 0xN004h and the global interrupt enable has been set.

- 0 = No Alarm
- 1 = Transmit output driver has failures

BIT 5 - FIFO Limit Status:

This bit indicates whether the RD/WR pointers are within 3-Bits. An interrupt will not occur unless the FLSIE is set High in register 0xN004h and the global interrupt enable has been set.

- 0 = No Alarm
- 1 = RD/WR FIFO pointers are within ±3-Bits

BIT 4 - Line Code Violation:

This bit serves a dual purpose. By default, this bit monitors the line code violation activity. However, if bit 7 in register 0x0101h is set High, this bit monitors the overflow status of the internal LCV counter. An interrupt will not occur unless the LCV/OFIE is set High in register 0xN004h and the global interrupt enable has been set.

- 0 = No Alarm
- 1 = A line code violation, bipolar violation, or excessive zeros has occurred

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal:

This bit indicates the AIS activity. An interrupt will not occur unless the AISIE is set High in register 0xN004h and the global interrupt enable has been set.

- 0 = No Alarm
- 1 = An all ones signal is detected

BIT 1 - Receive Loss of Signal:

This bit indicates the RLOS activity. An interrupt will not occur unless the RLOSIE is set High in register 0xN004h and the global interrupt enable has been set.

- 0 = No Alarm
- 1 = An RLOS condition is present

BIT 0 - Quasi Random Pattern Detection:

This bit indicates that a QRPD has been detected. An interrupt will not occur unless the QRPDIE is set High in register 0xN004h and the global interrupt enable has been set.

- 0 = No Alarm
- 1 = A QRP is detected

TABLE 380: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN006)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMOIS	FLSIS	LCVIS	Reserved	AISDIS	RLOSIS	QRPDIS
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTE: *These register bits are Reset Upon Read. They will be set High anytime a change in status occurs. Once these bits are read back, they will automatically be set Low.*

BIT7 - Reserved:

BIT6 - Digital Monitor Output Interrupt Enable:

- 0 = No change
- 1 = Change in status occurred

BIT 5 - FIFO Limit Status Interrupt Enable:

- 0 = No change
- 1 = Change in status occurred

BIT 4 - Line Code Violation Interrupt Enable:

- 0 = No change
- 1 = Change in status occurred

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal Interrupt Enable:

- 0 = No change
- 1 = Change in status occurred

BIT 1 - Receive Loss of Signal Interrupt Enable:

- 0 = No change

- 1 = Change in status occurred

BIT 0 - Quasi Random Pattern Detection Interrupt Enable:

- 0 = No change
- 1 = Change in status occurred

TABLE 381: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN007)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ENROM	Reserved	Reserved	RSTALL	UPDATEALL	HI/LO	UPDATE	RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Enable ROM for LCV Counter:

This bit is used to enable data from an internal LCV counter to be read back.

- 0 = Disabled.
- 1 = Enabled.

BIT [6:5] - Reserved:

BIT 4 - Reset All Internal LCV Counters:

This bit is used to reset all 28 Internal LCV counters to their default state 0000h. This bit must be set High for a minimum of 1mS.

- 0 = Normal Operation
- 1 = Resets All LCV Counters

BIT 3 - Update All LCV Counters:

This bit is used to latch the contents of all 28 internal LCV counters so that the values can be read. When the HI/LO bit is set Low, initiating this update bit places the lower 8 bits of the 16-bit word in register 0xN011h. When the HI/LO bit is set High, initiating this update bit places the upper 8 bits of the 16-bit word in register 0xN010h.

- 0 = Normal Operation
- 1 = Updates All LCV Counters

BIT 2 - High Byte / Low Byte Select:

This bit is used to select which byte of the 16-bit LCV value will be placed in the read back registers.

- 0 = Lower Byte LCV[7:0]
- 1 = Upper Byte LCV[15:8]

BIT 1 - Update LCV Counter:

This bit is used to latch the contents of the internal LCV counter for this channel so that the value can be read. When the HI/LO bit is set Low, initiating this update bit places the lower 8 bits of the 16-bit word in register 0xN011h. When the HI/LO bit is set High, initiating this update bit places the upper 8 bits of the 16-bit word in register 0xN010h.

- 0 = Normal Operation
- 1 = Update LCV Counter

BIT 0 - Reset Internal LCV Counter:

This bit is used to reset the Internal LCV for this channel to its default state 0000h. This bit must be set High for a minimum of 1mS.

- 0 = Normal Operation
- 1 = Reset LCV Counter

TABLE 382: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN008)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S1	B5S1	B4S1	B3S1	B2S1	B1S1	B0S1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 1:

The transmit output pulse is divided into 8 individual segments. This register is used to program the first segment which corresponds to the overshoot of the pulse amplitude. There are four segments for the top portion of the pulse and four segments for the bottom portion of the pulse. Segment number 5 corresponds to the undershoot of the pulse. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**
  - 0 - Negative Direction
  - 1 - Positive Direction

TABLE 383: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN009)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S2	B5S2	B4S2	B3S2	B2S2	B1S2	B0S2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 2:

The transmit output pulse is divided into 8 individual segments. This register is used to program the second segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**
  - 0 - Negative Direction
  - 1 - Positive Direction

TABLE 384: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN00A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S3	B5S3	B4S3	B3S3	B2S3	B1S3	B0S3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 3:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Third segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**
  - 0 - Negative Direction
  - 1 - Positive Direction

TABLE 385: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN00B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S4	B5S4	B4S4	B3S4	B2S4	B1S4	B0S4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 4:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Fourth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**
  - 0 - Negative Direction
  - 1 - Positive Direction

TABLE 386: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN00C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S5	B5S5	B4S5	B3S5	B2S5	B1S5	B0S5
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 5:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Fifth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**
  - 0 - Negative Direction
  - 1 - Positive Direction

TABLE 387: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN00D)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S6	B5S6	B4S6	B3S6	B2S6	B1S6	B0S6
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 6:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Sixth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**
  - 0 - Negative Direction
  - 1 - Positive Direction

TABLE 388: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN00E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S7	B5S7	B4S7	B3S7	B2S7	B1S7	B0S7
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 7:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Seventh segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**
  - 0 - Negative Direction
  - 1 - Positive Direction

TABLE 389: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN00F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S8	B5S8	B4S8	B3S8	B2S8	B1S8	B0S8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 8:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Eighth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**
  - 0 - Negative Direction
  - 1 - Positive Direction

TABLE 390: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN010)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVHI7	LCVHI6	LCVHI5	LCVHI4	LCVHI3	LCVHI2	LCVHI1	LCVHI0
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT [7:0] - Internal LCV Counter High Byte:

Once the internal LCV counter has been enabled and updated, these bits contain the upper byte of the 16-bit LCV counter word.

TABLE 391: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN011)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVLO7	LCVLO6	LCVLO5	LCVLO4	LCVLO3	LCVLO2	LCVLO1	LCVLO0
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT [7:0] - Internal LCV Counter Low Byte:

Once the internal LCV counter has been enabled and updated, these bits contain the lower byte of the 16-bit LCV counter word.

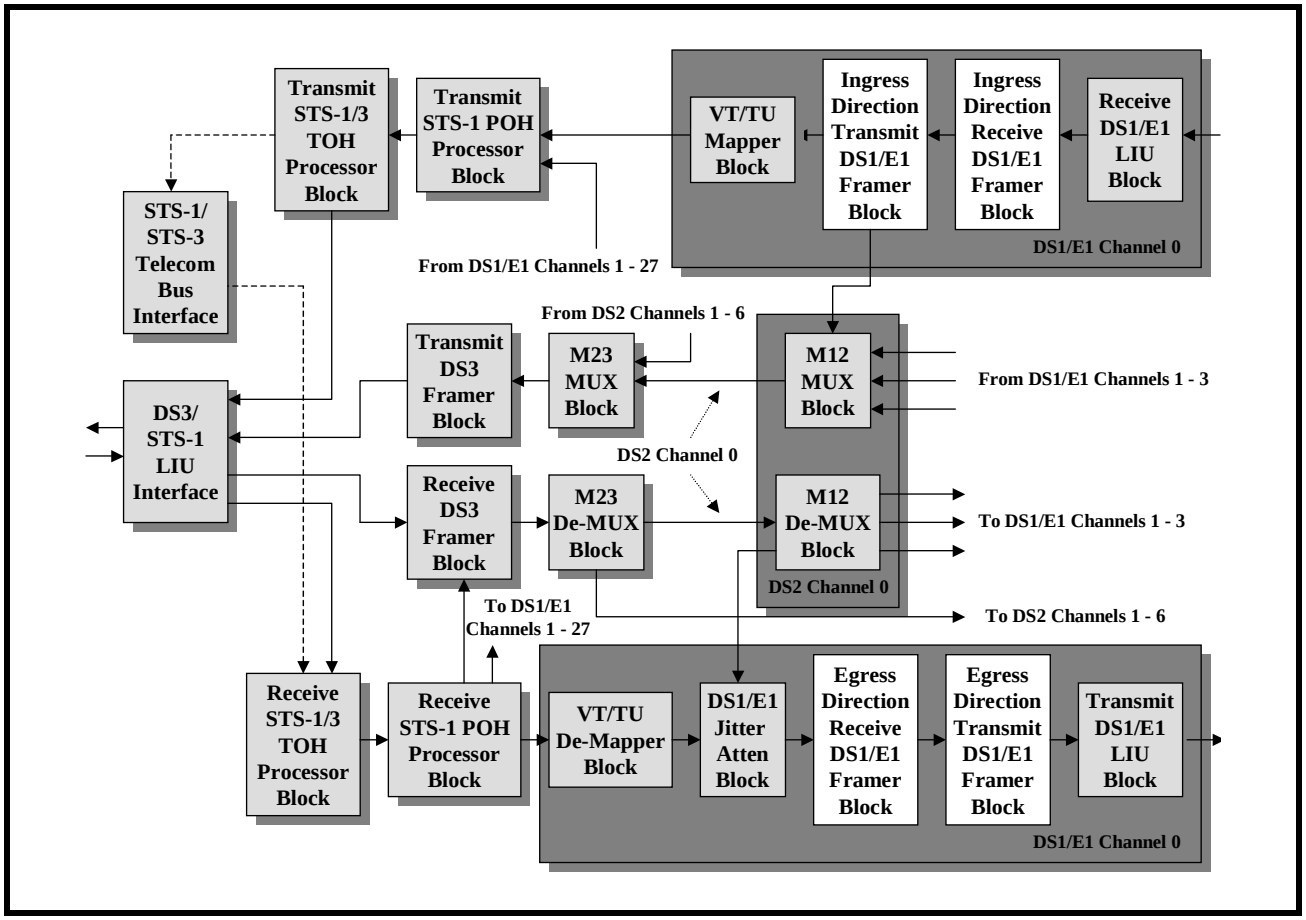
2.13 DS1/E1 FRAMER BLOCK REGISTERS - DS1 APPLICATIONS

The register map for the DS1/E1 Framer blocks (for DS1 Applications) is presented in the Table below. Additionally, a detailed description of each of the DS1/E1 Framer Block register is presented below.

NOTE: *The register map/description for the DS1/E1 Framer blocks (for E1 Applications) is presented in Section _.*

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328 device, with both the Ingress and Egress Direction Transmit/Receive DS1/E1 Framer blocks highlighted is presented below in Figure 17..

FIGURE 17. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328 DEVICE, WITH THE TRANSMIT/RECEIVE DS1/E1 FRAMER BLOCKS HIGHLIGHTED



SOME COMMENTS ABOUT ADDRESSING DS1/E1 FRAMER BLOCK REGISTERS

Throughout the XRT86SH328 Data Sheet, the user can control/monitor the function/performance of the T1/E1 Framer blocks consists of the following sets of Registers.

- Channel Control Registers
- Receive Signaling Array Registers
- LAPD Buffer 0 Data Registers
- LAPD Buffer 1 Data Registers
- Channel - Framer Performance Monitor Registers
- Channel - Framer Interrupt Register

In the XRT86SH328 Data Sheet, we indicate that the following sets of Register have the following Address Locations.

TABLE 392: MEMORY MAP - T1/E1 FRAMER BLOCK

ADDRESS LOCATION	REGISTER SET
0xN100 - 0xN1FF	Channel X - Control Registers
0xN200 - 0xN2FF	Reserved
0xN300 - 0xN3FF	Channel X - Channel Control Registers
0xN400 - 0xN4FF	Reserved
0xN500 - 0xN5FF	Channel X - Receive Signaling Array Registers
0xN600 - 0xN6FF	Channel X - LAPD Buffer 0 Data Register
0xN700 - 0xN7FF	Channel X - LAPD Buffer 1 Data Register
0xN800 - 0xN8FF	Reserved
0xN900 - 0xN9FF	Channel X - Framer Performance Monitor Registers
0xNA00 - 0xNAFF	Reserved
0xNB00 - 0xNBFF	Channel X - Framer Interrupt Registers

NOTE: *The XRT86SH328 has a total of 28 Ingress Direction Transmit/Receive DS1/E1 Framer blocks and 28 Egress Direction Transmit/Receive DS1/E1 Framer Blocks. Hence, the XRT86SH328 device contains a total of 56 Transmit/Receive DS1/E1 Framer blocks. Therefore, in Table _-1, the value of N can range in value from 0x01 to 0x38.*

OBVIOUS QUESTION: What value of N pertains to which of the 56 T1/E1 Framer blocks within the chip?

The answer to this question depends upon whether the XRT86SH328 has been configured to operate in the VT-Mapper (with T1/E1 Framing) or in the M13 MUX (with T1/E1 Framing) Mode. **Table 393** and **Table 394** present the values for N (for each T1/E1 Framer block) as a function of Channel Number and Signal Direction for VT- Mapper (with T1/E1 Framing) and M13 MUX (with T1/E1 Framing) applications, respectively. Further, **Figure 18** (which depicts an illustration of the various T1/E1 Framer blocks within a given channel) can be used as a point of reference when looking at **Table 393** and **Table 394**.

FIGURE 18. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328 DEVICE WITH BOTH THE INGRESS AND EGRESS DIRECTION T1/E1 FRAMER BLOCKS (OF A GIVEN T1/E1 CHANNEL) HIGHLIGHTED

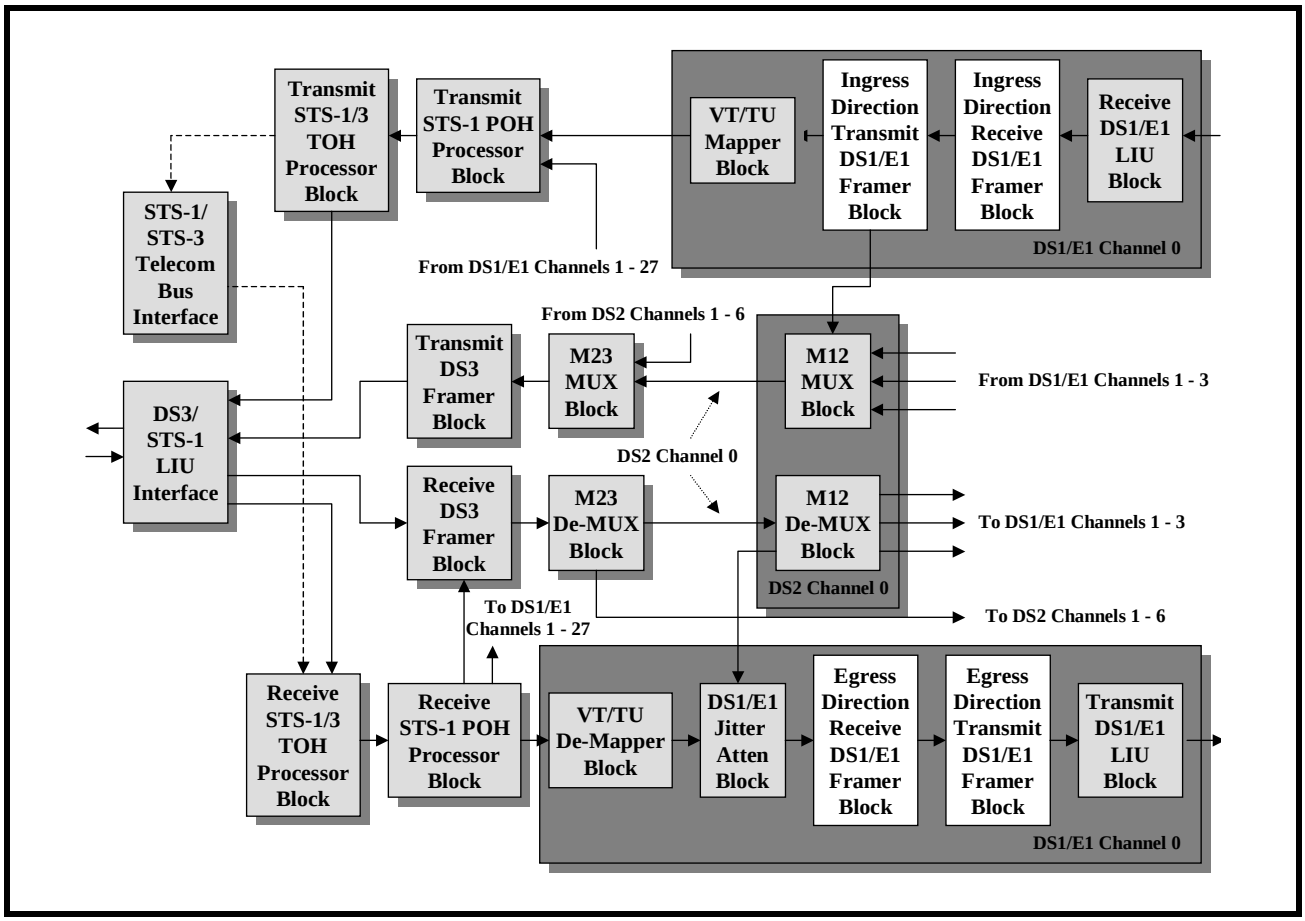


TABLE 393: RELATIONSHIP BETWEEN VALUE OF N AND CHANNEL NUMBER, SIGNAL DIRECTION - VT-MAPPER (WITH T1/E1 FRAMING) MODE APPLICATIONS

	INGRESS DIRECTION		EGRESS DIRECTION	
CHANNEL NUMBER	RECEIVE DS1/E1 FRAMER BLOCK	TRANSMIT DS1/E1 FRAMER BLOCK	RECEIVE DS1/E1 FRAMER BLOCK	TRANSMIT DS1/E1 FRAMER BLOCK
1	0x1D	0x01	0x01	0x1D
2	0x1E	0x02	0x02	0x1E
3	0x1F	0x03	0x03	0x1F
4	0x20	0x04	0x04	0x20
5	0x21	0x05	0x05	0x21
6	0x22	0x06	0x06	0x22
7	0x23	0x07	0x07	0x23
8	0x24	0x08	0x08	0x24
9	0x25	0x09	0x09	0x25

TABLE 393: RELATIONSHIP BETWEEN VALUE OF N AND CHANNEL NUMBER, SIGNAL DIRECTION - VT-MAPPER (WITH T1/E1 FRAMING) MODE APPLICATIONS

	INGRESS DIRECTION		EGRESS DIRECTION	
CHANNEL NUMBER	RECEIVE DS1/E1 FRAMER BLOCK	TRANSMIT DS1/E1 FRAMER BLOCK	RECEIVE DS1/E1 FRAMER BLOCK	TRANSMIT DS1/E1 FRAMER BLOCK
10	0x26	0x0A	0x0A	0x26
11	0x27	0x0B	0x0B	0x27
12	0x28	0x0C	0x0C	0x28
13	0x29	0x0D	0x0D	0x29
14	0x2A	0x0E	0x0E	0x2A
15	0x2B	0x0F	0x0F	0x2B
16	0x2C	0x10	0x10	0x2C
17	0x2D	0x11	0x11	0x2D
18	0x2E	0x12	0x12	0x2E
19	0x2F	0x13	0x13	0x2F
20	0x30	0x14	0x14	0x30
21	0x31	0x15	0x15	0x31
22	0x32	0x16	0x16	0x32
23	0x33	0x17	0x17	0x33
24	0x34	0x18	0x18	0x34
25	0x35	0x19	0x19	0x35
26	0x36	0x1A	0x1A	0x36
27	0x37	0x1B	0x1B	0x37
28	0x38	0x1C	0x1C	0x38

TABLE 394: RELATIONSHIP BETWEEN VALUE OF N AND CHANNEL NUMBER, SIGNAL DIRECTION - M13 MUX (WITH T1/E1 FRAMING) MODE APPLICATIONS

	INGRESS DIRECTION	EGRESS DIRECTION		
CHANNEL NUMBER	RECEIVE DS1/E1 FRAMER BLOCK	TRANSMIT DS1/E1 FRAMER BLOCK	RECEIVE DS1/E1 FRAMER BLOCK	TRANSMIT DS1/E1 FRAMER BLOCK
1	0x01	0x1D	0x1D	0x01
2	0x02	0x1E	0x1E	0x02
3	0x03	0x1F	0x1F	0x03
4	0x04	0x20	0x20	0x04
5	0x05	0x21	0x21	0x05
6	0x06	0x22	0x22	0x06

TABLE 394: RELATIONSHIP BETWEEN VALUE OF N AND CHANNEL NUMBER, SIGNAL DIRECTION - M13 MUX (WITH T1/E1 FRAMING) MODE APPLICATIONS

	INGRESS DIRECTION	EGRESS DIRECTION		
CHANNEL NUMBER	RECEIVE DS1/E1 FRAMER BLOCK	TRANSMIT DS1/E1 FRAMER BLOCK	RECEIVE DS1/E1 FRAMER BLOCK	TRANSMIT DS1/E1 FRAMER BLOCK
7	0x07	0x23	0x23	0x07
8	0x08	0x24	0x24	0x08
9	0x09	0x25	0x25	0x09
10	0x0A	0x26	0x26	0x0A
11	0x0B	0x27	0x27	0x0B
12	0x0C	0x28	0x28	0x0C
13	0x0D	0x29	0x29	0x0D
14	0x0E	0x2A	0x2A	0x0E
15	0x0F	0x2B	0x2B	0x0F
16	0x10	0x2C	0x2C	0x10
17	0x11	0x2D	0x2D	0x11
18	0x12	0x2E	0x2E	0x12
19	0x13	0x2F	0x2F	0x13
20	0x14	0x30	0x30	0x14
21	0x15	0x31	0x31	0x15
22	0x16	0x32	0x32	0x16
23	0x17	0x33	0x33	0x17
24	0x18	0x34	0x34	0x18
25	0x19	0x35	0x35	0x19
26	0x1A	0x36	0x36	0x1A
27	0x1B	0x37	0x37	0x1B
28	0x1C	0x38	0x38	0x1C

TABLE 395: T1 FRAMER BLOCK - CLOCK SELECT REGISTER (ADDRESS = 0XN100, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Set T1 Mode	Force all Channels to Sync to 8kHz	Unused			Clock Source Select[1:0]	
R/O	R/W	R/W	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	1

BIT7 - Reserved

BIT6 - Set T1 Mode:

This READ/WRITE bit-field is used to configure the Channel to operate in either the T1 or E1 Mode.

- 0 - Configures the Framer Channel to operate in the E1 Mode
- 1 - Configures the Framer Channel to operate in the T1 Mode

BIT 5 - Force all Channels to Sync to 8kHz:

This READ/WRITE bit-field is used to configure all active (either 28 or 56) Transmit DS1 Framer blocks to synchronize their transmit output frame alignment with the 8kHz signal that is derived from the MCLK PLL.

- 0 - Does not configure each of the Transmit DS1 Framer blocks to synchronize their transmit output frame alignment with the 8kHz signal (from the MCLK PLL).
- 1 - Configures each of the Transmit DS1 Framer blocks to synchronize their transmit output frame alignment with the 8kHz signal (from the MCLK PLL).

NOTE: *This feature should only be used if the XRT86SH328 has been configured to operate in the 28-Channel DS1 Framer/LIU Combo Mode. The user MUST NOT use this feature if the XRT86SH328 has been configured to operate in any of the Aggregation Modes.*

BIT [4:2] - Reserved

BIT [1:0] - Clock Source Select[1:0]:

These two READ/WRITE bit-fields is used to specify the timing source for the Ingress and Direction Transmit DS1 Framer block, within this particular channel.

The Relationship between the Clock Source Select[1:0] bit-fields and the resulting timing source for the Transmit DS1 Framer block, within this particular Channel

CLOCK SOURCE SELECT[1:0]	TIMING SOURCE FOR TRANSMIT DS1 FRAMER BLOCK
00	Loop-Timing Mode:The Transmit DS1 Framer block will derive its timing from the Received or Recovered Clock signal within the corresponding Receive DS1 Framer block.NOTE: This timing option is only available if the user has configured the XRT86SH328 to operate in the 28-Channel DS1 Framer/LIU Combo Mode
01	Local-Timing Mode (TxDS1CLK_n Input)The Transmit DS1 Framer block will either use up-stream timing or the TxDS1CLK_n input as its timing source.NOTE: For Aggregation Applications, the user MUST configure all active DS1 Framer blocks to operate in this timing mode.
10	Local-Timing Mode (MCLK PLL Input)The Transmit DS1 Framer block will derive its timing from the MCLK PLL.NOTE: This timing option is only available if the user has configured the XRT86SH328 to operate in the 28-Channel DS1 Framer/LIU Combo Mode.
11	Loop-Timing ModeThe Transmit DS1 Framer block will derive its timing from the Received or Recovered Clock signal within the corresponding Receive DS1 Framer blockNOTE: This timing option is only available if the user has configured the XRT86SH328 to operate in the 28-Channel DS1 Framer/LIU Combo Mode.

TABLE 396: T1 FRAMER BLOCK - LINE INTERFACE CONTROL REGISTER (ADDRESS = 0XN101, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit LOS Pattern	Reserved	Framer Loop-Back[1:0]		Reserved			
R/W	R/O	R/W	R/W	R/O	R/O	R/O	R/O
0	1	0	0	0	0	0	0

BIT7 - Transmit LOS Pattern:

This READ/WRITE bit-field configures the Transmit DS1 Framer block to generate and transmit the LOS Pattern to the remote terminal.

- 0 - Configures the Transmit DS1 Framer Block to transmit normal DS1 traffic
- 1 - Configures the Transmit DS1 Framer Block to transmit the LOS pattern.

NOTE: *The user MUST set this bit-field to 0 for Normal Operation.*

BIT6 - Reserved:

BIT [5:4] - Framer Loop-back[1:0]:

These two READ/WRITE bit-fields are used to configure the Transmit/Receive DS1 Framer blocks to operate in a variety of possible loop-back modes, as depicted in the Table below.

Relationship between the Framer Loop-back[1:0] bit-fields and the Corresponding Loop-Back Mode within the DS1 Framer block

FRAMER LOOP-BACK[1:0]	RESULTING LOOP-BACK MODE (WITHIN FRAMER BLOCK)
00	Normal Operation (No Loop-back) Mode
01	Local Loop-back Mode
10	Remote Loop-back Mode
11	Reserved

TABLE 397: T1 FRAMER BLOCK - FRAMING SELECT REGISTER (ADDRESS = 0XN107, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Signaling Update on Super Frame Boundaries	Force CRC Errors	Set J1 Mode	One & Only	Fast Sync	DS1 Framing Format Select[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Signaling Update on Super Frame Boundaries:

This READ/WRITE bit-field is used to either enable or disable Signaling Update on Super-Frame Boundaries, in both the Transmit and Receive Directions, as described below.

In the Receive Direction

If the user enables this feature, then signaling data will update (via the Receive Signaling Array Registers) only upon the Super-Frame Boundaries. If the user does NOT to enable this feature, then signaling data will be updated (within the Receive Signaling Array Registers) as soon as they are received within the incoming DS1 data-stream.

In the Transmit Direction

If the user enables this feature, then any signaling data that occur (within the Transmit Output DS1 data-stream) will be updated upon the Super-Frame boundaries. If the user does NOT to enable this feature, then signaling data (within the outbound DS1 data-stream) will be updated as soon as it is changed.

- 0 = Disables the Signaling Update on Super-Frame Boundaries features.
- 1 = Enables the Signaling Update on Super-Frame Boundaries features.

BIT6 - Force CRC Errors:

This READ/WRITE bit-field is used to force the Transmit DS1 Framer block to transmit CRC errors within the outbound DS1 data-stream.

- 0 = Configures the Transmit DS1 Framer block to transmit DS1 data with correct CRC values

- 1 = Configures the Transmit DS1 Framer block to transmit DS1 data with erred CRC values.

NOTE: *The Transmit DS1 Framer block will transmit DS1 data, with erred CRC values, for the duration that this bit-field is set to 1.*

BIT 5 - Set J1 Mode:

This READ/WRITE bit-field, along with BIT6 (Set T1 Mode) within the T1/E1 Framer Block - Clock Select Register (Address = 0xN100) is used to configure the Channel to operate in the J1 Mode.

The Relationship between the States of the Set T1 Mode and the Set J1 Mode bit-fields and the Corresponding Mode of Channel

SET J1 MODE	SET T1 MODE (BIT6 IN 0XN100)	OPERATING MODE OF CHANNEL
0	0	E1 Mode
0	1	T1 Mode
1	0	E1 Mode
1	1	J1 Mode

BIT 4 - One & Only:

BIT 3 - Fast Sync:

BIT [2:0] - DS1 Framing Format Select[2:0]:

These three READ/WRITE bit-fields is used to select the Framing format that the DS1 Framer Channel will operate ini.

The Relationship between the state of the DS1 Framing Format Select[2:0] bits and the resulting Framing format of the channel

DS1 FRAMING FORMAT SELECT[2:0]	RESULTING FRAMING FORMAT
0XX	DS1, ESF - Extended Super-Frame
100	Do Not Use
101	DS1, SF - Super-Frame
11X	Do Not Use

TABLE 398: T1 FRAMER BLOCK - ALARM GENERATION REGISTER (ADDRESS = 0XN108, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Yellow Alarm - One Second Rule	Transmit Yellow Alarm	Yellow Alarm Format[1:0]		Transmit AIS Pattern Select[1:0]		AIS Defect Declaration Criteria[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Yellow Alarm - One Second Rule:

This READ/WRITE bit-field is used to configure the Transmit DS1 Framer to transmit the RAI (or Yellow Alarm) indicator per the One Second Rule (as described in the ANSI standards).

Transmission of the RAI Indicator per the One Second Rule

If the user invokes the One Second Rule, then the following will happen.

- Whenever the Transmit DS1 Framer block generates and transmits the RAI indicator, it will do so for at least one second (for both the ESF and the SF framing formats)

- The Transmit DS1 Framer block will insure that there is a minimum of a one-second delay between the time that it terminates transmission of the RAI indicator, and the instant that it proceeds to transmit the RAI indicator again.

Transmission of the RAI Indicator when the One Second Rule is NOT in-force

If the user does NOT invoke the One Second Rule, then the following will happen.

- Whenever the Transmit DS1 Framer block generates and transmits the RAI indicator, it will do so for at least one second (for both the ESF and the SF framing formats).
- The Transmit DS1 Framer block will NOT insure that there is a minimum of a one-second delay between the time that it terminates transmission of the RAI indicator, and the instant that it proceeds to transmit the RAI indicator again.

▶ 0 = Does not configure the Transmit DS1 Framer block to transmit the RAI indicator per the One Second Rule.

▶ 1 = Configures the Transmit DS1 Framer block to transmit the RAI indicator per the One Second Rule.

BIT6 - Transmit Yellow Alarm:

BIT [5:4] - Yellow Alarm Format[1:0]:

BIT [3:2] - Transmit AIS Pattern Select[1:0]:

These two READ/WRITE bit-fields serves the following two functions.

- To command the Transmit DS1 Framer block to transmit the AIS indicator (per Software Command), and
- To specify the type of AIS Pattern that the Transmit DS1 Framer block will transmit, whenever it has been commanded to transmit the AIS indicator to the remote terminal equipment.

The Relationship between Transmit AIS Pattern Select[1:0] and the resulting behavior of the Transmit DS1 Framer block

TRANSMIT AIS PATTERN SELECT[1:0]	TRANSMIT DS1 FRAMER BLOCK ACTION
00/10	Transmits Normal TrafficTransmit DS1 Framer block does not transmit the AIS indicator. It will (instead) transmit normal traffic
01	Unframed All Ones PatternThe Transmit DS1 Framer block will transmit an Unframed All Ones Pattern (as an AIS pattern) for the duration that these bit-fields are set to [0, 1].
11	Framed All Ones PatternThe Transmit DS1 Framer block will transmit a Framed All Ones Pattern (as an AIS pattern) for the duration that these bit-fields are set to [1, 0].

BIT [1:0] - AIS Defect Declaration Criteria[1:0]:

These two READ/WRITE bit-fields are used to select the type of AIS Pattern that the Receive DS1 Framer block will look for in order to determine whether or not it should declare or clear the AIS defect condition

The Relationship between AIS Defect Declaration Criteria[1:0] and the resulting AIS Pattern that the Receive DS1 Framer block will look for in declaring/clearing the AIS defect condition

AIS DEFECT DECLARATION CRITERIA[1:0]	RECEIVE DS1 FRAMER BLOCK - AIS DEFECT DECLARATION CRITERIA
00/10	AIS Defect Declaration is DisabledThe Receive DS1 Framer block will NOT declare the AIS defect condition at all.
01	Unframed and Framed All Ones Pattern:The Receive DS1 Framer block will declare the AIS defect condition whenever it receives either the Framed or Unframed All Ones pattern for at least 42ms.
11	Framed All Ones Pattern:The Receive DS1 Framer block will only declare the AIS defect condition whenever it receives the Framed All Ones Pattern for at least 42ms.

TABLE 399: T1 FRAMER BLOCK - SYNCHRONIZATION MUX REGISTER (ADDRESS = 0XN109, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						CRC-6 Source Select	Framing Bits Source Select
R/O	R/W	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:2] - Reserved

BIT 1 - CRC-6 Source Select:

This READ/WRITE bit-field is used to specify the source of the CRC-6 bits, within the outbound DS1 data-stream.

- 0 = Configures the Transmit DS1 Framer block to internally compute and insert the CRC-6 bits within the outbound DS1 data-stream.
- 1 = Configures the Transmit DS1 Framer block to externally accept data from the TxDS1DATA_n input pin (or from upstream circuitry) and to insert this data into the CRC-6 bit-fields within the outbound DS1 data-stream.

BIT 0 - Framing Bits Source Select:

This READ/WRITE bit-field is used to specify the source of the Framing bits, within the outbound DS1 data-stream.

- 0 = Configures the Transmit DS1 Framer block to internally generate and insert the Framing bits within the outbound DS1 data-stream
- 1 = Configures the Transmit DS1 Framer block to externally accept data from the TxDS1DATA_n input pin (or from upstream circuitry) and to insert this data into the Framing bit-fields within the outbound DS1 data-stream.

TABLE 400: T1 FRAMER BLOCK - TRANSMIT DATA LINK SELECT REGISTER (ADDRESS = 0XN10A, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Transmit Data Link Band-width[1:0]		Transmit D/E Time Source Select[1:0]		Transmit Data Link Source Select[1:0]	
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Reserved:

BIT [5:4] - Transmit Data Link Bandwidth[1:0]:

These two READ/WRITE bit-fields are used to select the Data Link Bandwidth (for the transmission of Data Link Messages) within the outbound DS1 data-stream. Data Link Messages can be transmitted at a rate of either 4kHz or 2kHz.

The Relationship between Transmit Data Link Bandwidth[1:0] and the resulting Bits/Bandwidth available for the transport of Data Link Messages within the outbound DS1 data-stream

TRANSMIT DATA LINK BANDWIDTH[1:0]	RESULTING BANDWIDTH AVAILABLE TO TRANSPORT DATA LINK MESSAGES WITHIN OUTBOUND DS1 DATA-STREAM
00	Data Link Bandwidth = 4kHzData Link Messages are being transported via every single DL bit-field within the outbound DS1 data-stream
01	Data Link Bandwidth = 2kHz (Frames 1, 5, 9, ….)Data Link Messages are being trans-ported via every other DL bit-field within the outbound DS1 data-stream.

The Relationship between Transmit Data Link Bandwidth[1:0] and the resulting Bits/Bandwidth available for the transport of Data Link Messages within the outbound DS1 data-stream

TRANSMIT DATA LINK BANDWIDTH[1:0]	RESULTING BANDWIDTH AVAILABLE TO TRANSPORT DATA LINK MESSAGES WITHIN OUTBOUND DS1 DATA-STREAM
10	Data Link Bandwidth = 2kHz (Frames 3, 7, 11,…)Data Link Messages are being transported via every other DL bit-field within the outbound DS1 data-stream.
11	Do not use

NOTE: *This bit-field only applies if the channel has been configured to operate in the T1-ESF Framing format.*

BIT [3:2] - Transmit D/E Time Source Select[1:0]:

These two READ/WRITE bit-fields are used to specify the source of the data that is to be transported via the D/E time-slots within the outbound Transmit DS1 Data-stream.

The Relationship between Transmit D/E Time Source Select[1:0] and the resulting source of the D/E-Time-Slot data within the outbound DS1 data-stream

TRANSMIT D/E TIME SOURCE SELECT[1:0]	SOURCE FOR TRANSMIT D/E TIME-SLOT DATA
00	Upstream Circuitry (for Aggregation Applications) or the TxDS1DATA_n input (for 28-Channel DS1 Framer/LIU Combo Mode applications).
01	The Transmit LAPD Controller Block
10	Reserved - Do NOT Use
11	

NOTE: *These two register bits are only active if the user has configured one of the Time-Slots (within the outbound DS1 data-stream) to function as the D/E Channel.*

BIT [1:0] - Transmit Data Link Source Select[1:0]:

These two READ/WRITE bit-fields are used to specify the source for the data that will be transported via the Data Link bits, within the outbound DS1 data-stream.

The Relationship between Transmit Data Link Source Select[1:0] and the Resulting source of the data (which is to be transported via the Data Link bits, within the outbound DS1 data-stream)

TRANSMIT DATA LINK SOURCE SELECT[1:0]	RESULTING SOURCE OF DATA LINK DATA
00	Transmit LAPD Controller Block (within the Transmit DS1 Framer block)
01	Upstream Circuitry (for Aggregation Applications) or the TxDS1DATA_n input (for 28-Channel DS1 Framer/LIU Combo Mode Applications)
10	Reserved
11	Data Link Bits are each Forced to 1.

TABLE 401: T1 FRAMER BLOCK - FRAMING CONTROL REGISTER (ADDRESS = 0XN10B, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reframe	Framing with CRC Checking	LOF Tolerance[2:0]			LOF Range[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	0	0

BIT7 - Reframe:

This READ/WRITE bit-field is used to command a Reframe to the Receive DS1 Framer block. A 0 to 1 transition (within this bit-field) will force the Receive DS1 Framer block to restart the frame synchronization process. The Receive DS1 Framer block will automatically clear this bit-field to 0 once it has reacquired frame synchronization with the incoming DS1 data-stream.

BIT6 - Framing with CRC Checking:

This READ/WRITE bit-field is used to configure the Receive DS1 Framer block to also include checking for correct CRC-6 values as a part of In-Frame Declaration criteria. More specifically, if the user enables this feature, then the Receive DS1 Framer block will also check and verify that the incoming DS1 data-stream contains correct CRC data, prior to declaring the In-Frame condition.

- 0 = CRC Verification is NOT included in the Framing Alignment process.
- 1 = The Receive DS1 Framer block will also check for correct CRC values prior to declaring the In-Frame condition.

BIT [5:3] - LOF Tolerance[2:0]:

NOTE: *These READ/WRITE bit-fields along with the LOF Range[2:0] bit-fields are used to define the LOF Defect Declaration criteria. The Receive DS1 Framer block will declare the LOF defect condition anytime it detects LOF_Tolerance[2:0](or more) framing bit errors, within any sliding window (consisting of LOF_Range[2:0] framing The recommended value for LOF_Tolerance[2:0] is 2.*

BIT [2:0] - LOF Range[2:0]:

These READ/WRITE bit-fields along with the LOF_Tolerance[2:0] bit-fields are used to define the LOF Defect Declaration criteria. The Receive DS1 Framer block will declare the LOF defect condition anytime it detects LOF_Tolerance[2:0] (or more) framing bit errors, within any sliding window (consisting of LOF_Range[2:0] framing alignments) within the incoming DS1 data-stream.

TABLE 402: T1 FRAMER BLOCK - RECEIVE SIGNALING & DATA LINK SELECT REGISTER (ADDRESS = 0XN10C, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Receive Data Link Bandwidth[1:0]		Receive D/E Time-Slot Destination Select[1:0]		Receive Data-Link Destination Select[1:0]	
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Reserved:

BIT [5:4] - Received Data Link Bandwidth[1:0]:

These two READ/WRITE bit-fields is used to select the Data Link Bandwidth (for the reception of Data Link Messages) within the incoming DS1 data-stream. Data Link Messages can be received at a rate of either 4kHz or 2kHz.

The Relationship between Receive Data Link Bandwidth[1:0] and the resulting Bits/Bandwidth available for the transport of Data Link Messages within the incoming DS1 data-stream

RECEIVE DATA LINK BANDIDTH[1:0]	RESULTING BANDWIDTH AVAILABLE TO TRANSPORT DATA LINK MESSAGES WITHIN INCOMING DS1 DATA-STREAM
00	Data Link Bandwidth = 4kHzData Link Messages are being transported via every single DL bit-field within the incoming DS1 data-stream
01	Data Link Bandwidth = 2kHz (Frames 1, 5, 9, ….)Data Link Messages are being transported via every other DL bit-field within the incoming DS1 data-stream.
10	Data Link Bandwidth = 2kHz (Frames 3, 7, 11,…)Data Link Messages are being transported via every other DL bit-field within the incoming DS1 data-stream.
11	Do not use

NOTE: *This bit-field only applies if the channel has been configured to operate in the T1-ESF Framing format.*

BIT [3:2] - Receive D/E Time-Slot Destination Select[1:0]:

These two READ/WRITE bit-fields are used to specify the source of the data that is to be transported via the D/E time-slots within the incoming Receive DS1 Data-stream.

The Relationship between Receive D/E Time Source Select[1:0] and the resulting source of the D/E-Time-Slot data within the incoming DS1 data-stream

RECEIVE D/E TIME SOURCE SELECT[1:0]	DESTINATION OF THE INCOMING RECEIVE D/E TIME-SLOT DATA
00	Downstream Circuitry (for Aggregation Applications) or the RxDS1DATA_n output (for 28-Channel DS1 Framer/LIU Combo Mode applications).
01	The Receive LAPD Controller Block
10	Reserved - Do NOT Use
11	

NOTE: *These two register bits are only active if the user has configured one of the Time-Slots (within the incoming DS1 data-stream) to function as the D/E Channel.*

BIT [1:0] - Receive Data Link Destination Select[1:0]:

These two READ/WRITE bit-fields are used to specify the source for the data that will be transported via the Data Link bits, within the incoming DS1 data-stream.

The Relationship between Receive Data Link Source Select[1:0] and the Resulting source of the data (which is to be transported via the Data Link bits, within the incoming DS1 data-stream)

TRANSMIT DATA LINK SOURCE SELECT[1:0]	RESULTING DESTINATION OF DATA LINK DATA
00	Receive LAPD Controller Block (within the Receive DS1 Framer block)
01	Downstream Circuitry (for Aggregation Applications) or the RxDS1DATA_n output (for 28-Channel DS1 Framer/LIU Combo Mode Applications)
10	Reserved
11	Data Link Bits are ignored

TABLE 403: T1 FRAMER BLOCK - RECEIVE SIGNALING CHANGE REGISTER - 0 (ADDRESS = 0XN10D, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Signaling Change - Channel 0	Receive Signaling Change - Channel 1	Receive Signaling Change - Channel 2	Receive Signaling Change - Channel 3	Receive Signaling Change - Channel 4	Receive Signaling Change - Channel 5	Receive Signaling Change - Channel 6	Receive Signaling Change - Channel 7
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Signaling Change - Channel n=[0:7]:

These RESET-upon-READ bit-fields indicate whether the Channel Associated Signaling data associated with Time-Slots 0 through 7 (within the incoming DS1 data-stream) has changed since the last read of this register.

- 0 = Indicates that CAS data (for Time-Slots 0 through 7) has NOT changed since the last read of this register.
- 1 = Indicates that CAS data (for Time-Slots 0 through 7) has changed since the last read of this register.

NOTE: *This register is only active if the incoming DS1 data-stream is using Channel Associated Signaling.*

TABLE 404: T1 FRAMER BLOCK - RECEIVE SIGNALING CHANGE REGISTER - 1 (ADDRESS = 0XN10E, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Signaling Change - Channel 8	Receive Signaling Change - Channel 9	Receive Signaling Change - Channel 10	Receive Signaling Change - Channel 11	Receive Signaling Change - Channel 12	Receive Signaling Change - Channel 13	Receive Signaling Change - Channel 14	Receive Signaling Change - Channel 15
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Signaling Change - Channel n=[8:15]:

These RESET-upon-READ bit-fields indicate whether the Channel Associated Signaling data associated with Time-Slots 8 through 15 (within the incoming DS1 data-stream) has changed since the last read of this register.

- 0 = Indicates that CAS data (for Time-Slots 8 through 15) has NOT changed since the last read of this register.
- 1 = Indicates that CAS data (for Time-Slots 8 through 15) has changed since the last read of this register.

TABLE 405: T1 FRAMER BLOCK - RECEIVE SIGNALING CHANGE REGISTER - 2 (ADDRESS = 0XN10F, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Signaling Change - Channel 16	Receive Signaling Change - Channel 17	Receive Signaling Change - Channel 18	Receive Signaling Change - Channel 19	Receive Signaling Change - Channel 20	Receive Signaling Change - Channel 21	Receive Signaling Change - Channel 22	Receive Signaling Change - Channel 23
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - Receive Signaling Change - Channel n=[16:23]:

These RESET-upon-READ bit-fields indicate whether the Channel Associated Signaling data associated with Time-Slots 16 through 23 (within the incoming DS1 data-stream) has changed since the last read of this register.

- 0 = Indicates that CAS data (for Time-Slots 16 through 23) has NOT changed since the last read of this register.
- 1 = Indicates that CAS data (for Time-Slots 16 through 23) has changed since the last read of this register.

NOTE: This register is only active if the incoming DS1 data-stream is using Channel Associated Signaling.

TABLE 406: T1 FRAMER BLOCK - RECEIVE EXTRA-BITS REGISTER (ADDRESS = 0XN112, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
In Frame State	Reserved						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT7 - In Frame State:

This READ-ONLY bit-field indicates whether or not the Receive DS1 Framer block is currently declaring the In-Frame condition within the incoming DS1 data-stream.

- 0 = Indicates that the Receive DS1 Framer block is currently declaring the LOF (Loss of Frame) defect condition.
- 1 = Indicates that the Receive DS1 Framer block is currently declaring itself to be in the In-Frame condition.

BIT [6:0] - Reserved

TABLE 407: T1 FRAMER BLOCK - DATA LINK CONTROL REGISTER (ADDRESS = 0XN113, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	MOS Abort Disable	Rx_FCS_DIS	AutoRx	Tx_ABORT	Tx_IDLE	Tx_FCS_EN	MOS/BOS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved

BIT6 - MOS Abort Disable:

This bit is used to either enable or disable the automatic MOS abort feature within the transmit HDLC controller. If the user enables this feature, then the transmit HDLC controller will automatically transmit the abort sequence (e.g., a zero followed by a string of 7 consecutive 1's) whenever it abruptly transitions from transmitting a MOS type of message to transmitting a BOS type of message.

- 0 = Enables the Automatic MOS Abort feature
- 1 = Disabled

BIT 5 - Receive Frame Check Sequence Disable:

This bit is used to configure the receive HDLC controller to compute and verify the FCS value within each incoming LAPD message frame.

- 0 = Enables FCS Verification
- 1 = Disabled

BIT 4 - Auto Receive:

This bit configures the receive HDLC controller to discard any incoming BOS or LAPD message frame that exactly match which is currently stored in the receive HDLC buffer.

- 0 = Disabled
- 1 = Enables this auto discard feature

BIT 3 - Transmit Abort:

This bit configures the transmit HDLC controller to transmit an abort sequence (string of 7 or more consecutive 1's) to

the remote terminal.

- 0 = Disabled
- 1 = Transmit the abort sequence

BIT 2 - Transmit Idle (Flag Sequence Byte):

This bit configures the transmit HDLC controller to unconditionally transmit a repeating string of flag sequence octets (0x7E) in the data link channel to the remote terminal. In normal conditions, the transmit HDLC controller will repeatedly transmit the flag sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this transmit idle sequence feature, then the transmit HDLC controller will UNCONDITIONALLY transmit a repeating stream of the flag sequence octet (thereby overwriting all outbound MOS data link messages).

- 0 = Disabled
- 1 = Transmit a repeating string of Flag Sequence Octets (0x7E)

NOTE: *This bit is ignored if the transmit HDLC controller is operating in the BOS mode (bit 0 within this register is set to 0).*

BIT 1 - Transmit Frame Check Sequence Enable:

This bit is used to configure the transmit HDLC controller to compute and append FCS octets to the back end of each outbound MOS data link message.

- 0 = Disabled
- 1 = Compute and append the FCS octets to the back end of each outbound MOS data link message

NOTE: *This bit is ignored if the transmit HDLC controller ahs been configured to operate in the BOS mode - BIT 0 within this register is set to 0).*

BIT 0 - MOS / BOS:

This bit is used to configure transmit and receive the HDLC to be transmitting and receiving either BOS (bit oriented signaling) or MOS (message oriented signaling) frames.

- 0 = Transmit and Receive BOS Messages
- 1 = Transmit and Receive MOS Messages

TABLE 408: T1 FRAMER BLOCK - TRANSMIT DATA LINK CONTROL REGISTER (ADDRESS = 0XN114, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxHDLC BUFAVAIL	Transmit HDLC Message Byte Count						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Transmit HDLC Buffer Available:

This bit has different functions depending upon whether the user is writing to or reading from this register.

If User is Writing Data Into This Register Bit

- 0 = Configures the transmit HDLC controller to read out and transmit the data, residing within the transmit HDLC buffer 0 via the data link channel to the remote terminal equipment.
- 1 = Configures the transmit HDLC controller to read out and transmit the data, residing within the transmit HDLC buffer 1 via the data link channel to the remote terminal equipment.

If User is Reading Data From This Register Bit

- 0 = Indicates that transmit buffer 0 is the next available buffer. In this case, to write in the contents of a new outbound data link message into the transmit HDLC message buffer, the message should be written into buffer 0.
- 1 = Indicates that transmit buffer 1 is the next available buffer. In this case, to write in the contents of a new outbound data link message into the transmit HDLC message buffer, the message should be written into buffer 1.

NOTE: If one of these transmit HDLC buffers contain a message which has yet to be completely read in and processed for transmission by the transmit HDLC controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in use buffer is not permitted.

BIT [6:0] - Transmit HDLC Message Byte Count:

The exact function of these bits depends on whether the transmit HDLC controller is configured to transmit MOS or BOS messages to the remote terminal equipment.

In BOS Mode:

These bit fields contain the number of repetitions the BOS message must be transmitted before the transmit HDLC controller generates the transmit end of transfer (TxEOT) interrupt and halts transmission. If these fields are set to 0000000, then the BOS message will be transmitted for an indefinite number of times.

In MOS Mode:

These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, and Control Field. However, it does not include the FCS bytes.

TABLE 409: T1 FRAMER BLOCK - RECEIVE DATA LINK CONTROL REGISTER (ADDRESS = 0XN115, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RBUFPTR	Receive HDLC Message Byte Count						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Receive HDLC Buffer Pointer:

This bit identifies which receive HDLC buffer contains the most recently received HDLC message.

- 0 = Indicates that receive HDLC buffer 0 contains the contents of the most recently received HDLC message.
- 1 = Indicates that receive HDLC buffer 1 contains the contents of the most recently received HDLC message.

BIT [6:0] - Receive HDLC Message Byte Count:

The exact function of these bits depends on whether the receive HDLC controller is configured to receive MOS or BOS messages.

In BOS Mode:

These seven bits contain the number of repetitions the BOS message must be received before the receive HDLC controller generates the receive end of transfer (RxEOT) interrupt. If these bits are set to 0000000, the message will be received indefinitely and no RxEOT interrupt will be generated.

In MOS Mode:

These seven bits contain the size in bytes of the HDLC message that has been received and written into the receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control Field, and the FCS bytes.

TABLE 410: T1 FRAMER BLOCK - CUSTOMER INSTALLATION ALARM GENERATION REGISTERS (ADDRESS = 0XN11C, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Customer Installation Alarm Generation[1:0]		Customer Installation Alarm Detection[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [3:2] - CI Alarm Transmit (Only in ESF)

These two bits are used to enable or disable AIS-CI or RAI-CI generation in T1 ESF mode only. AIS-CI and RAI-CI are

intended for use in a network to differentiate between an issue within the network or the Customer Installation (CI).

AIS-CI

AIS-CI is an all ones with an embedded signature of 01111100 11111111 (right-to-left) which recurs at 386 bit intervals in the DS-1 signal.

RAI-CI

Remote Alarm Indication (RAI-CI) is a repetitive pattern with a period of 1.08 seconds. It comprises 0.99 seconds of RAI message (00000000 11111111 right-to-left) and a 90 ms of RAI-CI signature (00111110 11111111 right-to-left) to form an RAI-CI signal.

- 00/11 = Disabled
- 01 = Enables unframed AIS-CI alarm generation
- 10 = Enables RAI-CI alarm generation

BIT [1:0] - CI Alarm Detect (Only in ESF)

These two bits are used to enable or disable AIS-CI or RAI-CI alarm detection in T1 ESF only.

- 00/11 = Disabled
- 01 = Enables unframed AIS-CI alarm detection
- 10 = Enables RAI-CI alarm detection

TABLE 411: T1 FRAMER BLOCK - DS1 TEST REGISTER - 2 (ADDRESS = 0XN121, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset by Register	Unused			PRBS Switch	BER Control[1:0]		Unframed PRBS
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reset by Register:

This READ/WRITE bit-field is used to execute a Software RESET to the T1/E1 Framer block, within a given channel.

- 0 = Configures the T1/E1 Framer block to operate normally.
- 1 = Configures the T1/E1 Framer block (of the corresponding channel) to operate in the Software RESET condition.

NOTE: *Once the T1/E1 Framer block exits the Software RESET state, it will automatically clear this bit-field to 0.*

BIT [6:4] - Reserved

These bits are reserved

BIT 3 - PRBS Switch:

This READ/WRITE bit-field is used to specify the direction that the PRBS Pattern will be transmitted.

- 0 = PRBS Pattern will be generated and transmitted towards Transmit Output of the Transmit DS1 Framer block. This PRBS Pattern will also be monitored at the Receive Input of the corresponding Receive DS1 Framer block.
- 1 = PRBS Pattern will be generated and transmitted towards the System Side Output of the Receive DS1 Framer block. This PRBS Pattern will also be monitored at the System-Side Input of the Transmit DS1 Framer block.

BIT [2:1] BER Control[1:0]:

These READ/WRITE bit-fields is used to configure the PRBS Generator (within the Transmit DS1 Framer block) to insert BIT-Errors.

Resulting Errors Generated by the PRBS Generator

BER CONTROL[1:0]	RESULTING ERRORS GENERATED BY THE PRBS GENERATOR
00	No Bit Error Inserted

Resulting Errors Generated by the PRBS Generator

BER CONTROL[1:0]	RESULTING ERRORS GENERATED BY THE PRBS GENERATOR
01	1 Erred bit per 1,000 bits is inserted
10	1 Erred bit per 1,000,000 bits is inserted
11	No Bit Error Inserted

BIT 0 - Unframed PRBS:

This READ/WRITE bit-field is used to configure the Transmit DS1 Framer block to generate and transmit either a framed or unframed PRBS Pattern. Likewise, this bit-field also configures the corresponding Receive DS1 Framer block to expect either a framed or unframed PRBS pattern.

- 0 = Transmit and Receive DS1 Framer block will handle framed PRBS Pattern.
- 1 = Transmit and Receive DS1 Framer block will handle unframed PRBS Pattern.

TABLE 412: T1 FRAMER BLOCK - DS1 TEST REGISTER - 1 (ADDRESS = 0XN123, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS Type	Error Insert	Data Invert	Receive PRBS Lock	Receive PRBS Enable	Transmit PRBS Enable	Receive DS1 By Pass	Transmit DS1 By Pass
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - PRBS Type:

This READ/WRITE bit-field is used to specify the type of random pattern that the PRBS Generator and PRBS Receiver will handle.

- 0 = A PRBS Pattern with the Polynomial of X^15 + X^14 + 1.
- 1 = A QRTS Pattern

BIT6 - Error Insert:

This READ/WRITE bit-field is used to configure the PRBS Generator to insert a single bit-error into the outbound PRBS data-stream.

- A 0 to 1 transition, within this bit-field causes the PRBS Generator to insert a single bit-error into the outbound PRBS data-stream.

BIT 5 - Data Invert:

This READ/WRITE bit-field is used to (1) configure the PRBS Generator to invert all of its outbound traffic (as it generates and transmits this data), and (2) configures the PRBS Receiver to invert all of the incoming PRBS pattern data prior to processing.

- 0 = No Inversion by either the PRBS Generator or the PRBS Receiver
- 1 = Configures Inversion by both the PRBS Generator and PRBS Receiver

BIT 4 - Receive PRBS Lock:

This READ-ONLY bit-field indicates whether or not the PRBS Receiver is currently declaring PRBS Lock with the incoming PRBS data-stream.

- 0 = PRBS Receiver is NOT currently declaring PRBS Lock.
- 1 = PRBS Receiver is CURRENTLY declaring PRBS Lock.

BIT 3 - Receive PRBS Detection/Generation Enable:

This READ/WRITE bit-field is used to either enable or disable the PRBS Receiver.

- 0 = Disables the PRBS Receiver

- 1 = Enables the PRBS Receiver

BIT 2 - Transmit PRBS Generation Enable:

This READ/WRITE bit-field is used to either enable or disable the PRBS Generator.

- 0 = Disables the PRBS Generator
- 1 = Enables the PRBS Generator

BIT 1 - Receive DS1 By-Pass:

This bits enables the receive T1 Framer Bypass Mode

- 0 = Disabled
- 1 = Enables Receive Framer Bypass

BIT 0 - Transmit DS1 By-Pass:

This bits enables the transmit T1 Framer Bypass Mode

- 0 = Disabled
- 1 = Enables Transmit Framer Bypass

TABLE 413: T1 FRAMER BLOCK - LOOP-BACK CODE CONTROL REGISTER - CODE 0(ADDRESS = 0XN124, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Code Activation Length[1:0]		Receive Loop-Back Code Deactivation Length[1:0]		Transmit Loop-back Code Length[1:0]		Framed Loop-Back Code	Loop-Back Automati-cally
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Receive Loop-Back Code Activation Length[1:0]:

These two READ/WRITE bit-fields are used to specify the length of the loop-back activation code that the Receive DS1 Framer block will will use (for Code 0).

Receive Loop-Back Code Activation Length

RECEIVE LOOP-BACK CODE ACTIVATION LENGTH[1:0]	LENGTH
00	4 Bit Sequence
01	5 Bit Sequence
10	6 Bit Sequence
11	7 Bit Sequence

BIT [5:4] - Receive Loop-Back Code Deactivation Length[1:0]:

These two READ/WRITE bit-fields are used to specify the length of the loop-back deactivation code that the Receive DS1 Framer block will use (for Code 0).

Receive Loop-Back Code De-activation Length

RECEIVE LOOP-BACK CODE DE-ACTIVATION LENGTH[1:0]	LENGTH
00	4 Bit Sequence
01	5 Bit Sequence

Receive Loop-Back Code De-activation Length

RECEIVE LOOP-BACK CODE DE-ACTIVATION LENGTH[1:0]	LENGTH
10	6 Bit Sequence
11	7 Bit Sequence

BIT [3:2] - Transmit Loop-Back Code Length[1:0]:

These two READ/WRITE bit-fields are used to specify the length of the loop-back codes that the Transmit DS1 Framer block will transmit to the remote terminal equipment anytime the user commands it to transmit the User-Specified Loop-code to the remote terminal equipment..

Transmit Loop-Back Code Length

TRANSMIT LOOP-BACK CODE LENGTH[1:0]	LENGTH
00	4 Bit Sequence
01	5 Bit Sequence
10	6 Bit Sequence
11	7 Bit Sequence

BIT 1 - Framed Loop-Back Code:

This READ/WRITE bit-field is used to configure the Transmit DS1 Framer and Receive DS1 Framer blocks to transmit and detect either framed or un-framed loop-codes (for Code 0)..

- 0 = Configures the Transmit DS1 Framer block to transmit loop-codes within an unframed DS1 data-stream, and configures the Receive DS1 Framer block to detect loop-codes within an unframed DS1 data-stream.
- 1 = Configures the Transmit DS1 Framer block to transmit loop-codes within a framed DS1 data-stream, and configures the Receive DS1 Framer block to detect loop-codes within a framed DS1 data-stream.

BIT 0 - Loop-Back Automatically:

This READ/WRITE bit-field is used to configure the Channel to operate in the Auto Loop-back Mode. If the user configures the Channel to operate in the Auto Loop-back Mode, then all of the following is TRUE.

- The DS1 Framer block will automatically enter the Remote Loop-back Mode anytime the Receive DS1 Framer block detects and validates the Loop-up code within the incoming DS1 data-stream.
- The DS1 Framer block will automatically exit the Remote Loop-back Mode anytime the Receive DS1 Framer block detects and validates the Loop-Down code within the incoming DS1 data-stream.

- 0 = Does not configure the Channel to operate in the Auto Loop-Back Mode.
- 1 = Configures the Channel to operate in the Auto Loop-Back Mode

TABLE 414: T1 FRAMER BLOCK - TRANSMIT LOOP-BACK CODE REGISTER (ADDRESS = 0XN125, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit Loop-back Code[6:0]							Transmit Loop-back Code Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

BIT [7:1] - Transmit Loop-back Code[6:0]:

These READ/WRITE bit-fields is used to specify the loop-back code that the Transmit DS1 Framer block will transmit (to the remote terminal equipment) whenever the user commands it to do so by setting BIT 0 (Transmit Loop-Back Code Enable) to 1, within this register.

BIT 0 - Transmit Loop-back Code Enable:

This READ/WRITE bit-field is used to command the Transmit DS1 Framer block to transmit the Loop-back Code (which has been written into Bits 7 through 1, within this register) to the remote terminal.

- 0 = Configures the Transmit DS1 Framer block to NOT transmit the Loop-back Code to the remote terminal equipment.
- 1 = Configures the Transmit DS1 Framer block to transmit the Loop-back code to the remote terminal equipment.

NOTE: *The Transmit DS1 Framer block will repeatedly transmit the loop-back code for the duration that this bit-field is set to 1.*

TABLE 415: RECEIVE T1 FRAMER BLOCK - RECEIVE LOOP-BACK ACTIVATION CODE REGISTER - CODE 0 (ADDRESS = 0XN126, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Activation Code[6:0]							Receive Activation Loop-Back Code Detect Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

BIT [7:1] - Receive Loop-Back Activation Code[6:0]:

These seven (7) READ/WRITE bit-fields are used to specify/define one of the threee possible loop-code patterns that the Receive DS1 Framer block should respond to, and interpret as being the Loop-Up (or Loop-Back Activate) code.

NOTES:

1. *These READ/WRITE bit-fields are only active if BIT 0 (Receive Activation Loop-Back Code Detect Enable) has been set to 1.*
2. *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as "Code 0", "Code 1" and "Code 2" within this document. This particular register applies to "Code 0".*

BIT 0 - Receive Activation Loop-Back Code Detect Enable:

This READ/WRITE bit-field is used to either enable or disable the Receive DS1 Framer block for Loop-Back Activation Code detection for Code 0. If the user enables the Receive DS1 Framer block for Loop-Back Activation Code detection for Code 0, then the Receive DS1 Framer block (as it is receiving its incoming DS1 data-stream) will also begin to check the incoming DS1 data-stream for the presence of the Loop-Back Activation Code (which has been defined in Bits 7 through 1 within this particular register).

- 0 = Configures the Receive DS1 Framer block to NOT check the incoming DS1 data-stream for the presence of the Loop-Back Activation code.
- 1 = Configures the Receive DS1 Framer block to check the incoming DS1 data-stream for the presence of the Loop-Back Activation code.

TABLE 416: RECEIVE T1 FRAMER BLOCK - RECEIVE LOOP-BACK DEACTIVATION CODE REGISTER - CODE 0 (ADDRESS = 0XN127, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Deactivation Code[6:0]							Receive Deactivation Loop-Back Code Detect Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

BIT [7:1] - Receive Loop-Back Deactivation Code[6:0]:

These seven (7) READ/WRITE bit-fields are used to specify/define one of the three possible loop-code pattern that the Receive DS1 Framer block should respond to, and interpret as being the Loop-Down (or Loop-Back Deactivate) code.

NOTES:

1. *These READ/WRITE bit-fields are only active if BIT 0 (Receive Deactivation Loop-Back Code Detect Enable) has been set to 1.*
2. *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as Code 0, Code 1"and Code 2 within this document. This particular register applies to "ode 0.*

BIT 0 - Receive Deactivation Loop-Back Code Detect Enable:

This READ/WRITE bit-field is used to either enable or disable the Receive DS1 Framer block for Loop-Back Deactivation Code detection for Code 0. If the user enables the Receive DS1 Framer block for Loop-Back Deactivation Code detection for Code 0, then the Receive DS1 Framer block (as it is receiving its incoming DS1 data-stream) will also begin to check the incoming DS1 data-stream for the presence of the Loop-Back Deactivation Code (which has been defined in Bits 7 through 1 within this particular register).

- 0 = Configures the Receive DS1 Framer block to NOT check the incoming DS1 data-stream for the presence of the Loop-Back Deactivation code.
- 1 = Configures the Receive DS1 Framer block to check the incoming DS1 data-stream for the presence of the Loop-Back Deactivation code.

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TABLE 417: T1 FRAMER BLOCK - LOOP-BACK CODE CONTROL REGISTER - CODE 1 (ADDRESS = 0XN12A, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Code Activation Length[1:0]		Receive Loop-Back Code Deactivation Length[1:0]		Unused		Framed Loop-Back Code	Unused
R/W	R/W	R/W	R/W	R/O	R/O	R/W	R/O
0	0	0	0	0	0	0	0

Bits [7:6] - Receive Loop-Back Code Activation Length[1:0]:

These two READ/WRITE bit-fields permit the user to specify the length of the "loop-back activation" code that the Receive DS1 Framer block will use (for Code 1), as depicted below in Table _.

RECEIVE LOOP-BACK CODE ACTIVATION LENGTH[1:0]	LENGTH
00	4 Bit Sequence
01	5 Bit Sequence
10	6 Bit Sequence
11	7 Bit Sequence

Bits [5:4] - Receive Loop-Back Code Deactivation Length[1:0]:

These two READ/WRITE bit-fields permit the user to specify the length of the "loop-back deactivation" code that the Receive DS1 Framer block will use (for Code 1), as depicted below in Table _.

RECEIVE LOOP-BACK CODE DE-ACTIVATION LENGTH[1:0]	LENGTH
00	4 Bit Sequence
01	5 Bit Sequence
10	6 Bit Sequence
11	7 Bit Sequence

Bits [3:2] - Reserved:

Bit 1 - Framed Loop-Back Code:

This READ/WRITE bit-field permits the user to configure the Transmit DS1 Framer and Receive DS1 Framer blocks to transmit and detect either "framed" or "un-framed" loop-codes (for Code 1), as depicted below.

- 0 = Configures the Transmit DS1 Framer block to transmit loop-codes within an "unframed" DS1 data-stream, and configures the Receive DS1 Framer block to detect loop-codes within an "unframed" DS1 data-stream.
- 1 = Configures the Transmit DS1 Framer block to transmit loop-codes within a "framed" DS1 data-stream, and configures the Receive DS1 Framer block to detect loop-codes within a "framed" DS1 data-stream.

Bit 0 - Reserved:

TABLE 418: RECEIVE T1 FRAMER BLOCK - RECEIVE LOOP-BACK ACTIVATION CODE REGISTER - CODE 1 (ADDRESS = 0XN12B, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Activation Code[6:0]							Receive Activation Loop-Back Code Detect Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

Bits [7:1] - Receive Loop-Back Activation Code[6:0]:

These seven (7) READ/WRITE bit-fields are used to specify/define one of the three possible "loop-code" patterns that the Receive DS1 Framer block should respond to, and interpret as being the "Loop-Up" (or Loop-Back Activate) code.

NOTES:

NOTES:

1. *These READ/WRITE bit-fields are only active if Bit 0 (Receive Activation Loop-Back Code Detect Enable) has been set to "1".*
2. *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as "Code 0", "Code 1" and "Code 2" within this document. This particular register applies to "Code 1".*

Bit 0 - Receive Activation Loop-Back Code Detect Enable:

This READ/WRITE bit-field permits the user to either enable or disable the Receive DS1 Framer block for "Loop-Back Activation" Code detection for "Code 1". If the user enables the Receive DS1 Framer block for "Loop-Back Activation" Code detection (for Code 1), then the Receive DS1 Framer block (as it is receiving its incoming DS1 data-stream) will also begin to check the incoming DS1 data-stream for the presence of the "Loop-Back Activation" Code (which has been defined in Bits 7 through 1 within this particular register).

- 0 = Configures the Receive DS1 Framer block to NOT check the incoming DS1 data-stream for the presence of the "Loop-Back Activation" code.
- 1 = Configures the Receive DS1 Framer block to check the incoming DS1 data-stream for the presence of the "Loop-Back Activation" code.

TABLE 419: RECEIVE T1 FRAMER BLOCK - RECEIVE LOOP-BACK DEACTIVATION CODE REGISTER - CODE 1 (ADDRESS = 0XN12C, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Deactivation Code[6:0]							Receive Deactivation Loop-Back Code Detect Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

Bits [7:1] - Receive Loop-Back Deactivation Code[6:0]:

These seven (7) READ/WRITE bit-fields permits the user to specify/define one of the three possible "loop-code" patterns that the Receive DS1 Framer block should respond to, and interpret as being the "Loop-Down" (or Loop-Back Deactivate) code.

NOTES:

1. *These READ/WRITE bit-fields are only active if Bit 0 (Receive Deactivation Loop-Back Code Detect Enable) has been set to "1".*
2. *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as "Code 0", "Code 1" and "Code 2" within this document. This particular register applies to "Code 1".*

Bit 0 - Receive Deactivation Loop-Back Code Detect Enable:

This READ/WRITE bit-field permits the user to either enable or disable the Receive DS1 Framer block for "Loop-Back Deactivation" Code detection for "Code 1". If the user enables the Receive DS1 Framer block for "Loop-Back Deactivation" Code detection (for Code 1), then the Receive DS1 Framer block (as it is receiving its incoming DS1 data-stream) will also begin to check the incoming DS1 data-stream for the presence of the "Loop-Back Deactivation" Code (which has been defined in Bits 7 through 1 within this particular register).

- 0 = Configures the Receive DS1 Framer block to NOT check the incoming DS1 data-stream for the presence of the "Loop-Back Deactivation" code.
- 1 = Configures the Receive DS1 Framer block to check the incoming DS1 data-stream for the presence of the "Loop-Back Deactivation" code.

TABLE 420: T1 FRAMER BLOCK - LOOP-BACK CODE CONTROL REGISTER - CODE 2 (ADDRESS = 0XN12D, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Code Activation Length[1:0]		Receive Loop-Back Code Deactivation Length[1:0]		Unused		Framed Loop-Back Code	Unused
R/W	R/W	R/W	R/W	R/O	R/O	R/W	R/O
0	0	0	0	0	0	0	0

Bits [7:6] - Receive Loop-Back Code Activation Length[1:0]:

These two READ/WRITE bit-fields permit the user to specify the length of the "loop-back activation" code that the Receive DS1 Framer block will use (for Code 2), as depicted below in Table _.

RECEIVE LOOP-BACK CODE ACTIVATION LENGTH[1:0]	LENGTH
00	4 Bit Sequence
01	5 Bit Sequence
10	6 Bit Sequence
11	7 Bit Sequence

Bits [5:4] - Receive Loop-Back Code Deactivation Length[1:0]:

These two READ/WRITE bit-fields permit the user to specify the length of the "loop-back deactivation" code that the Receive DS1 Framer block will use (for Code 2), as depicted below in Table _.

RECEIVE LOOP-BACK CODE DE-ACTIVATION LENGTH[1:0]	LENGTH
00	4 Bit Sequence
01	5 Bit Sequence
10	6 Bit Sequence
11	7 Bit Sequence

Bits [3:2] - Reserved:

Bit 1 - Framed Loop-Back Code:

This READ/WRITE bit-field permits the user to configure the Transmit DS1 Framer and Receive DS1 Framer blocks to transmit and detect either "framed" or "un-framed" loop-codes (for Code 2), as depicted below.

- 0 = Configures the Transmit DS1 Framer block to transmit loop-codes within an "unframed" DS1 data-stream, and configures the Receive DS1 Framer block to detect loop-codes within an "unframed" DS1 data-stream.
- 1 = Configures the Transmit DS1 Framer block to transmit loop-codes within a "framed" DS1 data-stream, and configures the Receive DS1 Framer block to detect loop-codes within a "framed" DS1 data-stream.

Bit 0 - Reserved:

TABLE 421: RECEIVE T1 FRAMER BLOCK - RECEIVE LOOP-BACK ACTIVATION CODE REGISTER - CODE 2 (ADDRESS = 0XN12E, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Activation Code[6:0]							Receive Activation Loop-Back Code Detect Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

Bits [7:1] - Receive Loop-Back Activation Code[6:0]:

These seven (7) READ/WRITE bit-fields permits the user to specify/define one of the three possible "loop-code" patterns that the Receive DS1 Framer block should respond to, and interpret as being the "Loop-Up" (or Loop-Back Activate) code.

NOTES:

1. *These READ/WRITE bit-fields are only active if Bit 0 (Receive Activation Loop-Back Code Detect Enable) has been set to "1".*
2. *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as "Code 0", "Code 1" and "Code 2" within this document. This particular register applies to "Code 2".*

Bit 0 - Receive Activation Loop-Back Code Detect Enable:

This READ/WRITE bit-field permits the user to either enable or disable the Receive DS1 Framer block for "Loop-Back Activation" Code detection for "Code 2". If the user enables the Receive DS1 Framer block for "Loop-Back Activation" Code detection (for Code 2), then the Receive DS1 Framer block (as it is receiving its incoming DS1 data-stream) will also begin to check the incoming DS1 data-stream for the presence of the "Loop-Back Activation" Code (which has been defined in Bits 7 through 1 within this particular register).

- 0 = Configures the Receive DS1 Framer block to NOT check the incoming DS1 data-stream for the presence of the "Loop-Back Activation" code.
- 1 = Configures the Receive DS1 Framer block to check the incoming DS1 data-stream for the presence of the "Loop-Back Activation" code.

TABLE 422: RECEIVE T1 FRAMER BLOCK - RECEIVE LOOP-BACK DEACTIVATION CODE REGISTER - CODE 2 (ADDRESS = 0XN12F, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive Loop-Back Deactivation Code[6:0]							Receive Deactivation Loop-Back Code Detect Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

Bits [7:1] - Receive Loop-Back Deactivation Code[6:0]:

These seven (7) READ/WRITE bit-fields permits the user to specify/define one of the three possible "loop-code" patterns that the Receive DS1 Framer block should respond to, and interpret as being the "Loop-Down" (or Loop-Back Deactivate) code.

NOTES:

1. *These READ/WRITE bit-fields are only active if Bit 0 (Receive Deactivation Loop-Back Code Detect Enable) has been set to "1".*

2. *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as "Code 0", "Code 1" and "Code 2" within this document. This particular register applies to "Code 2".*

Bit 0 - Receive Deactivation Loop-Back Code Detect Enable:

This READ/WRITE bit-field permits the user to either enable or disable the Receive DS1 Framer block for "Loop-Back Deactivation" Code detection for "Code 2". If the user enables the Receive DS1 Framer block for "Loop-Back Deactivation" Code detection (for Code 2), then the Receive DS1 Framer block (as it is receiving its incoming DS1 data-stream) will also begin to check the incoming DS1 data-stream for the presence of the "Loop-Back Deactivation" Code (which has been defined in Bits 7 through 1 within this particular register).

- 0 = Configures the Receive DS1 Framer block to NOT check the incoming DS1 data-stream for the presence of the "Loop-Back Deactivation" code.
- 1 = Configures the Receive DS1 Framer block to check the incoming DS1 data-stream for the presence of the "Loop-Back Deactivation" code.

TABLE 423: T1 FRAMER BLOCK - TRANSMIT CHANNEL CONTROL REGISTER - T1 TIME SLOT # 0 (ADDRESS = 0XN300, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Transmit Zero Suppression[1:0]		Transmit Channel Conditioning[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Reserved.

BIT [5:4] - Transmit Zero Suppression[1:0]:

BIT [3:0] - Transmit Channel Conditioning[3:0]:

These READ/WRITE bit-fields are used to specify how Time-Slot # 0 (within the Transmit DS1 signal is conditioned or modified).

Transmit Channel Conditioning

TRANSMIT CHANNEL CONDITIONING[3:0]	RESULTING CONDITIONING OF TIME-SLOT # 0
0000	The Input PCM data is unchanged (Normal Operation)
0001	All 8-bits of the PCM data are inverted
0010	The even bits of the PCM data are inverted
0011	The odd bits of the PCM data are inverted
0100	PCM Data is replaced with User Code Data
0101	PCM Data is replaced with the BUSY Code (0x7F)
0110	PCM Data is replaced with the VACANT Code (0xFF)
0111	PCM Data is replaced with the BUSY Time-Slot Pattern (0xE0 in the case of Time-Slot # 0).
1000	PCM Data is replaced with the MUX Out of Frame (MOOF) Pattern (0x1A).

TABLE 424: T1 FRAMER BLOCK - LAPD BUFFER 0 CONTROL REGISTER (ADDRESS = 0XN600 - 0XN640, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LAPD Buffer 0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] LAPD Buffer 0:

This register is used to transmit and receive LAPD messages within buffer 0 of the HDLC controller. Users should determine the next available buffer by reading the BUFAVAL bit (BIT7 of the Transmit Data Link Byte Count Register 0xN114h). If buffer 0 is available, writing to buffer 0 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer cannot be retrieved.

After detecting the receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the receive data link byte count register 0xN115h) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 0 is available to be read, reading buffer 0 continuously will retrieve the entire received LAPD message.

NOTE: *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 64 Byte LAPD message can be written into or read from buffer 0 continuously.*

TABLE 425: T1 FRAMER BLOCK - LAPD BUFFER 1 CONTROL REGISTER (ADDRESS = 0XN700 - 0XN740, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LAPD Buffer 1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:0] LAPD Buffer 1:

This register is used to transmit and receive LAPD messages within buffer 1 of the HDLC controller. Users should determine the next available buffer by reading the BUFAVAL bit (BIT7 of the Transmit Data Link Byte Count Register 0xN114h). If buffer 1 is available, writing to buffer 1 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer cannot be retrieved.

After detecting the receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the receive data link byte count register 0xN115h) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 1 is available to be read, reading buffer 1 continuously will retrieve the entire received LAPD message.

NOTE: *When writing to or reading from Buffer 1, the register is automatically incremented such that the entire 64 Byte LAPD message can be written into or read from buffer 1 continuously.*

TABLE 426: T1 FRAMER INTERRUPT REGISTER - RECEIVE LOOP-BACK CODE INTERRUPT AND STATUS REGISTER - CODE 0 (ADDRESS = 0XNB0A, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AUXP Pattern State	Change of AUXP State Interrupt Status	CRC-4 to Non CRC-4 Inter-net-working Status	Change of CRC-4 to Non-CRC-4 Inter-net-working Sta-tus	Receive Loop-Back Activation Status -Code 0	Receive Loop-Back Deactivation Status -Code 0	Change of Receive Loop-Back Activation State Interrupt Status -Code 0	Change of Receive Loop-Back Deactivation State I nterrupt Status -Code 0
R/O	RUR	R/O	RUR	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT7 - AUXP Pattern State:

This READ-ONLY register bit indicates whether or not the Receive DS1 Framer block is currently detecting the AUXP pattern within the incoming DS1 data-stream.

- 0 = Indicates that the Receive DS1 Framer block is NOT currently detecting the AUXP pattern within the incoming DS1 data-stream.
- 1 = Indicates that the Receive DS1 Framer block is currently detecting the AUXP pattern within the incoming DS1 data-stream.

BIT6 - Change of AUXP State Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Receive DS1 Framer block has declared the Change of AUXP State Interrupt since the last read of this register. The Receive DS1 Framer block will generate the Change of AUXP State Interrupt in response to either of the following conditions.

- Whenever it begins to detect the AUXP Pattern within the incoming DS1 data-stream, and
- Whenever it ceases to detect the AUXP Pattern within the incoming DS1 data-stream.

- 0 = Indicates that the Change of AUXP Status Interrupt has NOT occurred since the last read of this register.
- 1 = Indicates that the Change of AUXP Status Interrupt has occurred since the last read of this register.r

BIT 5 - CRC-4 to Non-CRC-4 Internetworking Status:

BIT 4 - Change of CRC-4 to Non-CRC-4 Internetworking Status:

BIT 3 - Receive Loop-Back Activation Status -Code 0:

This READ-ONLY bit-field indicates whether or not the Receive DS1 Framer block is currently detecting (and flagging) the Loop-Up (or Loop-Back Activate) code (associated with "Code 0") within the incoming DS1 data-stream.

- 0 = Indicates that the Receive DS1 Framer block is NOT currently detecting (nor flagging) the Loop-Back Activate Code (associated with "Code 0") within the incoming DS1 data-stream.
- 1 = Indicates that the Receive DS1 Framer block is currently detecting (and flagging) the Loop-Back Activate Code (associated with "Code 0") within the incoming DS1 data-stream.

NOTE: *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as "Code 0", "Code 1" and "Code 2" within this document. This particular register applies to "Code 0".*

BIT 2 - Receive Loop-Back Deactivation Status - Code 0:

This READ-ONLY bit-field indicates whether or not the Receive DS1 Framer block is currently detecting (and flagging) the Loop-Down (or Loop-Back Deactivate) code (associated with Code 0) within the incoming DS1 data-stream.

- 0 = Indicates that the Receive DS1 Framer block is NOT currently detecting (nor flagging) the Loop-Back Deactivate Code (associated with "Code 0") within the incoming DS1 data-stream.
- 1 = Indicates that the Receive DS1 Framer block is currently detecting (and flagging) the Loop-Back Deactivate Code (associated with "Code 0") within the incoming DS1 data-stream.

BIT 1 - Change of Receive Loop-Back Activation State Interrupt Status - mCode 0:

This RESET-upon-READ bit-field indicates whether or not the Receive DS1 Framer block has generated the Change of Receive Loop-Back Activation State Interrupt, since the last read of this register. The Receive DS1 Framer block will generate the Change of Receive Loop-Back Activation State Interrupt in response to either of the following events.

- Whenever the Receive DS1 Framer block detects (and validates) the Loop-Back Activate Code (associated with Code 0) within the incoming DS1 data-stream
- Whenever the Receive DS1 Framer block ceases to detect the Loop-Back Activate code (associated with Code 0) within the incoming DS1 data-stream.

▶ 0 = Indicates that the Receive DS1 Framer block has NOT generated the Change of Receive Loop-Back Activation State Interrupt for Code 0 since the last read of this register.

▶ 1 = Indicates that the Receive DS1 Framer block has generated the Change of Receive Loop-Back Activation State Interrupt for Code 0 since the last read of this register.

BIT 0 - Change of Receive Loop-Back Deactivation Status Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the Receive DS1 Framer block has generated the Change of Receive Loop-Back Deactivation State Interrupt (based upon loop-code Code 0), since the last read of this register. The Receive DS1 Framer block will generate the Change of Receive Loop-Back Deactivation State Interrupt in response to either of the following events.

- Whenever the Receive DS1 Framer block detects (and validates) the Loop-Back Deactivate Code (associated with Code 0) within the incoming DS1 data-stream
- Whenever the Receive DS1 Framer block ceases to detect the Loop-Back Deactivate code (associated with Code 0) within the incoming DS1 data-stream.

▶ 0 = Indicates that the Receive DS1 Framer block has NOT generated the Change of Receive Loop-Back Deactivation State Interrupt for Code 0 since the last read of this register.

▶ 1 = Indicates that the Receive DS1 Framer block has generated the Change of Receive Loop-Back Deactivation State Interrupt for Code 0 since the last read of this register.

TABLE 427: T1 FRAMER INTERRUPT REGISTER - RECEIVE LOOP-BACK CODE INTERRUPT ENABLE REGISTER - CODE 0 (ADDRESS = 0XNB0B, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Change of AUXP State Interrupt Enable	Reserved	Change of CRC-4 to Non-CRC-4 Inter-Net-working State Interrupt Enable	Reserved		Change of Receive Loop-Back Activation Interrupt Enable - Code 0	Change of Receive Loop-Back Deactivation Interrupt Enable - Code 0
R/O	R/W	R/O	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT6 - Change of AUXP State Interrupt Enable:

This READ/WRITE bit-field is used to either enable or disable the Change of AUXP State Interrupt. If the user enables the Change of AUXP State Interrupt, then the Receive DS1 Framer block will generate the Change of AUXP State Interrupt in response to the following events.

- Whenever it begins to detect the AUXP Pattern within the incoming DS1 data-stream, and
- Whenever it ceases to detect the AUXP Pattern within the incoming DS1 data-stream.

▶ 0 = Disables the Change of AUXP State Interrupt.

▶ 1 = Enables the Change of AUXP State Interrupt

BIT 5 - Reserved

BIT 4 - Change of CRC-4 to Non-CRC-4 Internetworking Status Interrupt Enable:

BIT [3:2] - Reserved

BIT 1 - Change of Receive Loop-Back Activation Interrupt Enable - Code 0:

This READ/WRITE bit-field is used to either enable or disable the Change of Receive Loop-Back Activation State Interrupt, associated with Code 0. If the user enables the Change of Receive Loop-Back Activation State Interrupt, then the Receive DS1 Framer block will generate the Change of Receive Loop-Back Activation State Interrupt in response to the following events.

- Whenever it detects and validates the Receive Loop-Back Activation Pattern (associated with Code 0) within the incoming DS1 data-stream, and
- Whenever it ceases to detect the Receive Loop-Back Activation Pattern (associated with Code 0) within the incoming DS1 data-stream.

▶ 0 = Disables the Change of Receive Loop-Back Activation State Interrupt for loop-code Code 0.

▶ 1 = Enables the Change of Receive Loop-Back Activation State Interrupt for loop-code Code 0

BIT 0 - Change of Receive Loop-Back Deactivation Interrupt Enable -Code 0:

This READ/WRITE bit-field is used to either enable or disable the Change of Receive Loop-Back Deactivation State Interrupt associated with Code 0. If the user enables the Change of Receive Loop-Back Deactivation State Interrupt, then the Receive DS1 Framer block will generate the Change of Receive Loop-Back Deactivation State Interrupt in response to the following events.

- Whenever it detects and validates the Receive Loop-Back Deactivation Pattern (associated with Code 0) within the incoming DS1 data-stream, and
- Whenever it ceases to detect the Receive Loop-Back Deactivation Pattern (associated with Code 0) within the incoming DS1 data-stream.

▶ 0 = Disables the Change of Receive Loop-Back Deactivation State Interrupt for Code 0.

▶ 1 = Enables the Change of Receive Loop-Back Deactivation State Interrupt for Code 0

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TABLE 428: T1 FRAMER INTERRUPT REGISTER - RECEIVE LOOP-BACK CODE INTERRUPT AND STATUS REGISTER - CODE 1 (ADDRESS = 0XNB14, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Receive Loop-Back Activation Status - Code 1	Receive Loop-Back Deactivation Status - Code 1	Change of Receive Loop-Back Activation State Interrupt Status - Code 1	Change of Receive Loop-Back Deactivation State Interrupt Status - Code 1
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

Bits 7 through 4 - Unused:

Bit 3 - Receive Loop-Back Activation Status - Code 1:

This READ-ONLY bit-field indicates whether or not the Receive DS1 Framer block is currently detecting (and flagging) the Loop-Up (or Loop-Back Activate) code (associated with Code 1) within the incoming DS1 data-stream, as depicted below.

▶ 0 = Indicates that the Receive DS1 Framer block is NOT currently detecting (nor flagging) the "Loop-Back Activate" Code (associated with "Code 1") within the incoming DS1 data-stream.

▶ 1 = Indicates that the Receive DS1 Framer block is currently detecting (and flagging) the "Loop-Back Activate" Code (associated with "Code 1") within the incoming DS1 data-stream.

NOTE: *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as "Code 0", "Code 1" and "Code 2" within this document. This particular register applies to "Code 1".*

Bit 2 - Receive Loop-Back Deactivation Status - Code 1:

This READ-ONLY bit-field indicates whether or not the Receive DS1 Framer block is currently detecting (and flagging) the Loop-Down (or Loop-Back Deactivate) code (associated with Code 1) within the incoming DS1 data-stream, as depicted below.

- 0 = Indicates that the Receive DS1 Framer block is NOT currently detecting (nor flagging) the "Loop-Back Deactivate" Code (associated with "Code 1") within the incoming DS1 data-stream.
- 1 = Indicates that the Receive DS1 Framer block is currently detecting (and flagging) the "Loop-Back Deactivate" Code (associated with "Code 1") within the incoming DS1 data-stream.

Bit 1 - Change of Receive Loop-Back Activation State Interrupt Status - Code 1:

This RESET-upon-READ bit-field indicates whether or not the Receive DS1 Framer block has generated the "Change of Receive Loop-Back Activation State" Interrupt (based upon loop-code "Code 1"), since the last read of this register. The Receive DS1 Framer block will generate the "Change of Receive Loop-Back Activation State" Interrupt in response to either of the following events.

- Whenever the Receive DS1 Framer block detects (and validates) the "Loop-Back Activate" Code (associated with "Code 1") within the incoming DS1 data-stream
- Whenever the Receive DS1 Framer block ceases to detect the "Loop-Back Activate" code (associated with "Code 1") within the incoming DS1 data-stream.

- 0 = Indicates that the Receive DS1 Framer block has NOT generated the "Change of Receive Loop-Back Activation State" Interrupt for "Code 1" since the last read of this register.
- 1 = Indicates that the Receive DS1 Framer block has generated the "Change of Receive Loop-Back Activation State" Interrupt for "Code 1" since the last read of this register.

Bit 0 - Change of Receive Loop-Back Deactivation Status Interrupt Status - Code 1:

This RESET-upon-READ bit-field indicates whether or not the Receive DS1 Framer block has generated the "Change of Receive Loop-Back Deactivation State" Interrupt (based upon loop-code "Code 1"), since the last read of this register. The Receive DS1 Framer block will generate the "Change of Receive Loop-Back Deactivation State" Interrupt in response to either of the following events.

- Whenever the Receive DS1 Framer block detects (and validates) the "Loop-Back Deactivate" Code (associated with "Code 1") within the incoming DS1 data-stream
- Whenever the Receive DS1 Framer block ceases to detect the "Loop-Back Deactivate" code (associated with "Code 1") within the incoming DS1 data-stream.

- 0 = Indicates that the Receive DS1 Framer block has NOT generated the "Change of Receive Loop-Back Deactivation State" Interrupt for "Code 1" since the last read of this register.
- 1 = Indicates that the Receive DS1 Framer block has generated the "Change of Receive Loop-Back Deactivation State" Interrupt for "Code 1" since the last read of this register.

TABLE 429: T1 FRAMER INTERRUPT REGISTER - RECEIVE LOOP-BACK CODE INTERRUPT ENABLE REGISTER - CODE 1 (ADDRESS = 0XNB15, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						Change of Receive Loop-Back Activation Interrupt Enable - Code 1	Change of Receive Loop-Back Deactivation Interrupt Enable - Code 1
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 through 2 - Reserved:

Bit 1 - Change of Receive Loop-Back Activation Interrupt Enable - Code 1:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of Receive Loop-Back Activation

State" Interrupt associated with Loop-Code "Code 1". If the user enables the "Change of Receive Loop-Back Activation State" Interrupt, then the Receive DS1 Framer block will generate the "Change of Receive Loop-Back Activation State" Interrupt in response to the following events.

- Whenever it detects and validates the "Receive Loop-Back Activation" Pattern (associated with "Code 1") within the incoming DS1 data-stream, and
- Whenever it ceases to detect the "Receive Loop-Back Activation" Pattern (associated with "Code 1") within the incoming DS1 data-stream.

▶ 0 = Disables the "Change of Receive Loop-Back Activation State" Interrupt for loop-code "Code 1".

▶ 1 = Enables the "Change of Receive Loop-Back Activation State" Interrupt for loop-code "Code 1".

Bit 0 - Change of Receive Loop-Back Deactivation Interrupt Enable - Code 1:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of Receive Loop-Back Deactivation State" Interrupt. If the user enables the "Change of Receive Loop-Back Deactivation State" Interrupt, then the Receive DS1 Framer block will generate the "Change of Receive Loop-Back Deactivation State" Interrupt in response to the following events.

- Whenever it detects and validates the "Receive Loop-Back Deactivation" Pattern (associated with "Code 1") within the incoming DS1 data-stream, and
- Whenever it ceases to detect the "Receive Loop-Back Deactivation" Pattern (associated with "Code 1") within the incoming DS1 data-stream.

▶ 0 = Disables the "Change of Receive Loop-Back Deactivation State" Interrupt for "Code 1".

▶ 1 = Enables the "Change of Receive Loop-Back Deactivation State" Interrupt for "Code 1".

TABLE 430: T1 FRAMER INTERRUPT REGISTER - RECEIVE LOOP-BACK CODE INTERRUPT AND STATUS REGISTER - CODE 2 (ADDRESS = 0XNB1A, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Receive Loop-Back Activation Status - Code 2	Receive Loop-Back Deactivation Status - Code 2	Change of Receive Loop-Back Activation State Interrupt Status - Code 2	Change of Receive Loop-Back Deactivation State Interrupt Status - Code 2
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

Bits 7 through 4 - Unused:

Bit 3 - Receive Loop-Back Activation Status - Code 2:

This READ-ONLY bit-field indicates whether or not the Receive DS1 Framer block is currently detecting (and flagging) the Loop-Up (or Loop-Back Activate) code (associated with Code 2) within the incoming DS1 data-stream, as depicted below.

▶ 0 = Indicates that the Receive DS1 Framer block is NOT currently detecting (nor flagging) the "Loop-Back Activate" Code (associated with "Code 2") within the incoming DS1 data-stream.

▶ 1 = Indicates that the Receive DS1 Framer block is currently detecting (and flagging) the "Loop-Back Activate" Code (associated with "Code 2") within the incoming DS1 data-stream.

NOTE: *The Receive DS1/E1 Framer block can be configured to detect three different loop activate/deactivate codes in parallel. These three (3) codes will be referred to as "Code 0", "Code 1" and "Code 2" within this document. This particular register applies to "Code 2".*

Bit 2 - Receive Loop-Back Deactivation Status - Code 2:

This READ-ONLY bit-field indicates whether or not the Receive DS1 Framer block is currently detecting (and flagging) the Loop-Down (or Loop-Back Deactivate) code (associated with Code 2) within the incoming DS1 data-stream.

▶ 0 = Indicates that the Receive DS1 Framer block is NOT currently detecting (nor flagging) the "Loop-Back Deactivate"

Code (associated with "Code 2") within the incoming DS1 data-stream.

▶ 1 = Indicates that the Receive DS1 Framer block is currently detecting (and flagging) the "Loop-Back Deactivate" Code (associated with "Code 2") within the incoming DS1 data-stream.

Bit 1 - Change of Receive Loop-Back Activation State Interrupt Status - Code 2:

This RESET-upon-READ bit-field indicates whether or not the Receive DS1 Framer block has generated the "Change of Receive Loop-Back Activation State" Interrupt (based upon loop-code "Code 2"), since the last read of this register. The Receive DS1 Framer block will generate the "Change of Receive Loop-Back Activation State" Interrupt in response to either of the following events.

- Whenever the Receive DS1 Framer block detects (and validates) the "Loop-Back Activate" Code (associated with "Code 2") within the incoming DS1 data-stream
- Whenever the Receive DS1 Framer block ceases to detect the "Loop-Back Activate" code (associated with "Code 2") within the incoming DS1 data-stream.

▶ 0 = Indicates that the Receive DS1 Framer block has NOT generated the "Change of Receive Loop-Back Activation State" Interrupt for "Code 2" since the last read of this register.

▶ 1 = Indicates that the Receive DS1 Framer block has generated the "Change of Receive Loop-Back Activation State" Interrupt for "Code 2" since the last read of this register.

Bit 0 - Change of Receive Loop-Back Deactivation Status Interrupt Status - Code 2:

This RESET-upon-READ bit-field indicates whether or not the Receive DS1 Framer block has generated the "Change of Receive Loop-Back Deactivation State" Interrupt (based upon loop-code "Code 2"), since the last read of this register. The Receive DS1 Framer block will generate the "Change of Receive Loop-Back Deactivation State" Interrupt in response to either of the following events.

- Whenever the Receive DS1 Framer block detects (and validates) the "Loop-Back Deactivate" Code (associated with "Code 2") within the incoming DS1 data-stream
- Whenever the Receive DS1 Framer block ceases to detect the "Loop-Back Deactivate" code (associated with "Code 2") within the incoming DS1 data-stream.

▶ 0 = Indicates that the Receive DS1 Framer block has NOT generated the "Change of Receive Loop-Back Deactivation State" Interrupt for "Code 2" since the last read of this register.

▶ 1 = Indicates that the Receive DS1 Framer block has generated the "Change of Receive Loop-Back Deactivation State" Interrupt for "Code 2" since the last read of this register.

TABLE 431: T1 FRAMER INTERRUPT REGISTER - RECEIVE LOOP-BACK CODE INTERRUPT ENABLE REGISTER - CODE 2 (ADDRESS = 0XNB1B, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved						Change of Receive Loop-Back Activation Interrupt Enable - Code 2	Change of Receive Loop-Back Deactivation Interrupt Enable - Code 2
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 through 2 - Reserved:

Bit 1 - Change of Receive Loop-Back Activation Interrupt Enable - Code 2:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of Receive Loop-Back Activation State" Interrupt associated with Loop-Code "Code 2". If the user enables the "Change of Receive Loop-Back Activation State" Interrupt, then the Receive DS1 Framer block will generate the "Change of Receive Loop-Back Activation State" Interrupt in response to the following events.

- Whenever it detects and validates the "Receive Loop-Back Activation" Pattern (associated with "Code 2") within the incoming DS1 data-stream, and

- Whenever it ceases to detect the "Receive Loop-Back Activation" Pattern (associated with "Code 2") within the incoming DS1 data-stream.

▶ 0 = Disables the "Change of Receive Loop-Back Activation State" Interrupt for loop-code "Code 2".

▶ 1 = Enables the "Change of Receive Loop-Back Activation State" Interrupt for loop-code "Code 2".

Bit 0 - Change of Receive Loop-Back Deactivation Interrupt Enable - Code 2:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of Receive Loop-Back Deactivation State" Interrupt. If the user enables the "Change of Receive Loop-Back Deactivation State" Interrupt, then the Receive DS1 Framer block will generate the "Change of Receive Loop-Back Deactivation State" Interrupt in response to the following events.

- Whenever it detects and validates the "Receive Loop-Back Deactivation" Pattern (associated with "Code 2") within the incoming DS1 data-stream, and
- Whenever it ceases to detect the "Receive Loop-Back Deactivation" Pattern (associated with "Code 2") within the incoming DS1 data-stream.

▶ 0 = Disables the "Change of Receive Loop-Back Deactivation State" Interrupt for "Code 2".

▶ 1 = Enables the "Change of Receive Loop-Back Deactivation State" Interrupt for "Code 2".

2.14 DS1/E1 FRAMER BLOCK REGISTERS - E1 APPLICATIONS

TABLE 432: E1 FRAMER BLOCK - CLOCK SELECT REGISTER (ADDRESS = 0XN100, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Set E1 Mode	Force all Channels to Sync to 8kHz	Unused			Clock Source Select[1:0]	
R/O	R/W	R/W	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	1

BIT7 - Reserved

BIT6 - Set T1 Mode:

This READ/WRITE bit-field is used to configure the Channel to operate in either the T1 or E1 Mode.

▶ 0 = Configures the Framer Channel to operate in the E1 Mode

▶ 1 = Configures the Framer Channel to operate in the T1 Mode

BIT 5 - Force all Channels to Sync to 8kHz:

This READ/WRITE bit-field is used to configure all active (either 21 or 42) Transmit E1 Framer blocks to synchronize their transmit output frame alignment with the 8kHz signal that is derived from the MCLK PLL.

▶ 0 = Does not configure each of the Transmit E1 Framer blocks to synchronize their transmit output frame alignment with the 8kHz signal (from the MCLK PLL).

▶ 1 = Configures each of the Transmit E1 Framer blocks to synchronize their transmit output frame alignment with the 8kHz signal (from the MCLK PLL).

NOTE: *This feature should only be used if the XRT86SH328 has been configured to operate in the 21-Channel E1 Framer/LIU Combo Mode. The user MUST NOT use this feature if the XRT86SH328 has been configured to operate in any of the Aggregation Modes.*

BIT [4:2] - Reserved

BIT [1:0] - Clock Source Select[1:0]:

These two READ/WRITE bit-fields is used to specify the timing source for the Ingress and Direction Transmit E1 Framer block, within this particular channel.

The Relationship between the Clock Source Select[1:0] bit-fields and the resulting timing source for the Transmit E1 Framer block, within this particular Channel

CLOCK SOURCE SELECT[1:0]	TIMING SOURCE FOR TRANSMIT E1 FRAMER BLOCK
00	Loop-Timing Mode:The Transmit E1 Framer block will derive its timing from the Received or Recovered Clock signal within the corresponding Receive E1 Framer block ***NOTE:*** *This timing option is only available if the user has configured the XRT86SH328 to operate in the 21-Channel E1 Framer/LIU Combo Mode*
01	Local-Timing Mode (TxE1CLK_n Input)The Transmit E1 Framer block will either use up-stream timing or the TxE1CLK_n input as its timing source. ***NOTE:*** *For Aggregation Applications, the user MUST configure all active T1/E1 Framer blocks to operate in this timing mode.*
10	Local-Timing Mode (MCLK PLL Input)The Transmit E1 Framer block will derive its timing from the MCLK PLL.NOTE: This timing option is only available if the user has configured the XRT86SH328 to operate in the 21-Channel E1 Framer/LIU Combo Mode.
11	Loop-Timing ModeThe Transmit E1 Framer block will derive its timing from the Received or Recovered Clock signal within the corresponding Receive E1 Framer block ***NOTE:*** *This timing option is only available if the user has configured the XRT86SH328 to operate in the 21-Channel E1 Framer/LIU Combo Mode.*

TABLE 433: E1 FRAMER BLOCK - LINE INTERFACE CONTROL REGISTER (ADDRESS = 0XN101, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit LOS Pattern	Reserved		Framer Loop-Back[1:0]	Reserved			
R/W	R/O	R/W	R/W	R/O	R/O	R/O	R/O
0	1	0	0	0	0	0	0

BIT7 - Transmit LOS Pattern:

This READ/WRITE bit-field configures the Transmit E1 Framer block to generate and transmit the LOS Pattern to the remote terminal.

- 0 = Configures the Transmit E1 Framer Block to transmit normal E1 traffic
- 1 = Configures the Transmit E1 Framer Block to transmit the LOS pattern.

NOTE: *The user MUST set this bit-field to 0 for Normal Operation.*

BIT6 - Reserved

BIT [5:4] - Framer Loop-back[1:0]:

These two READ/WRITE bit-fields are used to configure the Transmit/Receive E1 Framer blocks to operate in a variety of possible loop-back modes, as depicted in the Table below.

Relationship between the Framer Loop-back[1:0] bit-fields and the Corresponding Loop-Back Mode within the E1 Framer block

FRAMER LOOP-BACK[1:0]	RESULTING LOOP-BACK MODE (WITHIN FRAMER BLOCK)
00	Normal Operation (No Loop-back) Mode
01	Local Loop-back Mode

Relationship between the Framer Loop-back[1:0] bit-fields and the Corresponding Loop-Back Mode within the E1 Framer block

FRAMER LOOP-BACK[1:0]	RESULTING LOOP-BACK MODE (WITHIN FRAMER BLOCK)
10	Remote Loop-back Mode
11	Reserved

TABLE 434: E1 FRAMER BLOCK - FRAMING SELECT REGISTER (ADDRESS = 0XN107, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Annex B	Tx CRC-4 Error	CAS MultiFrame Sel[1:0]		CRC MultiFrame Sel[1:0]		Add Frame ChkEnable	FAS Frame Alignment
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - G.706 Annex B CRC-4 Calculation Enable:

This bit configures the E1 receive framer block to be compliant with ITU-T G.706 Annex B for CRC-to-non-CRC interworking detection. If Annex B is enabled, G.706 Annex B CRC-4 multi frame alignment algorithm is implemented. If CRC-4 alignment is enabled and not achieved in 400 msec while the basic frame alignment signal is present, it is assumed that the remote end is a non CRC-4 equipment. A CRC-to-non-CRC interworking interrupt will be generated.

- 0 = Configures the receive E1 framer block to NOT support the G.706 Annex B CRC-4 multi frame alignment algorithm.
- 1 = Configures the receive E1 framer block to support the G.706 Annex B CRC-4 multi frame alignment algorithm.

BIT6 - Transmit CRC-4 Error:

This bit is used to force a continuous errored CRC pattern in the outbound CRC multi frame to be sent on the transmission line. The transmit E1 framer block will implement this error by inverting the value of CRC bit (C1).

- 0 = Disabled
- 1 = Forces the transmit E1 framer block to transmit continuous errored CRC bit.

BIT [5:4] - CAS Multi Frame Select[1:0]:

These bits allow the user to select which CAS multi frame alignment declaration algorithm the receive E1 framer block will employ, according to the table below.

E1 Framer Block - Framing Select Register (Address = 0xN107, where N ranges in value from 0x01 to 0x38)

CAS MF ALIGN SEL[1:0]	CAS MULTI FRAME ALIGNMENT DECLARATION ALGORITHM SELECTED
00, 11	CAS multi frame alignment disabled.
01	The 16-Frame AlgorithmIf this alignment algorithm is selected, then the receive E1 framer block will monitor the 16th timeslot of each incoming E1 frame and will declare CAS multi frame alignment (e.g., clear the loss of CAS multi frame defect) condition anytime that it detects 15 consecutive E1 frames in which bits 1-4 (of time slot 16) do not contain the CAS Multi Frame Alignment pattern, which is immedi-ately followed by an E1 frame that DOES contain the CAS Multi Frame Alignment pattern.
10	The 2-Frame (ITU-T G.732) AlgorithmIf this alignment algorithm is selected, then the receive E1 framer block will declare CAS multi frame alignment anytime it detects a single E1 frame rather than 15 consecutive E1 frames as described above in the 16-Frame Algorithm.

NOTE: For information on the criteria that the receive E1 framer block uses in order to declare the Loss of CAS Multi Frame defect condition, please see the register description for the Framing Control Register 0xN10Bh.

BIT [3:2] - CRC Multi Frame Alignment Declaration Criteria Select[1:0]:

These bits allow the user to select which CRC Multi Frame Alignment declaration criteria the receive E1 framer block will employ. The receive E1 framer block will check for CRC Multi Frame Alignmnet by checking the incoming E1 data stream and determining whether the international bits (bit 1 of time slot 0) of non-FAS frames match the CRC multi frame alignment pattern (0,0,1,0,1,1,E1,E2).

CAS MF Align Sel

CAS MF ALIGN SEL[1:0]	CAS MULTI FRAME ALIGNMENT DECLARATION ALGORITHM CRITERIA
00	CRC Multi Frame Alignment Disabled.
01	CRC Multi Frame Alignment is enabled. Alignment is declared if at least 1 valid CRC multi frame alignment signal is observed within 8 msec.
10	CRC Multi Frame Alignment is enabled. Alignment is declared if at least 2 valid CRC multi frame alignment signals are observed within 8 msec.
11	CRC Multi Frame Alignment is enabled. Alignment is declared if at least 3 valid CRC multi frame alignment signals are observed within 8 msec.

NOTE: For information on the criteria that the receive E1 framer block uses to declare the Loss of CRC Multi Frame Alignment defect condition, please see the register description for the Framing Control Register 0xN10Bh.

BIT 1 - Additional Frame Check Enable - FAS Frame Alignment Declaration:

This bit is used to configure the receive E1 framer block to perform some additional FAS frame synchronization checking prior to declaration FAS frame alignment. If the user implements this feature, then the receive E1 framer block will perform some more testing on two additional E1 frames, prior to declaring the FAS frame Alignment condition.

- 0 = Disabled.
- 1 = Enables additional FAS frame checking.

BIT 0 - FAS Alignment Declaration Algorithm Select:

This bit specifies which algorithm the receive E1 framer block uses in its search for the FAS alignment.

- 0 = FAS Alignment Algorithm 1
- 1 = FAS Alignment Algorithm 2

FAS Alignment Algorithm 1 Desciption

a. Step 1: The receive E1 Framer block begins by searching for the correct 7-bit FAS pattern. Go to step 2 if found.

b. Step 2: Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed time slot 0 of the Non-FAS frame is a one. Go back to step 1 if failed, otherwise go to step 3.

c. Step 3: check if the FAS is present in the assumed time slot 0 of the third frame. Go back to step 1 if failed.

After the first three steps (if all passed), the receive E1 framer block will declare FAS in Sync if Frame Check Sequence (BIT 1 of this register) is disabled. If frame check sequence is enabled, then the receive E1 framer block will need to verify the correct frame alignment.

FAS Alignment Algorithm 2 Description

Algorithm 2 is similar to algorithm 1 but adds a one-frame hold off time after the second step fails. After the second step fails, it waits for the next assumed FAS in the next frame before it begins the new search for the correct FAS pattern.

TABLE 435: E1 FRAMER BLOCK - ALARM GENERATION REGISTER (ADDRESS = 0XN108, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmi-tAUXP Pat-tern	LOF Decla-rationCriteria	Transmit YEL and Multi YEL[1:0]		Transmit AIS Pattern Select[1:0]		AIS Defect Declaration Cri-teria[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Transmit Auxiliary Pattern:

This bit is used to transmit an auxiliary pattern (repeating …010101) to the transmit line interface.

- 0 = Disabled
- 1 = Enable AUXP Pattern

BIT6 - Loss of Frame Declaration Criteria

This bit is used to select Loss of Frame Declaration Criteria for the receive E1 framer block.

- 0 = Loss of frame is declared immediately if either CRC multi frame alignment or FAS alignment is lost.
- 1 = Loss of frame is declared immediately if FAS alignment is lost. If CRC multi frame alignment is lost for more than 8 msec, the E1 receive framer will force a frame search.

BIT [5:4] - Yellow Alarm and Multi Yellow Alarm Generation [1:0]:

These bits activate or deactivate the transmission of yellow and multi frame yellow alarm. The yellow alarm and multi frame yellow alarm can be forced to transmit as 1, or be inserted upon detection of loss of alignment.

YEL and Multi YE

YEL AND MULTI YEL[1:0]	YELLOW ALARM TRANSMITTED
00 / 10	Disabled.
01	Automatic Transmission of YEL and CAS Multi YELWhenever the receive E1 framer block declares LOF or Loss CAS Multi Frame Alignment, the corresponding transmit E1 framer block will automatically transmit the Yellow Alarm indicator by setting BIT 3 of time slot 0 within the non-FAS frames to 1.
11	Force Transmission of YEL and CAS Multi YELBoth Yellow and Multi Frame Yel-low Alarm are transmitted as '1'

BIT [3:2] - Transmit AIS Pattern Select[1:0]

These two READ/WRITE bit-fields are used to select the type of AIS Pattern that the Transmit E1 Framer block will send if enabled.

The Relationship between Transmit AIS Pattern Select[1:0] and the resulting behavior of the Transmit E1 Framer block

TRANSMIT AIS PATTERN SELECT[1:0]	TRANSMIT E1 FRAMER BLOCK ACTION
00	Transmits Normal TrafficTransmit E1 Framer block does not transmit the AIS indicator. It will (instead) transmit normal traffic
01	Unframed All Ones PatternThe Transmit E1 Framer block will transmit an Unframed All Ones Pattern (as an AIS pattern) for the duration that these bit-fields are set to [0, 1].

The Relationship between Transmit AIS Pattern Select[1:0] and the resulting behavior of the Transmit E1 Framer block

TRANSMIT AIS PATTERN SELECT[1:0]	TRANSMIT E1 FRAMER BLOCK ACTION
10	The AIS-16 PatternIn this case, time slot 16 in each frame will be set to an All Ones Pattern.
11	Framed All Ones PatternThe Transmit E1 Framer block will transmit a Framed All Ones Pattern (as an AIS pattern) for the duration that these bit-fields are set to [1, 0].

BIT[1:0] - AIS Defect Declaration Criteria[1:0]

These two READ/WRITE bit-fields are used to select the type of AIS Pattern that the Receive E1 Framer block will look for in order to determine whether or not it should declare or clear the AIS defect condition.

The Relationship between AIS Defect Declaration Criteria[1:0] and the resulting AIS Pattern that the Receive E1 Framer block will look for in declaring/clearing the AIS defect condition

AIS DEFECT DECLARATION CRITERIA[1:0]	RECEIVE E1 FRAMER BLOCK - AIS DEFECT DECLARATION CRITERIA
00	AIS Defect Declaration is DisabledThe Receive E1 Framer block will NOT declare the AIS defect condition at all.
01	Unframed and Framed All Ones Pattern:The Receive E1 Framer block will declare the AIS defect condition whenever it receives either the Framed or Unframed All Ones pattern for at least 42ms.
10	AIS-16 All Ones Pattern:The Receive E1 Framer block will declare the AIS defect condition whenever it receives all ones in the 16th time slot.
11	Framed All Ones Pattern:The Receive E1 Framer block will only declare the AIS defect condition whenever it receives the Framed All Ones Pattern for at least 42ms.

TABLE 436: E1 FRAMER BLOCK - SYNCHRONIZATION MUX REGISTER (ADDRESS = 0XN109, WHERE N RANGES IN VALUE FROM 0X01 TO 0X38)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
E-Bit SourceSelect		Reserved		Data Link SourceSelect		CRC-4 Source Select	Framing Alignment Pattern Select
R/O	R/W	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - E-Bit Source Select

- These bits are used to specify the source of E-bits wihin each outbound E1 frame.

E-bits

E-BITS [1:0]	E-BIT SOURCE SELECT
00	Internal Framer BlockThe E-bits are used to indicate whether the receive E1 framer block has detected a CRC error within the most recently received sub-multi frame. The receive E1 framer will indicate a received errored sub-multi frame by setting the binary state of the E-bits from 1 to 0 for each errored sub-multi frame.

E-bits

E-BITS [1:0]	E-BIT SOURCE SELECT
01	All E-bits within the outbound E1 data stream are set to 0.
10	All E-bits within the outbound E1 data stream are set to 1.
11	The E-bits are used to carry the data link information.

BIT [5:4] - Reserved

BIT [3:2] - Data Link Source Select

These bits are used to specify the source of the data link bits that will be inserted in the outbound E1 frames.

YEL and Multi YEL

YEL AND MULTI YEL[1:0]	YELLOW ALARM TRANSMITTED
00 / 11	The transmit serial input from the transmit payload data input block will be the source for the data link bits.
01	The Transmit HDLC Controller will generate either BOS (bit oriented signaling) or MOS (message oriented signaling) messages which will be inserted into the data link bits in the outbound E1 frames.
10	Reserved.

BIT 1 - CRC-4 Source Select

BIT 0 - Framing Alignment Pattern Select

2.15 CHANNEL CONTROL-VT MAPPER BLOCK REGISTERS

The register map for the Channel Control VT-Mapper Block registers is presented in the Table below. Additionally, a detailed description of each of the Channel Control VT-Mapper Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT86SH328, with both the VT/TU Mapper and VT/TU De-Mapper Blocks highlighted is presented below in Figure 19.

FIGURE 19. ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328 DEVICE, WITH THE VT-MAPPER BLOCK HIGHLIGHTED

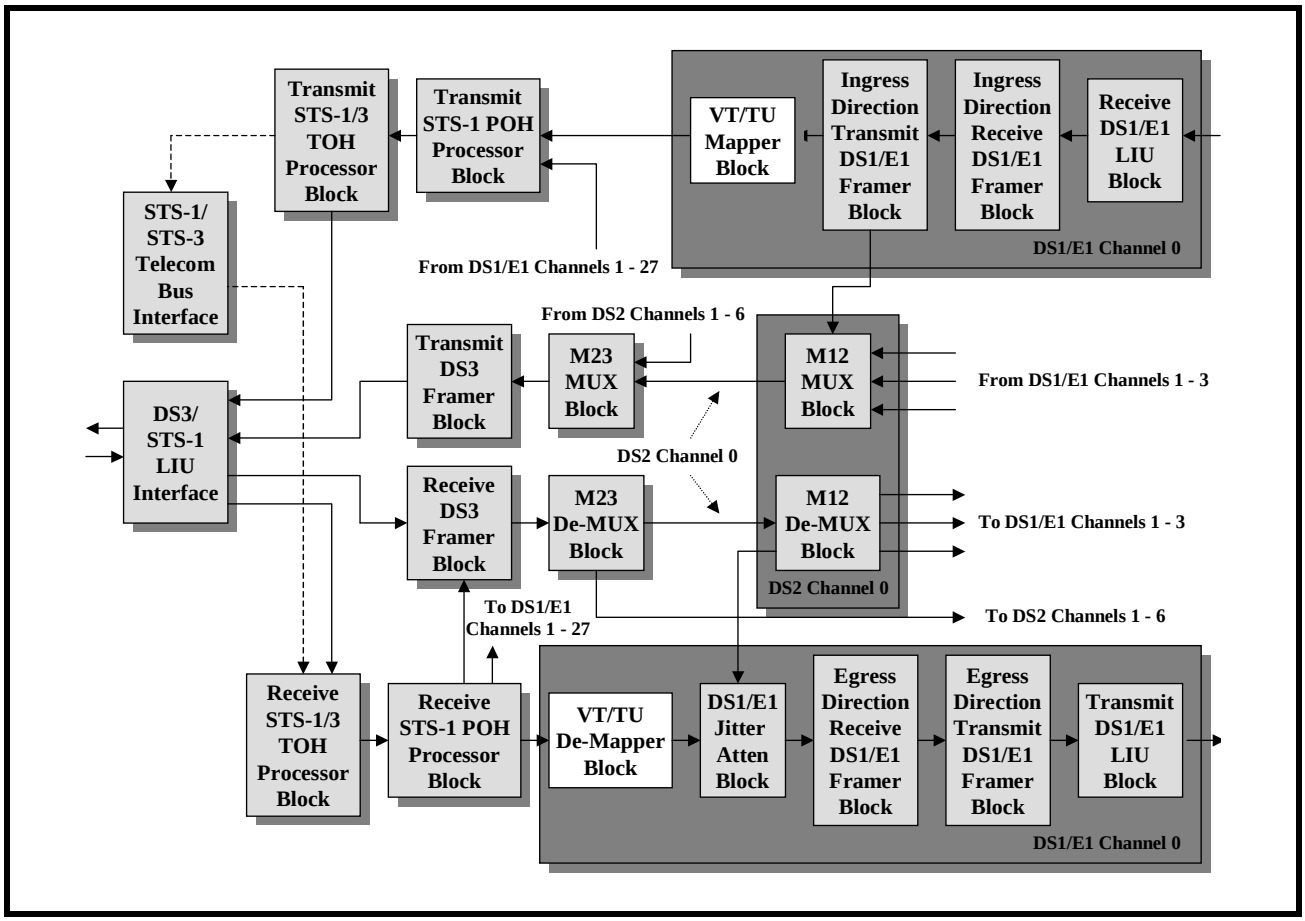


TABLE 437: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION DS1/E1 INSERTION CONTROL REGISTER - 2 (ADDRESS = 0XND41)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Transmit RDI-V Source[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT[7:2] - Unused:

BIT[1:0] - Transmit RDI-V Type[1:0]:

This READ/WRITE bit-field is used to specify the source of Bits 5, 6 and 7 (within the K4 VT-POH byte), whenever the Transmit VT-Mapper Block is configured to support the transmission of the Extended RDI-V indicators.

Transmit RDI-V Source

TRANSMIT RDI-V SOURCE[1:0]	RESULTING SOURCE OF BITS 5, 6 AND 7 OF K4 BYTE
00	Receive Status per the corresponding Receive VT-Mapper Block
01	From On-Chip Register

Transmit RDI-V Source

TRANSMIT RDI-V SOURCE[1:0]	RESULTING SOURCE OF BITS 5, 6 AND 7 OF K4 BYTE
10	Do Not Use
11	Receive Status per the corresponding Receive VT-Mapper Block

TABLE 438: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - DS1/E1 INSERTION CONTROL REGISTER - 1 (ADDRESS = 0XND42, WHERE N RANGES FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Ingress Direction DS1/E1 AIS Defect Declared	Unused	BIP-2 Error Insert	VT Signal Label[2:0]			Auto Transmit RFI-V Indicator	Auto Transmit RDI-V Indicator
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Receive (Ingress Direction) DS1/E1 AIS Defect Declared:

This READ/WRITE bit-field indicates whether or not the corresponding DS1 or E1 signal (that is being handled by this Transmit VT-Mapper block) is transporting the AIS indicator.

- 0 - Indicates that the Ingress Direction DS1 or E1 signal is NOT currently transporting the AIS indicator.
- 1 - Indicates that the Ingress Direction DS1 or E1 signal is currently transporting the AIS indicator.

BIT 6 - Unused

BIT 5 - BIP-2 Error Insert

This READ/WRITE bit-field is used to configure the corresponding VT-Mapper block to transmit VTs with erred BIP-2 bits into the "Ingress Direction VT-data-stream (towards the Transmit STS-1/STS-3 POH Processor block). If the user opts to invoke this feature, then the VT-Mapper block will automatically invert the value of the "locally-computed" BIP-2 bits (within each outbound VT), prior to transmitting this data to the Transmit STS-1/STS-3 POH Processor block.

- 0 - Configures the Transmit VT-Mapper block to NOT transmit VTs with erred BIP-2 bits to downstream circuitry (normal operation).
- 1 - Configures the Transmit VT-Mapper block to transmit VTs with erred BIP-2 bits to downstream circuitry(normal operation).

NOTE: *For normal operation, the user should set this bit-field to 0.*

BIT [4:2] - VT Label[2:0]:

These three (3) READ/WRITE bit-fields are used to set the VT Label bit-fields (within each outbound V5 byte) the value of the users choice.

BIT 1 - Auto Transmit RFI-V Indicator

This READ/WRITE bit-field is used to select the source of the RFI-V bit-field, within the V5 byte of the outbound VT1.5/VT2 traffic. In this case, the user has the following two options.

a. The user can configure the VT-Mapper block to use an on-chip register as the source of the RFI-V bit-fields (within the V5 byte). More specifically, the VT-Mapper block will read out the contents within Bit 7 (Transmit RFI-V Value) within the "VT-Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register (Address = 0xND43)" and it will load this value into RFI-V bit-field position within each outbound VT. In this case, the user will have Software Control over the state of the RFI-V bit-field, within the V5 byte of the outbound VT traffic) or

b. The Transmit VT-Mapper block will set the RFI-V bit-fields to the appropriate value, based upon any defect conditions that are currently being declared by the corresponding VT-De-Mapper block.

- 0 - Configures the Transmit VT-Mapper Block to use the on-chip register as the source of the RFI-V bit-field.

▶ 1 - Configures the Transmit VT-Mapper block to set the RFI-V bit-fields to the appropriate value, based upon any defects that the corresponding Receive VT-Mapper block is currently declaring.

BIT 0 - Auto Transmit RDI-V Indicator

This READ/WRITE bit-field is used to select the source of the RDI-V bit-field, within the V5 byte of each outbound VT1.5/VT2 traffic. In this case, the user has the following two options.

a. The user can configure the Transmit VT-Mapper block to use an on-chip register as the source of the RDI-V bit-fields (within the V5 byte). More specifically, the Transmit VT-Mapper block will read out the contents within BIT6 (Transmit RDI-V value) within the VT Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register (Address = 0xND43) and it will load this value into the RDI-V bit-field position within each outbound VT. In this case, the user will have Software Control over the state of the RDI-V bit-fields, within the outbound VT traffic) or

b. The Transmit VT-Mapper block will set the RDI-V bit-fields to the appropriate value, based upon any defect conditions that are currently being declared by the corresponding VT-De-Mapper block.

▶ 0 - Configures the Transmit VT-Mapper Block to use the on-chip register as the source of the RDI-V bit-field.

▶ 1 - Configures the Transmit VT-Mapper block to set the RDI-V bit-fields to the appropriate value, based upon any defects that the corresponding VT-De-Mapper block is currently declaring.

TABLE 439: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - DS1/E1 INSERTION CONTROL REGISTER - 0 (ADDRESS = 0XND43 , WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit RFI-V Value	Transmit RDI-V Value	Transmit AIS-V Indicator	DS1/E1 Cross Connect Channel Select_Ingress Direction[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Transmit RFI-V Value:

This READ/WRITE bit-field is used to exercise Software Control over the state of the RFI-V bit-field (within each V5 byte) of the outbound VT data-stream. If the user sets BIT 1 (Auto Transmit RFI-V Indicator), within the VT-Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register - 2 to 0, then the Transmit VT-Mapper block will read out the contents within this bit-field, and it will load this value into the RFI-V bit-field within each V5 byte of the outbound VT-data-stream.

NOTE: *This bit-field is ignored if the user sets Bit 1 (Auto Transmit RFI-V Indicator), within the VT Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register - 1 to 1.*

BIT6 - Transmit RDI-V Value:

This READ/WRITE bit-field is used to exercise Software Control over the state of the RDI-V bit-field (within each V5 byte) of the outbound VT data-stream. If the user sets BIT 0 (Auto Transmit RDI-V Indicator), within the VT-Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register - 2 to 0, then the Transmit VT-Mapper block will read out the contents within this bit-field, and it will load this value into the RDI-V bit-field within each V5 byte of the outbound VT-data-stream.

NOTE: *This bit-field is ignored if the user sets Bit 0 (Auto Transmit RDI-V Indicator), within the VT Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register - 1 to 1.*

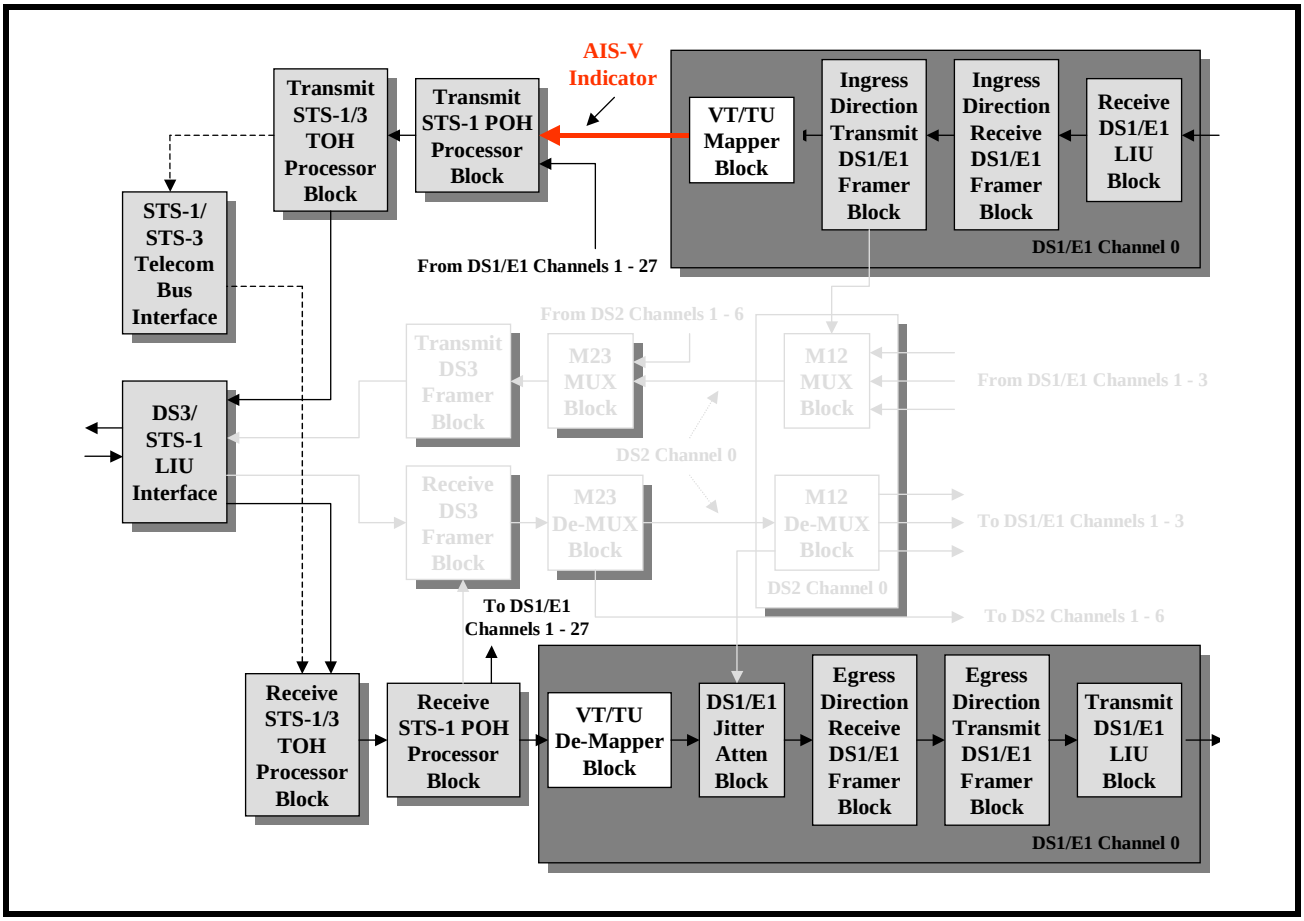
BIT 5 - Transmit AIS-V Indicator

This READ/WRITE bit-field is used to command the Transmit VT-Mappper block to transmit the AIS-V indicator (within the corresponding VT1.5 or VT2) within the outbound VT-data-stream.

0 - Configures the Transmit VT-Mapper block to NOT transmit the AIS-V indicator within the outbound VT-data-stream.

1 - Configures the Transmit VT-Mapper block to transmit the AIS-V indicator within the outbound VT-data-stream as shown in **Figure 20**.

FIGURE 20. AN ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328 WHENEVER THE VT-MAPPER BLOCK (ASSOCIATED WITH A GIVEN CHANNEL) HAS BEEN CONFIGURED TO TRANSMIT THE AIS-V INDICATOR TOWARDS DOWN-STREAM CIRCUITRY



BIT[4:0] - DS1/E1 (Cross-Connect) Channel Select[4:0]:

These READ/WRITE bit-fields is used to configure the Internal VT-Cross Connect. More specifically, these READ/WRITE bit-fields are used to select which (of the 28 Ingress Direction) T1/E1 signals to be mapped into either a VT1.5 or VT2 by this particular Transmit VT-Mapper block. The following table presents the relationship between the settings of these bit-fields and the resulting Cross Connect Configuration.

Cross Connect Configuration

DS1/E1 (CROSS-CONNECT) CHANNEL SELECT[4:0]	RESULTING INGRESS DIRECTION T1/E1 CHANNEL BEING HANDLED BY THIS PARTICULAR TRANSMIT VT-MAPPER BLOCK	COMMENTS
00000	NONE	This particular VT will be transmitted as an Un-equipped signal
00001	Ingress Direction T1/E1 Channel 1	
00010	Ingress Direction T1/E1 Channel 2	
00011	Ingress Direction T1/E1 Channel 3	
00100	Ingress Direction T1/E1 Channel 4	
00101	Ingress Direction T1/E1 Channel 5	

Cross Connect Configuration

DS1/E1 (Cross-Connect) Channel Select[4:0]	Resulting Ingress Direction T1/E1 Channel being handled by this particular Transmit VT-Mapper block	Comments
00110	Ingress Direction T1/E1 Channel 6	
00111	Ingress Direction T1/E1 Channel 7	
01000	Ingress Direction T1/E1 Channel 8	
01001	Ingress Direction T1/E1 Channel 9	
01010	Ingress Direction T1/E1 Channel 10	
01011	Ingress Direction T1/E1 Channel 11	
01100	Ingress Direction T1/E1 Channel 12	
01101	Ingress Direction T1/E1 Channel 13	
01110	Ingress Direction T1/E1 Channel 14	
01111	Ingress Direction T1/E1 Channel 15	
10000	Ingress Direction T1/E1 Channel 16	
10001	Ingress Direction T1/E1 Channel 17	
10010	Ingress Direction T1/E1 Channel 18	
10011	Ingress Direction T1/E1 Channel 19	
10100	Ingress Direction T1/E1 Channel 20	
10101	Ingress Direction T1/E1 Channel 21	
10110	Ingress Direction T1/E1 Channel 22	
10111	Ingress Direction T1/E1 Channel 23	
11000	Ingress Direction T1/E1 Channel 24	
11001	Ingress Direction T1/E1 Channel 25	
11010	Ingress Direction T1/E1 Channel 26	
11011	Ingress Direction T1/E1 Channel 27	
11100	Ingress Direction T1/E1 Channel 28	
11101	NONE	
11110	The Test Channel	
11111	Test Pattern - From VT Pattern Generator	

TABLE 440: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - DS1/E1 DROP CONTROL REGISTER - BYTE 3 (ADDRESS = 0XND44, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDI-V Accepted Value[3:0]				RDI-V Accept Threshold[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT[7:4] - RDI-V Accepted Value[3:0]:

These READ-ONLY bit-fields reflect the most recently value for RDI-V that has been accepted (or validated) by the VTDe--Mapper Block. The VT-De--Mapper block will accept (or validate) a given RDI-V value, once it has received this same RDI-V value, within RDI-V_Accept_Threshold[3:0] number of consecutive, incoming VT Multi-frames.

NOTES:

1. These bit-fields are only active if the user has configured the Receive VT-De-Mapper block to support ERDI-V (Enhanced RDI-V).

2. These bit-fields reflect the four-bit RDI-V value that the VT De-Mapper block has accepted via the K4 bytes within the incoming VT/TU data-stream.

BIT[3:0] - RDI-V Accept Threshold[3:0]:

These READ/WRITE bit-fields are used to define the RDI-V Validation criteria for the VT-De-Mapper block. More specifically, these bit-fields are used to specify the number of consecutive, incoming VT Multi-frame, in which the VT-De-Mapper block MUST receive a given RDI-V value BEFORE it validates it and loads it into BIT[7:4] (RDI-V Accepted Value[3:0]).

TABLE 441: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - DS1/E1 DROP CONTROL REGISTER - BYTE 2 (ADDRESS = 0XND45, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							RDI-V Type
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT[7:1] - Unused:

BIT 0 - RDI-V Type:

This READ/WRITE bit-field is used to configure the VT-De-Mapper blocks (associated with a given channel) to support either the SRDI-V (Single Bit - RDI-V) or ERDI-V (Extended - RDI-V) form of signaling. If the user uses only Single-Bit RDI-V, then the RDI-V indicator will only be transported via Bit 8 (RDI-V) within the V5 byte in a VT-data-stream. Conversely, if a user uses Extended RDI-V, then the RDI-V indicator will be transported via both Bits 8 (RDI-V) within the V5 byte, and Bits 5, 6 and 7 within the Z7/K4 byte.

- 0 - Configures the VT-De-Mapper blocks to use the SRDI-V form of Signaling.
- 1 - Configures the VT-De-Mapper blocks to use the ERDI-V form of signaling.

NOTE: *This configuration setting only applies to the VT-De-Mapper block. If the user wishes to configure the VT-Mapper block to support either the "SRDI-V" or the "ERDI-V" form of signaling, then he/she must set Bit 1 (RDI-V Type) within the "Channel Control - VT-Mapper Block - Ingress Direction - Transmit RDI-V Control Register - Byte 0" to the appropriate state.*

TABLE 442: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - ENGRESS DIRECTION - DS1/E1 DROP CONTROL REGISTER - BYTE 1 (ADDRESS = 0XND46, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	VT Size Error Defect Declared	LOP-V Defect Declared	Change in VT Label Value[2:0] Indicator	VT Label Value[2:0]			AIS-V Defect Declared
R/O	R/O	R/O	R/W1C	R/O	R/O	R/O	R/O
0	0	1	0	0	0	0	0

BIT7 -Unused:

BIT6 - VT Size ErroDefect Declared:

This READ-ONLY bit-field indicates whether or not the Receive VT-De-Mapper block is currently declaring the VT Size Error defect condition. The Receive VT-De-Mapper block will declare the VT Size Error defect condition anytime it receives a VT data-stream with V1 bytes that contains the incorrect VT-Size bit values, as depicted below.

- 0 - Indicates that the Receive VT-De-Mapper block is NOT currently declaring the VT Size Error Defect condition.
- 1 - Indicates that the Receive VT-De-Mapper block is currently declaring the VT Size Error Defect condition.

BIT 5 - LOP-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the Receive VT-Mapper block is currently declaring the LOP-V Defect condition.

- 0 - Indicates that the Receive VT-De-Mapper Block is currently NOT declaring the LOP-V Defect Condition.
- 1 - Indicates that the Receive VT-De-Mapper block is currently declaring the LOP-V Defect Condition

BIT 4 - Change in VT Label[2:0] Indicator:

This READ/WRITE 1 to CLEAR bit-field indicates whether or not the Receive VT-De-Mapper block has detected a Change in VT Signal Label, since the last time the user read and cleared this register bit

0 - Indicates that the Receive VT-De-Mapper block has NOT detected a Change in VT Signal Label since the last time the user read and cleared this register bit.

BIT[3:1] - VT Label Value[2:0]:

This READ-ONLY bit-field reflects the value of the most recently accepted (or validated) VT Signal Label value.

BIT 0 - AIS-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the Receive VT-De- Mapper block is currently declaring the AIS-V defect condition.

- 0 - Indicates that the Receive VT-De-Mapper Block is NOT currently declaring the AIS-V defect condition.
- 1 - Indicates that the Receive VT-De-Mapper Block is currently declaring the AIS-V defect condition.

TABLE 443: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - ENGRESS DIRECTION - DS1/E1 DROP CONTROL REGISTER - BYT E 0 (ADDRESS = 0XND47, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFI-V Defect Declared	RDI-V Defect Declared	Force DS1/E1 AIS In Egress Direction	DS1/E1 Cross Connect Channel Select_Egress Direction[4:0]				
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - RFI-V Defect Declared:

This READ/WRITE bit-field indicates whether or not the Receive VT-De-Mapper Block is currently declaring the RFI-V defect condition.

- 0 - Indicates that the Receive VT-De-Mapper Block is NOT currently declaring the RFI-V defect condition.
- 1 - Indicates that the Receive VT-De-Mapper Block is currently declaring the RFI-V defect condition.

BIT6 - RDI-V Defect Declared:

This READ/WRITE bit-field indicates whether or not the Receive VT-De-Mapper Block is currently declaring the RDI-V defect condition.

- 0 - Indicates that the Receive VT-De-Mapper Block is NOT currently declaring the RDI-V defect condition.
- 1 - Indicates that the Receive VT-De-Mapper Block is currently declaring the RDI-V defect condition.

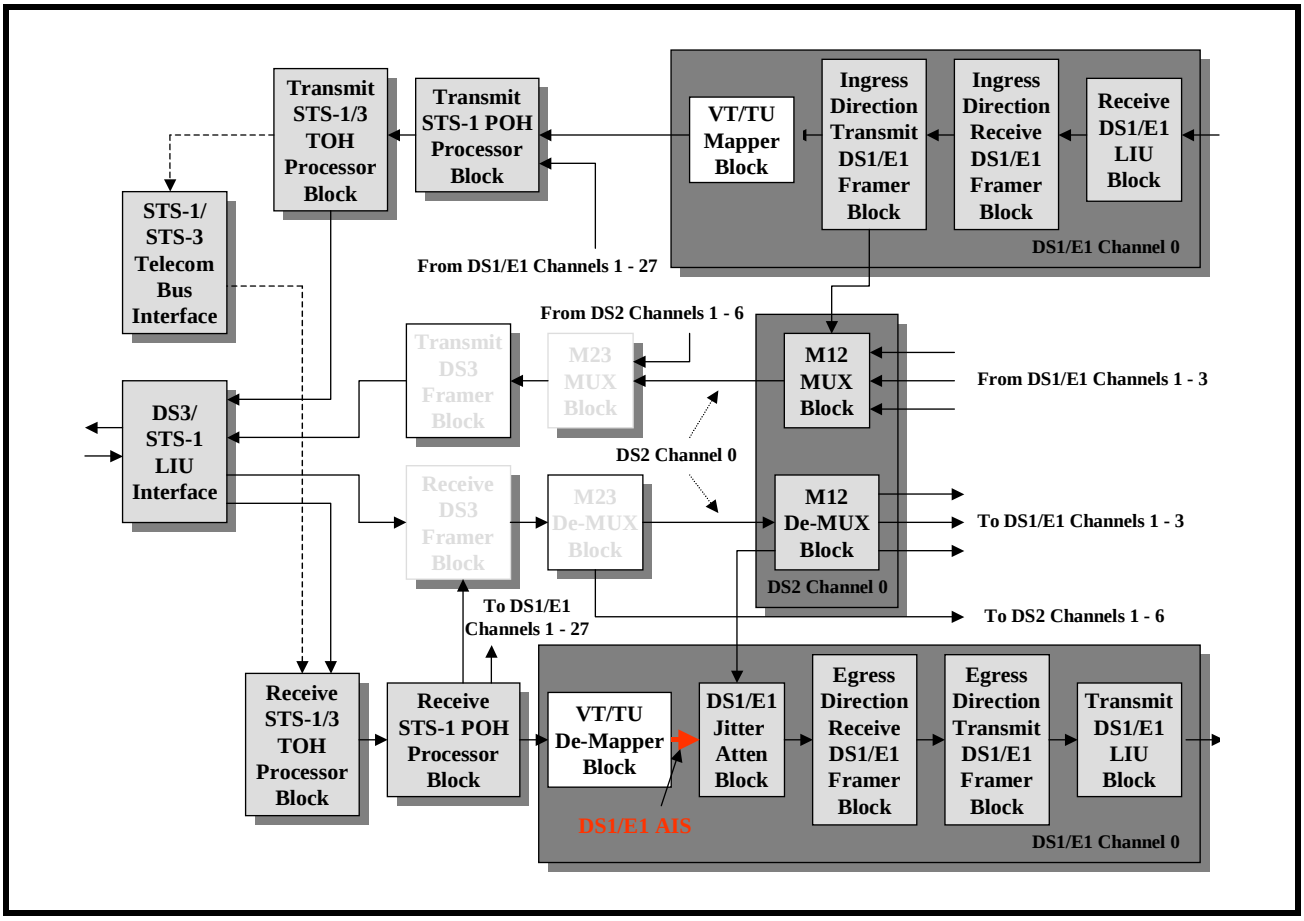
BIT 5 - Force DS1/E1 AIS In Egress Direction

This READ/WRITE bit-field is used to configure this particular Receive VT-De-Mapper block to transmit the DS1/E1 AIS indicator within the Egress Direction of this particular DS1/E1 Channel.

- 0 - Configures the Receive VT-De-Mapper Block to NOT transmit the DS1/E1 AIS Pattern within the Egress Direction corresponding to this particular channel.
- 1 - Configures the Receive VT-De-Mapper block to transmit the DS1/E1 AIS Pattern within the Egress Direction corresponding to this particular channel.

Figure 21 presents an illustration of the Functional Block Diagram of the XRT86SH328, whenever the VT-De-Mapper block has been configured to overwrite the contents within the corresponding DS1/E1 channel with the DS1/E1 AIS pattern (as it is being de-mapped from the VT1.5 or VT2 data-stream by the VT De-Mapper block.

FIGURE 21. AN ILLUSTRATION OF THE FUNCTIONAL BLOCK DIAGRAM OF THE XRT86SH328, WHENEVER THE VT-DE-MAPPER BLOCK (ASSOCIATED WITH A GIVEN CHANNEL) OVERWRITES THE CONTENTS OF A DE-MAPPED DS1/E1 SIGNAL WITH THE DS1/E1 AIS PATTERN



BIT[4:0] - DS1/E1 Cross Connect Channel Select_Egress Direction[4:0]:

These READ/WRITE bit-fields are used to configure the Internal VT-Cross Connect.

More specifically, these READ/WRITE bit-fields are used to select which (of the 28 Egress Direction) T1/E1 Ports, that this particular Receive VT-Mapper block will route (or direct) its Egress Direction T1/E1 Signal to.

The following table presents the relationship between the settings of these bit-fields and the resulting Cross-Connect Configuration.

Cross Connect Configuration

DS1/E1 (Cross Connect) Channel Select[4:0]	Resulting Port that this Receive VT-Mapper block will direct its T1/E1 Traffic to	Comments
00000	No Clock or Data is output via Corresponding Egress Direction T1/E1 Port	
00001	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 1	
00010	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 2	
00011	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 3	
00100	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 4	
00101	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 5	
00110	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 6	
00111	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 7	
01000	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 8	
01001	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 9	
01010	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 10	
01011	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 11	
01100	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 12	
01101	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 13	
01110	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 14	
01111	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 15	
10000	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 16	

Cross Connect Configuration

DS1/E1 (Cross Connect) Channel Select[4:0]	Resulting Port that this Receive VT-Mapper block will direct its T1/E1 Traffic to	Comments
10001	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 17	
10010	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 18	
10011	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 19	
10100	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 20	
10101	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 21	
10110	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 22	
10111	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 23	
11000	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 24	
11001	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 25	
11010	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 26	
11011	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 27	
11100	Egress Direction T1/E1 Signal is routed to the Egress Direction Output of T1/E1 Channel 28	
11101		
11110		
11111		

Table 444: Channel Control - VT-De-Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 1 (Address = 0xND4A, where N ranges in value from 0x01 to 0x1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT Payload Pointer Increment Count[3:0]				BIP-2 Error Count[11:8]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - 4 - VT Payload Pointer Increment Count[3:0]:

These RESET-upon-READ bit-fields reflect the number of VT Payload Pointer Increment events that the Receive VT-De-Mapper block has detected since the last read of this register. The Receive VT-Mapper block will increment the contents within these bit-fields each time that it detects a VT Payload Pointer Increment event within the incoming VT data-stream.

NOTE: The user must induce a "0 to 1 transition" within Bit 3 (Latch Count) within the "Global VT-Mapper Block - VT Mapper Block Control Register (Address = 0x0C03) prior to reading out the contents within these bit-fields.

BIT[3:0] - BIP-2 Error Count[11:8]:

These RESET-upon-READ bit-fields, along with those within the VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 0, presents a 12-bit expression that reflects the number of BIP-2 Errors that the Receive VT-Mapper Block has detected (within the incoming VT-data-stream) since the last read of this register.

These particular bit-fields are the four most significant bit-fields within this 12-bit expression.

NOTE: The user must induce a "0 to 1 transition" within Bit 3 (Latch Count) within the "Global VT-Mapper Block - VT De-Mapper Block Control Register (Address = 0x0C03) prior to reading out the contents within these bit-fields

TABLE 445: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - BIP-2 ERROR COUNT REGISTER - BYTE 0 (ADDRESS = 0XND4B, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIP-2 Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:0] - BIP-2 Error Count[7:0]:

These RESET-upon-READ bit-fields, along with those within the VT Mapper Block - Egress Direction - BIP-2 Error Count Register - Byte 1, presents a 12-bit expression that reflects the number of BIP-2 Errors that the Receive VT-De-Mapper Block has detected (within the incoming VT-data-stream) since the last read of this register.

These particular bit-fields are the eight least significant bit-fields within this 12-bit expression.

NOTE: The user must induce a "0 to 1 transition" within Bit 3 (Latch Count) within the "Global VT-Mapper Block - VT Mapper Block Control Register (Address = 0x0C03) prior to reading out the contents within these bit-fields.

TABLE 446: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - REI-V EVENT COUNT REGISTER - BYTE 1 (ADDRESS = 0XND4E, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT-Payload Pointer Decrement Count[3:0]				REI-V Event Count[11:8]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT [7:4] - VT Payload Pointer Decrement Count[3:0]:

These RESET-upon-READ bit-fields reflect the number of VT Payload Pointer Decrement events that the Receive VT-De-Mapper block has detected since the last read of this register. The Receive VT-Mapper block will increment the contents within these bit-fields each time that it detects a VT Payload Pointer Decrement event within the incoming VT data-stream.

NOTE: The user must induce a "0 to 1 transition" within Bit 3 (Latch Count) within the "Global VT-Mapper Block - VT Mapper Block Control Register (Address = 0x0C03) prior to reading out the contents within these bit-fields

BIT [3:0] - REI-V Event Count[11:8]:

These RESET-upon-READ bit-fields, along with those within the VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 0, presents a 12-bit expression that reflects the number of REI-V Events that the Receive VT-Mapper Block has detected (within the incoming VT-data-stream) since the last read of this register.

These particular bit-fields are the four most significant bit-fields within this 12-bit expression.

NOTE: The user must induce a "0 to 1 transition" within Bit 3 (Latch Count) within the "Global VT-Mapper Block - VT Mapper Block Control Register (Address = 0x0C03) prior to reading out the contents within these bit-fields.

TABLE 447: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - REI-V EVENT COUNT REGISTER - BYTE 0 (ADDRESS = 0XND4F, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-V Event Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT[7:0] - REI-V Event Count[7:0]:

These RESET-upon-READ bit-fields, along with those within the VT Mapper Block - Egress Direction - REI-V Event Count Register - Byte 1, presents a 12-bit expression that reflects the number of REI-V Events that the Receive VT-De-Mapper Block has detected (within the incoming VT-data-stream) since the last read of this register.

These particular bit-fields are the eight least significant bit-fields within this 12-bit expression.

NOTE: *The user must induce a "0 to 1 transition" within Bit 3 (Latch Count) within the "Global VT-Mapper Block - VT Mapper Block Control Register (Address = 0x0C03) prior to reading out the contents within these bit-fields.*

TABLE 448: CHANNEL CONTROL - VT-MAPPER BLOCK - EGRESS DIRECTION - RECEIVE APS REGISTER - BYTE 0 (ADDRESS = 0XND53, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Receive APS Value[3:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - 4 - Unused:

This READ/WTC bit-field indicates whether or not the Change of Receive APS Value event has occurred (within this Tributary) since the last time that the user has written a 1 to clear this bit-field. The Receive VT-De-Mapper block will declare the Change of Receive APS Value whenever it has accepted a new value from the K4 bytes within the incoming VT data-stream.

- 0 - Indicates that the Change of Receive APS Value event has NOT occurred since the last time the user has written a 1 to clear this bit-field.
- 1 - Indicates that the Change of Receive APS Value event has occurred since the last time the user has written a 1 to clear this bit-field.

BIT 3 - 0 - Receive APS Value[3:0]:

These four (4) READ-ONLY bit-field reflects the APS value that the VT-De-Mapper block has received (via Bits 1 through 4, within the K4 byte) and has validated.

TABLE 449: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT APS REGISTER - BYTE 2 (ADDRESS = 0XND56, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS1/E1 AIS - Event Mask	DS1/E1 LOC -Event Mask	Reserved		Transmit Elastic Store Overflow	Reserved		
R/W	R/O	R/O	R/O	RUR	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Change of DS1/E1 AIS Defect Condition - Event Mask:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of DS1/E1 AIS Defect Condition" event to/from causing the "Change of DS1/E1 AIS Defect Condition" interrupt to be generated. If the user enables this

feature, then the VT-Mapper block will assert the "Change of DS1/E1 AIS Defect Condition" interrupt in response to either of the following conditions.

- Whenever the VT-Mapper block declares the "DS1/E1 AIS" defect condition within the Ingress Direction DS1/E1 Data-stream.
- Whenever the VT-Mapper block clears the "DS1/E1 AIS" defect condition within the Ingress Direction DS1/E1 Data Stream.

▶ 0 - Configures the VT-Mapper Block to NOT generate the "Change of DS1/E1 AIS Defect Condition" interrupt, whenever it declares or clears the DS1/E1 AIS defect condition.

▶ 1 - Configures the VT-Mapper Block to generate the "Change of DS1/E1 AIS Defect Condition" interrupt, whenever it declares or clears the "DS1/E1 AIS defect condition.

BIT 6 - 4 Reserved:

BIT 3 - Transmit Elastic Store Overflow:

This RESET-upon-READ bit-field indicates whether or not the VT Mapper block has declared a "Transmit Elastic Store Overflow" event since the last read of this register. The VT-Mapper Block will declare a "Transmit Elastic Store Overflow" event anytime that the "Transmit FIFO" (within the VT-Mapper block) has experience an "overflow" event.

▶ 0 - Indicates that the "Transmit Elastic Store Overflow" event has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Transmit Elastic Store Overflow" event has occurred since the last read of this register.

NOTE: *The VT-Mapper block will typically handle "small timing offsets" (between the Ingress Direction T1/E1 signal and the "Transmit Direction" 19.44MHz or 51.84MHz clock signal via bit-stuffing (as it maps this T1/E1 data into VTs. However, if this bit-field is set to "1", this is typically a indication of a significant clock frequency accuracy problem within the system.*

BIT 0 - Reserved:

TABLE 450: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT APS/K4 REGISTER (ADDRESS = 0XND57, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	TxERDI]			TxAPS[3:0			
R/W	R/W	R/W	R/W	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - Unused:

BIT 6 - 4 - Transmit ERDI-V[2:0]

These three (3) READ/WRITE bit-fields permit the user to exercise software control over the value of the "ERDI-V" bits that are transported via "Bits 5 through 7" (within the K4 byte) within the outbound VT data-stream.

NOTE: *This bit-field is only active if both of the following is true.*

a. The user has configured VT-Mapper/De-Mapper blocks to support the ERDI-V (Extended - RDI-V) form of signaling and,

b. The user has set Bit 6 (Transmit RDI-V Value) within the "Channel Control - VT Mapper Block - Ingress Direction - DS1/E1 Insertion Control Register - 0" to "1".

BIT 3 - 0 - Transmit APS Value[3:0]

These four (4) READ/WRITE bit-fields permit the user to exercise software control over the value of the "APS" bits that are transported via Bits 1 through 4 (within the K4 byte) within the outbound VT data-stream

TABLE 451: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - J2 BYTE STATUS REGISTER (ADDRESS = 0XND63, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					TIM-V Defect Declared	VT Path Trace Message Unstable Defect Declared	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT 7 - 3 - Unused:

BIT 2 - TIM-V Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "VT Trace Identification Mismatch" (TIM-V) defect condition.

The VT-De-Mapper block will declare the TIM-V defect condition, when none of the received 1, 16 or 64-byte string (received via the J2 byte, within the incoming VT-data-stream) matches the expected 1, 16 or 64 byte message.

The VT-De-Mapper block will clear the "TIM-V" defect condition, when 80% of the received 1, 16 or 64 byte string (received via the J2 byte) matches the 1, 16 or 64 byte message.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the TIM-V defect condition.
- 1 - Indicates that the VT-De-Mapper block is currently declaring the TIM-V defect condition.

BIT 1 - VT Path Trace Message Unstable Defect Declared:

This READ-ONLY bit-field indicates whether or not the VT-De-Mapper block is currently declaring the "VT Path Trace Message Unstable" defect condition. The VT-De-Mapper block will declare the "VT Path Trace Message Unstable" defect condition, whenever the "VT Path Trace Message Unstable" counter reaches the value "8". The VT-De-Mapper block will increment the "VT Path Trace Message Unstable" counter for each time that it receives a "VT Path Trace Message" that differs from the previously received message. The "VT Path Trace Message Unstable" counter is cleared to "0" whenever the VT-De-Mapper block has received a given "VT Path Trace Message" 3 (or 5) consecutive times.

- 0 - Indicates that the VT-De-Mapper block is NOT currently declaring the "VT:Path Trace Message Unstable" defect condition.
- 1 - Indicates that the VT De-Mapper block is currently declaring the "VT Path Trace Message Unstable" defect condition.

NOTE: *The VT-De-Mapper block will also set this bit-field "0" anytime it receives a given "VT Path Trace Message" 3 (or 5) consecutive times.*

BIT 0 - Unused:

TABLE 452: CHANNEL CONTROL - VT-MAPPER BLOCK - EGRESS DIRECTION - COMPOSITE STATUS REGISTER - BYTE 0 (ADDRESS = 0XND64, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of Receive APS Value - Composite	Elastic Store Overflow Event - Composite
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

Bits 7 - 2: Unused:

Bit 1 - Change of Receive APS Value Interrupt:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of

Receive APS Value" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt whenever it has "accepted" a new "APS" value (from the K4 bytes within the incoming VT-data-stream).

- 0 - Indicates that the "Change of Receive APS Value" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of Receive APS Value" Interrupt has occurred since the last read of this register.

Bit 0 - Transmit or Receive Elastic Store Overflow Event Interrupt:

This RESET-upon-READ bit-field indicates whether or not the "VT Mapper/VT-De-Mapper" block has generated the "Elastic Store Overflow Event" Interrupt since the last read of this register. The VT-Mapper/De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the "Transmit FIFO" within the VT-Mapper Block, experiences an overflow event.
- Whenever the "Receive FIFO" within the VT-De-Mapper Block, experiences an overflow event.

- 0 - Indicates that the channel has NOT generated an "Elastic Store Overflow" Interrupt since the last read of this register.
- 1 - Indicates that the channel has generated an "Elastic Store Overflow" interrupt since the last read of this register.

TABLE 453: CHANNEL CONTROL - VT-MAPPER BLOCK - EGRESS DIRECTION - COMPOSITE STATUS REGISTER - BYTE 0 (ADDRESS = 0XND65, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT Size Error Interrupt Status	Change of LOP-V Defect Condition Interrupt Status	Change of RFI-V Defect Condition Interrupt Status	Change of RDI-V Defect Condition Interrupt Status	Change of AIS-V Fail-ure Condition Interrupt Status	Change of AIS-V Defect Condition Interrupt Status	Change of VT Label Interrupt Status	Change of DS1/E1 AIS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Bit 7 - VT Size Error Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "VT Size Error" Interrupt since the last read of this register. The VT-De-Mapper block will generate the "VT Size Error" Interrupt anytime it declares the "VT Size Error" defect condition.

- 0 - Indicates that the VT Size Error Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the VT Size Error Interrupt has occurred since the last read of this register.

Bit 6 - Change of LOP-V Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of LOP-V Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the LOP-V defect condition
- Whenever the VT-De-Mapper block clears the LOP-V defect condition.

- 0 - Indicates that the "Change of LOP-V Defect Condition" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of LOP-V Defect Condition" Interrupt has occurred since the last read of this register.

Bit 5 - Change of RFI-V Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of RFI-V Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the RFI-V defect condition
- Whenever the VT-De-Mapper block clears the RFI-V defect condition.

- 0 - Indicates that the "Change of RFI-V Defect Condition" Interrupt has NOT occurred since the last read of this

register.

- 1 - Indicates that the "Change of RFI-V Defect Condition" Interrupt has occurred since the last read of this register.

Bit 4 - Change of RDI-V Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of RDI-V Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the RDI-V defect condition
- Whenever the VT-De-Mapper block clears the RDI-V defect condition.

- 0 - Indicates that the "Change of RDI-V Defect Condition" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of RDI-V Defect Condition" Interrupt has occurred since the last read of this register.

Bit 3 - Change of AIS-V Failure Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of AIS-V Failure Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the AIS-V failure condition
- Whenever the VT-De-Mapper block clears the AIS-V failure condition.

- 0 - Indicates that the "Change of AIS-V Failure Condition" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of AIS-V Failure Condition" Interrupt has occurred since the last read of this register.

Bit 2 - Change of AIS-V Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of AIS-V Defect Condition" Interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the AIS-V defect condition
- Whenever the VT-De-Mapper block clears the AIS-V defect condition.

0 - Indicates that the "Change of AIS-V Defect Condition" Interrupt has NOT occurred since the last read of this register.

1 - Indicates that the "Change of AIS-V Defect Condition" Interrupt has occurred since the last read of this register.

Bit 1 - Change of VT Label Value Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "Change of VT Label Value" Interrupt has occurred since the last read of this register. The VT-De-Mapper block will generate this interrupt anytime it has "accepted" a new VT Label value (that it has received via the V5 byte within the incoming VT data-stream).

- 0 - Indicates that the "Change of VT Label Value" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of VT Label Value" Interrupt has occurred since the last read of this register.

Bit 0 - Change of DS1/E1 AIS Defect Condition Interrupt Status

This RESET-upon-READ bit-field indicates whether or not the "Change of DS1/E1 AIS Defect Condition" Interrupt has occurred since the last read of this register. The VT-Mapper block will generate this interrupt in response to any one of the following conditions.

- Whenever the VT-Mapper block declares the DS1/E1 AIS Defect (with the Ingress Direction T1/E1 traffic).
- Whenever the VT-Mapper block clears the DS1/E1 AIS Defect (within the Ingress Direction T1/E1 traffic)

- 0 - Indicates that the "Change of DS1/E1 AIS Defect Condition" Interrupt has NOT occurred since the last read of this register.
- 1 - Indicates that the "Change of DS1/E1 AIS Defect Condition" Interrupt has occurred since the last read of this register.

TABLE 454: CHANNEL CONTROL - VT-MAPPER BLOCK - EGRESS DIRECTION - INTERRUPT STATUS REGISTER (ADDRESS = 0XND67, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change of VT Path Trace Message Unstable Defect Condition Interrupt Status	New VT Path Trace Message Interrupt Status	Change of TIM-V Defect Condition Interrupt Status	Unused		
R/O	R/O	RUR	RUR	RUR	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bits 7 - 6 - Unused:

Bit 5 - Change of VT Path Trace Message Unstable Defect Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever the VT-De-Mapper block declares the "VT Path Trace Message Unstable" Defect condition.
- Whenever the VT De-Mapper block clears the "VT Path Trace Message Unstable" Defect condition.

▶ 0 - Indicates that the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.

Bit 4 - New VT Path Trace Message Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "New VT Path Trace Message" Interrupt has occurred since the last read of this register. The VT-De-Mapper block will generate this interrupt whenever it has "accepted" a new "VT Path Trace Message" via the incoming VT-data-stream.

▶ 0 - Indicates that the "New VT Path Trace Message" Interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "New VT Path Trace Message" Interrupt has occurred since the last read of this register.

Bit 3 - Change of TIM-V Defect Condition Interrupt Status:

This RESET-upon-READ bit-field indicates whether or not the "VT-De-Mapper" block has generated the "Change of TIM-V Defect Condition" interrupt since the last read of this register. The VT-De-Mapper block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the TIM-V Defect condition.
- Whenever it clears the TIM-V Defect condition.

▶ 0 - Indicates that the "Change of TIM-V Defect Condition" interrupt has NOT occurred since the last read of this register.

▶ 1 - Indicates that the "Change of TIM-V Defect Condition" interrupt has occurred since the last read of this register.

Bits 2 - 0 - Unused:

TABLE 455: CHANNEL CONTROL - VT-MAPPER BLOCK - EGRESS DIRECTION - INTERRUPT ENABLE REGISTER (ADDRESS = 0XND68, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of Receive APS Value Interrupt Enable	Elastic Store Overflow Event Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 2: Unused:

Bit 1 - Change of Receive APS Value Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of Receive APS Value" Interrupt. If the user enables this interrupt, then the VT-De-Mapper block will generate this interrupt anytime it has "accepted" a new APS value (via the K4 byte within the incoming VT-data-stream).

- 0 - Disables the "Change of Receive APS Value" Interrupt.
- 1 - Enables the "Change of Receive APS Value" Interrupt.

Bit 0 - Transmit or Receive Elastic Store Overflow Event Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Elastic Store Overflow Event" interrupt. If the user enables this interrupt, then the channel will generate this interrupt in response to either of the following conditions.

- Whenever the "Transmit FIFO" within the VT-Mapper Block, experiences an overflow event.
- Whenever the "Receive FIFO" within the VT-De-Mapper block, experiences an overflow event.

- 0 - Disables the "Elastic Store Overflow Event" Interrupt
- 1 - Enables the "Elastic Store Overflow Event" Interrupt

TABLE 456: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - INTERRUPT ENABLE REGISTER (ADDRESS = 0XND69, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VT Size Error Interrupt Enable	Change of LOP-V Defect Condition I nterrupt Enable	Change of RFI-V Defect Condition Interrupt Enable	Change of RDI-V Defect Condition Interrupt Enable	Change of AIS-V Failure Condition Interrupt Enable	Change of AIS-V Defect Condition Interrupt Enable	Change of VT Label Interrupt Enable	Change of DS1/E1 AIS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - VT Size Error Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "VT Size Error" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt anytime it declares the "VT Size Error" defect condition.

- 0 - Disables the "VT Size Error" Interrupt.
- 1 - Enables the "VT Size Error" Interrupt.

Bit 6 - Change of LOP-V Defect Condition Interrupt Enable

This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOP-V Defect Condition"

Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the LOP-V Defect Condition
- Whenever it clears the LOP-V Defect condition

▶ 0 - Disables the "Change of LOP-V Defect Condition" Interrupt

▶ 1 - Enables the "Change of LOP-V Defect Condition" Interrupt

Bit 5 - Change of RFI-V Defect Condition Interrupt Enable

This READ/WRITE bit-field permits the user to either enable or disable the "Change of RFI-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the RFI-V Defect Condition
- Whenever it clears the RFI-V Defect condition

▶ 0 - Disables the "Change of RFI-V Defect Condition" Interrupt

▶ 1 - Enables the "Change of RFI-V Defect Condition" Interrupt

Bit 4 - Change of RDI-V Defect Condition Interrupt Enable

This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the RDI-V Defect Condition
- Whenever it clears the RDI-V Defect condition

▶ 0 - Disables the "Change of RDI-V Defect Condition" Interrupt

▶ 1 - Enables the "Change of RDI-V Defect Condition" Interrupt

Bit 3 - Change of AIS-V Failure Condition Interrupt Enable

This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-V Failure Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the AIS-V Failure Condition
- Whenever it clears the AIS-V Failure condition

▶ 0 - Disables the "Change of AIS-V Failure Condition" Interrupt

▶ 1 - Enables the "Change of AIS-V Failure Condition" Interrupt

Bit 2 - Change of AIS-V Defect Condition Interrupt Enable

This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-V Defect Condition" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt in response to either of the following conditions.

- Whenever it declares the AIS-V Defect Condition
- Whenever it clears the AIS-V Defect condition

▶ 0 - Disables the "Change of AIS-V Defect Condition" Interrupt

▶ 1 - Enables the "Change of AIS-V Defect Condition" Interrupt

Bit 1 - Change of VT Label Value Interrupt Enable

This READ/WRITE bit-field permits the user to either enable or disable the "Change of VT Label Value" Interrupt. If the user enables this interrupt, then the "VT-De-Mapper" block will generate this interrupt anytime it has "accepted" a new "VT Label Value" via the V5 bytes within the incoming VT-data-stream.

▶ 0 - Disables the "Change of VT Label Value" Interrupt.

▶ 1 - Enables the "Change of VT Label Value" Interrupt.

Bit 0 - Change of DS1/E1 AIS Defect Condition Interrupt Enable

This READ/WRITE bit-field permits the user to either enable or disable the "Change of DS1/E1 AIS Defect Condition" interrupt. If the user enables this interrupt, then the "VT-Mapper" block will generate this interrupt in response to either

of the following events.

- Whenever it declares the DS1/E1 AIS defect condition.
- Whenever it clears the DS1/E1 AIS defect condition

▶ 0 - Disables the "Change of DS1/E1 AIS Defect Condition" interrupt.

▶ 1 - Enables the "Change of DS1/E1 AIS Defect Condition" interrupt.

TABLE 457: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - INTERRUPT ENABLE REGISTER (ADDRESS = 0XND6B, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Change of VT Path Trace Message Unstable Defect Condition Interrupt Enable	New VT Path Trace Message Interrupt Status	Change of TIM-V Defect Condition Interrupt Status	Unused		
R/O	R/O	RUR	RUR	RUR	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bits 7 - 6 - Unused:

Bit 5 - Change of VT Path Trace Message Unstable Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of VT Path Trace Message Unstable Defect Condition" interrupt. If the user enables this interrupt, then the VT-De-Mapper block will generate this interrupt in response to either of the following events.

- Whenever the VT-De-Mapper block declares the "VT-Path Trace Message Unstable" defect condition.
- Whenever the VT-De-Mapper block clears the "VT-Path Trace Message Unstable" defect condition.

▶ 0 - Disables the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt.

▶ 1 - Enables the "Change of VT Path Trace Message Unstable Defect Condition" Interrupt.

Bit 4 - New VT Path Trace Message Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "New VT Path Trace Message" Interrupt. If the user enables this interrupt, then the VT-De-Mapper block will generate this interrupt whenever it has "accepted" a new "VT Path Trace Message" via the incoming VT-data-stream.

▶ 0 - Disables the "New VT Path Trace Message" Interrupt.

▶ 1 - Enables the "New VT Path Trace Message" Interrupt

Bit 3 - Change of TIM-V Defect Condition Interrupt Enable:

This READ/WRITE bit-field permits the user to either enable or disable the "Change of TIM-V Defect Condition" Interrupt. If the user enables this interrupt, then the VT-De-Mapper block will generate this interrupt in response to either of the following events.

- Whenever it declares the TIM-V Defect Condition
- Whenever it clears the TIM-V Defect Condition

▶ 0 - Disables the "Change of TIM-V Defect Condition" Interrupt

▶ 1 - Enables the "Change of TIM-V Defect Condition" Interrupt

Bits 2 - 0 - Unused:

TABLE 458: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - VT-PATH TRACE BUFFER CONTROL REGISTER (ADDRESS = 0XND71, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Unused	Receive VT Path Trace Message Buffer Select	VT Path Trace Message Accept Threshold	VT Path Trace Message Type	VT Path Trace Message Length[1:0]	
R/W	R/W	RUR	RUR	RUR	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit 7 - 6 - Reserved

For Normal Operation, please set these two bit-fields to "0".

Bit 5 - Unused

Bit 4 - Receive VT Path Trace Message Buffer Select:

This READ/WRITE bit-field permits a user to specify which of the following "Receive VT Path Trace Message" buffer segments that the Microprocessor will read out whenever it reads out the contents of the Receive Path Trace Message buffer.

a. The "Actual" Receive VT Path Trace Message Buffer. The "Actual" Receive VT Path Trace Message Buffer contains the contents of the most recently received (and accepted) VT Path Trace Messages via the incoming VT-data-stream.

b. The "Expected" Receive VT Path Trace Message Buffer. The "Expected" Receive Path Trace Message Buffer contains the contents of the "VT Path Trace Message" that the user "expects" to receive. The contents of this particular buffer are usually specified by the user.

- 0 - Configures the chip to return the contents of the "Actual" Receive VT Path Trace Message" Buffer, whenever the user executes a READ to the "Receive VT Path Trace Message" Buffer.
- 1 - Configures the chip to return the contents of the "Expected" Receive VT Path Trace Message" Buffer, whenever the user executes a READ to the "Receive VT Path Trace Message" Buffer.

Bit 3 - Receive VT Path Trace Message Accept Threshold

This READ/WRITE bit-field permits a user to select the number of consecutive times that the "VT-De-Mapper" block must receive a given "VT Path Trace Message" before it is "validated" and loaded into the "Actual" Receive VT Path Trace Message Buffer, as described below.

- 0 - Configures the VT-De-Mapper block to "validate" the incoming VT Path Trace Message after it has received it the third time in succession.
- 1 - Configures the VT-De-Mapper block to "validate" the incoming VT Path Trace Message after it has received it the fifth time in succession.

Bit 2 - Receive VT Path Trace Message Type

This READ/WRITE bit-field permits the user to specify how the "VT-De-Mapper" block will locate the boundary of the incoming VT Path Trace Message (within the incoming VT-data-stream) as depicted below.

- 0 - Configures the VT-De-Mapper block to expect the "VT Path Trace Message" boundary to be denoted by a "Line Feed" character.
- 1 - Configures the VT-De-Mapper block to except the "VT Path Trace Message" boundary to be denoted by the presence of a "1" in the "MSB" (Most Significant bit) of the first byte (within the incoming VT Path Trace Message). In this case, all of the remaining bytes (within the incoming VT Path Trace Message) will each have a "0" within their MSBs.

Bits 1 - 0 - VT Path Trace Message Length[1:0]:

These READ/WRITE bit-fields permit the user to specify the length of the "Receive VT Path Trace Message that the "VT-De-Mapper" block will accept and load into the "Actual" Receive VT Path Trace Message Buffer. The relationship between the contents of these bit-fields and the corresponding "Receive VT Path Trace Message" Length is presented

below.

VT Path Trace Message Length[1:0]	Resulting VT Path Trace Message Length (Bytes)
00	1
01	16
1X	64

Table 459: Channel Control - VT-De-Mapper Block - Egress Direction - Auto AIS Control Register - Byte 1 (Address = 0xND72, where N ranges in value from 0x01 to 0x1C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused		Auto Transmit AIS-V upon AIS-V Defect	Auto Transmit AIS-V upon UNEQ-V Defect	Unused	Auto Transmit AIS-V upon LOP-V Defect	Auto Transmit AIS-V upon PLM-V Defect	Unused
R/O	R/O	R/W	R/W	R/O	R/W	R/W	R/O
0	0	0	0	0	0	0	0

Bits 7 - 6 - Unused:

Bit 5 - Auto Transmit AIS-V upon AIS-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit T1/E1 LIU Block), anytime (and for the duration that) it declares the AIS-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the AIS-V defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the AIS-V defect condition.

Note: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

Bit 4 - Auto Transmit AIS-V upon UNEQ-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit T1/E1 LIU Block), anytime (and for the duration that) it declares the UNEQ-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the UNEQ-V defect condition.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the UNEQ-V defect condition.

Note: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

Bit 3 - Unused:

Bit 2 - Auto Transmit AIS-V upon LOP-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit T1/E1 LIU Block), anytime (and for the duration that) it declares the LOP-V defect condition within the incoming VT-data-stream.

- 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the LOP-V defect condition.

▶ 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the LOP-V defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

Bit 1 - Auto Transmit AIS-V upon PLM-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit T1/E1 LIU Block), anytime (and for the duration that) it declares the PLM-V defect condition within the incoming VT-data-stream.

▶ 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the PLM-V defect condition.

▶ 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the PLM-V defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

Bit 0 - Unused:

TABLE 460: CHANNEL CONTROL - VT-DE-MAPPER BLOCK - EGRESS DIRECTION - AUTO AIS CONTROL REGISTER - BYTE 0 (ADDRESS = 0XND73, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Auto Transmit AIS-V upon VT Path Trace Message Unstable Defect	Auto Transmit AIS-V upon TIM-V Defect	Reserved (Set to "[0, 0, 0, 0, 0]" for Normal Operation)					Auto Transmit AIS-V Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit 7 - Auto Transmit AIS-V upon VT Path Trace Message Unstable Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit T1/E1 LIU Block), anytime (and for the duration that) it declares the VT Path Trace Message Unstable defect condition within the incoming VT-data-stream.

▶ 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the VT Path Trace Message Unstable defect condition.

▶ 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the VT Path Trace Message Unstable defect condition.

NOTE: *The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.*

Bit 6 - Auto Transmit AIS-V upon TIM-V Defect:

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator via the "Egress Direction" traffic (e.g., towards the Transmit T1/E1 LIU Block), anytime (and for the duration that) it declares the TIM-V defect condition within the incoming VT-data-stream.

▶ 0 - Does not configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TIM-V defect condition.

▶ 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream" traffic) whenever it declares the TIM-V defect condition.

NOTE: The user must also set Bit 0 (Auto Transmit AIS-V Enable) within the "Channel Control - VT-De-Mapper Block - Egress Direction - Receive VT Auto AIS Control" Register to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator, in response to this defect condition.

Bits 5 - 1 - Reserved:

Please set each of these bit-fields to "0" for normal operation.

Bit 0 - Auto Transmit AIS-V Enable

This READ/WRITE bit-field permits the user to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the down-stream traffic) whenever (and for the duration that) it declares either the AIS-V, LOP-V, TIM-V, UNEQ-V, PLM-V or "VT Path Trace Message Unstable" defect conditions.

- 0 - Configures the VT-De-Mapper block to NOT automatically transmit the AIS-V indicator (via the "downstream traffic) upon declaration of any of the "above-mentioned" defect conditions.
- 1 - Configures the VT-De-Mapper block to automatically transmit the AIS-V indicator (via the "downstream traffic) upon declaration of any of the "above-mentioned" defect conditions.

NOTE: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the VT-De-Mapper block to automatically transmit the AIS-V indicator upon detection of a given alarm/defect condition.

TABLE 461: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT J2 BYTE VALUE REGISTER (ADDRESS = 0XND76, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit J2 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 - Transmit J2 Byte Value[7:0]:

These READ/WRITE bit-fields permit the user to have software control over the value of the J2 byte, within the outbound VT data-stream.

If the user configures the VT-Mapper block to use this register as the source of the J2 byte, then it will automatically write the contents of this register into the J2 byte location, within each "outbound" VT multi-frame.

This feature is enabled whenever the user writes the value "[1, 0]" into Bits 1 and 0 (Transmit VT-Path Trace Message Source[1:0]) within the "Channel Control - VT Mapper Block - Ingress Direction - VT Path Trace Message Control" Register.

TABLE 462: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT N2 BYTE VALUE REGISTER (ADDRESS = 0XND77, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit N2 Byte Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 0 - Transmit N2 Byte Value[7:0]:

These READ/WRITE bit-fields permit the user to have software control over the value of the N2 byte, within the outbound VT data-stream.

The VT-Mapper block will (unconditionally) use this register as the source of the N2 byte, then it will automatically write the contents of this register into the J2 byte location, within each "outbound" VT multi-frame.

TABLE 463: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT VT-PATH TRACE MESSAGE CONTROL REGISTER (ADDRESS = 0XND79, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved		Unused		Transmit VT Path Trace Message Length[1:0]		Transmit VT Path Trace Message Source[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bits 7 - 6 - Reserved:

NOTE: *The user must set these two bits to "[0, 0]" for normal operation.*

Bit 5 - TxAIS:

Bit 4 - Unused:

Bits 3 - 2 - Transmit VT Path Trace Message Length[1:0]:

These READ/WRITE bit-fields permit the user to specify the length of the VT Path Trace Message that the VT-Mapper block will repeatedly transmit to the remote VT PTE. The relationship between the contents of these bit-fields and the corresponding VT Path Trace Message Length is presented below.

TRANSMIT VT PATH TRACE MESSAGE LENGTH[1:0]	RESULTING VT PATH TRACE MESSAGE LENGTH (IN TERMS OF BYTES)
00	1 Byte
01	16 Bytes
1X	64 Bytes

Bits 1 - 0 - Transmit VT Path Trace Message Source[1:0]:

These READ/WRITE bit-fields permit the user to specify the source of the "outbound" VT Path Trace Message that will transported via the J2 byte channel (within the outbound VT-data-stream) as depicted below.

TRANSMIT VT PATH TRACE MESSAGE SOURCE[1:0]	RESULTING SOURCE OF THE VT PATH TRACE MESSAGE
00	Fixed Value:The VT-Mapper block will automatically set the J2 byte, within the each outbound VT-multi-frame to the value "0x01".
01	The Transmit VT Path Trace Message Buffer:The VT-Mapper Block will read out the contents within the "Transmit VT-Path Trace Message" Buffer, and will transmit this message to the remote VT PTE.
10	From the "Transmit J2 Byte Value[7:0]" Register:In this setting, the VT-Mapper block will read out the contents of the "Transmit J2 Byte Value Register, and will insert this value into the J2 byte-position within each outbound VT-multi-frame.
11	DO NOT USE

TABLE 464: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT RDI-V CONTROL REGISTER - BYTE 3 (ADDRESS = 0XND84, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	PLM-V RDI CODE[2:0]	Transmit RDI-V upon PLM-V					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

Bits 7 - 4 - Unused:

Bits 3- 1 - PLM-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the PLM-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 0 (Transmit RDI-V upon PLM-V) within this register to "1".*

Bit 0 - Transmit RDI-V upon PLM-V

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 3 through 1 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the PLM-V defect condition.

TABLE 465: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT RDI-V CONTROL REGISTER - BYTE 2 (ADDRESS = 0XND85, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-V RDI CODE[2:0]			Transmit RDI-V upon TIM-V	UNEQ-V RDI CODE[2:0]			Transmit RDI-V upon UNEQ-V
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	1	1	0	0

Bits 7 - 5 - TIM-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the TIM-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 0 (Transmit RDI-V upon TIM-V) within this register to "1".*

Bit 4 - Transmit RDI-V upon TIM-V

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 3 through 1 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the TIM-V defect condition.

Bits 3 - 1 - UNEQ-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the UNEQ-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 0 (Transmit RDI-V upon UNEQ-V) within this register to "1".*

Bit 0 - Transmit RDI-V upon UNEQ-V

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 3 through 1 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the UNEQ-V defect condition.

TABLE 466: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT RDI-V CONTROL REGISTER - BYTE 1 (ADDRESS = 0XND86, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOP-V RDI CODE[2:0]			Transmit RDI-V upon LOP-V	AIS-V RDI CODE[2:0]			Transmit RDI-V upon AIS-V
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

Bits 7 - 5 - LOP-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the LOP-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 0 (Transmit RDI-V upon LOP-V) within this register to "1".*

Bit 4 - Transmit RDI-V upon LOP-V

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 3 through 1 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the LOP-V defect condition.

Bits 3 - 1 - AIS-V RDI Code[2:0]:

These three READ/WRITE bit-field permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) whenever (and for the duration that) the corresponding VT-De-Mapper block detects and declare the AIS-V defect condition.

NOTE: *In order to enable this feature, the user must set Bit 0 (Transmit RDI-V upon AIS-V) within this register to "1".*

Bit 0 - Transmit RDI-V upon AIS-V

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RDI Code (as configured in Bits 3 through 1 - within this register) towards the remote VT PTE whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.

- 0 - Configures the VT-Mapper block to NOT automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RDI Code (via the K4 byte) whenever (and for the duration that) the corresponding VT-De-Mapper block declares the AIS-V defect condition.

TABLE 467: CHANNEL CONTROL - VT-MAPPER BLOCK - INGRESS DIRECTION - TRANSMIT RDI-V CONTROL REGISTER - BYTE 0 (ADDRESS = 0XND87, WHERE N RANGES IN VALUE FROM 0X01 TO 0X1C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFI-V upon DS1/E1 RAI Enable	Unused		Transmit RDI-V Value[2:0]			RDI-V Type	RDI-V Insert Type
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

Bit 7 - RFI-V upon DS1/E1 RAI Enable:

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to automatically transmit the RFI-V indicator (within the outbound VT-data-stream) whenever (and for the duration) that the corresponding Ingress Direction Receive DS1/E1 Framer block declares the RAI defect condition.

- 0 - Does not configure the VT-Mapper block to automatically transmit the RFI-V indicator whenever (and for the duration) that the corresponding Ingress Direction Receive DS1/E1 Framer block declares the RAI defect condition.
- 1 - Configures the VT-Mapper block to automatically transmit the RFI-V indicator whenever (and for the duration) that the corresponding Ingress Direction Receive DS1/E1 Framer block declares the RAI defect condition.

Bits 6 - 5 - Unused:

Bits 4 - 2 - Transit RDI-V Value[2:0]:

These three READ/WRITE bit-fields permits the user to specify the value that the VT-Mapper block will transmit, within the RDI-V bit-fields of the K4 byte (within each outbound VT-frame) regardless of any defects that the corresponding VT-De-Mapper block is (or is NOT) currently declaring.

NOTE: *The user MUST set bit 0 (RDI-V Insert Type) within this register to "1" in order to configure the VT-Mapper block to use these bit-fields as the "source" of the RDI-V value.*

Bit 1 - RDI-V Type

This READ/WRITE bit-field permits the user to configure the VT-Mapper block to either support the "SRDI-V" (Single-Bit - RDI-V) or "ERDI-V" (Extended - RDI-V) form of signaling. If the user opts to use only "Single-Bit" RDI-V, then the RDI-V indicator will only be transported via Bit 8 (RDI-V) within the V5 byte in a VT-data-stream. Conversely, if the user opts to use the "Extended" RDI-V, then the RDI-V indicator will be transported via both Bit 8 (RDI-V) within the V5 byte, and Bits 5, 6 and 7 within the Z7/K4 byte.

- 0 - Configures the VT Mapper block to use the SRDI-V form of signaling.
- 1 - Configures the VT-Mapper block to use the ERDI-V form of signaling.

NOTE: *This configuration setting only applies to the VT-Mapper block. If the user wishes to configure the VT-De-Mappe block to support either the "SRDI-V" or the "ERDI-V" form of signaling, then he/she must set Bit 0 (RDI-V Type) within the "Channel Control - VT-De-Mapper Block - Egress Direction - DS1/E1 Drop Control Register - Byte 2.*

Bit 0 - RDI-V Insert Type:

This READ/WRITE bit-field permits the user to select the source of the RDI-V code word that the VT-Mapper block will transmit within the outbound VT-data-stream, as depicted below. In this case, the user has two options.

- To configure the VT-Mapper block to transmit the appropriate RDI-V code (based upon defects that the corresponding VT-De-Mapper block declares). In this case, the VT-Mapper block will transmit the RDI-V codes, as configured in the "Channel Control - VT Mapper Block - Ingress Direction - Transmit RDI-V Control Register - Bytes 3 - 1" registers.
- To configure the VT-Mapper block to use the value written into the "Transmit RDI-V Value[2:0]" bit-fields within this register.

- 0 - Configures the VT-Mapper block to transmit the appropriate RDI-V code (based upon defects that the corresponding VT-De-Mapper block declares).
- 1 - Configures the VT-Mapper block to use the value written into the "Transmit RDI-V Value[2:0]" bit-fields within this register.

REVISIONS

DATE	REV #	DESCRIPTION
09/09/06	P1.0.0	Initial issue of register information.
11/09/06	P1.0.5	Made edits to register map.
1/17/07	P1.0.6	Made edits to register map and register definitions.

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